

CPU


AVR-64da32 U1

USART-2

USART-1

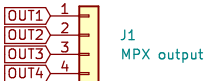
Note: R20 depends on LED

Multiplex Signal connector



J7
MPX output

1x4 terminal connector (optional)



J1
MPX output

2x2 pin header

Power

LDO is optional to protect CPU against high voltage on the bus. The D1 protects against reverse polarity. Close JP1 if LDO is not fitted.

The diagram shows the power supply circuit for the CPU. The +5V input is connected to a diode D1 (SSA33L) in series with a capacitor C1 (4.7u/10V). The output of the diode is connected to the IN pin of the LDO U2 (MIC5205-5.0YM5). The EN pin of U2 is connected to the same input line. The OUT pin of U2 is connected to the VDD pin of the CPU. A jumper JP1 (SolderJumper_2_Open) is connected between the input line and the VDD pin. A capacitor C4 (4.7u/10V) is connected between the VDD pin and GND. The GND pin of U2 is connected to the common GND.

Interfaces

The diagram illustrates the internal connections of the 8255 PPI. It shows a central vertical bus with several connection points. The signals and their connections are as follows:

- J2 (WS-bus output):** Pins 1, 2, and 3 are connected to the DO signal.
- J3 (WS-bus input):** Pins 1, 2, and 3 are connected to the DI signal. Pin 2 is also connected to +5V.
- J4 (UPDI IF):** Pins 1, 2, 3, 4, 5, and 6 are connected to the UPDI signal. Pins 3, 4, 5, and 6 are marked with an 'X'.
- J5 (Debug IF):** Pins 1, 2, 3, 4, 5, and 6 are connected to the V24 signals. Pins 2, 3, 4, 5, and 6 are marked with an 'X'.

The signals are connected to the 8255 pins as follows:

- DO:** Connected to J2 pins 1, 2, and 3.
- DI:** Connected to J3 pins 1, 2, and 3.
- UPDI:** Connected to J4 pins 1, 2, 3, 4, 5, and 6.
- V24:** Connected to J5 pins 1, 2, 3, 4, 5, and 6.

The diagram also shows the connection of the 8255 pins to the GND signal.

Legend:

- DO:** Data Output
- DI:** Data Input
- UPDI:** Universal Parallel Digital Interface
- V24:** Voltage Input

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