SystemVerilog Assignment: Build a digital calculator

Digital Systems (ELEC ENG 2100)

Objective

In this assignment, you are required to design and implement a simple digital calculator using the Basys3 FPGA board. You will use SystemVerilog to program the FPGA, leveraging its hardware resources to perform basic arithmetic operations.

Assessment Scheme

This is an individual assignment that will assess your ability to develop an application using the skills you have learnt in SystemVerilog.

Your work must be submitted by Wednesday of Week 11. For this assignment, you need to submit your SystemVerilog program, a video demonstrating its functionality, and the required design documents. You will be assessed in the Week 12 workshops. If you do not present, the assignment will receive 0 marks. Late penalties of 20% per 24 hours late apply to this assessment.

Requirements

1. The calculator should be capable of performing the following operations:

- Addition (+)
- Subtraction (-)
- The calculator should handle two 4-bit binary values representing unsigned integers (0-15).

2. Input and Output

- sw[3:0] are used for inputting 4-bit binary values.
- sw4 is used for the selecting operator (1 for addition and 0 for subtraction).
- BTNL is used for resetting at any time.
- BTNU is used to confirm operand values.
- Seven-segment display is used to display values.
- BTND is used for changing the display mode.

3. Design Specifications

- The design must be implemented in SystemVerilog.
- The calculation should use combinational logic for performing arithmetic operations.
- Use modular design, such as creating separate modules for input handling, storing operands, arithmetic operations, control logic, and output display.
- You need to draw and submit a block diagram for your design. The diagram is required to demonstrate the system hierarchy. Each module is required to have a brief discussion about its function.
- There are two display modes. Values and results should be displayed in either decimal or hexadecimal. The display mode can be changed at any time.
- Operations can be reset at any time.

4. Operation procedures

i. Select operand 1, then confirm. While selecting, the value of operand 1 needs to be displayed on the seven-segment display.

ii. Select operand 2, then confirm. While selecting, the value of operand 2 needs to be displayed on the seven-segment display.

iii. Display result on the seven-segment display.

Submission

For your submission, you are required to upload the following files by **11:59 pm on the 16th of October**,

- A short video (no more than 1 minute) demonstrating the functionality on the FPGA
- All SystemVerilog files (in a zip file)
- A block diagram for your design (in a pdf file)

Assessment Criteria

This assignment is worth 8% of your final mark. For this SystemVerilog assignment, you will be assessed based on,

- Correct functionality of the digital calculator (60%)
- Modular design (20%)
- Understanding and explanation (20%)