| ✓ Asynchronous ✓ Submit You have used 1 of 1 attempt | Show Answer |
|--|--|
| Question 0/1.0 point (graded) | Snow Answel |
| Vhich communication protocol is less memory efficient? Synchronous Asynchronous | |
| Submit You have used 1 of 1 attempt | Show Answer |
| Question 0/1.0 point (graded) When any of you post on Google Classroom or Slack platform for any issue, then ommunication does take place? | which |
| Synchronous Asynchronous | |
| Submit You have used 1 of 1 attempt | Show Answer |
| Question 0/2.0 points (graded) Asynchronous communication is slower because: | |
| It is limitted to carry 8 bits only ✓ It has extra overhead of bit synchronizitaion ✓ It has to add and remove extra bits, which is complex and time consuming. | |
| No it is as same speed as synchronous ✓ Submit You have used 1 of 2 attempts | a |
| Question 0/1.0 point (graded) | Show Answer |
| How can Master or slave check that the reciver has successfully received the trans SPI sends data to unique addressed Slave There is ACK//NACK bits | mitted data in SPI? |
| ☐ There is stop condition and "syn" character indicating successful transmission of data. ✓ No mechanism in SPI to acknowledge successful transmission | |
| Submit You have used 1 of 1 attempt | Show Answer |
| Question 0/1.0 point (graded) Ve know, In SPI, slave sends data to master along with the pre-generated clock si an master know how many bits of data the slave want to transfer? | gnal of master. Hov |
| Master sends random number of clock pulses Slave informs master about how many bits it wants to transfer | |
| Master generates clock pulses depends on the maximum number of bits the data bus can transfer on those devices. There is a fixed amount of clock pulses that master generates all the time in all devices | |
| Submit You have used 1 of 1 attempt Question | Show Answer |
| O/1.0 point (graded) PI can check error using parity bit. Is this statement true or false? False You have used 1 of 1 attempt | • |
| Submit You have used 1 of 1 attempt Question 0/1.0 point (graded) | Show Answe |
| When there is no data flow through asynchronous line then the line is held at O High voltage level | |
| ○ Low voltage level ○ Neutral level (No voltage transfer) ✓ | |
| Submit You have used 1 of 1 attempt Question | Show Answer |
| Vhen the sending UART drives the data transmission line from a low voltage to a ndicates | high voltage, it |
| Start condition Stop condition Parity checking | |
| ○ Total transmission of whole data is finished ○ Also needs to check Clock line to determine the condition. | |
| Submit You have used 1 of 1 attempt | Show Answer |
| we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration | aves, then how can |
| Using unique addressing to each master and slave devices | 1 |
| we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration Vultimeter to single master configuration we submit You have used 1 of 1 attempt | Show Answer |
| we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration Vou have used 1 of 1 attempt Question 0/1.0 point (graded) A communication protocol which is limited to carry 8 bits, and synchronous, does out error checking mechanism. What is it? | Show Answer |
| fewe want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration Submit You have used 1 of 1 attempt Question O/1.0 point (graded) A communication protocol which is limited to carry 8 bits, and synchronous, does not error checking mechanism. What is it? SPI UART | Show Answer |
| fewe want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration vou have used 1 of 1 attempt Question O/1.0 point (graded) communication protocol which is limited to carry 8 bits, and synchronous, does it error checking mechanism. What is it? SPI UART O 12C Vou have used 1 of 1 attempt | Show Answer |
| Two point (graded) we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration Vou have used 1 of 1 attempt Question A communication protocol which is limited to carry 8 bits, and synchronous, does it error checking mechanism. What is it? SPI UART Question QUART Question QUA point (graded) You have used 1 of 1 attempt Question QUA point (graded) You have used 1 of 1 attempt Question QUA point (graded) You have used 1 of 1 attempt Question QUA point (graded) You want to transfer continous stream of data, at a faster speed then which one | Show Answer |
| five want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration Vou have used 1 of 1 attempt Communication protocol which is limited to carry 8 bits, and synchronous, does atternor checking mechanism. What is it? SPI UART Cuestion O/1.0 point (graded) Vou have used 1 of 1 attempt Cuestion O/1.0 point (graded) Fyou want to transfer continous stream of data, at a faster speed then which one spi SPI UART Cuestion O/1.0 point (graded) Fyou want to transfer continous stream of data, at a faster speed then which one spi UART O/1.0 point (graded) Fyou want to transfer continous stream of data, at a faster speed then which one spi UART O/1.0 point (graded) You have used 1 of 1 attempt Vou have used 1 of 1 attempt Vou have used 1 of 1 attempt | show Answel |
| Five want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration It is limited to single master configuration Communication protocol which is limited to carry 8 bits, and synchronous, does at error checking mechanism. What is it? SPI UART Question QUART Depoint (graded) Five want to transfer continous stream of data, at a faster speed then which one of the point (graded) UART DEPOINT OF THE PROPERTY OF THE PROPE | Show Answer Show Answer Show Answer |
| if we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration Vou have used 1 of 1 attempt | Show Answer Show Answer Show Answer Show Answer |
| if we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration | not have any data show Answer show Answer Show Answer Show Answer |
| we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using TX-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration If it is limited to single master configuration Vou have used 1 of 1 attempt | show Answer Show Answer Show Answer Show Answer Show Answer Show Answer |
| if we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using 1X-RX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration It is limited to single master configuration It is | show Answer |
| in we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? by using 174-80 lines from both the masters Using unique addressing to each master and slave devices Can implement daily chain configuration It is limited to single master configuration | show Answer |
| inverwant to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using VALEX lines from both the masters Using unique addressing to each master and slave devices Can implement daisy chain configuration | show Answer |
| The want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? Sy using 176-82 lines from both the masters Using unique addressing to each master and slave devices Can implement disky chain configuration | show Answer so Show Answer |
| Two want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? dy using 10/40 Kines from both the masters dy using 10/40 Kines from both th | show Answer so Show Answer |
| in we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? by using 12 KP Stitles from hoth the masters by using 12 KP Stitles from hoth the following statement by using 12 KP Stitles from hoth the pictors of the following statement by using 12 KP Stitles from hoth the pictors of the following statement by using 12 KP Stitles from hoth the pictors of the following statement by using 12 KP Stitles from hoth the pictors of the following statement by using 12 KP Stitles from hoth the pictors of the following statement by using 12 KP Stitles from hoth the pictors of the following statement by using 12 KP Stitles from hoth the following statement by using 12 KP Stitles from hoth the following statement by using 12 KP Stitles from hoth the following statement by using 12 KP Stitles from hoth the following statement by using 12 KP Stitles from hoth the following statement by using 12 KP Sti | show Answer |
| Two want to connect a MPU, a MCU as master with some peripheral devices as a lata transfer will take place through UART? by using TX 60 lines from both the masters carry unique addressing to cath master and slive devices can implement daily chain configuration. call involves and 1 of 1 atherpt busistion business and 1 of 1 atherpt | show Answer T 2 finds that SDA ents are true? |
| we want to connect a MPU, a MCU as master with some peripheral devices as slata transfer will take place through UART? By using 17 KR floss tom both the masters Using using are RR floss tom both the masters Using using are differential to the configuration Call implement daily chair configuration Via post regulation Via how used 1 of 1 attempt | Show Answer |
| we want to connect a MPU, a MCU as master with some peripheral devices as slatat transfer will take place through UART? we want to connect a MPU, a MCU as master with some peripheral devices as slatat transfer will take place through UART? we wing 12-60 free from both the masters class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each master and slave devices class unique addressing to each slave and slave an | show Answer |
| According to the same and to desire the same time. What is 18? Street would be same to the same and to desire the same time. What is 18? Street would be same to desire the same to desire the same time. What is 18? Street would be same to desire the same time. What is 18? Street would be same to desire the same time. What is 18? Street would be same to desire the same time. What is 18? Street would be same to desire the same time. What is 18? Street would be same to desire the same time. What is 18? Street would be same to desire the same time. What is 18? Street would be same to desire the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18? Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the same time. What is 18. Street would be same to the | show Answer state of the state |
| we want to connect a MPU, a MCU as master with some peripheral devices as slat transfer will take place through UART? we want to connect a MPU, a MCU as master with some peripheral devices as slat transfer will take place through UART? winding 16.00 five from both the masters winding singles addressing to soft master and size occless winding singles addressing to soft master and size occless winding singles addressing to soft master contigeration winding singles addressing to soft master contigeration winding singles and size of a size of a size occless winding singles and size occurrence of a size occurrence occ | Show Answer |
| we want to connect a MPU, a MCU as master with some peripheral devices as slated transfer will take place through UART? | is preferred? Show Answer |
| we want to connect a MPU, a MCU as master with some peripheral devices as a latar transfer will take place through UART? we want to fitne from both the nazos with a wine address to each make and we advices with a wine address to each make and we advices with a wine address to each make and we advices with a wine address to each make and we advices with a wine and all all allered. we will not be the make and all allered. we will not be the make all allered. we will not be the make allered. we will not be t | is preferred? Show Answer is preferred? Show Answer show Answer action of slaves, also show Answer show Answer action of slaves, also show Answer show Answer action of slaves, also show Answer action |
| we want to connect a MPU, a MCU as master with some peripheral devices as side transfer will take place through UART? In your to 55 of tree from both the master | show Answer solvents are true? Show Answer |
| we want to connect a MPU. a MCU as master with some peripheral devices as all attentions will take place through UART? we want to connect a MPU. a MCU as master with some peripheral devices as all attentions of the connection | show Answer show Answer show Answer show Answer eferred from the show Answer eration of slaves, also show Answer show Answer show Answer eration is eration is eration is |
| we want to connect a MPU, a MCU as master with some peripheral devices as all attention will take place through UART? was to a State to make the constant was to state the constant of constant or constant o | show Answe is preferred? is preferred? show Answe eferred from the show Answe are true? show Answe are true? show Answe are true? |
| we want to connect a MPU. a MCU as matter with some peripheral devices as all at arransfer will take place through UART? was to produce the device of the devices | show Answe is preferred? is preferred? show Answe eferred from the show Answe are 2 finds that SDA ents are true? show Answe show Answe are true? |