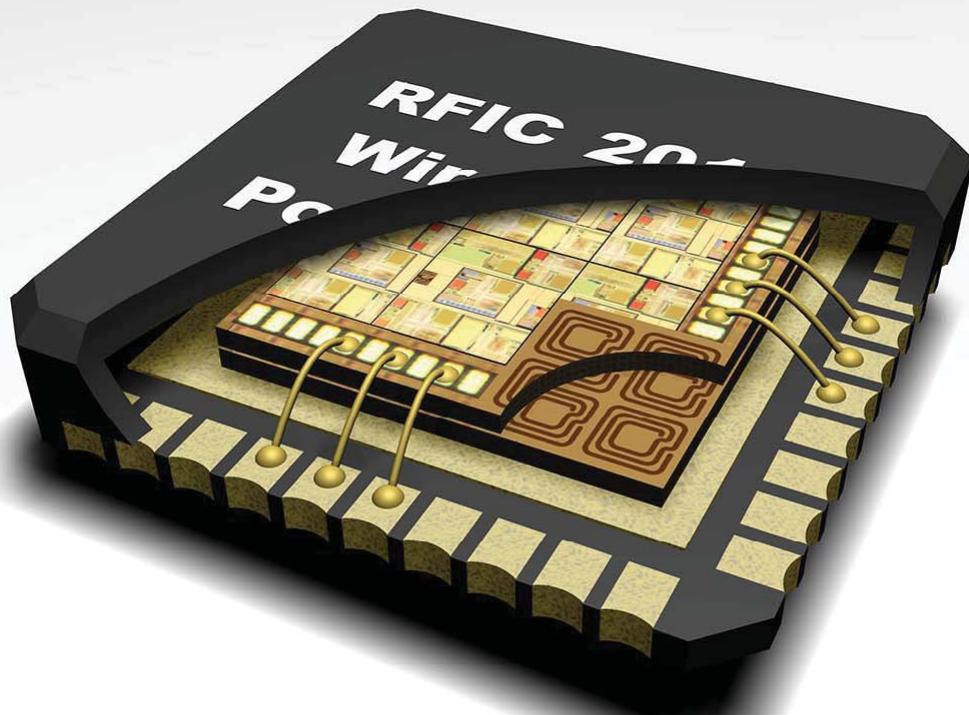


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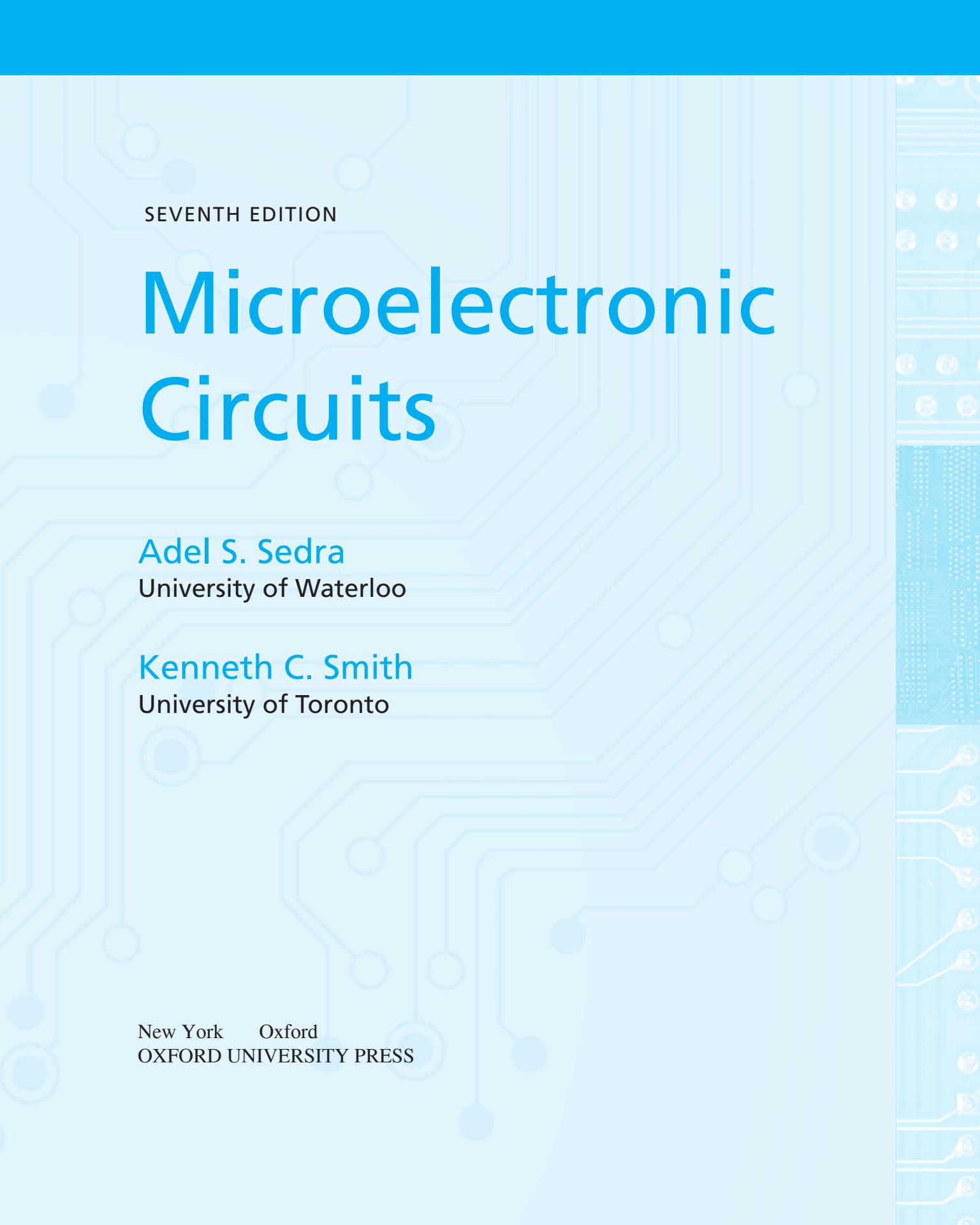


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(Photo Credit: The picture is courtesy of Professor David Wentzloff, Director of the Wireless Integrated Circuits Group at the University of Michigan, and was edited by Muhammad Faisal, Founder of Movellus Circuits Incorporated.)

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# PREFACE

*Microelectronic Circuits*, Seventh Edition, is intended as a text for the core courses in electronic circuits taught to majors in electrical and computer engineering. It should also prove useful to engineers and other professionals wishing to update their knowledge through self-study.

As was the case with the first six editions, the objective of this book is to develop in the reader the ability to analyze and design electronic circuits, both analog and digital, discrete and integrated. While the application of integrated circuits is covered, emphasis is placed on transistor circuit design. This is done because of our belief that even if the majority of those studying this book were not to pursue a career in IC design, knowledge of what is inside the IC package would enable intelligent and innovative application of such chips. Furthermore, with the advances in VLSI technology and design methodology, IC design itself has become accessible to an increasing number of engineers.

## Prerequisites

The prerequisite for studying the material in this book is a first course in circuit analysis. As a review, some linear circuits material is included here in the appendices: specifically, two-port network parameters in Appendix C; some useful network theorems in Appendix D; single-time-constant circuits in Appendix E; and s-domain analysis in Appendix F. In addition, a number of relevant circuit analysis problems are included at the beginning of the end-of-chapter problems section of Chapter 1. No prior knowledge of physical electronics is assumed. All required semiconductor device physics is included, and Appendix A provides a brief description of IC fabrication. All these appendices can be found on the book's website.

## Emphasis on Design

It has been our philosophy that circuit design is best taught by pointing out the various tradeoffs available in selecting a circuit configuration and in selecting component values for a given configuration. The emphasis on design has been retained in this edition. In addition to design examples, and design-oriented exercises and end-of-chapter problems (indicated with a D), the book includes on its website an extensive appendix (Appendix B) where a large number of simulation and design examples are presented. These emphasize the use of SPICE, the most valuable circuit-design aid.

## New to the Seventh Edition

While maintaining the philosophy and pedagogical approach of the first six editions, several changes have been made to both organization and coverage. Our goal in making structural changes has been to increase modularity and thus flexibility for the instructor, without causing disturbance to courses currently using the sixth edition. Changes in coverage are necessitated by the continuing advances in technology which make some topics of greater relevance and others of less interest. As well, advances in IC process technology require that the numbers used in the examples, exercises and end-of-chapter problems be updated to reflect the parameters of newer generations of IC technologies (e.g., some problems utilize the parameters of the 65-nm CMOS process). This ensures that students are acquiring a real-world perspective on technology.

To improve presentation, a number of chapters and sections have been rewritten for greater clarity. Specific, noteworthy changes are:

1. **New End-of-Chapter Problems and a New Instructor's Solutions Manual.** The number of the end-of-chapter problems has increased by about 50. Of the resulting 1532 problems, 176 are entirely new and 790 have new data. The new Instructor's Solutions Manual is written by Adel Sedra.
2. **Expand-Your-Perspective Notes.** This is a new feature providing historical and application perspectives. About two such notes are included in each chapter. Most are focused on notable circuit engineers and key inventions.
3. **Greater Flexibility in Presenting the MOSFET and the BJT.** Two short and completely parallel chapters present the MOSFET (Chapter 5) and the BJT (Chapter 6). Here the focus is on the device structure and its physical operation, its current-voltage characteristics, and its application in dc circuits. The order of coverage of these two chapters is entirely at the instructor's discretion as they have been written to be completely independent of each other.
4. **A Unified Treatment of Transistor Amplifiers.** The heart of a first course in electronics is the study of transistor amplifiers. The seventh edition provides a new approach to this subject: A new Chapter 7 begins with the basic principles that underlie the operation of a transistor of either type as an amplifier, and presents such concepts as small-signal operation and modeling. This is followed by the classical configurations of transistor amplifiers, biasing methods, and practical discrete-circuit amplifiers. The combined presentation emphasizes the unity of the basic principles while allowing for separate treatment of the two device types where this is warranted. Very importantly, we are able to compare the two devices and to draw conclusions about their unique areas of application.
5. **Improved Presentation of Cascoding.** Chapter 8 dealing with the basic building blocks of IC amplifiers has been rewritten to improve presentation. Specifically, the development of cascoding and the key circuit building blocks, the cascode amplifier and the cascode current source, is now much clearer.
6. **Clearer and Simplified Study of Feedback.** The feedback chapter has been rewritten to improve, simplify and clarify the presentation of this key subject.
7. **Streamlined Presentation of Frequency Response.** While keeping the treatment of frequency response all together, the chapter has been rewritten to streamline its flow, and simplify and clarify the presentation.
8. **Updated Treatment of Output Stages and Power Amplifiers.** Here, we have updated the material on MOS power transistors and added a new section on the increasingly important class-D switching power amplifier.
9. **A More Contemporary Approach to Operational Amplifier Circuits.** While maintaining coverage of some of the enduring features and subcircuits of the classical 741 op amp, its total coverage is somewhat reduced to make room for modern IC op amp design techniques.

10. **Better Organized and Modernized Coverage of Digital IC Design.** Significant improvements have been made to the brief but comprehensive coverage of digital IC design in Part III. These include a better motivated study of CMOS logic circuits (Chapter 14) which now begins with logic gate circuits. The material on logic circuit technologies and design methodologies as well as the advanced topic of technology scaling and its implications have been moved to Chapter 15. This modularly structured chapter now deals with a selection of advanced and somewhat specialized topics. Since bipolar is hardly ever used in new digital design, coverage of ECL has been significantly reduced. Similarly, BiCMOS has become somewhat of a specialty topic and its coverage has been correspondingly reduced. Nevertheless, the complete material on both ECL and BiCMOS is now available on the book's website. Finally, we have added a new section on image sensors to Chapter 16 (Memory Circuits).
11. **Increased Emphasis on Integrated-Circuit Filters and Oscillators.** A section on a popular approach to integrated-circuit filter design, namely, Transconductance-C filters, has been added to Chapter 17. To make room for this new material, the subsection on stagger-tuned amplifiers has been removed and placed in Appendix H, on the website. The cross-coupled LC oscillator, popular in IC design, has been added to Chapter 18. The section on precision diode circuits has been removed but is still made available on the website.
12. **A Useful and Insightful Comparison of the MOSFET and the BJT.** This is now included in Appendix G, available on the website.

## The Book's Website

A Companion Website for the book has been set up at [www.oup.com/us/sedrasmith](http://www.oup.com/us/sedrasmith). Its content will change frequently to reflect new developments. The following material is available on the website:

1. Data sheets for hundreds of useful devices to help in laboratory experiments as well as in design projects.
2. Links to industrial and academic websites of interest.
3. A message center to communicate with the authors and with Oxford University Press.
4. Links to the student versions of both Cadence PSpice® and National Instruments Multisim™.
5. The input files for all the PSpice® and Multisim™ examples of Appendix B.
6. Step-by-step guidance to help with the simulation examples and the end-of-chapter problems identified with a SIM icon.
7. Bonus text material of specialized topics which are either not covered or covered briefly in the current edition of the textbook. These include:
  - Junction Field-Effect Transistors (JFETs)
  - Gallium Arsenide (GaAs) Devices and Circuits
  - Transistor-Transistor Logic (TTL) Circuits
  - Emitter-Coupled Logic (ECL) Circuits
  - BiCMOS Circuits
  - Precision Rectifier Circuits
8. Appendices for the Book:
  - Appendix A: VLSI Fabrication Technology
  - Appendix B: SPICE Device Models and Design and Simulation Examples Using PSpice® and Multisim™
  - Appendix C: Two-Port Network Parameters
  - Appendix D: Some Useful Network Theorems
  - Appendix E: Single-Time-Constant Circuits
  - Appendix F: *s*-domain Analysis: Poles, Zeros, and Bode Plots
  - Appendix G: Comparison of the MOSFET and the BJT

- Appendix H: Design of Stagger-Tuned Amplifiers
- Appendix I: Bibliography
- Appendix L: Answers to Selected Problems

## Exercises and End-of-Chapter Problems

Over 475 Exercises are integrated throughout the text. The answer to each exercise is given below the exercise so students can check their understanding of the material as they read. Solving these exercises should enable the reader to gauge his or her grasp of the preceding material. In addition, more than 1530 end-of-chapter Problems, 65% of which are new or revised in this edition, are provided. The problems are keyed to the individual chapter sections and their degree of difficulty is indicated by a rating system: difficult problems are marked with an asterisk (\*); more difficult problems with two asterisks (\*\*); and very difficult (and/or time consuming) problems with three asterisks (\*\*\*)�. We must admit, however, that this classification is by no means exact. Our rating no doubt depended to some degree on our thinking (and mood!) at the time a particular problem was created. Answers to sample problems are given in Appendix L (on the website), so students have a checkpoint to tell if they are working out the problems correctly. Complete solutions for all exercises and problems are included in the *Instructor's Solutions Manual*, which is available from the publisher to those instructors who adopt the book.

As in the previous six editions, many examples are included. The examples, and indeed most of the problems and exercises, are based on real circuits and anticipate the applications encountered in designing real-life circuits. This edition continues the use of numbered solution steps in the figures for many examples, as an attempt to recreate the dynamics of the classroom.

## Course Organization

The book contains sufficient material for a sequence of two single-semester courses, each of 40-50 lecture hours. The modular organization of the book provides considerable flexibility for course design. In the following, we suggest content for a sequence of two classical or standard courses. We also describe some variations on the content of these two courses and specify supplemental material for a possible third course.

### The First Course

The first course is based on Part I of the book, that is, Chapters 1–7. It can be taught, most simply by starting at the beginning of Chapter 1 and concluding with the end of Chapter 7. However, as guidance to instructors who wish to follow a different order of presentation or a somewhat modified coverage, or to deal with situations where time might be constrained, we offer the following remarks:

The core of the first course is the study of the two transistor types, Chapters 5 and 6, in whatever order the instructor wishes, and transistor amplifiers in Chapter 7. These three chapters must be covered in full.

Another important part of the first course is the study of diodes (Chapter 4). Here, however, if time does not permit, some of the applications in the later part of the chapter can be skipped.

We have found it highly motivational to cover op amps (Chapter 2) near the beginning of the course. This provides the students with the opportunity to work with a practical integrated circuit and to experiment with non-trivial circuits.

Coverage of Chapter 1, at least of the amplifier sections, should prove helpful. Here the sections on signals can be either covered in class or assigned as reading material. Section 1.6 on frequency response is needed if the frequency-response of op-amp circuits is to be studied; otherwise this section can be delayed to the second course.

Finally, if the students have not taken a course on physical electronics, Chapter 3 needs to be covered. Otherwise, it can be used as review material or skipped altogether.

## The Second Course

The main subject of the second course is integrated-circuit amplifiers and is based on Part II of the book, that is, Chapters 8-13. Here also, the course can be taught most simply by beginning with Chapter 8 and concluding with Chapter 13. However, this being a second course, considerable flexibility in coverage is possible to satisfy particular curriculum designs and/or to deal with time constraints.

First, however, we note that the core material is presented in Chapters 8-11 and these four chapters must be covered, though not necessarily in their entirety. For instance, some of the sections near the end of a chapter and identified by the “advanced material” icon can be skipped, usually with no loss of continuity.

Beyond the required chapters, (8-11), the instructor has many possibilities for the remainder of the course. These include one or both of the two remaining chapters in Part II, namely, Output Stages and Power Amplifier (Chapter 12), and Op-Amp Circuits (Chapter 13).

Another possibility, is to include an introduction to digital integrated circuits by covering Chapter 14, and if time permits, selected topics of Chapters 15 and 16.

Yet another possibility for the remainder of the second course is selected topics from the filters chapter (17) and/or the oscillators chapter (18).

## A Digitally Oriented First Course

A digitally-oriented first course can include the following: Chapter 1 (without Section 1.6), Chapter 2, Chapter 3 (if the students have not had any exposure to physical electronics), Chapter 4 (perhaps without some of the later applications sections), Chapter 5, selected topics from Chapter 7 emphasizing the basics of the application of the MOSFET as an amplifier, Chapter 14, and selected topics from Chapters 15 and 16. Such a course would be particularly suited for Computer Engineering students.

## Supplemental Material/Third Course

Depending on the selection of topics for the first and second courses, some material will remain and can be used for part of a third course or as supplemental material to support student design projects. These can include Chapter 12 (Output Stages and Power Amplifiers), Chapter 13 (Op-Amp Circuits), Chapter 17 (Filters) and Chapter 18 (Oscillators), which can be used to support a third course on analog circuits. These can also include Chapters 14, 15 and 16 which can be used for a portion of a senior-level course on digital IC design.

## The Accompanying Laboratory

Courses in electronic circuits are usually accompanied by laboratory experiments. To support the laboratory component for courses using this book, Professor Vincent Gaudet of the University of Waterloo has, in collaboration with K.C. Smith, authored a laboratory manual. *Laboratory Explorations*, together with an Instructor’s Manual, is available from Oxford University Press.

Another innovative laboratory instruction system, designed to accompany this book, has been recently developed. Specifically, Illuster Technologies Inc. has developed a digitally controlled lab platform, AELabs. The platform is realized on printed circuit boards using surface mount devices. A wide variety of circuits can be configured on this platform through a custom graphical user interface. This allows students to conduct many experiments relatively quickly. More information is available from Illuster (see link on the Companion Website).

## An Outline for the Reader

Part I, *Devices and Basic Circuits*, includes the most fundamental and essential topics for the study of electronic circuits. At the same time, it constitutes a complete package for a first course on the subject.

**Chapter 1.** The book starts with an introduction to the basic concepts of electronics in Chapter 1. Signals, their frequency spectra, and their analog and digital forms are presented. Amplifiers are introduced as circuit building blocks and their various types and models are studied. This chapter also establishes some of the terminology and conventions used throughout the text.

**Chapter 2.** Chapter 2 deals with operational amplifiers, their terminal characteristics, simple applications, and practical limitations. We chose to discuss the op amp as a circuit building block at this early stage simply because it is easy to deal with and because the student can experiment with op-amp circuits that perform nontrivial tasks with relative ease and with a sense of accomplishment. We have found this approach to be highly motivating to the student. We should point out, however, that part or all of this chapter can be skipped and studied at a later stage (for instance, in conjunction with Chapter 9, Chapter 11, and/or Chapter 13) with no loss of continuity.

**Chapter 3.** Chapter 3 provides an overview of semiconductor concepts at a level sufficient for understanding the operation of diodes and transistors in later chapters. Coverage of this material is useful in particular for students who have had no prior exposure to device physics. Even those with such a background would find a review of Chapter 3 beneficial as a refresher. The instructor can choose to cover this material in class or assign it for outside reading.

**Chapter 4.** The first electronic device, the diode, is studied in Chapter 4. The diode terminal characteristics, the circuit models that are used to represent it, and its circuit applications are presented. Depending on the time available in the course, some of the diode applications (e.g. Section 4.6) can be skipped. Also, the brief description of special diode types (Section 4.7) can be left for the student to read.

**Chapters 5 and 6.** The foundation of electronic circuits is established by the study of the two transistor types in use today: the MOS transistor in Chapter 5 and the bipolar transistor in Chapter 6. ***These two chapters have been written to be completely independent of one another and thus can be studied in either order, as desired.*** Furthermore, the two chapters have the same structure, making it easier and faster to study the second device, as well as to draw comparisons between the two device types.

Each of Chapters 5 and 6 begins with a study of the device structure and its physical operation, leading to a description of its terminal characteristics. Then, to allow the student to become very familiar with the operation of the transistor as a circuit element, a large number of examples are presented of dc circuits utilizing the device. The last section of each of Chapters 5 and 6 deals with second-order effects that are included for completeness, but that can be skipped if time does not permit detailed coverage.

**Chapter 7.** The heart of a first course in electronics is the study of transistor amplifiers. Chapter 7 (new to this edition) presents a unified treatment of the subject. It begins with the basic principles that underlie the operation of a transistor, of either type, as an amplifier, and proceeds to present the important concepts of small-signal operation and modeling. This is followed by a study of the basic configurations of single-transistor amplifiers. After a presentation of dc biasing methods, the chapter concludes with practical examples of discrete-circuit amplifiers. The combined presentation emphasizes the unity of the basic principles while allowing for separate treatment of the two device types where this is warranted. Very importantly, we are able to compare the two devices and to draw conclusions about their unique areas of application.

After the study of Part I, the reader will be fully prepared to study either integrated-circuit amplifiers in Part II, or digital integrated circuits in Part III.

Part II, *Integrated-Circuit Amplifiers*, is devoted to the study of practical amplifier circuits that can be fabricated in the integrated-circuit (IC) form. Its six chapters constitute a coherent treatment of IC amplifier design and can thus serve as a second course in electronic circuits.

**MOS and Bipolar.** Throughout Part II, both MOS and bipolar circuits are presented side-by-side. Because the MOSFET is by far the dominant device, its circuits are presented first. Bipolar circuits are discussed to the same depth but occasionally more briefly.

**Chapter 8.** Beginning with a brief introduction to the philosophy of IC design, Chapter 8 presents the basic circuit building blocks that are used in the design of IC amplifiers. These include current mirrors, current sources, gain cells, and cascode amplifiers.

**Chapter 9.** The most important IC building block, the differential pair, is the main topic of Chapter 9. The last section of Chapter 9 is devoted to the study of multistage amplifiers.

**Chapter 10.** Chapter 10 presents a comprehensive treatment of the important subject of amplifier frequency response. Here, Sections 10.1, 10.2, and 10.3 contain essential material; Section 10.4 provides an in-depth treatment of very useful new tools; and Sections 10.5 to 10.8 present the frequency response analysis of a variety of amplifier configurations that can be studied as and when needed. A selection of the latter sections can be made depending on the time available and the instructor's preference.

**Chapter 11.** The fourth of the essential topics of Part II, feedback, is the subject of Chapter 11. Both the theory of negative feedback and its application in the design of practical feedback amplifiers are presented. We also discuss the stability problem in feedback amplifiers and treat frequency compensation in some detail.

**Chapter 12.** In Chapter 12 we switch gears from dealing with small-signal amplifiers to those that are required to handle large signals and large amounts of power. Here we study the different amplifier classes—A, B, and AB—and their realization in bipolar and CMOS technologies. We also consider power BJTs and power MOSFETs, and study representative IC power amplifiers. A brief study of the increasingly popular Class D amplifier is also presented. Depending on the availability of time, some of the later sections can be skipped in a first reading.

**Chapter 13.** Finally, Chapter 13 brings together all the topics of Part II in an important application; namely, the design of operational amplifier circuits. We study both CMOS and bipolar op amps. In the latter category, besides the classical and still timely 741 circuit, we present modern techniques for the design of low-voltage op amps (Section 13.4).

Part III, *Digital Integrated Circuits*, provides a brief but nonetheless comprehensive and sufficiently detailed study of digital IC design. Our treatment is almost self-contained, requiring for the most part only a thorough understanding of the MOSFET material presented in Chapter 5. Thus, Part III can be studied right after Chapter 5. The only exceptions to this are the last section in Chapter 15 which requires knowledge of the BJT (Chapter 6). Also, knowledge of the MOSFET internal capacitances (Section 10.2.2) will be needed.

**Chapter 14.** Chapter 14 is the foundation of Part III. It begins with the motivating topic of CMOS logic-gate circuits. Then, following a detailed study of digital logic inverters, we concentrate on the CMOS inverter; its static and dynamic characteristics and its design. Transistor sizing and power dissipation round out the topics of Chapter 14. The material covered in this chapter is the minimum needed to learn something meaningful about digital circuits.

**Chapter 15.** Chapter 15 has a modular structure and presents six topics of somewhat advanced nature. It begins with a presentation of Moore's law and the technology scaling that has made the multi-billion-transistor chip possible. This is followed by an overview of digital IC technologies, and the design methodologies that make the design of super-complex digital ICs possible. Four different logic-circuit types are then presented. Only the last of these includes bipolar transistors.

**Chapter 16.** Digital circuits can be broadly divided into logic and memory circuits. The latter is the subject of Chapter 16.

Part IV, *Filters and Oscillators*, is intentionally oriented toward applications and systems. The two topics illustrate powerfully and dramatically the application of both negative and positive feedback.

**Chapter 17.** Chapter 17 deals with the design of filters, which are important building blocks of communication and instrumentation systems. A comprehensive, design-oriented treatment of the subject is presented. The material provided should allow the reader to perform a complete filter design, starting from specification and ending with a complete circuit realization. A wealth of design tables is included.

**Chapter 18.** Chapter 18 deals with circuits for the generation of signals with a variety of waveforms: sinusoidal, square, and triangular. We also present circuits for the nonlinear shaping of waveforms.

**Appendices.** The twelve appendices contain much useful background and supplementary material. We wish to draw the reader's attention in particular to the first two: Appendix A provides a concise introduction to the important topic of IC fabrication technology including IC layout. Appendix B provides SPICE device models as well as a large number of design and simulation examples in PSpice® and Multisim™. The examples are keyed to the book chapters. These Appendices and a great deal more material on these simulation examples can be found on the Companion Website.

## Ancillaries

A complete set of ancillary materials is available with this text to support your course.

### For the Instructor

The Ancillary Resource Center (ARC) at [www.oup-arc.com/sedrasmith](http://www.oup-arc.com/sedrasmith) is a convenient destination for all the instructor resources that accompany *Microelectronic Circuits*. Accessed online through individual user accounts, the ARC provides instructors with access to up-to-date ancillaries at any time while guaranteeing the security of grade-significant resources. The ARC replaces the Instructor's Resource CD that accompanied the sixth edition. On the ARC, you will find:

- An electronic version of the Instructor's Solutions Manual.
- PowerPoint-based figure slides that feature all the images and summary tables from the text, with their captions, so they can easily be displayed and explained in class.
- Detailed instructor's support for the SPICE circuit simulations in Multisim™ and PSpice®.

The **Instructor's Solutions Manual** (ISBN 978-0-19-933915-0), written by Adel Sedra, contains detailed solutions to all in-text exercises and end-of-chapter problems found in *Microelectronic Circuits*. The Instructor's Solutions Manual for *Laboratory Explorations to Accompany Microelectronic Circuits* (ISBN 978-0-19-933926-6) contains detailed solutions to all the exercises and problems found in this student's laboratory guide.

### For the Student and Instructor

A **Companion Website** at [www.oup.com/us/sedrasmith](http://www.oup.com/us/sedrasmith) features permanently cached versions of device datasheets, so students can design their own circuits in class. The website also contains SPICE circuit simulation examples and lessons. Bonus text topics and the Appendices are also featured on the website.

The *Laboratory Explorations to Accompany Microelectronic Circuits* (ISBN 978-0-19-933925-9) invites students to explore the realm of real-world engineering through practical, hands-on experiments. Keyed to sections in the text and taking a "learn-by-doing" approach, it presents labs that focus on the development of practical engineering skills and design practices.

## Acknowledgments

Many of the changes in this seventh edition were made in response to feedback received from instructors who adopted the sixth edition. We are grateful to all those who took the time to write to us. In addition, many of the reviewers provided detailed commentary on the sixth edition and suggested a number of the changes that we have incorporated in this edition. They are listed later; to all of them, we extend our sincere thanks. Adel Sedra is also grateful for the feedback received from the students who have taken his electronics courses over the past number of years at the University of Waterloo.

A number of individuals made significant contributions to this edition. Vincent Gaudet of the University of Waterloo contributed to Part III as well as co-authoring the laboratory manual. Wai-Tung Ng of the University of Toronto contributed to Chapter 12 and updated Appendix A (of which he is the original author). Muhammad Faisal of the University of Michigan updated Appendix B, which he helped create for the sixth edition; helped in obtaining the cover photo, and has over a number of years been the source of many good ideas. Olivier Trescases and his students at the University of Toronto pioneered the laboratory system described elsewhere in the Preface. Jennifer Rodrigues typed all the revisions, as she did for a number of the previous editions, with tremendous skill and good humour. Chris Schroeder was of great assistance to Adel Sedra with local logistics. Laura Fujino assisted in many ways and in particular with the “Expand-Your-Perspective” notes. To all of these friends and colleagues we say thank you.

Over the recent years we have benefited greatly from discussions with a number of colleagues and friends. In particular we are very grateful to the following: James Barby, University of Waterloo; David Nairn, University of Waterloo; Anthony Chan Carusone, University of Toronto; David Johns, University of Toronto; Ken Martin, University of Toronto; Khoman Phang, University of Toronto; Gordon Roberts, McGill University; Ali Sheikholeslami, University of Toronto; and Amir Yazdani, Ryerson University.

The cover photograph shows a 3D IC system, which demonstrates the concept of wireless power delivery and communication through multiple layers of CMOS chips. The communication circuits were demonstrated in an IBM 45 nm SOI CMOS process. This technology is designed to serve a multi-Gb/s interconnect between cores spread across several IC layers for high-performance processors. We are grateful to Professor David Wentzloff, Director of the Wireless Integrated Circuits Group at the University of Michigan, who allowed us to use this image, and to Muhammad Faisal, Founder of Movellus Circuits Incorporated, who edited the image.

A large number of people at Oxford University Press contributed to the development of this edition and its various ancillaries. We would like to specifically mention Marketing Manager David Jurman, Marketing Director Frank Mortimer, Higher Ed Sales Director Bill Marting, Copywriter Kristin Maffei, Art Director Michele Laseau, Production Manager Lisa Grzan, Team Leader Amy Whitmer, and Senior Production Editor Jane Lee.

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Finally, we wish to thank our families for their support and understanding, and to thank all the students and instructors who have valued this book throughout its history.

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Kenneth C. (KC) Smith  
Waterloo, Ontario, Canada  
August 2014

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# Microelectronic Circuits

**PART I**

# Devices and Basic Circuits

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**P**art I, *Devices and Basic Circuits*, includes the most fundamental and essential topics for the study of electronic circuits. At the same time, it constitutes a complete package for a first course on the subject.

The heart of Part I is the study of the three basic semiconductor devices: the diode (Chapter 4), the MOS transistor (Chapter 5), and the bipolar transistor (Chapter 6). In each case, we study the device operation, its characterization, and its basic circuit applications. Chapter 7 then follows with a study of the most fundamental application of the two transistor types; namely, their use in amplifier design. This side-by-side study of MOSFET and BJT amplifiers allows us to see similarities between these amplifiers and to compare them, which in turn highlights the distinct areas of applicability of each, as well as showing the unity of the basic principles that underlie the use of transistors as amplifiers.

For those who have not had a prior course on device physics, Chapter 3 provides an overview of semiconductor concepts at a level sufficient for the study of electronic circuits. A review of Chapter 3 should prove useful even for those with prior knowledge of semiconductors.

Since the purpose of electronic circuits is the processing of signals, it is essential to understand signals, their characterization in the time and frequency domains, and their analog and digital representations. The basis for such understanding is provided in Chapter 1, which also introduces the most common signal-processing function, *amplification*, and the characterization and types of *amplifiers*.

Besides diodes and transistors, the basic electronic devices, the op amp is studied in Part I. Although not an electronic device in the most fundamental sense, the op amp is commercially available as an integrated circuit (IC) package and has well-defined terminal characteristics. Thus, even though the op amp's internal circuit is complex, typically incorporating 20 or more transistors, its almost-ideal terminal behavior makes it possible to treat the op amp as a circuit element and to use it in the design of powerful circuits, as we do in Chapter 2, without any knowledge of its internal construction. We should mention, however, that the study of op amps can be delayed until a later point, and Chapter 2 can be skipped with no loss of continuity.

The foundation of this book, and of any electronics course, is the study of the two transistor types in use today: the MOS transistor in Chapter 5 and the bipolar transistor in Chapter 6. These two chapters have been written to be completely independent of each other and thus can be studied in either order, as desired.

After the study of Part I, the reader will be fully prepared to undertake the study of either integrated-circuit amplifiers in Part II or digital integrated circuits in Part III.

## CHAPTER 1

# Signals and Amplifiers

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## IN THIS CHAPTER YOU WILL LEARN

1. That electronic circuits process signals, and thus understanding electrical signals is essential to appreciating the material in this book.
2. The Thévenin and Norton representations of signal sources.
3. The representation of a signal as the sum of sine waves.
4. The analog and digital representations of a signal.
5. The most basic and pervasive signal-processing function: signal amplification, and correspondingly, the signal amplifier.
6. How amplifiers are characterized (modeled) as circuit building blocks independent of their internal circuitry.
7. How the frequency response of an amplifier is measured, and how it is calculated, especially in the simple but common case of a single-time-constant (STC) type response.

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## Introduction

The subject of this book is modern electronics, a field that has come to be known as **microelectronics**. **Microelectronics** refers to the integrated-circuit (IC) technology that at the time of this writing is capable of producing circuits that contain billions of components in a small piece of silicon (known as a **silicon chip**) whose area is on the order of  $100 \text{ mm}^2$ . One such microelectronic circuit, for example, is a complete digital computer, which accordingly is known as a **microcomputer** or, more generally, a **microprocessor**. The microelectronic circuits you will learn to design in this book are used in almost every device we encounter in our daily lives: in the appliances we use in our homes; in the vehicles and transportation systems we use to travel; in the cell phones we use to communicate; in the medical equipment we need to care for our health; in the computers we use to do our work; and in the audio and video systems, the radio and TV sets, and the multitude of other digital devices we use to entertain ourselves. Indeed, it is difficult to conceive of modern life without microelectronic circuits.

In this book we shall study electronic devices that can be used singly (in the design of **discrete circuits**) or as components of an **integrated-circuit (IC)** chip. We shall study the design and analysis of interconnections of these devices, which form discrete and integrated

circuits of varying complexity and perform a wide variety of functions. We shall also learn about available IC chips and their application in the design of electronic systems.

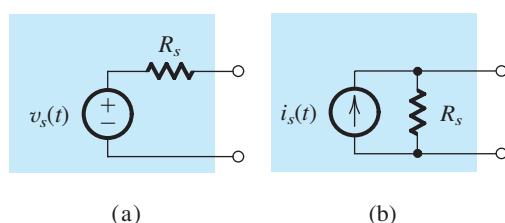
The purpose of this first chapter is to introduce some basic concepts and terminology. In particular, we shall learn about signals and about one of the most important signal-processing functions electronic circuits are designed to perform, namely, signal amplification. We shall then look at circuit representations or models for linear amplifiers. These models will be employed in subsequent chapters in the design and analysis of actual amplifier circuits.

In addition to motivating the study of electronics, this chapter serves as a bridge between the study of linear circuits and that of the subject of this book: the design and analysis of electronic circuits.

## 1.1 Signals

Signals contain information about a variety of things and activities in our physical world. Examples abound: Information about the weather is contained in signals that represent the air temperature, pressure, wind speed, etc. The voice of a radio announcer reading the news into a microphone provides an acoustic signal that contains information about world affairs. To monitor the status of a nuclear reactor, instruments are used to measure a multitude of relevant parameters, each instrument producing a signal.

To extract required information from a set of signals, the observer (be it a human or a machine) invariably needs to **process** the signals in some predetermined manner. This **signal processing** is usually most conveniently performed by electronic systems. For this to be possible, however, the signal must first be converted into an electrical signal, that is, a voltage or a current. This process is accomplished by devices known as **transducers**. A variety of transducers exist, each suitable for one of the various forms of physical signals. For instance, the sound waves generated by a human can be converted into electrical signals by using a microphone, which is in effect a pressure transducer. It is not our purpose here to study transducers; rather, we shall assume that the signals of interest already exist in the electrical domain and represent them by one of the two equivalent forms shown in Fig. 1.1. In Fig. 1.1(a) the signal is represented by a voltage source  $v_s(t)$  having a source resistance  $R_s$ . In the alternate representation of Fig. 1.1(b) the signal is represented by a current source  $i_s(t)$  having a source resistance  $R_s$ . Although the two representations are equivalent, that in Fig. 1.1(a) (known as the Thévenin form) is preferred when  $R_s$  is low. The representation of Fig. 1.1(b) (known as the Norton form) is preferred when  $R_s$  is high. The reader will come to appreciate this point later in this chapter when we study the different types of amplifiers. For the time being, it is important to be familiar with Thévenin's and Norton's theorems (for a



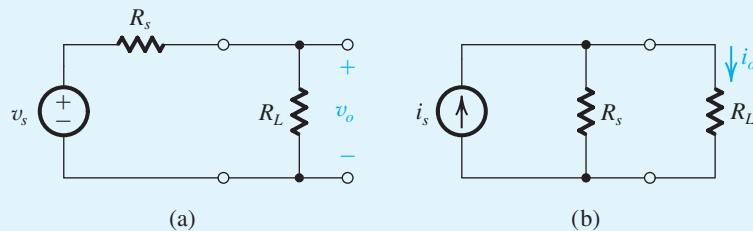
**Figure 1.1** Two alternative representations of a signal source: (a) the Thévenin form; (b) the Norton form.

brief review, see Appendix D) and to note that for the two representations in Fig. 1.1 to be equivalent, their parameters are related by

$$v_s(t) = R_s i_s(t)$$

### Example 1.1

The output resistance of a signal source, although inevitable, is an imperfection that limits the ability of the source to deliver its full signal strength to a **load**. To see this point more clearly, consider the signal source when connected to a load resistance  $R_L$  as shown in Fig. 1.2. For the case in which the source is represented by its Thévenin equivalent form, find the voltage  $v_o$  that appears across  $R_L$ , and hence the condition that  $R_s$  must satisfy for  $v_o$  to be close to the value of  $v_s$ . Repeat for the Norton-represented source; in this case finding the current  $i_o$  that flows through  $R_L$  and hence the condition that  $R_s$  must satisfy for  $i_o$  to be close to the value of  $i_s$ .



**Figure 1.2** Circuits for Example 1.1.

### Solution

For the Thévenin-represented signal source shown in Fig. 1.2(a), the output voltage  $v_o$  that appears across the load resistance  $R_L$  can be found from the ratio of the voltage divider formed by  $R_s$  and  $R_L$ ,

$$v_o = v_s \frac{R_L}{R_L + R_s}$$

From this equation we see that for

$$v_o \simeq v_s$$

the source resistance  $R_s$  must be much lower than the load resistance  $R_L$ ,

$$R_s \ll R_L$$

Thus, for a source represented by its Thévenin equivalent, ideally  $R_s = 0$ , and as  $R_s$  is increased, relative to the load resistance  $R_L$  with which this source is intended to operate, the voltage  $v_o$  that appears across the load becomes smaller, not a desirable outcome.

**Example 1.1** *continued*

Next, we consider the Norton-represented signal source in Fig. 1.2(b). To obtain the current  $i_o$  that flows through the load resistance  $R_L$ , we utilize the ratio of the current divider formed by  $R_s$  and  $R_L$ ,

$$i_o = i_s \frac{R_s}{R_s + R_L}$$

From this relationship we see that for

$$i_o \simeq i_s$$

the source resistance  $R_s$  must be much larger than  $R_L$ ,

$$R_s \gg R_L$$

Thus for a signal source represented by its Norton equivalent, ideally  $R_s = \infty$ , and as  $R_s$  is reduced, relative to the load resistance  $R_L$  with which this source is intended to operate, the current  $i_o$  that flows through the load becomes smaller, not a desirable outcome.

Finally, we note that although circuit designers cannot usually do much about the value of  $R_s$ , they may have to devise a circuit solution that minimizes or eliminates the loss of signal strength that results when the source is connected to the load.

## EXERCISES

- 1.1** For the signal-source representations shown in Figs. 1.1(a) and 1.1(b), what are the open-circuit output voltages that would be observed? If, for each, the output terminals are short-circuited (i.e., wired together), what current would flow? For the representations to be equivalent, what must the relationship be between  $v_s$ ,  $i_s$ , and  $R_s$ ?

**Ans.** For (a),  $v_{oc} = v_s(t)$ ; for (b),  $v_{oc} = R_s i_s(t)$ ; for (a),  $i_{sc} = v_s(t)/R_s$ ; for (b),  $i_{sc} = i_s(t)$ ; for equivalency,  $v_s(t) = R_s i_s(t)$

- 1.2** A signal source has an open-circuit voltage of 10 mV and a short-circuit current of 10  $\mu$ A. What is the source resistance?

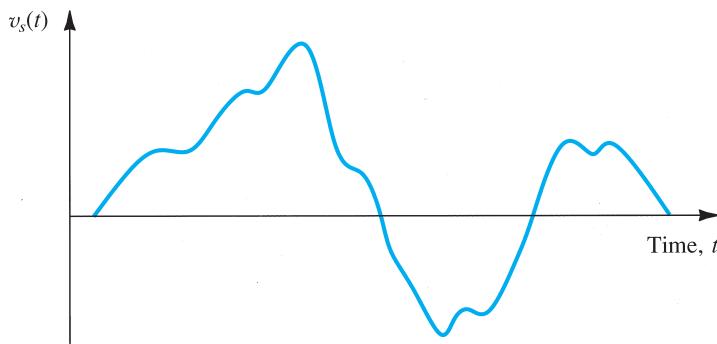
**Ans.** 1 k $\Omega$

- 1.3** A signal source that is most conveniently represented by its Thévenin equivalent has  $v_s = 10$  mV and  $R_s = 1$  k $\Omega$ . If the source feeds a load resistance  $R_L$ , find the voltage  $v_o$  that appears across the load for  $R_L = 100$  k $\Omega$ , 10 k $\Omega$ , 1 k $\Omega$ , and 100  $\Omega$ . Also, find the lowest permissible value of  $R_L$  for which the output voltage is at least 80% of the source voltage.

**Ans.** 9.9 mV; 9.1 mV; 5 mV; 0.9 mV; 4 k $\Omega$

- 1.4** A signal source that is most conveniently represented by its Norton equivalent form has  $i_s = 10$   $\mu$ A and  $R_s = 100$  k $\Omega$ . If the source feeds a load resistance  $R_L$ , find the current  $i_o$  that flows through the load for  $R_L = 1$  k $\Omega$ , 10 k $\Omega$ , 100 k $\Omega$ , and 1 M $\Omega$ . Also, find the largest permissible value of  $R_L$  for which the load current is at least 80% of the source current.

**Ans.** 9.9  $\mu$ A; 9.1  $\mu$ A; 5  $\mu$ A; 0.9  $\mu$ A; 25 k $\Omega$



**Figure 1.3** An arbitrary voltage signal  $v_s(t)$ .

From the discussion above, it should be apparent that a signal is a time-varying quantity that can be represented by a graph such as that shown in Fig. 1.3. In fact, the information content of the signal is represented by the changes in its magnitude as time progresses; that is, the information is contained in the “wiggles” in the signal waveform. In general, such waveforms are difficult to characterize mathematically. In other words, it is not easy to describe succinctly an arbitrary-looking waveform such as that of Fig. 1.3. Of course, such a description is of great importance for the purpose of designing appropriate signal-processing circuits that perform desired functions on the given signal. An effective approach to signal characterization is studied in the next section.

## 1.2 Frequency Spectrum of Signals

An extremely useful characterization of a signal, and for that matter of any arbitrary function of time, is in terms of its **frequency spectrum**. Such a description of signals is obtained through the mathematical tools of **Fourier series** and **Fourier transform**.<sup>1</sup> We are not interested here in the details of these transformations; suffice it to say that they provide the means for representing a voltage signal  $v_s(t)$  or a current signal  $i_s(t)$  as the sum of sine-wave signals of different frequencies and amplitudes. This makes the sine wave a very important signal in the analysis, design, and testing of electronic circuits. Therefore, we shall briefly review the properties of the sinusoid.

Figure 1.4 shows a sine-wave voltage signal  $v_a(t)$ ,

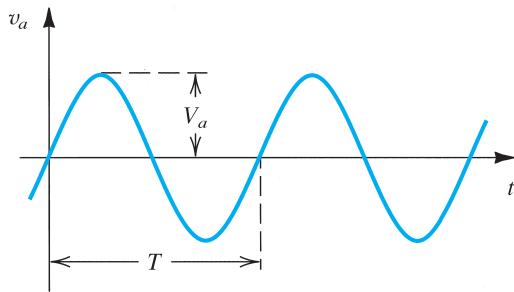
$$v_a(t) = V_a \sin \omega t \quad (1.1)$$

where  $V_a$  denotes the peak value or amplitude in volts and  $\omega$  denotes the angular frequency in radians per second; that is,  $\omega = 2\pi f$  rad/s, where  $f$  is the frequency in hertz,  $f = 1/T$  Hz, and  $T$  is the period in seconds.

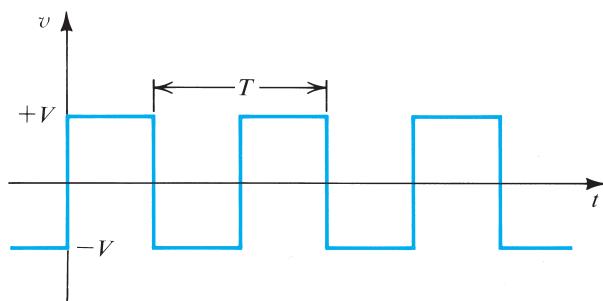
The sine-wave signal is completely characterized by its peak value  $V_a$ , its frequency  $\omega$ , and its phase with respect to an arbitrary reference time. In the case depicted in Fig. 1.4, the time

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<sup>1</sup>The reader who has not yet studied these topics should not be alarmed. No detailed application of this material will be made until Chapter 10. Nevertheless, a general understanding of Section 1.2 should be very helpful in studying early parts of this book.



**Figure 1.4** Sine-wave voltage signal of amplitude  $V_a$  and frequency  $f = 1/T$  Hz. The angular frequency  $\omega = 2\pi f$  rad/s.



**Figure 1.5** A symmetrical square-wave signal of amplitude  $V$ .

origin has been chosen so that the phase angle is 0. It should be mentioned that it is common to express the amplitude of a sine-wave signal in terms of its root-mean-square (rms) value, which is equal to the peak value divided by  $\sqrt{2}$ . Thus the rms value of the sinusoid  $v_a(t)$  of Fig. 1.4 is  $V_a/\sqrt{2}$ . For instance, when we speak of the wall power supply in our homes as being 120 V, we mean that it has a sine waveform of  $120\sqrt{2}$  volts peak value.

Returning now to the representation of signals as the sum of sinusoids, we note that the Fourier series is utilized to accomplish this task for the special case of a signal that is a periodic function of time. On the other hand, the Fourier transform is more general and can be used to obtain the frequency spectrum of a signal whose waveform is an arbitrary function of time.

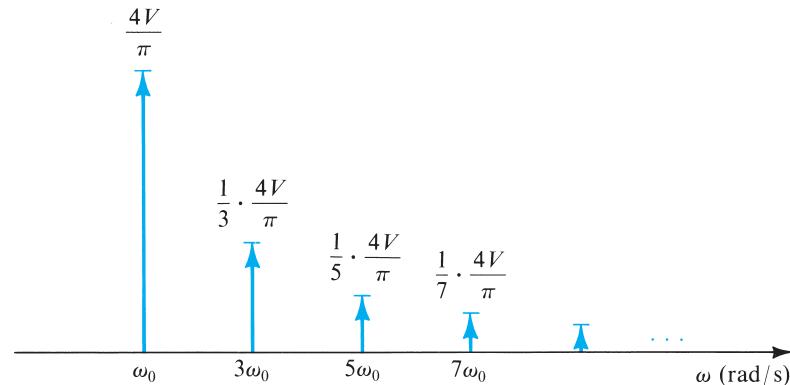
The Fourier series allows us to express a given periodic function of time as the sum of an infinite number of sinusoids whose frequencies are harmonically related. For instance, the symmetrical square-wave signal in Fig. 1.5 can be expressed as

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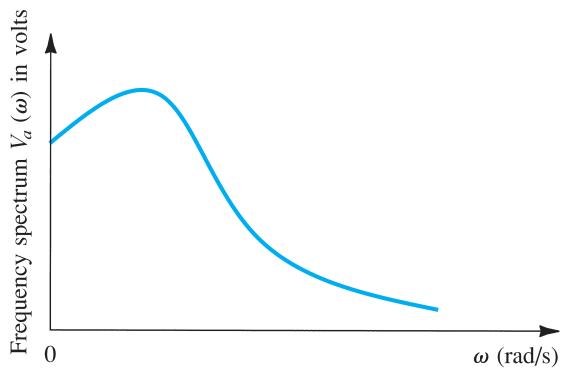
$$v(t) = \frac{4V}{\pi} \left( \sin \omega_0 t + \frac{1}{3} \sin 3\omega_0 t + \frac{1}{5} \sin 5\omega_0 t + \dots \right) \quad (1.2)$$

where  $V$  is the amplitude of the square wave and  $\omega_0 = 2\pi/T$  ( $T$  is the period of the square wave) is called the **fundamental frequency**. Note that because the amplitudes of the harmonics progressively decrease, the infinite series can be truncated, with the truncated series providing an approximation to the square waveform.

The sinusoidal components in the series of Eq. (1.2) constitute the frequency spectrum of the square-wave signal. Such a spectrum can be graphically represented as in Fig. 1.6, where the horizontal axis represents the angular frequency  $\omega$  in radians per second.



**Figure 1.6** The frequency spectrum (also known as the **line spectrum**) of the periodic square wave of Fig. 1.5.



**Figure 1.7** The frequency spectrum of an arbitrary waveform such as that in Fig. 1.3.

The Fourier transform can be applied to a nonperiodic function of time, such as that depicted in Fig. 1.3, and provides its frequency spectrum as a continuous function of frequency, as indicated in Fig. 1.7. Unlike the case of periodic signals, where the spectrum consists of discrete frequencies (at  $\omega_0$  and its harmonics), the spectrum of a nonperiodic signal contains in general all possible frequencies. Nevertheless, the essential parts of the spectra of practical signals are usually confined to relatively short segments of the frequency ( $\omega$ ) axis—an observation that is very useful in the processing of such signals. For instance, the spectrum of audible sounds such as speech and music extends from about 20 Hz to about 20 kHz—a frequency range known as the **audio band**. Here we should note that although some musical tones have frequencies above 20 kHz, the human ear is incapable of hearing frequencies that are much above 20 kHz. As another example, analog video signals have their spectra in the range of 0 MHz to 4.5 MHz.

We conclude this section by noting that a signal can be represented either by the manner in which its waveform varies with time, as for the voltage signal  $v_a(t)$  shown in Fig. 1.3, or in terms of its frequency spectrum, as in Fig. 1.7. The two alternative representations are known as the time-domain representation and the frequency-domain representation, respectively. The frequency-domain representation of  $v_a(t)$  will be denoted by the symbol  $V_a(\omega)$ .

## EXERCISES

- 1.5** Find the frequencies  $f$  and  $\omega$  of a sine-wave signal with a period of 1 ms.

**Ans.**  $f = 1000 \text{ Hz}$ ;  $\omega = 2\pi \times 10^3 \text{ rad/s}$

- 1.6** What is the period  $T$  of sine waveforms characterized by frequencies of (a)  $f = 60 \text{ Hz}$ ? (b)  $f = 10^{-3} \text{ Hz}$ ? (c)  $f = 1 \text{ MHz}$ ?

**Ans.** 16.7 ms; 1000 s; 1  $\mu\text{s}$

- 1.7** The UHF (ultra high frequency) television broadcast band begins with channel 14 and extends from 470 MHz to 806 MHz. If 6 MHz is allocated for each channel, how many channels can this band accommodate?

**Ans.** 56; channels 14 to 69

- 1.8** When the square-wave signal of Fig. 1.5, whose Fourier series is given in Eq. (1.2), is applied to a resistor, the total power dissipated may be calculated directly using the relationship  $P = 1/T \int_0^T (v^2/R) dt$  or indirectly by summing the contribution of each of the harmonic components, that is,  $P = P_1 + P_3 + P_5 + \dots$ , which may be found directly from rms values. Verify that the two approaches are equivalent. What fraction of the energy of a square wave is in its fundamental? In its first five harmonics? In its first seven? First nine? In what number of harmonics is 90% of the energy? (Note that in counting harmonics, the fundamental at  $\omega_0$  is the first, the one at  $2\omega_0$  is the second, etc.)

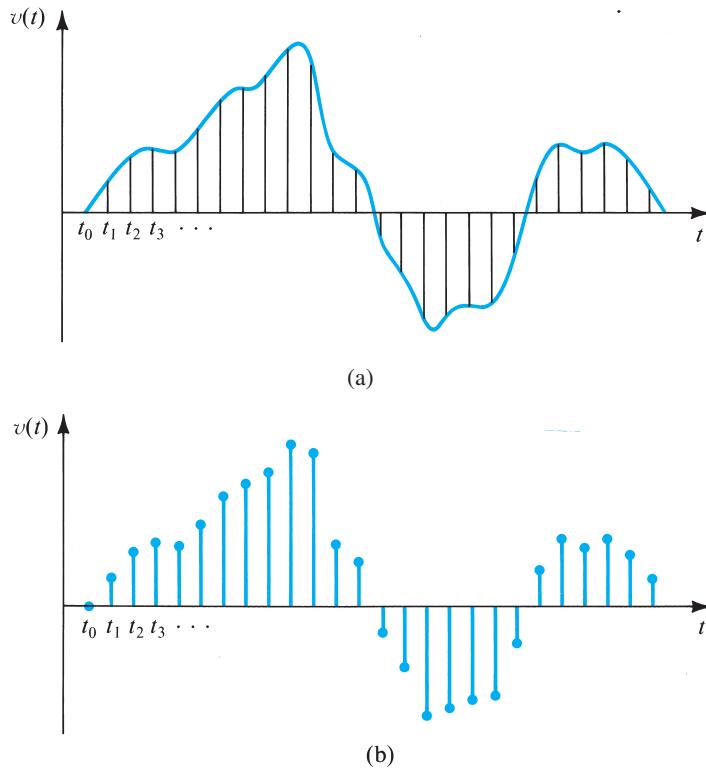
**Ans.** 0.81; 0.93; 0.95; 0.96; 3

## 1.3 Analog and Digital Signals

The voltage signal depicted in Fig. 1.3 is called an **analog signal**. The name derives from the fact that such a signal is *analogous* to the physical signal that it represents. The magnitude of an analog signal can take on any value; that is, the amplitude of an analog signal exhibits a continuous variation over its range of activity. The vast majority of signals in the world around us are analog. Electronic circuits that process such signals are known as **analog circuits**. A variety of analog circuits will be studied in this book.

An alternative form of signal representation is that of a sequence of numbers, each number representing the signal magnitude at an instant of time. The resulting signal is called a **digital signal**. To see how a signal can be represented in this form—that is, how signals can be converted from analog to digital form—consider Fig. 1.8(a). Here the curve represents a voltage signal, identical to that in Fig. 1.3. At equal intervals along the time axis, we have marked the time instants  $t_0, t_1, t_2$ , and so on. At each of these time instants, the magnitude of the signal is measured, a process known as **sampling**. Figure 1.8(b) shows a representation of the signal of Fig. 1.8(a) in terms of its samples. The signal of Fig. 1.8(b) is defined only at the sampling instants; it no longer is a continuous function of time; rather, it is a **discrete-time signal**. However, since the magnitude of each sample can take any value in a continuous range, the signal in Fig. 1.8(b) is still an analog signal.

Now if we represent the magnitude of each of the signal samples in Fig. 1.8(b) by a number having a finite number of digits, then the signal amplitude will no longer be continuous; rather,



**Figure 1.8** Sampling the continuous-time analog signal in (a) results in the discrete-time signal in (b).

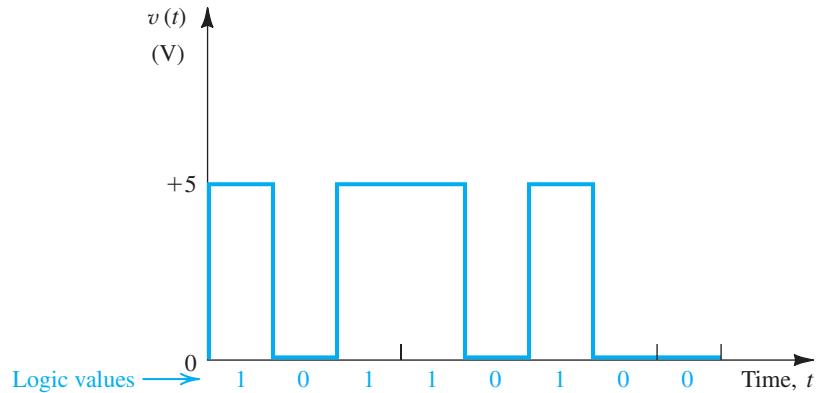
it is said to be **quantized**, **discretized**, or **digitized**. The resulting digital signal then is simply a sequence of numbers that represent the magnitudes of the successive signal samples.

The choice of number system to represent the signal samples affects the type of digital signal produced and has a profound effect on the complexity of the digital circuits required to process the signals. It turns out that the **binary** number system results in the simplest possible digital signals and circuits. In a binary system, each digit in the number takes on one of only two possible values, denoted 0 and 1. Correspondingly, the digital signals in binary systems need have only two voltage levels, which can be labeled low and high. As an example, in some of the digital circuits studied in this book, the levels are 0 V and +5 V. Figure 1.9 shows the time variation of such a digital signal. Observe that the waveform is a pulse train with 0 V representing a 0 signal, or logic 0, and +5 V representing logic 1.

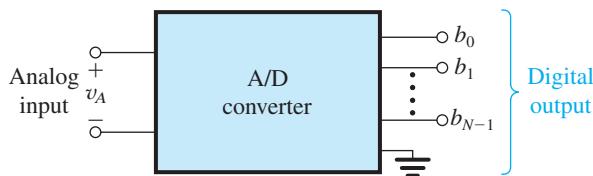
If we use  $N$  *binary digits* (bits) to represent each sample of the analog signal, then the digitized sample value can be expressed as

$$D = b_0 2^0 + b_1 2^1 + b_2 2^2 + \cdots + b_{N-1} 2^{N-1} \quad (1.3)$$

where  $b_0, b_1, \dots, b_{N-1}$  denote the  $N$  bits and have values of 0 or 1. Here bit  $b_0$  is the **least significant bit (LSB)**, and bit  $b_{N-1}$  is the **most significant bit (MSB)**. Conventionally, this binary number is written as  $b_{N-1} b_{N-2} \dots b_0$ . We observe that such a representation quantizes the analog sample into one of  $2^N$  levels. Obviously the greater the number of bits (i.e., the larger the  $N$ ), the closer the digital word  $D$  approximates the magnitude of the analog sample. That is, increasing the number of bits reduces the *quantization error* and increases the resolution of the



**Figure 1.9** Variation of a particular binary digital signal with time.



**Figure 1.10** Block-diagram representation of the analog-to-digital converter (ADC).

analog-to-digital conversion. This improvement is, however, usually obtained at the expense of more complex and hence more costly circuit implementations. It is not our purpose here to delve into this topic any deeper; we merely want the reader to appreciate the nature of analog and digital signals. Nevertheless, it is an opportune time to introduce a very important circuit building block of modern electronic systems: the **analog-to-digital converter (A/D or ADC)** shown in block form in Fig. 1.10. The ADC accepts at its input the samples of an analog signal and provides for each input sample the corresponding  $N$ -bit digital representation (according to Eq. 1.3) at its  $N$  output terminals. Thus although the voltage at the input might be, say, 6.51 V, at each of the output terminals (say, at the  $i$ th terminal), the voltage will be either low (0 V) or high (5 V) if  $b_i$  is supposed to be 0 or 1, respectively. The dual circuit of the ADC is the **digital-to-analog converter (D/A or DAC)**. It converts an  $N$ -bit digital input to an analog output voltage.

Once the signal is in digital form, it can be processed using **digital circuits**. Of course digital circuits can deal also with signals that do not have an analog origin, such as the signals that represent the various instructions of a digital computer.

Since digital circuits deal exclusively with binary signals, their design is simpler than that of analog circuits. Furthermore, digital systems can be designed using a relatively few different kinds of digital circuit blocks. However, a large number (e.g., hundreds of thousands or even millions) of each of these blocks are usually needed. Thus the design of digital circuits poses its own set of challenges to the designer but provides reliable and economic implementations of a great variety of signal-processing functions, many of which are not possible with analog circuits. At the present time, more and more of the signal-processing functions are being performed digitally. Examples around us abound: from the digital watch and the calculator to digital audio systems, digital cameras, and digital television. Moreover, some long-standing

analog systems such as the telephone communication system are now almost entirely digital. And we should not forget the most important of all digital systems, the digital computer.

The basic building blocks of digital systems are logic circuits and memory circuits. We shall study both in this book, beginning in Chapter 14.

One final remark: Although the digital processing of signals is at present all-pervasive, there remain many signal-processing functions that are best performed by analog circuits. Indeed, many electronic systems include both analog and digital parts. It follows that a good electronics engineer must be proficient in the design of both analog and digital circuits, or **mixed-signal** or **mixed-mode** design as it is currently known. Such is the aim of this book.

## EXERCISE

- 1.9** Consider a 4-bit digital word  $D = b_3b_2b_1b_0$  (see Eq. 1.3) used to represent an analog signal  $v_A$  that varies between 0 V and +15 V.
- Give  $D$  corresponding to  $v_A = 0$  V, 1 V, 2 V, and 15 V.
  - What change in  $v_A$  causes a change from 0 to 1 in (i)  $b_0$ , (ii)  $b_1$ , (iii)  $b_2$ , and (iv)  $b_3$ ?
  - If  $v_A = 5.2$  V, what do you expect  $D$  to be? What is the resulting error in representation?
- Ans.** (a) 0000, 0001, 0010, 1111; (b) +1 V, +2 V, +4 V, +8 V; (c) 0101, -4%

### ANALOG VS. DIGITAL CIRCUIT ENGINEERS:

As digital became the preferred implementation of more and more signal-processing functions, the need arose for greater numbers of digital circuit design engineers. Yet despite predictions made periodically that the demand for analog circuit design engineers would lessen, this has not been the case. Rather, the demand for analog engineers has, if anything, increased. What is true, however, is that the skill level required of analog engineers has risen. Not only are they asked to design circuits of greater sophistication and tighter specifications, but they also have to do this using technologies that are optimized for digital (and not analog) circuits. This is dictated by economics, as digital usually constitutes the larger part of most systems.

## 1.4 Amplifiers

In this section, we shall introduce the most fundamental signal-processing function, one that is employed in some form in almost every electronic system, namely, signal amplification. We shall study the amplifier as a circuit building block; that is, we shall consider its external characteristics and leave the design of its internal circuit to later chapters.

### 1.4.1 Signal Amplification

From a conceptual point of view the simplest signal-processing task is that of **signal amplification**. The need for amplification arises because transducers provide signals that

are said to be “weak,” that is, in the microvolt ( $\mu\text{V}$ ) or millivolt (mV) range and possessing little energy. Such signals are too small for reliable processing, and processing is much easier if the signal magnitude is made larger. The functional block that accomplishes this task is the **signal amplifier**.

It is appropriate at this point to discuss the need for **linearity** in amplifiers. Care must be exercised in the amplification of a signal, so that the information contained in the signal is not changed and no new information is introduced. Thus when we feed the signal shown in Fig. 1.3 to an amplifier, we want the output signal of the amplifier to be an exact replica of that at the input, except of course for having larger magnitude. In other words, the “wiggles” in the output waveform must be identical to those in the input waveform. Any change in waveform is considered to be **distortion** and is obviously undesirable.

An amplifier that preserves the details of the signal waveform is characterized by the relationship

$$v_o(t) = Av_i(t) \quad (1.4)$$

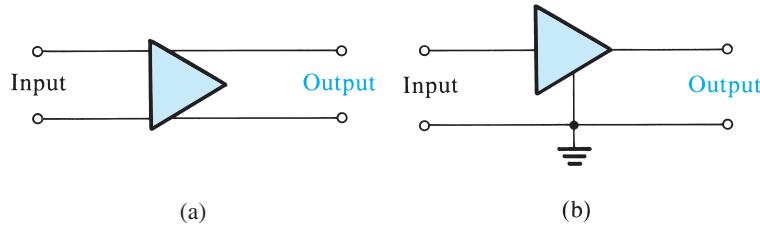
where  $v_i$  and  $v_o$  are the input and output signals, respectively, and  $A$  is a constant representing the magnitude of amplification, known as **amplifier gain**. Equation (1.4) is a linear relationship; hence the amplifier it describes is a **linear amplifier**. It should be easy to see that if the relationship between  $v_o$  and  $v_i$  contains higher powers of  $v_i$ , then the waveform of  $v_o$  will no longer be identical to that of  $v_i$ . The amplifier is then said to exhibit **nonlinear distortion**.

The amplifiers discussed so far are primarily intended to operate on very small input signals. Their purpose is to make the signal magnitude larger, and therefore they are thought of as **voltage amplifiers**. The **preamplifier** in the home stereo system is an example of a voltage amplifier.

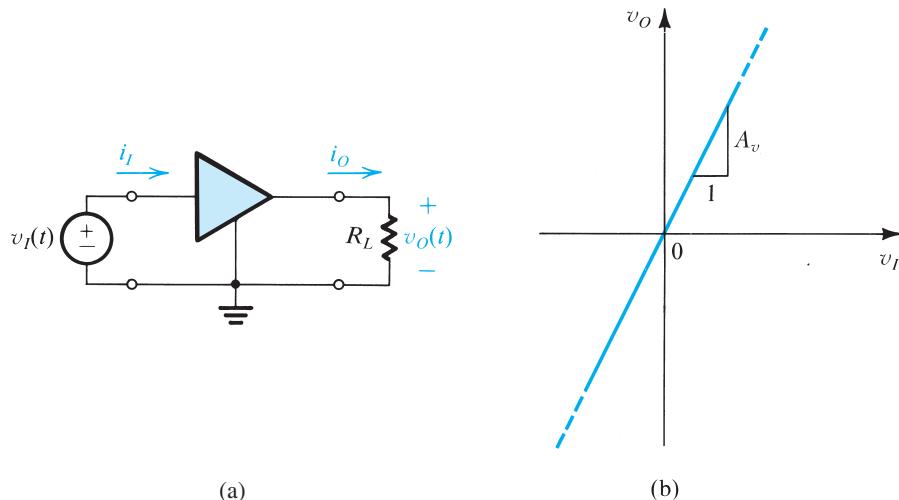
At this time we wish to mention another type of amplifier, namely, the **power amplifier**. Such an amplifier may provide only a modest amount of voltage gain but substantial current gain. Thus while absorbing little power from the input signal source to which it is connected, often a preamplifier, it delivers large amounts of power to its load. An example is found in the power amplifier of the home stereo system, whose purpose is to provide sufficient power to drive the loudspeaker, which is the amplifier load. Here we should note that the loudspeaker is the output transducer of the stereo system; it converts the electric output signal of the system into an acoustic signal. A further appreciation of the need for linearity can be acquired by reflecting on the power amplifier. A linear power amplifier causes both soft and loud music passages to be reproduced without distortion.

### 1.4.2 Amplifier Circuit Symbol

The signal amplifier is obviously a two-port circuit. Its function is conveniently represented by the circuit symbol of Fig. 1.11(a). This symbol clearly distinguishes the input and output ports and indicates the direction of signal flow. Thus, in subsequent diagrams it will not be necessary to label the two ports “input” and “output.” For generality we have shown the amplifier to have two input terminals that are distinct from the two output terminals. A more common situation is illustrated in Fig. 1.11(b), where a common terminal exists between the input and output ports of the amplifier. This common terminal is used as a reference point and is called the **circuit ground**.



**Figure 1.11** (a) Circuit symbol for amplifier. (b) An amplifier with a common terminal (ground) between the input and output ports.



**Figure 1.12** (a) A voltage amplifier fed with a signal  $v_I(t)$  and connected to a load resistance  $R_L$ . (b) Transfer characteristic of a linear voltage amplifier with voltage gain  $A_v$ .

### 1.4.3 Voltage Gain

A linear amplifier accepts an input signal  $v_I(t)$  and provides at the output, across a load resistance  $R_L$  (see Fig. 1.12(a)), an output signal  $v_o(t)$  that is a magnified replica of  $v_I(t)$ . The **voltage gain** of the amplifier is defined by

$$\text{Voltage gain } (A_v) = \frac{v_o}{v_I} \quad (1.5)$$

Fig. 1.12(b) shows the **transfer characteristic** of a linear amplifier. If we apply to the input of this amplifier a sinusoidal voltage of amplitude  $\hat{V}$ , we obtain at the output a sinusoid of amplitude  $A_v \hat{V}$ .

### 1.4.4 Power Gain and Current Gain

An amplifier increases the signal power, an important feature that distinguishes an amplifier from a transformer. In the case of a transformer, although the voltage delivered to the load could be greater than the voltage feeding the input side (the primary), the power delivered to the load (from the secondary side of the transformer) is less than or at most equal to the

power supplied by the signal source. On the other hand, an amplifier provides the load with power greater than that obtained from the signal source. That is, amplifiers have power gain. The **power gain** of the amplifier in Fig. 1.12(a) is defined as

➤ Power gain ( $A_p$ )  $\equiv \frac{\text{load power } (P_L)}{\text{input power } (P_i)}$  (1.6)

➤  $= \frac{v_o i_o}{v_i i_l}$  (1.7)

where  $i_o$  is the current that the amplifier delivers to the load ( $R_L$ ),  $i_o = v_o/R_L$ , and  $i_l$  is the current the amplifier draws from the signal source. The **current gain** of the amplifier is defined as

➤ Current gain ( $A_i$ )  $\equiv \frac{i_o}{i_l}$  (1.8)

From Eqs. (1.5) to (1.8) we note that

➤  $A_p = A_v A_i$  (1.9)

### 1.4.5 Expressing Gain in Decibels

The amplifier gains defined above are ratios of similarly dimensioned quantities. Thus they will be expressed either as dimensionless numbers or, for emphasis, as V/V for the voltage gain, A/A for the current gain, and W/W for the power gain. Alternatively, for a number of reasons, some of them historic, electronics engineers express amplifier gain with a logarithmic measure. Specifically the voltage gain  $A_v$  can be expressed as

➤ Voltage gain in decibels  $= 20 \log |A_v| \text{ dB}$

and the current gain  $A_i$  can be expressed as

➤ Current gain in decibels  $= 20 \log |A_i| \text{ dB}$

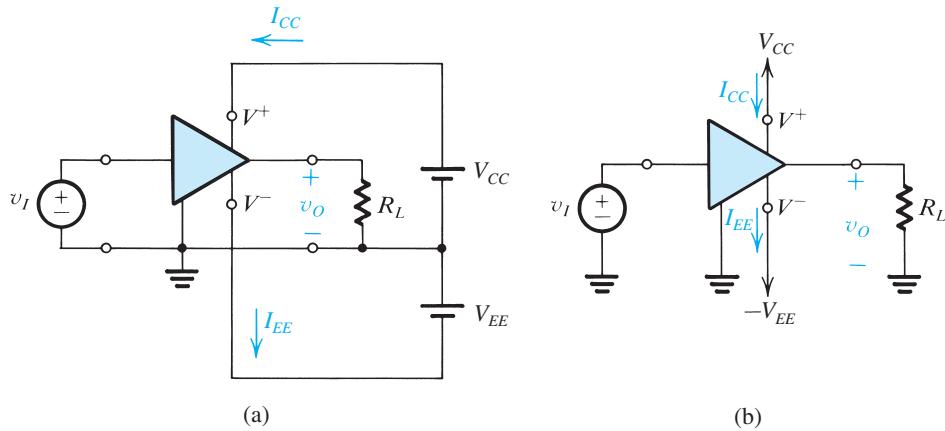
Since power is related to voltage (or current) squared, the power gain  $A_p$  can be expressed in decibels as

➤ Power gain in decibels  $= 10 \log A_p \text{ dB}$

The absolute values of the voltage and current gains are used because in some cases  $A_v$  or  $A_i$  will be a negative number. A negative gain  $A_v$  simply means that there is a 180° phase difference between input and output signals; it does not imply that the amplifier is **attenuating** the signal. On the other hand, an amplifier whose voltage gain is, say, -20 dB is in fact attenuating the input signal by a factor of 10 (i.e.,  $A_v = 0.1 \text{ V/V}$ ).

### 1.4.6 The Amplifier Power Supplies

Since the power delivered to the load is greater than the power drawn from the signal source, the question arises as to the source of this additional power. The answer is found by observing that amplifiers need dc power supplies for their operation. These dc sources supply the extra power delivered to the load as well as any power that might be dissipated in the internal circuit



**Figure 1.13** An amplifier that requires two dc supplies (shown as batteries) for operation.

of the amplifier (such power is converted to heat). In Fig. 1.12(a) we have not explicitly shown these dc sources.

Figure 1.13(a) shows an amplifier that requires two dc sources: one positive of value  $V_{CC}$  and one negative of value  $V_{EE}$ . The amplifier has two terminals, labeled  $V^+$  and  $V^-$ , for connection to the dc supplies. For the amplifier to operate, the terminal labeled  $V^+$  has to be connected to the positive side of a dc source whose voltage is  $V_{CC}$  and whose negative side is connected to the circuit ground. Also, the terminal labeled  $V^-$  has to be connected to the negative side of a dc source whose voltage is  $V_{EE}$  and whose positive side is connected to the circuit ground. Now, if the current drawn from the positive supply is denoted  $I_{CC}$  and that from the negative supply is  $I_{EE}$  (see Fig. 1.13a), then the dc power delivered to the amplifier is

$$P_{dc} = V_{CC}I_{CC} + V_{EE}I_{EE}$$

If the power dissipated in the amplifier circuit is denoted  $P_{\text{dissipated}}$ , the power-balance equation for the amplifier can be written as

$$P_{dc} + P_I = P_L + P_{\text{dissipated}}$$

where  $P_I$  is the power drawn from the signal source and  $P_L$  is the power delivered to the load. Since the power drawn from the signal source is usually small, the amplifier power **efficiency** is defined as

$$\eta \equiv \frac{P_L}{P_{dc}} \times 100 \quad (1.10)$$

The power efficiency is an important performance parameter for amplifiers that handle large amounts of power. Such amplifiers, called power amplifiers, are used, for example, as output amplifiers of stereo systems.

In order to simplify circuit diagrams, we shall adopt the convention illustrated in Fig. 1.13(b). Here the  $V^+$  terminal is shown connected to an arrowhead pointing upward and the  $V^-$  terminal to an arrowhead pointing downward. The corresponding voltage is indicated next to each arrowhead. Note that in many cases we will not explicitly show the connections

of the amplifier to the dc power sources. Finally, we note that some amplifiers require only one power supply.

### Example 1.2

Consider an amplifier operating from  $\pm 10\text{-V}$  power supplies. It is fed with a sinusoidal voltage having  $1\text{ V}$  peak and delivers a sinusoidal voltage output of  $9\text{ V}$  peak to a  $1\text{-k}\Omega$  load. The amplifier draws a current of  $9.5\text{ mA}$  from each of its two power supplies. The input current of the amplifier is found to be sinusoidal with  $0.1\text{ mA}$  peak. Find the voltage gain, the current gain, the power gain, the power drawn from the dc supplies, the power dissipated in the amplifier, and the amplifier efficiency.

#### Solution

$$A_v = \frac{9}{1} = 9 \text{ V/V}$$

or

$$A_v = 20 \log 9 = 19.1 \text{ dB}$$

$$\hat{I}_o = \frac{9 \text{ V}}{1 \text{ k}\Omega} = 9 \text{ mA}$$

$$A_i = \frac{\hat{I}_o}{\hat{I}_i} = \frac{9}{0.1} = 90 \text{ A/A}$$

or

$$A_i = 20 \log 90 = 39.1 \text{ dB}$$

$$P_L = V_{o_{\text{rms}}} I_{o_{\text{rms}}} = \frac{9}{\sqrt{2}} \frac{9}{\sqrt{2}} = 40.5 \text{ mW}$$

$$P_I = V_{i_{\text{rms}}} I_{i_{\text{rms}}} = \frac{1}{\sqrt{2}} \frac{0.1}{\sqrt{2}} = 0.05 \text{ mW}$$

$$A_p = \frac{P_L}{P_I} = \frac{40.5}{0.05} = 810 \text{ W/W}$$

or

$$A_p = 10 \log 810 = 29.1 \text{ dB}$$

$$P_{dc} = 10 \times 9.5 + 10 \times 9.5 = 190 \text{ mW}$$

$$\begin{aligned} P_{\text{dissipated}} &= P_{dc} + P_I - P_L \\ &= 190 + 0.05 - 40.5 = 149.6 \text{ mW} \end{aligned}$$

$$\eta = \frac{P_L}{P_{dc}} \times 100 = 21.3\%$$

From the above example we observe that the amplifier converts some of the dc power it draws from the power supplies to signal power that it delivers to the load.

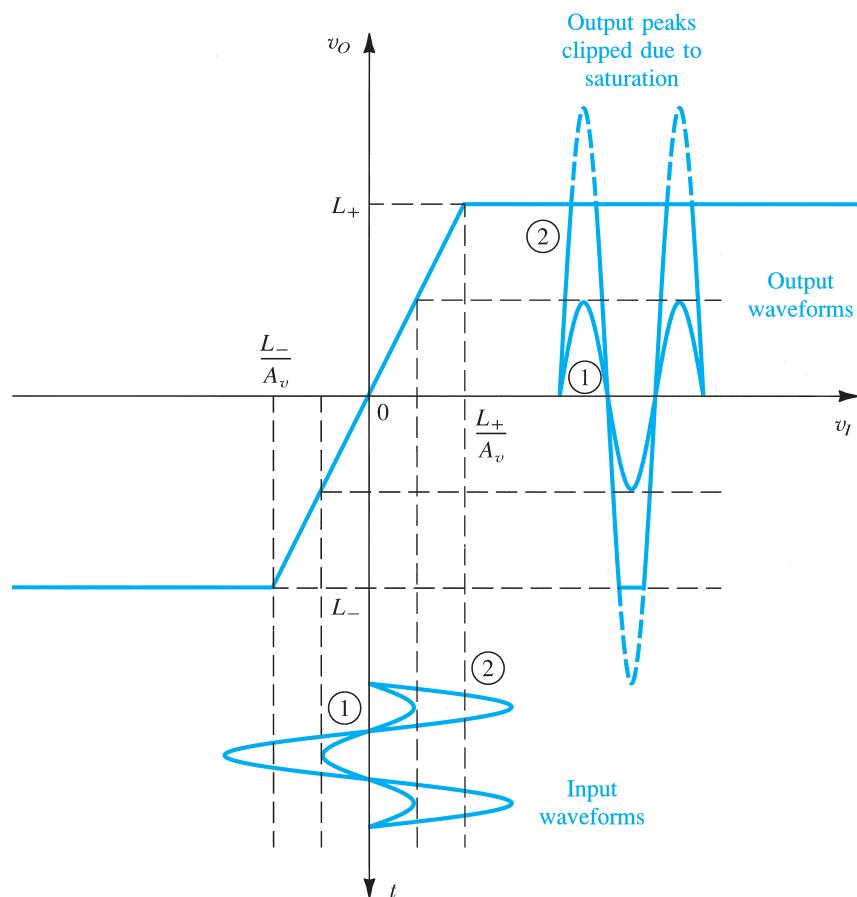
### 1.4.7 Amplifier Saturation

Practically speaking, the amplifier transfer characteristic remains linear over only a limited range of input and output voltages. For an amplifier operated from two power supplies the output voltage cannot exceed a specified positive limit and cannot decrease below a specified negative limit. The resulting transfer characteristic is shown in Fig. 1.14, with the positive and negative saturation levels denoted  $L_+$  and  $L_-$ , respectively. Each of the two saturation levels is usually within a fraction of a volt of the voltage of the corresponding power supply.

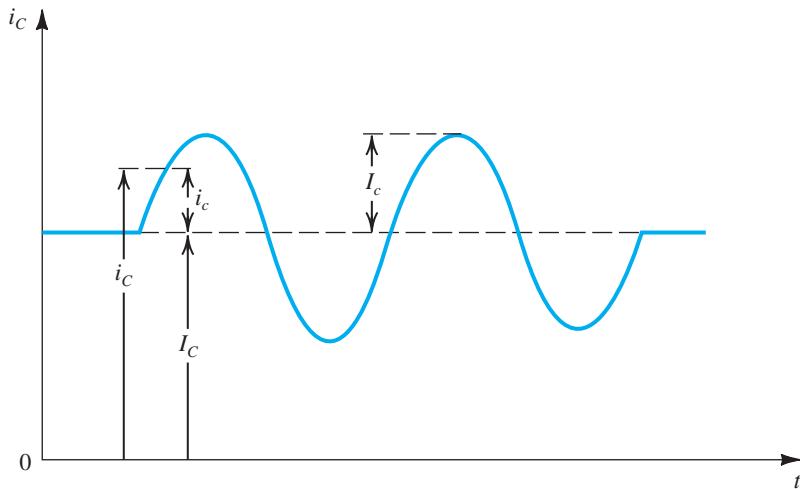
Obviously, in order to avoid distorting the output signal waveform, the input signal swing must be kept within the linear range of operation,

$$\frac{L_-}{A_v} \leq v_I \leq \frac{L_+}{A_v}$$

In Fig. 1.14, which shows two input waveforms and the corresponding output waveforms, the peaks of the larger waveform have been clipped off because of amplifier saturation.



**Figure 1.14** An amplifier transfer characteristic that is linear except for output saturation.



**Figure 1.15** Symbol convention employed throughout the book.

### 1.4.8 Symbol Convention

At this point, we draw the reader's attention to the terminology we shall employ throughout the book. To illustrate the terminology, Fig. 1.15 shows the waveform of a current  $i_C(t)$  that is flowing through a branch in a particular circuit. The current  $i_C(t)$  consists of a dc component  $I_C$  on which is superimposed a sinusoidal component  $i_c(t)$  whose peak amplitude is  $I_c$ . Observe that at a time  $t$ , the **total instantaneous** current  $i_C(t)$  is the sum of the dc current  $I_C$  and the signal current  $i_c(t)$ ,

$$i_C(t) = I_C + i_c(t) \quad (1.11)$$

where the signal current is given by

$$i_c(t) = I_c \sin \omega t$$

Thus, we state some conventions: Total instantaneous quantities are denoted by a lowercase symbol with uppercase subscript(s), for example,  $i_C(t)$ ,  $v_{DS}(t)$ . Direct-current (dc) quantities are denoted by an uppercase symbol with uppercase subscript(s), for example,  $I_C$ ,  $V_{DS}$ . Incremental signal quantities are denoted by a lowercase symbol with lowercase subscript(s), for example,  $i_c(t)$ ,  $v_{gs}(t)$ . If the signal is a sine wave, then its amplitude is denoted by an uppercase symbol with lowercase subscript(s), for example,  $I_c$ ,  $V_{gs}$ . Finally, although not shown in Fig. 1.15, dc power supplies are denoted by an uppercase letter with a double-letter uppercase subscript, for example,  $V_{CC}$ ,  $V_{DD}$ . A similar notation is used for the dc current drawn from the power supply, for example,  $I_{CC}$ ,  $I_{DD}$ .

## EXERCISES

- 1.10** An amplifier has a voltage gain of 100 V/V and a current gain of 1000 A/A. Express the voltage and current gains in decibels and find the power gain.

**Ans.** 40 dB; 60 dB; 50 dB

- 1.11** An amplifier operating from a single 15-V supply provides a 12-V peak-to-peak sine-wave signal to a 1-k $\Omega$  load and draws negligible input current from the signal source. The dc current drawn from the 15-V supply is 8 mA. What is the power dissipated in the amplifier, and what is the amplifier efficiency?

**Ans.** 102 mW; 15%

## 1.5 Circuit Models for Amplifiers

A substantial part of this book is concerned with the design of amplifier circuits that use transistors of various types. Such circuits will vary in complexity from those using a single transistor to those with 20 or more devices. In order to be able to apply the resulting amplifier circuit as a building block in a system, one must be able to characterize, or **model**, its terminal behavior. In this section, we study simple but effective amplifier models. These models apply irrespective of the complexity of the internal circuit of the amplifier. The values of the model parameters can be found either by analyzing the amplifier circuit or by performing measurements at the amplifier terminals.

### 1.5.1 Voltage Amplifiers

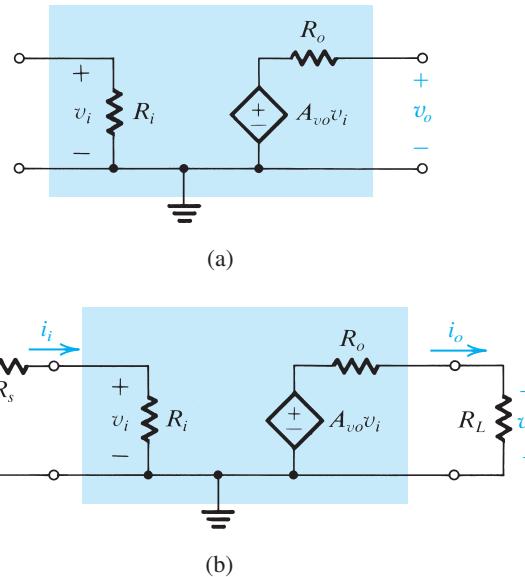
Figure 1.16(a) shows a circuit model for the voltage amplifier. The model consists of a voltage-controlled voltage source having a gain factor  $A_{vo}$ , an input resistance  $R_i$  that accounts for the fact that the amplifier draws an input current from the signal source, and an output resistance  $R_o$  that accounts for the change in output voltage as the amplifier is called upon to supply output current to a load. To be specific, we show in Fig. 1.16(b) the amplifier model fed with a signal voltage source  $v_s$  having a resistance  $R_s$  and connected at the output to a load resistance  $R_L$ . The nonzero output resistance  $R_o$  causes only a fraction of  $A_{vo}v_i$  to appear across the output. Using the voltage-divider rule we obtain

$$v_o = A_{vo}v_i \frac{R_L}{R_L + R_o}$$

Thus the voltage gain is given by

$$A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \quad (1.12)$$

It follows that in order not to lose gain in coupling the amplifier output to a load, the output resistance  $R_o$  should be much smaller than the load resistance  $R_L$ . In other words, for a given  $R_L$  one must design the amplifier so that its  $R_o$  is much smaller than  $R_L$ . Furthermore, there are applications in which  $R_L$  is known to vary over a certain range. In order to keep the output voltage  $v_o$  as constant as possible, the amplifier is designed with  $R_o$  much smaller than the lowest value of  $R_L$ . An ideal voltage amplifier is one with  $R_o = 0$ . Equation (1.12) indicates also that for  $R_L = \infty, A_v = A_{vo}$ . Thus  $A_{vo}$  is the voltage gain of the unloaded amplifier, or the **open-circuit voltage gain**. It should also be clear that in specifying the voltage gain of an amplifier, one must also specify the value of load resistance at which this gain is measured or



**Figure 1.16** (a) Circuit model for the voltage amplifier. (b) The voltage amplifier with input signal source and load.

calculated. If a load resistance is not specified, it is normally assumed that the given voltage gain is the open-circuit gain  $A_{vo}$ .

The finite input resistance  $R_i$  introduces another voltage-divider action at the input, with the result that only a fraction of the source signal  $v_s$  actually reaches the input terminals of the amplifier; that is,

$$v_i = v_s \frac{R_i}{R_i + R_s} \quad (1.13)$$

It follows that in order not to lose a significant portion of the input signal in coupling the signal source to the amplifier input, the amplifier must be designed to have an input resistance  $R_i$  much greater than the resistance of the signal source,  $R_i \gg R_s$ . Furthermore, there are applications in which the source resistance is known to vary over a certain range. To minimize the effect of this variation on the value of the signal that appears at the input of the amplifier, the design ensures that  $R_i$  is much greater than the largest value of  $R_s$ . An ideal voltage amplifier is one with  $R_i = \infty$ . In this ideal case both the current gain and power gain become infinite.

The overall voltage gain ( $v_o/v_s$ ) can be found by combining Eqs. (1.12) and (1.13),

$$\frac{v_o}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o}$$

There are situations in which one is interested not in voltage gain but only in a significant power gain. For instance, the source signal can have a respectable voltage but a source resistance that is much greater than the load resistance. Connecting the source directly to the load would result in significant signal attenuation. In such a case, one requires an amplifier with a high input resistance (much greater than the source resistance) and a low output resistance (much smaller than the load resistance) but with a modest voltage gain (or even unity gain).

Such an amplifier is referred to as a **buffer amplifier**. We shall encounter buffer amplifiers often throughout this book.

## EXERCISES

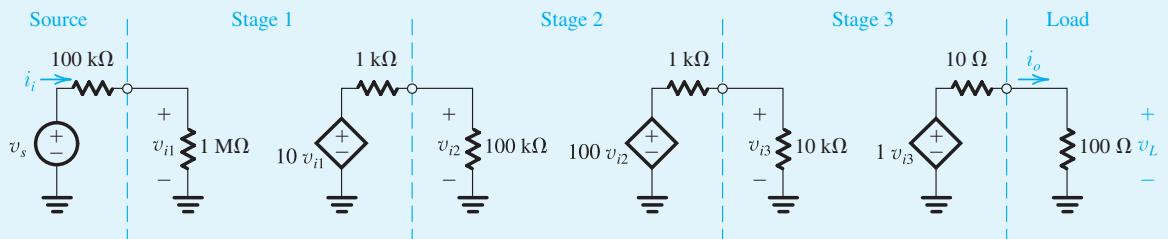
- 1.12** A transducer characterized by a voltage of 1 V rms and a resistance of  $1 \text{ M}\Omega$  is available to drive a  $10\text{-}\Omega$  load. If connected directly, what voltage and power levels result at the load? If a unity-gain (i.e.,  $A_{vo} = 1$ ) buffer amplifier with  $1\text{-M}\Omega$  input resistance and  $10\text{-}\Omega$  output resistance is interposed between source and load, what do the output voltage and power levels become? For the new arrangement, find the voltage gain from source to load, and the power gain (both expressed in decibels).  
**Ans.**  $10 \mu\text{V}$  rms;  $10^{-11} \text{ W}$ ;  $0.25 \text{ V}$ ;  $6.25 \text{ mW}$ ;  $-12 \text{ dB}$ ;  $44 \text{ dB}$
- 1.13** The output voltage of a voltage amplifier has been found to decrease by 20% when a load resistance of  $1 \text{ k}\Omega$  is connected. What is the value of the amplifier output resistance?  
**Ans.**  $250 \Omega$
- 1.14** An amplifier with a voltage gain of  $+40 \text{ dB}$ , an input resistance of  $10 \text{ k}\Omega$ , and an output resistance of  $1 \text{ k}\Omega$  is used to drive a  $1\text{-k}\Omega$  load. What is the value of  $A_{vo}$ ? Find the value of the power gain in decibels.  
**Ans.**  $100 \text{ V/V}$ ;  $44 \text{ dB}$

## 1.5.2 Cascaded Amplifiers

To meet given amplifier specifications, we often need to design the amplifier as a cascade of two or more stages. The stages are usually not identical; rather, each is designed to serve a specific purpose. For instance, in order to provide the overall amplifier with a large input resistance, the first stage is usually required to have a large input resistance. Also, in order to equip the overall amplifier with a low output resistance, the final stage in the cascade is usually designed to have a low output resistance. To illustrate the analysis and design of cascaded amplifiers, we consider a practical example.

### Example 1.3

Figure 1.17 depicts an amplifier composed of a cascade of three stages. The amplifier is fed by a signal source with a source resistance of  $100 \text{ k}\Omega$  and delivers its output into a load resistance of  $100 \Omega$ . The first stage has a relatively high input resistance and a modest gain factor of 10. The second stage has a higher gain factor but lower input resistance. Finally, the last, or output, stage has unity gain but a low output resistance. We wish to evaluate the overall voltage gain, that is,  $v_L/v_s$ , the current gain, and the power gain.

**Example 1.3** *continued***Figure 1.17** Three-stage amplifier for Example 1.3.**Solution**

The fraction of source signal appearing at the input terminals of the amplifier is obtained using the voltage-divider rule at the input, as follows:

$$\frac{v_{i1}}{v_s} = \frac{1 \text{ M}\Omega}{1 \text{ M}\Omega + 100 \text{ k}\Omega} = 0.909 \text{ V/V}$$

The voltage gain of the first stage is obtained by considering the input resistance of the second stage to be the load of the first stage; that is,

$$A_{v1} \equiv \frac{v_{i2}}{v_{i1}} = 10 \frac{100 \text{ k}\Omega}{100 \text{ k}\Omega + 1 \text{ k}\Omega} = 9.9 \text{ V/V}$$

Similarly, the voltage gain of the second stage is obtained by considering the input resistance of the third stage to be the load of the second stage,

$$A_{v2} \equiv \frac{v_{i3}}{v_{i2}} = 100 \frac{10 \text{ k}\Omega}{10 \text{ k}\Omega + 1 \text{ k}\Omega} = 90.9 \text{ V/V}$$

Finally, the voltage gain of the output stage is as follows:

$$A_{v3} \equiv \frac{v_L}{v_{i3}} = 1 \frac{100 \Omega}{100 \Omega + 10 \Omega} = 0.909 \text{ V/V}$$

The total gain of the three stages in cascade can now be found from

$$A_v \equiv \frac{v_L}{v_{i1}} = A_{v1} A_{v2} A_{v3} = 818 \text{ V/V}$$

or 58.3 dB.

To find the voltage gain from source to load, we multiply  $A_v$  by the factor representing the loss of gain at the input; that is,

$$\begin{aligned} \frac{v_L}{v_s} &= \frac{v_L}{v_{i1}} \frac{v_{i1}}{v_s} = A_v \frac{v_{i1}}{v_s} \\ &= 818 \times 0.909 = 743.6 \text{ V/V} \end{aligned}$$

or 57.4 dB.

The current gain is found as follows:

$$\begin{aligned} A_i &\equiv \frac{i_o}{i_i} = \frac{v_L/100\ \Omega}{v_{i1}/1\ M\Omega} \\ &= 10^4 \times A_v = 8.18 \times 10^6 \text{ A/A} \end{aligned}$$

or 138.3 dB.

The power gain is found from

$$\begin{aligned} A_p &\equiv \frac{P_L}{P_I} = \frac{v_L i_o}{v_{i1} i_i} \\ &= A_v A_i = 818 \times 8.18 \times 10^6 = 66.9 \times 10^8 \text{ W/W} \end{aligned}$$

or 98.3 dB. Note that

$$A_p(\text{dB}) = \frac{1}{2}[A_v(\text{dB}) + A_i(\text{dB})]$$

A few comments on the cascade amplifier in the above example are in order. To avoid losing signal strength at the amplifier input where the signal is usually very small, the first stage is designed to have a relatively large input resistance ( $1\ M\Omega$ ), which is much larger than the source resistance. The trade-off appears to be a moderate voltage gain (10 V/V). The second stage does not need to have such a high input resistance; rather, here we need to realize the bulk of the required voltage gain. The third and final, or output, stage is not asked to provide any voltage gain; rather, it functions as a buffer amplifier, providing a relatively large input resistance and a low output resistance, much lower than  $R_L$ . It is this stage that enables connecting the amplifier to the  $100\text{-}\Omega$  load. These points can be made more concrete by solving the following exercises. In so doing, observe that in finding the gain of an amplifier stage in a cascade amplifier, the loading effect of the succeeding amplifier stage must be taken into account as we have done in the above example.

## EXERCISES

- 1.15** What would the overall voltage gain of the cascade amplifier in Example 1.3 be without stage 3 (i.e., with the load resistance connected to the output of the second stage)?

**Ans.** 81.8 V/V; a decrease by a factor of 9.

- 1.16** For the cascade amplifier of Example 1.3, let  $v_s$  be 1 mV. Find  $v_{i1}$ ,  $v_{i2}$ ,  $v_{i3}$ , and  $v_L$ .

**Ans.** 0.91 mV; 9 mV; 818 mV; 744 mV

- 1.17** (a) Model the three-stage amplifier of Example 1.3 (without the source and load), using the voltage amplifier model of Fig. 1.16(a). What are the values of  $R_i$ ,  $A_{vo}$ , and  $R_o$ ?

(b) If  $R_L$  varies in the range  $10\ \Omega$  to  $1000\ \Omega$ , find the corresponding range of the overall voltage gain,  $v_o/v_s$ .

**Ans.**  $1\ M\Omega$ , 900 V/V,  $10\ \Omega$ ; 409 V/V to 810 V/V

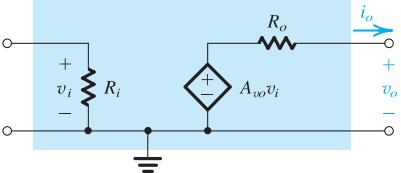
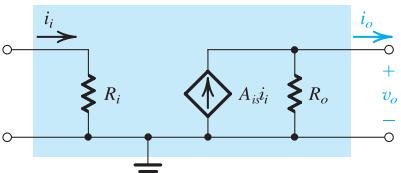
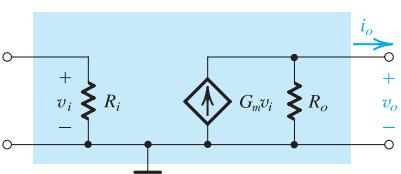
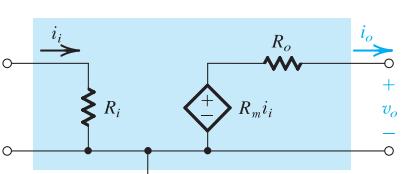
### 1.5.3 Other Amplifier Types

In the design of an electronic system, the signal of interest—whether at the system input, at an intermediate stage, or at the output—can be either a voltage or a current. For instance, some transducers have very high output resistances and can be more appropriately modeled as current sources. Similarly, there are applications in which the output current rather than the voltage is of interest. Thus, although it is the most popular, the voltage amplifier considered above is just one of four possible amplifier types. The other three are the current amplifier, the transconductance amplifier, and the transresistance amplifier. Table 1.1 shows the four amplifier types, their circuit models, the definition of their gain parameters, and the ideal values of their input and output resistances.

### 1.5.4 Relationships between the Four Amplifier Models

Although for a given amplifier a particular one of the four models in Table 1.1 is most preferable, *any of the four can be used to model any amplifier*. In fact, simple relationships can be derived to relate the parameters of the various models. For instance, the open-circuit

**Table 1.1** The Four Amplifier Types

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{vo} \equiv \frac{v_o}{v_i} \Big _{i_o=0}$ (V/V)	$R_i = \infty$ $R_o = 0$
Current Amplifier		Short-Circuit Current Gain $A_{is} \equiv \frac{i_o}{i_i} \Big _{v_o=0}$ (A/A)	$R_i = 0$ $R_o = \infty$
Transconductance Amplifier		Short-Circuit Transconductance $G_m \equiv \frac{i_o}{v_i} \Big _{v_o=0}$ (A/V)	$R_i = \infty$ $R_o = \infty$
Transresistance Amplifier		Open-Circuit Transresistance $R_m \equiv \frac{v_o}{i_i} \Big _{i_o=0}$ (V/A)	$R_i = 0$ $R_o = 0$

voltage gain  $A_{vo}$  can be related to the short-circuit current gain  $A_{is}$  as follows: The open-circuit output voltage given by the voltage amplifier model of Table 1.1 is  $A_{vo}v_i$ . The current amplifier model in the same table gives an open-circuit output voltage of  $A_{is}i_iR_o$ . Equating these two values and noting that  $i_i = v_i/R_i$  gives

$$A_{vo} = A_{is} \left( \frac{R_o}{R_i} \right) \quad (1.14)$$

Similarly, we can show that

$$A_{vo} = G_m R_o \quad (1.15)$$

and

$$A_{vo} = \frac{R_m}{R_i} \quad (1.16)$$

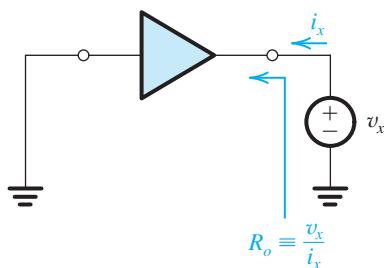
The expressions in Eqs. (1.14) to (1.16) can be used to relate any two of the gain parameters  $A_{vo}$ ,  $A_{is}$ ,  $G_m$ , and  $R_m$ .

### 1.5.5 Determining $R_i$ and $R_o$

From the amplifier circuit models given in Table 1.1, we observe that the input resistance  $R_i$  of the amplifier can be determined by applying an input voltage  $v_i$  and measuring (or calculating) the input current  $i_i$ ; that is,  $R_i = v_i/i_i$ . The output resistance is found as the ratio of the open-circuit output voltage to the short-circuit output current. Alternatively, the output resistance can be found by eliminating the input signal source (then  $i_i$  and  $v_i$  will both be zero) and applying a voltage signal  $v_x$  to the output of the amplifier, as shown in Fig. 1.18. If we denote the current drawn from  $v_x$  into the output terminals as  $i_x$  (note that  $i_x$  is opposite in direction to  $i_o$ ), then  $R_o = v_x/i_x$ . Although these techniques are conceptually correct, in actual practice more refined methods are employed in measuring  $R_i$  and  $R_o$ .

### 1.5.6 Unilateral Models

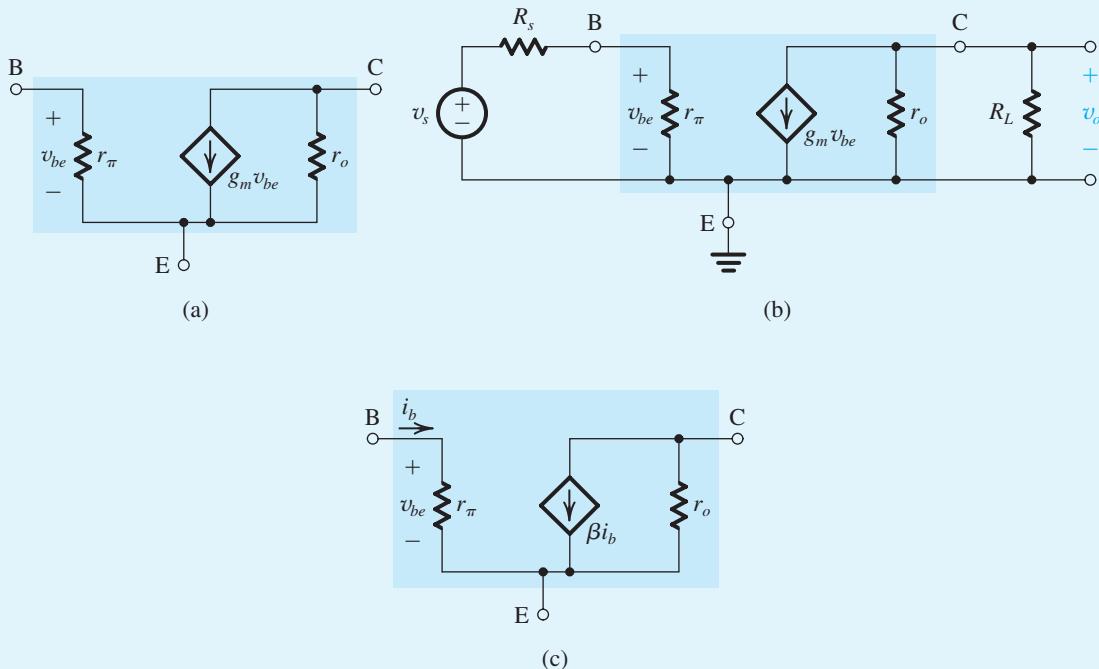
The amplifier models considered above are **unilateral**; that is, signal flow is unidirectional, from input to output. Most real amplifiers show some reverse transmission, which is usually undesirable but must nonetheless be modeled. We shall not pursue this point further at this time except to mention that more complete models for linear two-port networks are given in Appendix C. Also, in later chapters, we will find it necessary in certain cases to augment the models of Table 1.1 to take into account the nonunilateral nature of some transistor amplifiers.



**Figure 1.18** Determining the output resistance.

### Example 1.4

The **bipolar junction transistor (BJT)**, which will be studied in Chapter 6, is a three-terminal device that when powered up by a dc source (battery) and operated with small signals can be modeled by the linear circuit shown in Fig. 1.19(a). The three terminals are the **base (B)**, the **emitter (E)**, and the **collector (C)**. The heart of the model is a transconductance amplifier represented by an input resistance between B and E (denoted  $r_\pi$ ), a short-circuit transconductance  $g_m$ , and an output resistance  $r_o$ .



**Figure 1.19** (a) Small-signal circuit model for a bipolar junction transistor (BJT). (b) The BJT connected as an amplifier with the emitter as a common terminal between input and output (called a common-emitter amplifier). (c) An alternative small-signal circuit model for the BJT.

- (a) With the emitter used as a common terminal between input and output, Fig. 1.19(b) shows a transistor amplifier known as a **common-emitter** or **grounded-emitter** circuit. Derive an expression for the voltage gain  $v_o/v_s$ , and evaluate its magnitude for the case  $R_s = 5 \text{ k}\Omega$ ,  $r_\pi = 2.5 \text{ k}\Omega$ ,  $g_m = 40 \text{ mA/V}$ ,  $r_o = 100 \text{ k}\Omega$ , and  $R_L = 5 \text{ k}\Omega$ . What would the gain value be if the effect of  $r_o$  were neglected?
- (b) An alternative model for the transistor in which a current amplifier rather than a transconductance amplifier is utilized is shown in Fig. 1.19(c). What must the short-circuit current gain  $\beta$  be? Give both an expression and a value.

### Solution

(a) Refer to Fig. 1.19(b). We use the voltage-divider rule to determine the fraction of input signal that appears at the amplifier input as

$$v_{be} = v_s \frac{r_\pi}{r_\pi + R_s} \quad (1.17)$$

Next we determine the output voltage  $v_o$  by multiplying the current ( $g_m v_{be}$ ) by the resistance ( $R_L \parallel r_o$ ),

$$v_o = -g_m v_{be} (R_L \parallel r_o) \quad (1.18)$$

Substituting for  $v_{be}$  from Eq. (1.17) yields the voltage-gain expression

$$\frac{v_o}{v_s} = -\frac{r_\pi}{r_\pi + R_s} g_m (R_L \parallel r_o) \quad (1.19)$$

Observe that the gain is negative, indicating that this amplifier is inverting. For the given component values,

$$\begin{aligned} \frac{v_o}{v_s} &= -\frac{2.5}{2.5+5} \times 40 \times (5 \parallel 100) \\ &= -63.5 \text{ V/V} \end{aligned}$$

Neglecting the effect of  $r_o$ , we obtain

$$\begin{aligned} \frac{v_o}{v_s} &\simeq -\frac{2.5}{2.5+5} \times 40 \times 5 \\ &= -66.7 \text{ V/V} \end{aligned}$$

which is quite close to the value obtained including  $r_o$ . This is not surprising, since  $r_o \gg R_L$ .

(b) For the model in Fig. 1.19(c) to be equivalent to that in Fig. 1.19(a),

$$\beta i_b = g_m v_{be}$$

But  $i_b = v_{be}/r_\pi$ ; thus,

$$\beta = g_m r_\pi$$

For the values given,

$$\begin{aligned} \beta &= 40 \text{ mA/V} \times 2.5 \text{ k}\Omega \\ &= 100 \text{ A/A} \end{aligned}$$

## EXERCISES

- 1.18** Consider a current amplifier having the model shown in the second row of Table 1.1. Let the amplifier be fed with a signal current-source  $i_s$  having a resistance  $R_s$ , and let the output be connected to a load resistance  $R_L$ . Show that the overall current gain is given by

$$\frac{i_o}{i_s} = A_{is} \frac{R_s}{R_s + R_i} \frac{R_o}{R_o + R_L}$$

- 1.19** Consider the transconductance amplifier whose model is shown in the third row of Table 1.1. Let a voltage signal source  $v_s$  with a source resistance  $R_s$  be connected to the input and a load resistance  $R_L$  be connected to the output. Show that the overall voltage gain is given by

$$\frac{v_o}{v_s} = G_m \frac{R_i}{R_i + R_s} (R_o \parallel R_L)$$

- 1.20** Consider a transresistance amplifier having the model shown in the fourth row of Table 1.1. Let the amplifier be fed with a signal current source  $i_s$  having a resistance  $R_s$ , and let the output be connected to a load resistance  $R_L$ . Show that the overall gain is given by

$$\frac{v_o}{i_s} = R_m \frac{R_s}{R_s + R_i} \frac{R_L}{R_L + R_o}$$

- 1.21** Find the input resistance between terminals B and G in the circuit shown in Fig. E1.21. The voltage  $v_x$  is a test voltage with the input resistance  $R_{in}$  defined as  $R_{in} \equiv v_x/i_x$ .

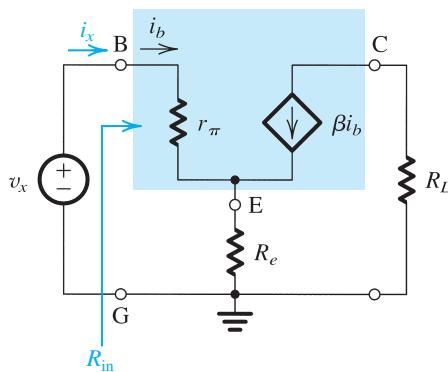


Figure E1.21

**Ans.**  $R_{in} = r_\pi + (\beta + 1)R_e$

## 1.6 Frequency Response of Amplifiers<sup>2</sup>

From Section 1.2 we know that the input signal to an amplifier can always be expressed as the sum of sinusoidal signals. It follows that an important characterization of an amplifier is in terms of its response to input sinusoids of different frequencies. Such a characterization of amplifier performance is known as the amplifier frequency response.

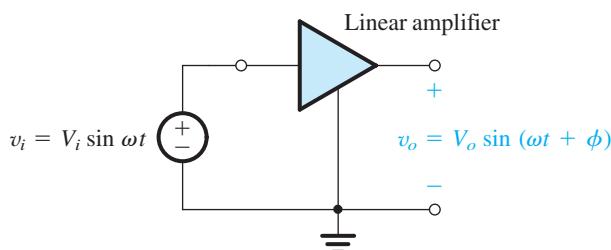
### 1.6.1 Measuring the Amplifier Frequency Response

We shall introduce the subject of amplifier frequency response by showing how it can be measured. Figure 1.20 depicts a linear voltage amplifier fed at its input with a sine-wave signal of amplitude  $V_i$  and frequency  $\omega$ . As the figure indicates, the signal measured at the amplifier output also is sinusoidal with exactly the same frequency  $\omega$ . This is an important point to note: *Whenever a sine-wave signal is applied to a linear circuit, the resulting output is sinusoidal with the same frequency as the input.* In fact, the sine wave is the only signal that does not change shape as it passes through a linear circuit. Observe, however, that the output sinusoid will in general have a different amplitude and will be shifted in phase relative to the input. The ratio of the amplitude of the output sinusoid ( $V_o$ ) to the amplitude of the input sinusoid ( $V_i$ ) is the magnitude of the amplifier gain (or transmission) at the test frequency  $\omega$ . Also, the angle  $\phi$  is the phase of the amplifier transmission at the test frequency  $\omega$ . If we denote the **amplifier transmission**, or **transfer function** as it is more commonly known, by  $T(\omega)$ , then

$$|T(\omega)| = \frac{V_o}{V_i}$$

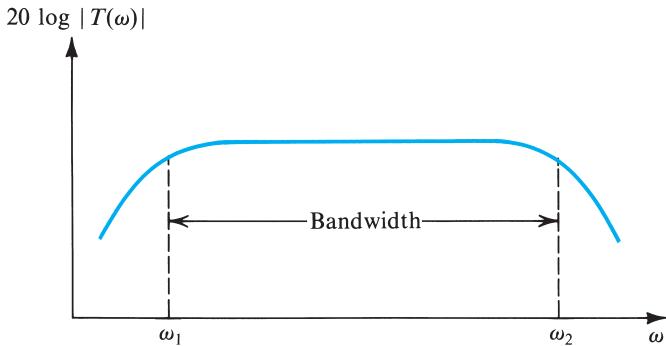
$$\angle T(\omega) = \phi$$

The response of the amplifier to a sinusoid of frequency  $\omega$  is completely described by  $|T(\omega)|$  and  $\angle T(\omega)$ . Now, to obtain the complete frequency response of the amplifier we simply change the frequency of the input sinusoid and measure the new value for  $|T|$  and  $\angle T$ . The end result will be a table and/or graph of gain magnitude [ $|T(\omega)|$ ] versus frequency and a table and/or graph of phase angle [ $\angle T(\omega)$ ] versus frequency. These two plots together constitute the frequency response of the amplifier; the first is known as the **magnitude** or **amplitude**



**Figure 1.20** Measuring the frequency response of a linear amplifier: At the test frequency, the amplifier gain is characterized by its magnitude ( $V_o/V_i$ ) and phase  $\phi$ .

<sup>2</sup>Except for its use in the study of the frequency response of op-amp circuits in Sections 2.5 and 2.7, the material in this section will not be needed in a substantial manner until Chapter 10.



**Figure 1.21** Typical magnitude response of an amplifier:  $|T(\omega)|$  is the magnitude of the amplifier transfer function—that is, the ratio of the output  $V_o(\omega)$  to the input  $V_i(\omega)$ .

**response**, and the second is the **phase response**. Finally, we should mention that it is a common practice to express the magnitude of transmission in decibels and thus plot  $20 \log |T(\omega)|$  versus frequency.

### 1.6.2 Amplifier Bandwidth

Figure 1.21 shows the magnitude response of an amplifier. It indicates that the gain is almost constant over a wide frequency range, roughly between  $\omega_1$  and  $\omega_2$ . Signals whose frequencies are below  $\omega_1$  or above  $\omega_2$  will experience lower gain, with the gain decreasing as we move farther away from  $\omega_1$  and  $\omega_2$ . The band of frequencies over which the gain of the amplifier is almost constant, to within a certain number of decibels (usually 3 dB), is called the **amplifier bandwidth**. Normally the amplifier is designed so that its bandwidth coincides with the spectrum of the signals it is required to amplify. If this were not the case, the amplifier would *distort* the frequency spectrum of the input signal, with different components of the input signal being amplified by different amounts.

### 1.6.3 Evaluating the Frequency Response of Amplifiers

Above, we described the method used to measure the frequency response of an amplifier. We now briefly discuss the method for analytically obtaining an expression for the frequency response. What we are about to say is just a preview of this important subject, whose detailed study is in Chapter 10.

To evaluate the frequency response of an amplifier, one has to analyze the amplifier equivalent circuit model, taking into account all reactive components.<sup>3</sup> Circuit analysis proceeds in the usual fashion but with inductances and capacitances represented by their reactances. An inductance  $L$  has a reactance or impedance  $j\omega L$ , and a capacitance  $C$  has a reactance or impedance  $1/j\omega C$  or, equivalently, a susceptance or admittance  $j\omega C$ . Thus in a *frequency-domain* analysis we deal with impedances and/or admittances. The result of the

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<sup>3</sup>Note that in the models considered in previous sections no reactive components were included. These were simplified models and cannot be used alone to predict the amplifier frequency response.

analysis is the amplifier transfer function  $T(\omega)$

$$T(\omega) = \frac{V_o(\omega)}{V_i(\omega)}$$

where  $V_i(\omega)$  and  $V_o(\omega)$  denote the input and output signals, respectively.  $T(\omega)$  is generally a complex function whose magnitude  $|T(\omega)|$  gives the magnitude of transmission or the magnitude response of the amplifier. The phase of  $T(\omega)$  gives the phase response of the amplifier.

In the analysis of a circuit to determine its frequency response, the algebraic manipulations can be considerably simplified by using the **complex frequency variable**  $s$ . In terms of  $s$ , the impedance of an inductance  $L$  is  $sL$  and that of a capacitance  $C$  is  $1/sC$ . Replacing the reactive elements with their impedances and performing standard circuit analysis, we obtain the transfer function  $T(s)$  as

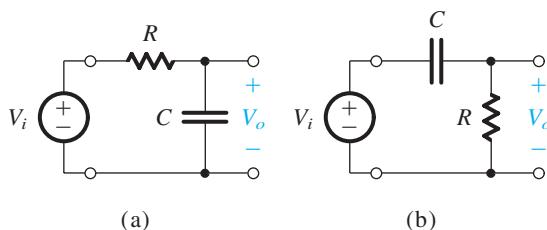
$$T(s) \equiv \frac{V_o(s)}{V_i(s)}$$

Subsequently, we replace  $s$  by  $j\omega$  to determine the transfer function for **physical frequencies**,  $T(j\omega)$ . Note that  $T(j\omega)$  is the same function we called  $T(\omega)$  above<sup>4</sup>; the additional  $j$  is included in order to emphasize that  $T(j\omega)$  is obtained from  $T(s)$  by replacing  $s$  with  $j\omega$ .

#### 1.6.4 Single-Time-Constant Networks

In analyzing amplifier circuits to determine their frequency response, one is greatly aided by knowledge of the frequency-response characteristics of single-time-constant (STC) networks. An STC network is one that is composed of, or can be reduced to, one reactive component (inductance or capacitance) and one resistance. Examples are shown in Fig. 1.22. An STC network formed of an inductance  $L$  and a resistance  $R$  has a time constant  $\tau = L/R$ . The time constant  $\tau$  of an STC network composed of a capacitance  $C$  and a resistance  $R$  is given by  $\tau = CR$ .

Appendix E presents a study of STC networks and their responses to sinusoidal, step, and pulse inputs. Knowledge of this material will be needed at various points throughout this book, and the reader will be encouraged to refer to the appendix. At this point we need in particular the frequency-response results; we will, in fact, briefly discuss this important topic now.



**Figure 1.22** Two examples of STC networks: (a) a low-pass network and (b) a high-pass network.

<sup>4</sup>At this stage, we are using  $s$  simply as a shorthand for  $j\omega$ . We shall not require detailed knowledge of  $s$ -plane concepts until Chapter 10. A brief review of  $s$ -plane analysis is presented in Appendix F.

Most STC networks can be classified into two categories,<sup>5</sup> **low pass (LP)** and **high pass (HP)**, with each of the two categories displaying distinctly different signal responses. As an example, the STC network shown in Fig. 1.22(a) is of the *low-pass* type and that in Fig. 1.22(b) is of the *high-pass* type. To see the reasoning behind this classification, observe that the transfer function of each of these two circuits can be expressed as a voltage-divider ratio, with the divider composed of a resistor and a capacitor. Now, recalling how the impedance of a capacitor varies with frequency ( $Z = 1/j\omega C$ ), it is easy to see that the transmission of the circuit in Fig. 1.22(a) will decrease with frequency and approach zero as  $\omega$  approaches  $\infty$ . Thus the circuit of Fig. 1.22(a) acts as a **low-pass filter**<sup>6</sup>; it passes low-frequency, sine-wave inputs with little or no attenuation (at  $\omega = 0$ , the transmission is unity) and attenuates high-frequency input sinusoids. The circuit of Fig. 1.22(b) does the opposite; its transmission is unity at  $\omega = \infty$  and decreases as  $\omega$  is reduced, reaching 0 for  $\omega = 0$ . The latter circuit, therefore, performs as a **high-pass filter**.

Table 1.2 provides a summary of the frequency-response results for STC networks of both types.<sup>7</sup> Also, sketches of the magnitude and phase responses are given in Figs. 1.23 and 1.24. These frequency-response diagrams are known as **Bode plots**, and the **3-dB frequency** ( $\omega_0$ ) is also known as the **corner frequency**, **break frequency**, or **pole frequency**. The reader is urged to become familiar with this information and to consult Appendix E if further clarifications are needed. In particular, it is important to develop a facility for the rapid

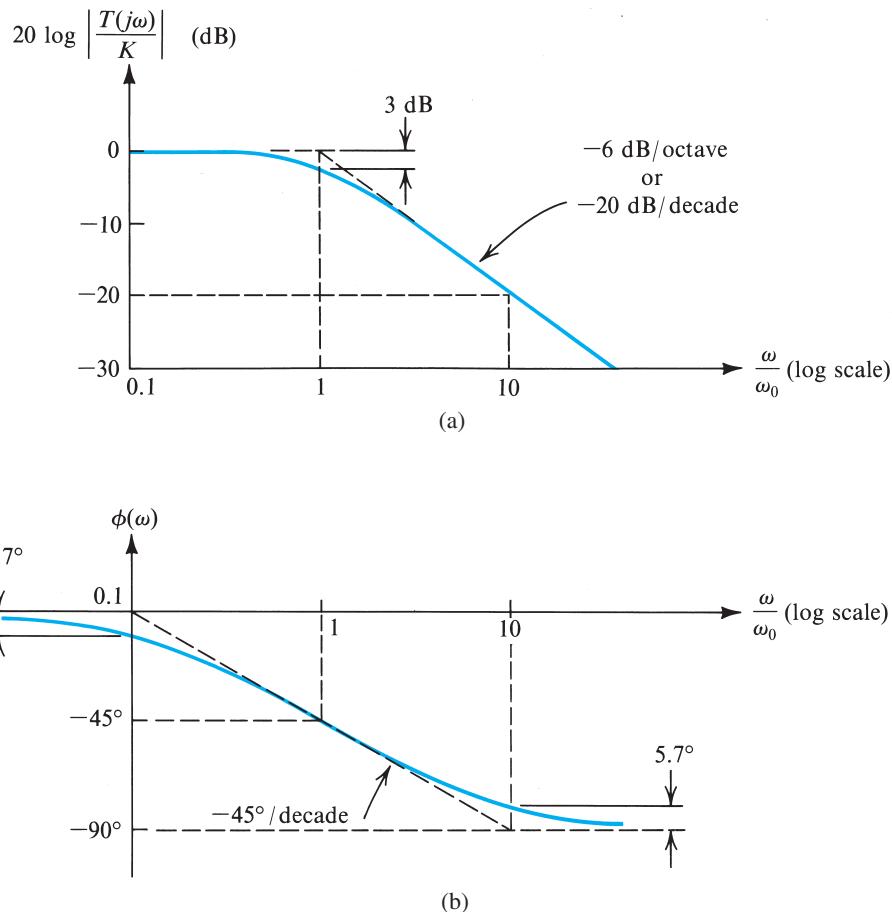
**Table 1.2** Frequency Response of STC Networks

	Low-Pass (LP)	High-Pass (HP)
Transfer Function $T(s)$	$\frac{K}{1 + (s/\omega_0)}$	$\frac{Ks}{s + \omega_0}$
Transfer Function (for physical frequencies) $T(j\omega)$	$\frac{K}{1 + j(\omega/\omega_0)}$	$\frac{K}{1 - j(\omega_0/\omega)}$
Magnitude Response $ T(j\omega) $	$\frac{ K }{\sqrt{1 + (\omega/\omega_0)^2}}$	$\frac{ K }{\sqrt{1 + (\omega_0/\omega)^2}}$
Phase Response $\angle T(j\omega)$	$-\tan^{-1}(\omega/\omega_0)$	$\tan^{-1}(\omega_0/\omega)$
Transmission at $\omega = 0$ (dc)	$K$	0
Transmission at $\omega = \infty$	0	$K$
3-dB Frequency	$\omega_0 = 1/\tau$ ; $\tau \equiv$ time constant $\tau = CR$ or $L/R$	
Bode Plots	in Fig. 1.23	in Fig. 1.24

<sup>5</sup> An important exception is the **all-pass** STC network studied in Chapter 17.

<sup>6</sup> A filter is a circuit that passes signals in a specified frequency band (the filter passband) and stops or severely attenuates (filters out) signals in another frequency band (the filter stopband). Filters will be studied in Chapter 17.

<sup>7</sup> The transfer functions in Table 1.2 are given in general form. For the circuits of Fig. 1.22,  $K = 1$  and  $\omega_0 = 1/CR$ .

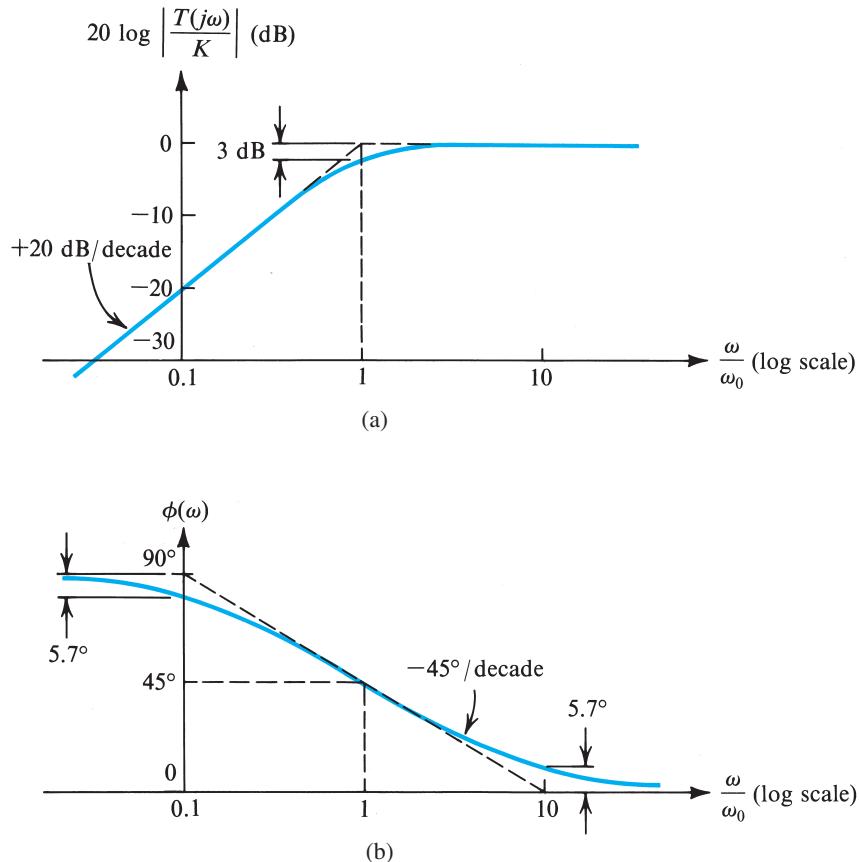


**Figure 1.23** (a) Magnitude and (b) phase response of STC networks of the low-pass type.

determination of the time constant  $\tau$  of an STC circuit. The process is very simple: Set the independent voltage or current source to zero; “grab hold” of the two terminals of the reactive element (capacitor  $C$  or inductor  $L$ ); and determine the equivalent resistance  $R$  that appears between these two terminals. The time constant is then  $CR$  or  $L/R$ .

### BODE PLOTS:

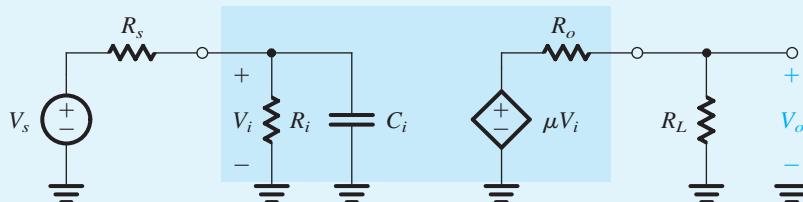
In the 1930s, while working at Bell Labs, Hendrik Bode devised a simple but accurate method for using linearized asymptotic responses to graph gain and phase shift against frequency on a logarithmic scale. Such gain and phase presentations, together called Bode plots, have enormous importance in the design and analysis of the frequency-dependent behavior of systems large and small.



**Figure 1.24** (a) Magnitude and (b) phase response of STC networks of the high-pass type.

### Example 1.5

Figure 1.25 shows a voltage amplifier having an input resistance  $R_i$ , an input capacitance  $C_i$ , a gain factor  $\mu$ , and an output resistance  $R_o$ . The amplifier is fed with a voltage source  $V_s$  having a source resistance  $R_s$ , and a load of resistance  $R_L$  is connected to the output.



**Figure 1.25** Circuit for Example 1.5.

- (a) Derive an expression for the amplifier voltage gain  $V_o/V_s$  as a function of frequency. From this find expressions for the dc gain and the 3-dB frequency.
- (b) Calculate the values of the dc gain, the 3-dB frequency, and the frequency at which the gain becomes 0 dB (i.e., unity) for the case  $R_s = 20 \text{ k}\Omega$ ,  $R_i = 100 \text{ k}\Omega$ ,  $C_i = 60 \text{ pF}$ ,  $\mu = 144 \text{ V/V}$ ,  $R_o = 200 \Omega$ , and  $R_L = 1 \text{ k}\Omega$ .
- (c) Find  $v_o(t)$  for each of the following inputs:
- $v_i = 0.1 \sin 10^2 t, \text{ V}$
  - $v_i = 0.1 \sin 10^5 t, \text{ V}$
  - $v_i = 0.1 \sin 10^6 t, \text{ V}$
  - $v_i = 0.1 \sin 10^8 t, \text{ V}$

### Solution

(a) Utilizing the voltage-divider rule, we can express  $V_i$  in terms of  $V_s$  as follows

$$V_i = V_s \frac{Z_i}{Z_i + R_s}$$

where  $Z_i$  is the amplifier input impedance. Since  $Z_i$  is composed of two parallel elements, it is obviously easier to work in terms of  $Y_i = 1/Z_i$ . Toward that end we divide the numerator and denominator by  $Z_i$ , thus obtaining

$$\begin{aligned} V_i &= V_s \frac{1}{1 + R_s Y_i} \\ &= V_s \frac{1}{1 + R_s [(1/R_i) + sC_i]} \end{aligned}$$

Thus,

$$\frac{V_i}{V_s} = \frac{1}{1 + (R_s/R_i) + sC_i R_s}$$

This expression can be put in the standard form for a low-pass STC network (see the top line of Table 1.2) by extracting  $[1 + (R_s/R_i)]$  from the denominator; thus we have

$$\frac{V_i}{V_s} = \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + sC_i[(R_s R_i)/(R_s + R_i)]} \quad (1.20)$$

At the output side of the amplifier we can use the voltage-divider rule to write

$$V_o = \mu V_i \frac{R_L}{R_L + R_o}$$

This equation can be combined with Eq. (1.20) to obtain the amplifier transfer function as

$$\frac{V_o}{V_s} = \mu \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + (R_o/R_L)} \frac{1}{1 + sC_i[(R_s R_i)/(R_s + R_i)]} \quad (1.21)$$

**Example 1.5** *continued*

We note that only the last factor in this expression is new (compared with the expression derived in the last section). This factor is a result of the input capacitance  $C_i$ , with the time constant being

$$\begin{aligned}\tau &= C_i \frac{R_s R_i}{R_s + R_i} \\ &= C_i (R_s \parallel R_i)\end{aligned}\quad (1.22)$$

We could have obtained this result by inspection: From Fig. 1.25 we see that the input circuit is an STC network and that its time constant can be found by reducing  $V_s$  to zero, with the result that the resistance seen by  $C_i$  is  $R_i$  in parallel with  $R_s$ . The transfer function in Eq. (1.21) is of the form  $K/(1 + (s/\omega_0))$ , which corresponds to a low-pass STC network. The dc gain is found as

$$K \equiv \frac{V_o}{V_s}(s = 0) = \mu \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + (R_o/R_L)} \quad (1.23)$$

The 3-dB frequency  $\omega_0$  can be found from

$$\omega_0 = \frac{1}{\tau} = \frac{1}{C_i (R_s \parallel R_i)} \quad (1.24)$$

Since the frequency response of this amplifier is of the low-pass STC type, the Bode plots for the gain magnitude and phase will take the form shown in Fig. 1.23, where  $K$  is given by Eq. (1.23) and  $\omega_0$  is given by Eq. (1.24).

- (b) Substituting the numerical values given into Eq. (1.23) results in

$$K = 144 \frac{1}{1 + (20/100)} \frac{1}{1 + (200/1000)} = 100 \text{ V/V}$$

Thus the amplifier has a dc gain of 40 dB. Substituting the numerical values into Eq. (1.24) gives the 3-dB frequency

$$\begin{aligned}\omega_0 &= \frac{1}{60 \text{ pF} \times (20 \text{ k}\Omega \parallel 100 \text{ k}\Omega)} \\ &= \frac{1}{60 \times 10^{-12} \times (20 \times 100 / (20 + 100)) \times 10^3} = 10^6 \text{ rad/s}\end{aligned}$$

Thus,

$$f_0 = \frac{10^6}{2\pi} = 159.2 \text{ kHz}$$

Since the gain falls off at the rate of  $-20 \text{ dB/decade}$ , starting at  $\omega_0$  (see Fig. 1.23a) the gain will reach 0 dB in two decades (a factor of 100); thus we have

$$\text{Unity-gain frequency} = 100 \times \omega_0 = 10^8 \text{ rad/s or } 15.92 \text{ MHz}$$

- (c) To find  $v_o(t)$  we need to determine the gain magnitude and phase at  $10^2$ ,  $10^5$ ,  $10^6$ , and  $10^8$  rad/s. This can be done either approximately utilizing the Bode plots of Fig. 1.23 or exactly utilizing the expression for the amplifier transfer function,

$$T(j\omega) \equiv \frac{V_o}{V_s}(j\omega) = \frac{100}{1+j(\omega/10^6)}$$

We shall do both:

- (i) For  $\omega = 10^2$  rad/s, which is  $(\omega_0/10^4)$ , the Bode plots of Fig. 1.23 suggest that  $|T| = K = 100$  and  $\phi = 0^\circ$ . The transfer function expression gives  $|T| \simeq 100$  and  $\phi = -\tan^{-1} 10^{-4} \simeq 0^\circ$ . Thus,

$$v_o(t) = 10 \sin 10^2 t, \text{ V}$$

- (ii) For  $\omega = 10^5$  rad/s, which is  $(\omega_0/10)$ , the Bode plots of Fig. 1.23 suggest that  $|T| \simeq K = 100$  and  $\phi = -5.7^\circ$ . The transfer function expression gives  $|T| = 99.5$  and  $\phi = -\tan^{-1} 0.1 = -5.7^\circ$ . Thus,

$$v_o(t) = 9.95 \sin(10^5 t - 5.7^\circ), \text{ V}$$

- (iii) For  $\omega = 10^6$  rad/s =  $\omega_0$ ,  $|T| = 100/\sqrt{2} = 70.7$  V/V or 37 dB and  $\phi = -45^\circ$ . Thus,

$$v_o(t) = 7.07 \sin(10^6 t - 45^\circ), \text{ V}$$

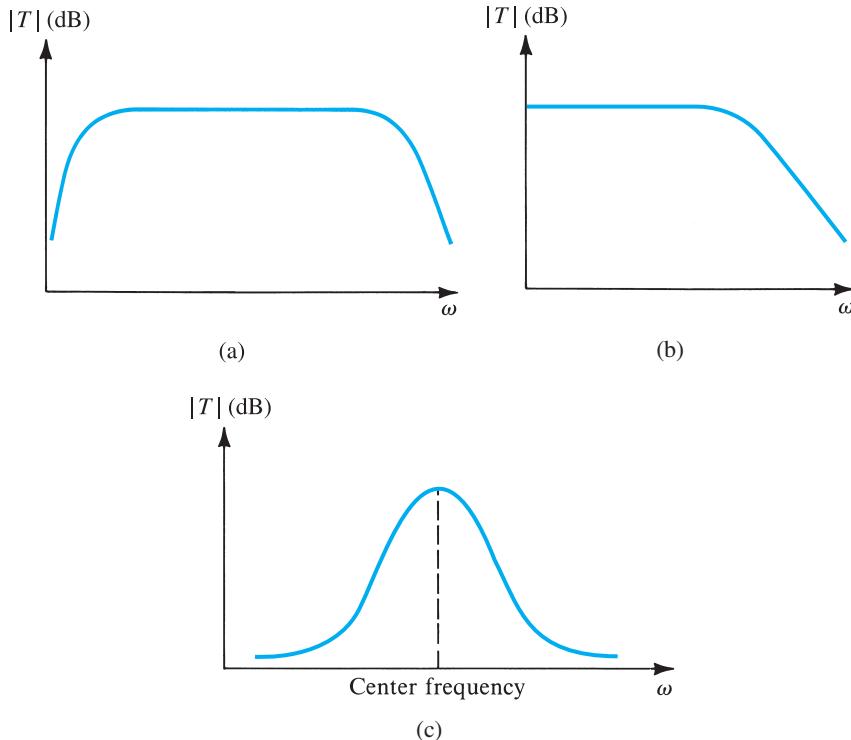
- (iv) For  $\omega = 10^8$  rad/s, which is  $(100 \omega_0)$ , the Bode plots suggest that  $|T| = 1$  and  $\phi = -90^\circ$ . The transfer function expression gives  $|T| \simeq 1$  and  $\phi = -\tan^{-1} 100 = -89.4^\circ$ . Thus,

$$v_o(t) = 0.1 \sin(10^8 t - 89.4^\circ), \text{ V}$$

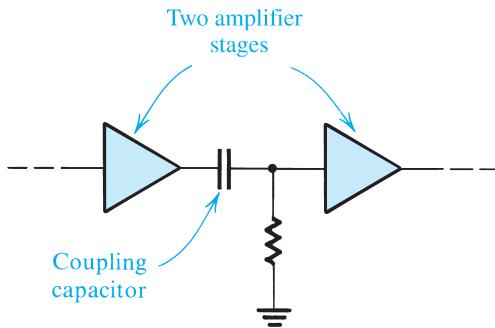
## 1.6.5 Classification of Amplifiers Based on Frequency Response

Amplifiers can be classified based on the shape of their magnitude-response curve. Figure 1.26 shows typical frequency-response curves for various amplifier types. In Fig. 1.26(a) the gain remains constant over a wide frequency range, but falls off at low and high frequencies. This type of frequency response is common in audio amplifiers.

As will be shown in later chapters, **internal capacitances** in the device (a transistor) cause the falloff of gain at high frequencies, just as  $C_i$  did in the circuit of Example 1.5. On the other hand, the falloff of gain at low frequencies is usually caused by **coupling capacitors** used to connect one amplifier stage to another, as indicated in Fig. 1.27. This practice is usually adopted to simplify the design process of the different stages. The coupling capacitors are usually chosen quite large (a fraction of a microfarad to a few tens of microfarads) so that their reactance (impedance) is small at the frequencies of interest. Nevertheless, at sufficiently low frequencies the reactance of a coupling capacitor will become large enough to cause part of the signal being coupled to appear as a voltage drop across the coupling capacitor, thus not reaching the subsequent stage. Coupling capacitors will thus cause loss of gain at low



**Figure 1.26** Frequency response for (a) a capacitively coupled amplifier, (b) a direct-coupled amplifier, and (c) a tuned or bandpass amplifier.



**Figure 1.27** Use of a capacitor to couple amplifier stages.

frequencies and cause the gain to be zero at dc. This is not at all surprising, since from Fig. 1.27 we observe that the coupling capacitor, acting together with the input resistance of the subsequent stage, forms a high-pass STC circuit. It is the frequency response of this high-pass circuit that accounts for the shape of the amplifier frequency response in Fig. 1.26(a) at the low-frequency end.

There are many applications in which it is important that the amplifier maintain its gain at low frequencies down to dc. Furthermore, monolithic integrated-circuit (IC) technology does not allow the fabrication of large coupling capacitors. Thus IC amplifiers are usually designed as **directly coupled** or **dc amplifiers** (as opposed to **capacitively coupled**, or **ac amplifiers**).

Figure 1.26(b) shows the frequency response of a dc amplifier. Such a frequency response characterizes what is referred to as a **low-pass amplifier**.

In a number of applications, such as in the design of radio and TV receivers, the need arises for an amplifier whose frequency response peaks around a certain frequency (called the **center frequency**) and falls off on both sides of this frequency, as shown in Fig. 1.26(c). Amplifiers with such a response are called **tuned amplifiers**, **bandpass amplifiers**, or **bandpass filters**. A tuned amplifier forms the heart of the front-end or tuner of a communication receiver; by adjusting its center frequency to coincide with the frequency of a desired communications channel (e.g., a radio station), the signal of this particular channel can be received while those of other channels are attenuated or filtered out.

## EXERCISES

- 1.22** Consider a voltage amplifier having a frequency response of the low-pass STC type with a dc gain of 60 dB and a 3-dB frequency of 1000 Hz. Find the gain in dB at  $f = 10$  Hz, 10 kHz, 100 kHz, and 1 MHz.

**Ans.** 60 dB; 40 dB; 20 dB; 0 dB

- D1.23** Consider a transconductance amplifier having the model shown in Table 1.1 with  $R_i = 5 \text{ k}\Omega$ ,  $R_o = 50 \text{ k}\Omega$ , and  $G_m = 10 \text{ mA/V}$ . If the amplifier load consists of a resistance  $R_L$  in parallel with a capacitance  $C_L$ , convince yourself that the voltage transfer function realized,  $V_o/V_i$ , is of the low-pass STC type. What is the lowest value that  $R_L$  can have while a dc gain of at least 40 dB is obtained? With this value of  $R_L$  connected, find the highest value that  $C_L$  can have while a 3-dB bandwidth of at least 100 kHz is obtained.

**Ans.**  $12.5 \text{ k}\Omega$ ;  $159.2 \text{ pF}$

- D1.24** Consider the situation illustrated in Fig. 1.27. Let the output resistance of the first voltage amplifier be  $1 \text{ k}\Omega$  and the input resistance of the second voltage amplifier (including the resistor shown) be  $9 \text{ k}\Omega$ . The resulting equivalent circuit is shown in Fig. E1.24. Convince yourself that  $V_2/V_s$  is a high-pass STC function. What is the smallest value for  $C$  that will ensure that the 3-dB frequency is not higher than 100 Hz?

**Ans.**  $0.16 \mu\text{F}$

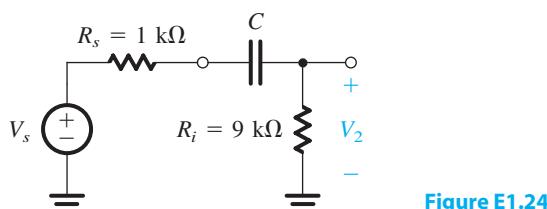


Figure E1.24

## Summary

- An electrical signal source can be represented in either the Thévenin form (a voltage source  $v_s$  in series with a source resistance  $R_s$ ) or the Norton form (a current source  $i_s$  in parallel with a source resistance  $R_s$ ). The Thévenin voltage  $v_s$  is the open-circuit voltage between the source terminals; the Norton current  $i_s$  is equal to the short-circuit current between the source terminals. For the two representations to be equivalent,  $v_s$  and  $R_s i_s$  must be equal.
- A signal can be represented either by its waveform versus time or as the sum of sinusoids. The latter representation is known as the frequency spectrum of the signal.
- The sine-wave signal is completely characterized by its peak value (or rms value, which is the peak/ $\sqrt{2}$ ), its frequency ( $\omega$  in rad/s or  $f$  in Hz;  $\omega = 2\pi f$  and  $f = 1/T$ , where  $T$  is the period in seconds), and its phase with respect to an arbitrary reference time.
- Analog signals have magnitudes that can assume any value. Electronic circuits that process analog signals are called analog circuits. Sampling the magnitude of an analog signal at discrete instants of time and representing each signal sample by a number results in a digital signal. Digital signals are processed by digital circuits.
- The simplest digital signals are obtained when the binary system is used. An individual digital signal then assumes one of only two possible values: low and high (say, 0 V and +5 V), corresponding to logic 0 and logic 1, respectively.
- An analog-to-digital converter (ADC) provides at its output the digits of the binary number representing the analog signal sample applied to its input. The output digital signal can then be processed using digital circuits. Refer to Fig. 1.10 and Eq. (1.3).
- The transfer characteristic,  $v_o$  versus  $v_i$ , of a linear amplifier is a straight line with a slope equal to the voltage gain. Refer to Fig. 1.12.
- Amplifiers increase the signal power and thus require dc power supplies for their operation.
- The amplifier voltage gain can be expressed as a ratio  $A_v$  in V/V or in decibels,  $20 \log |A_v|$ , dB. Similarly, for current gain:  $A_i$  A/A or  $20 \log |A_i|$ , dB. For power gain:  $A_p$  W/W or  $10 \log |A_p|$ , dB.
- Depending on the signal to be amplified (voltage or current) and on the desired form of output signal (voltage or current), there are four basic amplifier types: voltage, current, transconductance, and transresistance amplifiers. For the circuit models and ideal characteristics of these four amplifier types, refer to Table 1.1. A given amplifier can be modeled by any one of the four models, in which case their parameters are related by the formulas in Eqs. (1.14) to (1.16).
- A sinusoid is the only signal whose waveform is unchanged through a linear circuit. Sinusoidal signals are used to measure the frequency response of amplifiers.
- The transfer function  $T(s) \equiv V_o(s)/V_i(s)$  of a voltage amplifier can be determined from circuit analysis. Substituting  $s = j\omega$  gives  $T(j\omega)$ , whose magnitude  $|T(j\omega)|$  is the magnitude response, and whose phase  $\phi(\omega)$  is the phase response, of the amplifier.
- Amplifiers are classified according to the shape of their frequency response,  $|T(j\omega)|$ . Refer to Fig. 1.26.
- Single-time-constant (STC) networks are those networks that are composed of, or can be reduced to, one reactive component ( $L$  or  $C$ ) and one resistance ( $R$ ). The time constant  $\tau$  is either  $L/R$  or  $CR$ .
- STC networks can be classified into two categories: low pass (LP) and high pass (HP). LP networks pass dc and low frequencies and attenuate high frequencies. The opposite is true for HP networks.
- The gain of an LP (HP) STC circuit drops by 3 dB below the zero-frequency (infinite-frequency) value at a frequency  $\omega_0 = 1/\tau$ . At high frequencies (low frequencies) the gain falls off at the rate of 6 dB/octave or 20 dB/decade. Refer to Table 1.2 on page 36 and Figs. 1.23 and 1.24. Further details are given in Appendix E.

## Circuit Basics

As a review of the basics of circuit analysis and in order for the readers to gauge their preparedness for the study of electronic circuits, this section presents a number of relevant circuit analysis problems. For a summary of Thévenin's and Norton's theorems, refer to Appendix D. The problems are grouped in appropriate categories.

### Resistors and Ohm's Law

**1.1** Ohm's law relates  $V$ ,  $I$ , and  $R$  for a resistor. For each of the situations following, find the missing item:

- (a)  $R = 1 \text{ k}\Omega$ ,  $V = 5 \text{ V}$
- (b)  $V = 5 \text{ V}$ ,  $I = 1 \text{ mA}$
- (c)  $R = 10 \text{ k}\Omega$ ,  $I = 0.1 \text{ mA}$
- (d)  $R = 100 \Omega$ ,  $V = 1 \text{ V}$

*Note:* Volts, millamps, and kilohms constitute a consistent set of units.

**1.2** Measurements taken on various resistors are shown below. For each, calculate the power dissipated in the resistor and the power rating necessary for safe operation using standard components with power ratings of  $1/8 \text{ W}$ ,  $1/4 \text{ W}$ ,  $1/2 \text{ W}$ ,  $1 \text{ W}$ , or  $2 \text{ W}$ :

- (a)  $1 \text{ k}\Omega$  conducting  $20 \text{ mA}$
- (b)  $1 \text{ k}\Omega$  conducting  $40 \text{ mA}$
- (c)  $100 \text{ k}\Omega$  conducting  $1 \text{ mA}$
- (d)  $10 \text{ k}\Omega$  conducting  $4 \text{ mA}$
- (e)  $1 \text{ k}\Omega$  dropping  $20 \text{ V}$
- (f)  $1 \text{ k}\Omega$  dropping  $11 \text{ V}$

**1.3** Ohm's law and the power law for a resistor relate  $V$ ,  $I$ ,  $R$ , and  $P$ , making only two variables independent. For each pair identified below, find the other two:

- (a)  $R = 1 \text{ k}\Omega$ ,  $I = 5 \text{ mA}$
- (b)  $V = 5 \text{ V}$ ,  $I = 1 \text{ mA}$
- (c)  $V = 10 \text{ V}$ ,  $P = 100 \text{ mW}$
- (d)  $I = 0.1 \text{ mA}$ ,  $P = 1 \text{ mW}$
- (e)  $R = 1 \text{ k}\Omega$ ,  $P = 1 \text{ W}$

### Combining Resistors

**1.4** You are given three resistors whose values are  $10 \text{ k}\Omega$ ,  $20 \text{ k}\Omega$ , and  $40 \text{ k}\Omega$ . How many different resistances can you create using series and parallel combinations of these three? List them in value order, lowest first. Be thorough and

organized. (*Hint:* In your search, first consider all parallel combinations, then consider series combinations, and then consider series-parallel combinations, of which there are two kinds.)

**1.5** In the analysis and test of electronic circuits, it is often useful to connect one resistor in parallel with another to obtain a nonstandard value, one which is smaller than the smaller of the two resistors. Often, particularly during circuit testing, one resistor is already installed, in which case the second, when connected in parallel, is said to "shunt" the first. If the original resistor is  $10 \text{ k}\Omega$ , what is the value of the shunting resistor needed to reduce the combined value by  $1\%$ ,  $5\%$ ,  $10\%$ , and  $50\%$ ? What is the result of shunting a  $10\text{-k}\Omega$  resistor by  $1 \text{ M}\Omega$ ? By  $100 \text{ k}\Omega$ ? By  $10 \text{ k}\Omega$ ?

### Voltage Dividers

**1.6** Figure P1.6(a) shows a two-resistor voltage divider. Its function is to generate a voltage  $V_o$  (smaller than the power-supply voltage  $V_{DD}$ ) at its output node X. The circuit looking back at node X is equivalent to that shown in Fig. P1.6(b). Observe that this is the Thévenin equivalent of the voltage-divider circuit. Find expressions for  $V_o$  and  $R_o$ .

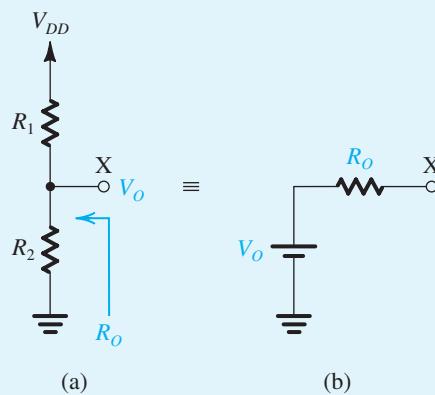


Figure P1.6

**1.7** A two-resistor voltage divider employing a  $2\text{-k}\Omega$  and a  $3\text{-k}\Omega$  resistor is connected to a  $5\text{-V}$  ground-referenced power supply to provide a  $2\text{-V}$  voltage. Sketch the circuit. Assuming exact-valued resistors, what output voltage (measured to ground) and equivalent output resistance result? If the resistors used are not ideal but have a  $\pm 5\%$  manufacturing tolerance, what are the extreme output voltages and resistances that can result?

## 46 Chapter 1 Signals and Amplifiers

**D 1.8** You are given three resistors, each of  $10\text{ k}\Omega$ , and a 9-V battery whose negative terminal is connected to ground. With a voltage divider using some or all of your resistors, how many positive-voltage sources of magnitude less than 9 V can you design? List them in order, smallest first. What is the output resistance (i.e., the Thévenin resistance) of each?

**D \*1.9** Two resistors, with nominal values of  $4.7\text{ k}\Omega$  and  $10\text{ k}\Omega$ , are used in a voltage divider with a +15-V supply to create a nominal +5-V output. Assuming the resistor values to be exact, what is the actual output voltage produced? Which resistor must be shunted (paralleled) by what third resistor to create a voltage-divider output of 5.00 V? If an output resistance of exactly  $3.33\text{ k}\Omega$  is also required, what do you suggest?

### Current Dividers

**1.10** Current dividers play an important role in circuit design. Therefore it is important to develop a facility for dealing with current dividers in circuit analysis. Figure P1.10 shows a two-resistor current divider fed with an ideal current source  $I$ . Show that

$$I_1 = \frac{R_2}{R_1 + R_2} I$$

$$I_2 = \frac{R_1}{R_1 + R_2} I$$

and find the voltage  $V$  that develops across the current divider.

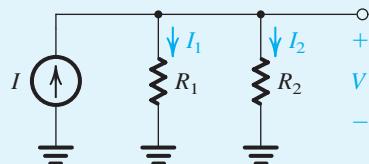


Figure P1.10

**D 1.11** Design a simple current divider that will reduce the current provided to a  $10\text{-k}\Omega$  load to one-third of that available from the source.

**D 1.12** A designer searches for a simple circuit to provide one-fifth of a signal current  $I$  to a load resistance  $R$ . Suggest a solution using one resistor. What must its value be? What is the input resistance of the resulting current divider? For a particular value  $R$ , the designer discovers that the otherwise-best-available resistor is 10% too high. Suggest two circuit topologies using one additional resistor that will solve

this problem. What is the value of the resistor required in each case? What is the input resistance of the current divider in each case?

**D 1.13** A particular electronic signal source generates currents in the range 0 mA to 0.5 mA under the condition that its load voltage not exceed 1 V. For loads causing more than 1 V to appear across the generator, the output current is no longer assured but will be reduced by some unknown amount. This circuit limitation, occurring, for example, at the peak of a sine-wave signal, will lead to undesirable signal distortion that must be avoided. If a  $10\text{-k}\Omega$  load is to be connected, what must be done? What is the name of the circuit you must use? How many resistors are needed? What is (are) the (ir) value(s)? What is the range of current through the load?

### Thévenin Equivalent Circuits

**1.14** For the circuit in Fig. P1.14, find the Thévenin equivalent circuit between terminals (a) 1 and 2, (b) 2 and 3, and (c) 1 and 3.

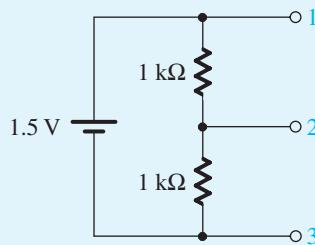


Figure P1.14

**1.15** Through repeated application of Thévenin's theorem, find the Thévenin equivalent of the circuit in Fig. P1.15 between node 4 and ground, and hence find the current that flows through a load resistance of  $3\text{ k}\Omega$  connected between node 4 and ground.

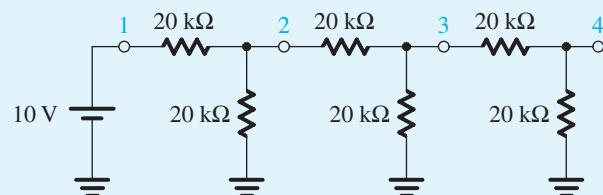


Figure P1.15

## Circuit Analysis

**1.16** For the circuit shown in Fig. P1.16, find the current in each of the three resistors and the voltage (with respect to ground) at their common node using two methods:

- Loop Equations: Define branch currents  $I_1$  and  $I_2$  in  $R_1$  and  $R_2$ , respectively; write two equations; and solve them.
- Node Equation: Define the node voltage  $V$  at the common node; write a single equation; and solve it.

Which method do you prefer? Why?

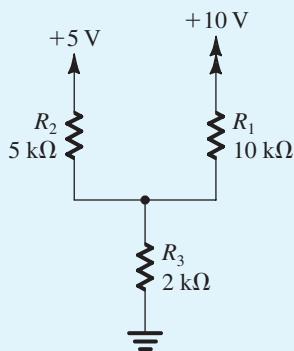


Figure P1.16

**1.17** The circuit shown in Fig. P1.17 represents the equivalent circuit of an unbalanced bridge. It is required to calculate the current in the detector branch ( $R_5$ ) and the voltage across it. Although this can be done by using loop and node equations,

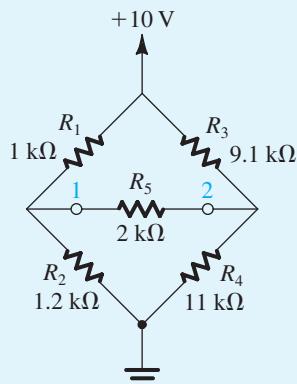


Figure P1.17

a much easier approach is possible: Find the Thévenin equivalent of the circuit to the left of node 1 and the Thévenin equivalent of the circuit to the right of node 2. Then solve the resulting simplified circuit.

**\*1.18** For the circuit in Fig. P1.18, find the equivalent resistance to ground,  $R_{eq}$ . To do this, apply a voltage  $V_x$  between terminal X and ground and find the current drawn from  $V_x$ . Note that you can use particular special properties of the circuit to get the result directly! Now, if  $R_4$  is raised to 1.2 kΩ, what does  $R_{eq}$  become?

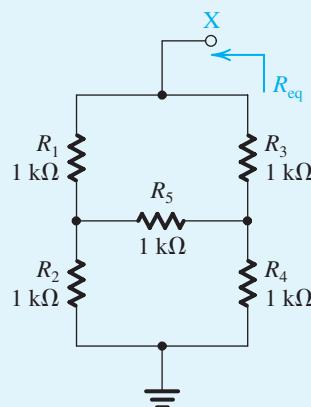


Figure P1.18

**1.19** Derive an expression for  $v_o/v_s$  for the circuit shown in Fig. P1.19.

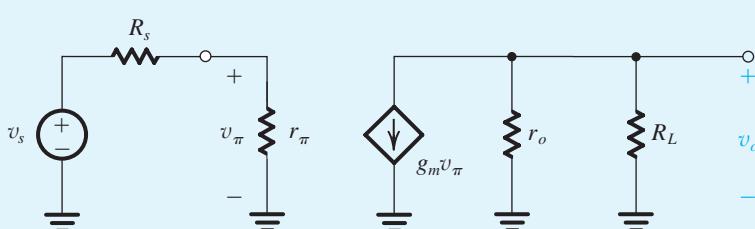


Figure P1.19

## AC Circuits

**1.20** The periodicity of recurrent waveforms, such as sine waves or square waves, can be completely specified using only one of three possible parameters: radian frequency,  $\omega$ , in radians per second (rad/s); (conventional) frequency,  $f$ , in hertz (Hz); or period  $T$ , in seconds (s). As well, each of the parameters can be specified numerically in one of several ways: using letter prefixes associated with the basic units, using scientific notation, or using some combination of both. Thus, for example, a particular period may be specified as 100 ns, 0.1  $\mu$ s,  $10^{-1}$   $\mu$ s,  $10^5$  ps, or  $1 \times 10^{-7}$  s. (For the definition of the various prefixes used in electronics, see Appendix J.) For each of the measures listed below, express the trio of terms in scientific notation associated with the basic unit (e.g.,  $10^{-7}$  s rather than  $10^{-1}$   $\mu$ s).

- (a)  $T = 10^{-4}$  ms
- (b)  $f = 1$  GHz
- (c)  $\omega = 6.28 \times 10^2$  rad/s
- (d)  $T = 10$  s
- (e)  $f = 60$  Hz
- (f)  $\omega = 1$  krad/s
- (g)  $f = 1900$  MHz

**1.21** Find the complex impedance,  $Z$ , of each of the following basic circuit elements at 60 Hz, 100 kHz, and 1 GHz:

- (a)  $R = 1$  k $\Omega$
- (b)  $C = 10$  nF
- (c)  $C = 10$  pF
- (d)  $L = 10$  mH
- (e)  $L = 1$   $\mu$ H

**1.22** Find the complex impedance at 10 kHz of the following networks:

- (a) 1 k $\Omega$  in series with 10 nF
- (b) 10 k $\Omega$  in parallel with 0.01  $\mu$ F
- (c) 100 k $\Omega$  in parallel with 100 pF
- (d) 100  $\Omega$  in series with 10 mH

## Section 1.1: Signals

**1.23** Any given signal source provides an open-circuit voltage,  $v_{oc}$ , and a short-circuit current,  $i_{sc}$ . For the following

sources, calculate the internal resistance,  $R_s$ ; the Norton current,  $i_s$ ; and the Thévenin voltage,  $v_s$ :

- (a)  $v_{oc} = 1$  V,  $i_{sc} = 0.1$  mA
- (b)  $v_{oc} = 0.1$  V,  $i_{sc} = 1$   $\mu$ A

**1.24** A particular signal source produces an output of 40 mV when loaded by a 100-k $\Omega$  resistor and 10 mV when loaded by a 10-k $\Omega$  resistor. Calculate the Thévenin voltage, Norton current, and source resistance.

**1.25** A temperature sensor is specified to provide 2 mV/ $^{\circ}$ C. When connected to a load resistance of 5 k $\Omega$ , the output voltage was measured to change by 10 mV, corresponding to a change in temperature of  $10^{\circ}$ C. What is the source resistance of the sensor?

**1.26** Refer to the Thévenin and Norton representations of the signal source (Fig. 1.1). If the current supplied by the source is denoted  $i_o$  and the voltage appearing between the source output terminals is denoted  $v_o$ , sketch and clearly label  $v_o$  versus  $i_o$  for  $0 \leq i_o \leq i_s$ .

**1.27** The connection of a signal source to an associated signal processor or amplifier generally involves some degree of signal loss as measured at the processor or amplifier input. Considering the two signal-source representations shown in Fig. 1.1, provide two sketches showing each signal-source representation connected to the input terminals (and corresponding input resistance) of a signal processor. What signal-processor input resistance will result in 95% of the open-circuit voltage being delivered to the processor? What input resistance will result in 95% of the short-circuit signal current entering the processor?

## Section 1.2: Frequency Spectrum of Signals

**1.28** To familiarize yourself with typical values of angular frequency  $\omega$ , conventional frequency  $f$ , and period  $T$ , complete the entries in the following table:

Case	$\omega$ (rad/s)	$f$ (Hz)	$T$ (s)
a			
b	$2 \times 10^9$		
c			$1 \times 10^{-10}$
d		60	
e	$6.28 \times 10^4$		
f			$1 \times 10^{-5}$

**1.29** For the following peak or rms values of some important sine waves, calculate the corresponding other value:

- 117 V rms, a household-power voltage in North America
- 33.9 V peak, a somewhat common peak voltage in rectifier circuits
- 220 V rms, a household-power voltage in parts of Europe
- 220 kV rms, a high-voltage transmission-line voltage in North America

**1.30** Give expressions for the sine-wave voltage signals having:

- 10-V peak amplitude and 1-kHz frequency
- 120-V rms and 60-Hz frequency
- 0.2-V peak-to-peak and 2000-rad/s frequency
- 100-mV peak and 1-ms period

**1.31** Using the information provided by Eq. (1.2) in association with Fig. 1.5, characterize the signal represented by  $v(t) = 1/2 + 2/\pi(\sin 2000\pi t + \frac{1}{3}\sin 6000\pi t + \frac{1}{5}\sin 10,000\pi t + \dots)$ . Sketch the waveform. What is its average value? Its peak-to-peak value? Its lowest value? Its highest value? Its frequency? Its period?

**1.32** Measurements taken of a square-wave signal using a frequency-selective voltmeter (called a spectrum analyzer) show its spectrum to contain adjacent components (spectral lines) at 98 kHz and 126 kHz of amplitudes 63 mV and 49 mV, respectively. For this signal, what would direct measurement of the fundamental show its frequency and amplitude to be? What is the rms value of the fundamental? What are the peak-to-peak amplitude and period of the originating square wave?

**1.33** Find the amplitude of a symmetrical square wave of period  $T$  that provides the same power as a sine wave of peak

amplitude  $\hat{V}$  and the same frequency. Does this result depend on equality of the frequencies of the two waveforms?

### Section 1.3: Analog and Digital Signals

**1.34** Give the binary representation of the following decimal numbers: 0, 6, 11, 28, and 59.

**1.35** Consider a 4-bit digital word  $b_3 b_2 b_1 b_0$  in a format called signed-magnitude, in which the most significant bit,  $b_3$ , is interpreted as a sign bit—0 for positive and 1 for negative values. List the values that can be represented by this scheme. What is peculiar about the representation of zero? For a particular analog-to-digital converter (ADC), each change in  $b_0$  corresponds to a 0.5-V change in the analog input. What is the full range of the analog signal that can be represented? What signed-magnitude digital code results for an input of +2.5 V? For -3.0 V? For +2.7 V? For -2.8 V?

**1.36** Consider an  $N$ -bit ADC whose analog input varies between 0 and  $V_{FS}$  (where the subscript  $FS$  denotes “full scale”).

- Show that the least significant bit (LSB) corresponds to a change in the analog signal of  $V_{FS}/(2^N - 1)$ . This is the resolution of the converter.
- Convince yourself that the maximum error in the conversion (called the quantization error) is half the resolution; that is, the quantization error =  $V_{FS}/2(2^N - 1)$ .
- For  $V_{FS} = 5$  V, how many bits are required to obtain a resolution of 2 mV or better? What is the actual resolution obtained? What is the resulting quantization error?

**1.37** Figure P1.37 shows the circuit of an  $N$ -bit digital-to-analog converter (DAC). Each of the  $N$  bits of the digital word to be converted controls one of the switches.

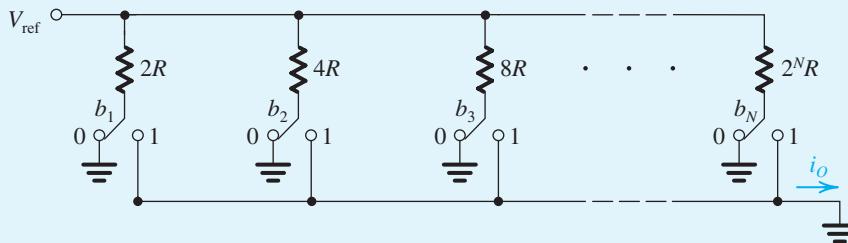


Figure P1.37

**50 Chapter 1** Signals and Amplifiers

When the bit is 0, the switch is in the position labeled 0; when the bit is 1, the switch is in the position labeled 1. The analog output is the current  $i_o$ .  $V_{\text{ref}}$  is a constant reference voltage.

(a) Show that

$$i_o = \frac{V_{\text{ref}}}{R} \left( \frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N} \right)$$

- (b) Which bit is the LSB? Which is the MSB?  
(c) For  $V_{\text{ref}} = 10 \text{ V}$ ,  $R = 10 \text{ k}\Omega$ , and  $N = 8$ , find the maximum value of  $i_o$  obtained. What is the change in  $i_o$  resulting from the LSB changing from 0 to 1?

**1.38** In compact-disc (CD) audio technology, the audio signal is sampled at 44.1 kHz. Each sample is represented by 16 bits. What is the speed of this system in bits per second?

### Section 1.4: Amplifiers

**1.39** Various amplifier and load combinations are measured as listed below using rms values. For each, find the voltage, current, and power gains ( $A_v$ ,  $A_i$ , and  $A_p$ , respectively) both as ratios and in dB:

- (a)  $v_i = 100 \text{ mV}$ ,  $i_i = 100 \mu\text{A}$ ,  $v_o = 10 \text{ V}$ ,  $R_L = 100 \Omega$   
(b)  $v_i = 10 \mu\text{V}$ ,  $i_i = 100 \text{nA}$ ,  $v_o = 1 \text{ V}$ ,  $R_L = 10 \text{k}\Omega$   
(c)  $v_i = 1 \text{ V}$ ,  $i_i = 1 \text{ mA}$ ,  $v_o = 5 \text{ V}$ ,  $R_L = 10 \Omega$

**1.40** An amplifier operating from  $\pm 3\text{-V}$  supplies provides a  $2.2\text{-V}$  peak sine wave across a  $100\text{-}\Omega$  load when provided with a  $0.2\text{-V}$  peak input from which  $1.0 \text{ mA}$  peak is drawn. The average current in each supply is measured to be  $20 \text{ mA}$ . Find the voltage gain, current gain, and power gain expressed as ratios and in decibels as well as the supply power, amplifier dissipation, and amplifier efficiency.

**1.41** An amplifier using balanced power supplies is known to saturate for signals extending within  $1.0 \text{ V}$  of either supply. For linear operation, its gain is  $200 \text{ V/V}$ . What is the rms value of the largest undistorted sine-wave output available, and input needed, with  $\pm 5\text{-V}$  supplies? With  $\pm 10\text{-V}$  supplies? With  $\pm 15\text{-V}$  supplies?

**1.42** Symmetrically saturating amplifiers, operating in the so-called clipping mode, can be used to convert sine waves to pseudo-square waves. For an amplifier with a small-signal gain of 1000 and clipping levels of  $\pm 10 \text{ V}$ , what peak value of input sinusoid is needed to produce an output whose extremes are just at the edge of clipping? Clipped 90% of the time? Clipped 99% of the time?

### Section 1.5: Circuit Models for Amplifiers

**1.43** Consider the voltage-amplifier circuit model shown in Fig. 1.16(b), in which  $A_{vo} = 100 \text{ V/V}$  under the following conditions:

- (a)  $R_i = 10R_s$ ,  $R_L = 10R_o$   
(b)  $R_i = R_s$ ,  $R_L = R_o$   
(c)  $R_i = R_s/10$ ,  $R_L = R_o/10$

Calculate the overall voltage gain  $v_o/v_s$  in each case, expressed both directly and in decibels.

**1.44** An amplifier with  $40 \text{ dB}$  of small-signal, open-circuit voltage gain, an input resistance of  $1 \text{ M}\Omega$ , and an output resistance of  $100 \Omega$ , drives a load of  $500 \Omega$ . What voltage and power gains (expressed in dB) would you expect with the load connected? If the amplifier has a peak output-current limitation of  $20 \text{ mA}$ , what is the rms value of the largest sine-wave input for which an undistorted output is possible? What is the corresponding output power available?

**1.45** A  $10\text{-mV}$  signal source having an internal resistance of  $100 \text{ k}\Omega$  is connected to an amplifier for which the input resistance is  $10 \text{ k}\Omega$ , the open-circuit voltage gain is  $1000 \text{ V/V}$ , and the output resistance is  $1 \text{ k}\Omega$ . The amplifier is connected in turn to a  $100\text{-}\Omega$  load. What overall voltage gain results as measured from the source internal voltage to the load? Where did all the gain go? What would the gain be if the source was connected directly to the load? What is the ratio of these two gains? This ratio is a useful measure of the benefit the amplifier brings.

**1.46** A buffer amplifier with a gain of  $1 \text{ V/V}$  has an input resistance of  $1 \text{ M}\Omega$  and an output resistance of  $20 \Omega$ . It is connected between a  $1\text{-V}$ ,  $200\text{-k}\Omega$  source and a  $100\text{-}\Omega$

load. What load voltage results? What are the corresponding voltage, current, and power gains (in dB)?

**1.47** Consider the cascade amplifier of Example 1.3. Find the overall voltage gain  $v_o/v_s$  obtained when the first and second stages are interchanged. Compare this value with the result in Example 1.3, and comment.

**1.48** You are given two amplifiers, A and B, to connect in cascade between a 10-mV, 100-k $\Omega$  source and a 100- $\Omega$  load. The amplifiers have voltage gain, input resistance, and output resistance as follows: for A, 100 V/V, 100 k $\Omega$ , 10 k $\Omega$ , respectively; for B, 10 V/V, 10 k $\Omega$ , 1 k $\Omega$ , respectively. Your problem is to decide how the amplifiers should be connected. To proceed, evaluate the two possible connections between source S and load L, namely, SABL and SBAL. Find the voltage gain for each both as a ratio and in decibels. Which amplifier arrangement is best?

**D \*1.49** A designer has available voltage amplifiers with an input resistance of 10 k $\Omega$ , an output resistance of 1 k $\Omega$ , and an open-circuit voltage gain of 10. The signal source has a 10-k $\Omega$  resistance and provides a 5-mV rms signal, and it is required to provide a signal of at least 3 V rms to a 200- $\Omega$  load. How many amplifier stages are required? What is the output voltage actually obtained?

**D \*1.50** Design an amplifier that provides 0.5 W of signal power to a 100- $\Omega$  load resistance. The signal source provides a 30-mV rms signal and has a resistance of 0.5 M $\Omega$ . Three types of voltage-amplifier stages are available:

- (a) A high-input-resistance type with  $R_i = 1 \text{ M}\Omega$ ,  $A_{vo} = 10$ , and  $R_o = 10 \text{ k}\Omega$
- (b) A high-gain type with  $R_i = 10 \text{ k}\Omega$ ,  $A_{vo} = 100$ , and  $R_o = 1 \text{ k}\Omega$
- (c) A low-output-resistance type with  $R_i = 10 \text{ k}\Omega$ ,  $A_{vo} = 1$ , and  $R_o = 20 \Omega$

Design a suitable amplifier using a combination of these stages. Your design should utilize the minimum number of stages and should ensure that the signal level is not reduced below 10 mV at any point in the amplifier chain. Find the load voltage and power output realized.

**D \*1.51** It is required to design a voltage amplifier to be driven from a signal source having a 5-mV peak amplitude and a source resistance of 10 k $\Omega$  to supply a peak output of 2 V across a 1-k $\Omega$  load.

- (a) What is the required voltage gain from the source to the load?
- (b) If the peak current available from the source is 0.1  $\mu\text{A}$ , what is the smallest input resistance allowed? For the design with this value of  $R_i$ , find the overall current gain and power gain.
- (c) If the amplifier power supply limits the peak value of the output open-circuit voltage to 3 V, what is the largest output resistance allowed?
- (d) For the design with  $R_i$  as in (b) and  $R_o$  as in (c), what is the required value of open-circuit voltage gain, i.e.,  $\left.\frac{v_o}{v_i}\right|_{R_L=\infty}$ , of the amplifier?
- (e) If, as a possible design option, you are able to increase  $R_i$  to the nearest value of the form  $1 \times 10^n \Omega$  and to decrease  $R_o$  to the nearest value of the form  $1 \times 10^m \Omega$ , find (i) the input resistance achievable; (ii) the output resistance achievable; and (iii) the open-circuit voltage gain now required to meet the specifications.

**D 1.52** A voltage amplifier with an input resistance of 20 k $\Omega$ , an output resistance of 100  $\Omega$ , and a gain of 1000 V/V is connected between a 100-k $\Omega$  source with an open-circuit voltage of 10 mV and a 100- $\Omega$  load. For this situation:

- (a) What output voltage results?
- (b) What is the voltage gain from source to load?
- (c) What is the voltage gain from the amplifier input to the load?
- (d) If the output voltage across the load is twice that needed and there are signs of internal amplifier overload, suggest the location and value of a single resistor that would produce the desired output. Choose an arrangement that would cause minimum disruption to an operating circuit. (*Hint:* Use parallel rather than series connections.)

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**1.53** A voltage amplifier delivers 200 mV across a load resistance of  $1\text{ k}\Omega$ . It was found that the output voltage decreases by 5 mV when  $R_L$  is decreased to  $780\ \Omega$ . What are the values of the open-circuit output voltage and the output resistance of the amplifier?

**1.54** A current amplifier supplies 1 mA to a load resistance of  $1\text{ k}\Omega$ . When the load resistance is increased to  $12\text{ k}\Omega$ , the output current decreases to 0.5 mA. What are the values of the short-circuit output current and the output resistance of the amplifier?

**1.55** A current amplifier for which  $R_i = 100\ \Omega$ ,  $R_o = 10\text{ k}\Omega$ , and  $A_{is} = 100\text{ A/A}$  is to be connected between a 100-mV source with a resistance of  $10\text{ k}\Omega$  and a load of  $1\text{ k}\Omega$ . What are the values of current gain  $i_o/i_i$ , of voltage gain  $v_o/v_s$ , and of power gain expressed directly and in decibels?

**1.56** A transconductance amplifier with  $R_i = 2\text{ k}\Omega$ ,  $G_m = 60\text{ mA/V}$ , and  $R_o = 20\text{ k}\Omega$  is fed with a voltage source having a source resistance of  $1\text{ k}\Omega$  and is loaded with a  $1\text{-k}\Omega$  resistance. Find the voltage gain realized.

**D \*\*1.57** A designer is required to provide, across a  $10\text{-k}\Omega$  load, the weighted sum,  $v_o = 10v_1 + 20v_2$ , of input signals  $v_1$  and  $v_2$ , each having a source resistance of  $10\text{ k}\Omega$ . She has a number of transconductance amplifiers for which the input and output resistances are both  $10\text{ k}\Omega$  and  $G_m = 20\text{ mA/V}$ , together with a selection of suitable resistors. Sketch an appropriate amplifier topology with additional resistors selected to provide the desired result. Your design should utilize the minimum number of amplifiers and resistors. (*Hint:* In your design, arrange to add currents.)

**1.58** Figure P1.58 shows a transconductance amplifier whose output is *fed back* to its input. Find the input resistance  $R_{in}$  of the resulting one-port network. (*Hint:* Apply a test voltage  $v_x$  between the two input terminals, and find the current  $i_x$  drawn from the source. Then,  $R_{in} \equiv v_x/i_x$ .)

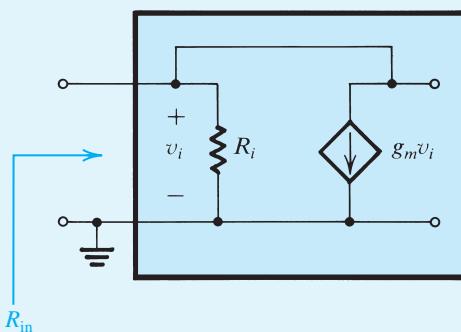


Figure P1.58

**D 1.59** It is required to design an amplifier to sense the open-circuit output voltage of a transducer and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of  $1\text{ k}\Omega$  to  $10\text{ k}\Omega$ . Also, the load resistance varies in the range of  $1\text{ k}\Omega$  to  $10\text{ k}\Omega$ . The change in load voltage corresponding to the specified change in  $R_s$  should be 10% at most. Similarly, the change in load voltage corresponding to the specified change in  $R_L$  should be limited to 10%. Also, corresponding to a 10-mV transducer open-circuit output voltage, the amplifier should provide a minimum of 1 V across the load. What type of amplifier is required? Sketch its circuit model, and specify the values of its parameters. Specify appropriate values for  $R_i$  and  $R_o$  of the form  $1 \times 10^m\ \Omega$ .

**D 1.60** It is required to design an amplifier to sense the short-circuit output current of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of  $1\text{ k}\Omega$  to  $10\text{ k}\Omega$ . Similarly, the load resistance is known to vary over the range of  $1\text{ k}\Omega$  to  $10\text{ k}\Omega$ . The change in load current corresponding to the specified change in  $R_s$  is required to be limited to 10%. Similarly, the change in load current corresponding to the specified change in  $R_L$

should be 10% at most. Also, for a nominal short-circuit output current of the transducer of  $10 \mu\text{A}$ , the amplifier is required to provide a minimum of  $1 \text{ mA}$  through the load. What type of amplifier is required? Sketch the circuit model of the amplifier, and specify values for its parameters. Select appropriate values for  $R_i$  and  $R_o$  in the form  $1 \times 10^m \Omega$ .

**D 1.61** It is required to design an amplifier to sense the open-circuit output voltage of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of  $1 \text{ k}\Omega$  to  $10 \text{ k}\Omega$ . Also, the load resistance is known to vary in the range of  $1 \text{ k}\Omega$  to  $10 \text{ k}\Omega$ . The change in the current supplied to the load corresponding to the specified change in  $R_s$  is to be 10% at most. Similarly, the change in load current corresponding to the specified change in  $R_L$  is to be 10% at most. Also, for a nominal transducer open-circuit output voltage of  $10 \text{ mV}$ , the amplifier is required to provide a minimum of  $1 \text{ mA}$  current through the load. What type of amplifier is required? Sketch the amplifier circuit model, and specify values for its parameters. For  $R_i$  and  $R_o$ , specify values in the form  $1 \times 10^m \Omega$ .

**D 1.62** It is required to design an amplifier to sense the short-circuit output current of a transducer and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of  $1 \text{ k}\Omega$  to  $10 \text{ k}\Omega$ . Similarly, the load resistance is known to vary in the range of  $1 \text{ k}\Omega$  to  $10 \text{ k}\Omega$ . The change in load voltage corresponding to the specified change in  $R_s$  should be 10% at most. Similarly, the change in load voltage corresponding to the specified change in  $R_L$  is to be limited to 10%. Also, for a nominal transducer short-circuit output current of  $10 \mu\text{A}$ , the amplifier is required to provide a minimum voltage across the load of  $1 \text{ V}$ . What type of amplifier is required? Sketch its circuit model, and specify the values of the model parameters. For  $R_i$  and  $R_o$ , specify appropriate values in the form  $1 \times 10^m \Omega$ .

**1.63** For the circuit in Fig. P1.63, show that

$$\frac{v_c}{v_b} = \frac{-\beta R_L}{r_\pi + (\beta + 1)R_E}$$

and

$$\frac{v_e}{v_b} = \frac{R_E}{R_E + [r_\pi/(\beta + 1)]}$$

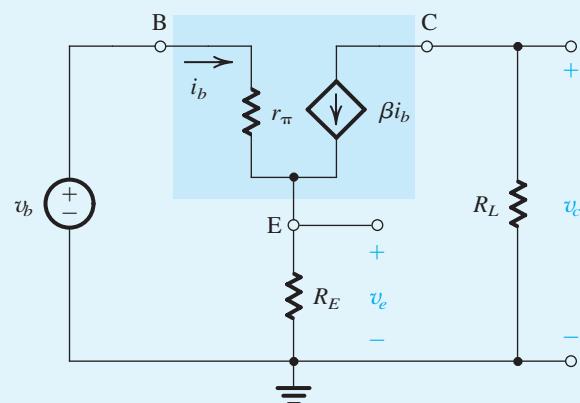


Figure P1.63

**1.64** An amplifier with an input resistance of  $5 \text{ k}\Omega$ , when driven by a current source of  $1 \mu\text{A}$  and a source resistance of  $200 \text{ k}\Omega$ , has a short-circuit output current of  $5 \text{ mA}$  and an open-circuit output voltage of  $10 \text{ V}$ . If the amplifier is used to drive a  $2\text{-k}\Omega$  load, give the values of the voltage gain, current gain, and power gain expressed as ratios and in decibels.

**1.65** Figure P1.65(a) shows two transconductance amplifiers connected in a special configuration. Find  $v_o$  in terms of  $v_1$  and  $v_2$ . Let  $g_m = 100 \text{ mA/V}$  and  $R = 5 \text{ k}\Omega$ . If  $v_1 = v_2 = 1 \text{ V}$ , find the value of  $v_o$ . Also, find  $v_o$  for the case  $v_1 = 1.01 \text{ V}$  and  $v_2 = 0.99 \text{ V}$ . (Note: This circuit is called a **differential amplifier** and is given the symbol shown

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in Fig. P1.65(b). A particular type of differential amplifier known as an **operational amplifier** will be studied in Chapter 2.)

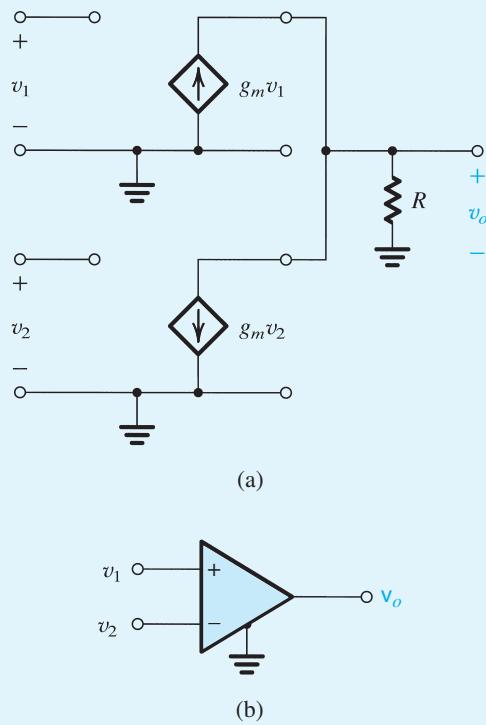


Figure P1.65

**1.66** Any linear two-port network including linear amplifiers can be represented by one of four possible parameter sets, given in Appendix C. For the voltage amplifier, the most convenient representation is in terms of the *g* parameters. If the amplifier input port is labeled as port 1 and the output port as port 2, its *g*-parameter representation is described by the two equations:

$$\begin{aligned} I_1 &= g_{11}V_1 + g_{12}I_2 \\ V_2 &= g_{21}V_1 + g_{22}I_2 \end{aligned}$$

Figure P1.66 shows an equivalent circuit representation of these two equations. By comparing this equivalent circuit

to that of the voltage amplifier in Fig. 1.16(a), identify corresponding currents and voltages as well as the correspondence between the parameters of the amplifier equivalent circuit and the *g* parameters. Hence give the *g* parameter that corresponds to each of  $R_i$ ,  $A_{vo}$ , and  $R_o$ . Notice that there is an additional *g* parameter with no correspondence in the amplifier equivalent circuit. Which one? What does it signify? What assumption did we make about the amplifier that resulted in the absence of this particular *g* parameter from the equivalent circuit in Fig. 1.16(a)?

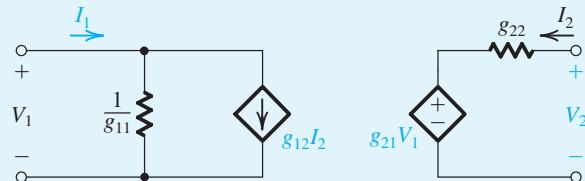


Figure P1.66

### Section 1.6: Frequency Response of Amplifiers

**1.67** Use the voltage-divider rule to derive the transfer functions  $T(s) \equiv V_o(s)/V_i(s)$  of the circuits shown in Fig. 1.22, and show that the transfer functions are of the form given at the top of Table 1.2.

**1.68** Figure P1.68 shows a signal source connected to the input of an amplifier. Here  $R_s$  is the source resistance, and  $R_i$  and  $C_i$  are the input resistance and input capacitance, respectively, of the amplifier. Derive an expression for  $V_i(s)/V_s(s)$ , and show that it is of the low-pass STC type. Find the 3-dB frequency for the case  $R_s = 10 \text{ k}\Omega$ ,  $R_i = 40 \text{ k}\Omega$ , and  $C_i = 5 \text{ pF}$ .

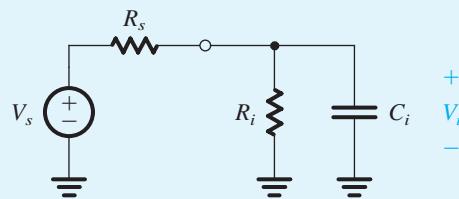


Figure P1.68

- 1.69** For the circuit shown in Fig. P1.69, find the transfer function  $T(s) = V_o(s)/V_i(s)$ , and arrange it in the appropriate standard form from Table 1.2. Is this a high-pass or a low-pass network? What is its transmission at very high frequencies? [Estimate this directly, as well as by letting  $s \rightarrow \infty$  in your expression for  $T(s)$ .] What is the corner frequency  $\omega_0$ ? For  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 40 \text{ k}\Omega$ , and  $C = 1 \mu\text{F}$ , find  $f_0$ . What is the value of  $|T(j\omega_0)|$ ?

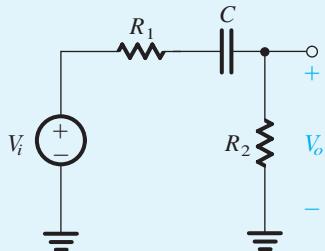


Figure P1.69

- D 1.70** It is required to couple a voltage source  $V_s$  with a resistance  $R_s$  to a load  $R_L$  via a capacitor  $C$ . Derive an expression for the transfer function from source to load (i.e.,  $V_o/V_s$ ), and show that it is of the high-pass STC type. For  $R_s = 5 \text{ k}\Omega$  and  $R_L = 20 \text{ k}\Omega$ , find the smallest coupling capacitor that will result in a 3-dB frequency no greater than 100 Hz.

- 1.71** Measurement of the frequency response of an amplifier yields the data in the following table:

$f$ (Hz)	$ T $ (dB)	$\angle T$ (°)
0	40	0
100	40	0
1000		
$10^4$	37	-45
$10^5$	20	
	0	

Provide plausible approximate values for the missing entries. Also, sketch and clearly label the magnitude frequency response (i.e., provide a Bode plot) for this amplifier.

- 1.72** Measurement of the frequency response of an amplifier yields the data in the following table:

$f$ (Hz)	10	$10^2$	$10^3$	$10^4$	$10^5$	$10^6$	$10^7$	
$ T $ (dB)	0	20	37	40		37	20	0

Provide approximate plausible values for the missing table entries. Also, sketch and clearly label the magnitude frequency response (Bode plot) of this amplifier.

- 1.73** The unity-gain voltage amplifiers in the circuit of Fig. P1.73 have infinite input resistances and zero output

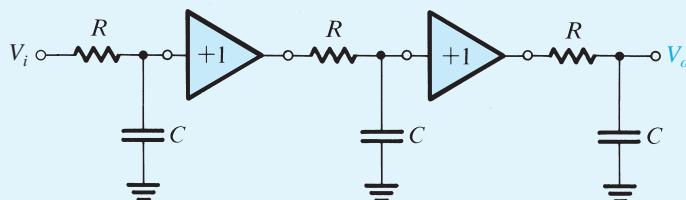


Figure P1.73

resistances and thus function as perfect buffers. Furthermore, assume that their gain is frequency independent. Convince yourself that the overall gain  $V_o/V_i$  will drop by 3 dB below the value at dc at the frequency for which the gain of each  $RC$  circuit is 1.0 dB down. What is that frequency in terms of  $CR$ ?

**1.74** A manufacturing error causes an internal node of a high-frequency amplifier whose Thévenin-equivalent node resistance is  $100 \text{ k}\Omega$  to be accidentally shunted to ground by a capacitor (i.e., the node is connected to ground through a capacitor). If the measured 3-dB bandwidth of the amplifier is reduced from the expected 5 MHz to 100 kHz, estimate the value of the shunting capacitor. If the original cutoff frequency can be attributed to a small parasitic capacitor at the same internal node (i.e., between the node and ground), what would you estimate it to be?

**D \*1.75** A designer wishing to lower the overall upper 3-dB frequency of a three-stage amplifier to 10 kHz considers shunting one of two nodes: Node A, between the output of the first stage and the input of the second stage, and Node B, between the output of the second stage and the input of the third stage, to ground with a small capacitor. While measuring the overall frequency response of the amplifier, she connects a capacitor of  $1 \text{ nF}$ , first to node A and then to node B, lowering the 3-dB frequency from 3 MHz to 200 kHz and 20 kHz, respectively. If she knows that each amplifier stage has an input resistance of  $100 \text{ k}\Omega$ , what output resistance must the driving stage have at node A? At node B? What capacitor value should she connect to which node to solve her design problem most economically?

**D 1.76** An amplifier with an input resistance of  $100 \text{ k}\Omega$  and an output resistance of  $1 \text{ k}\Omega$  is to be capacitor-coupled to a  $10\text{-k}\Omega$  source and a  $1\text{-k}\Omega$  load. Available capacitors have values only of the form  $1 \times 10^{-n} \text{ F}$ . What are the values of the smallest capacitors needed to ensure that the corner frequency associated with each is less than 100 Hz? What actual corner frequencies result? For the situation in which the basic amplifier has an open-circuit voltage gain ( $A_{vo}$ ) of  $100 \text{ V/V}$ , find an expression for  $T(s) = V_o(s)/V_s(s)$ .

**\*1.77** A voltage amplifier has the transfer function

$$A_v = \frac{1000}{\left(1 + j \frac{f}{10^5}\right)\left(1 + j \frac{10^2}{f}\right)}$$

Using the Bode plots for low-pass and high-pass STC networks (Figs. 1.23 and 1.24), sketch a Bode plot for  $|A_v|$ . Give approximate values for the gain magnitude at  $f = 10 \text{ Hz}$ ,  $10^2 \text{ Hz}$ ,  $10^3 \text{ Hz}$ ,  $10^4 \text{ Hz}$ ,  $10^5 \text{ Hz}$ ,  $10^6 \text{ Hz}$ ,  $10^7 \text{ Hz}$ , and  $10^8 \text{ Hz}$ . Find the bandwidth of the amplifier (defined as the frequency range over which the gain remains within 3 dB of the maximum value).

**\*1.78** For the circuit shown in Fig. P1.78, first evaluate  $T_i(s) = V_i(s)/V_s(s)$  and the corresponding cutoff (corner) frequency. Second, evaluate  $T_o(s) = V_o(s)/V_i(s)$  and the corresponding cutoff frequency. Put each of the transfer functions in the standard form (see Table 1.2), and combine them to form the overall transfer function,  $T(s) = T_i(s) \times T_o(s)$ . Provide a Bode magnitude plot for  $|T(j\omega)|$ . What is the bandwidth between 3-dB cutoff points?

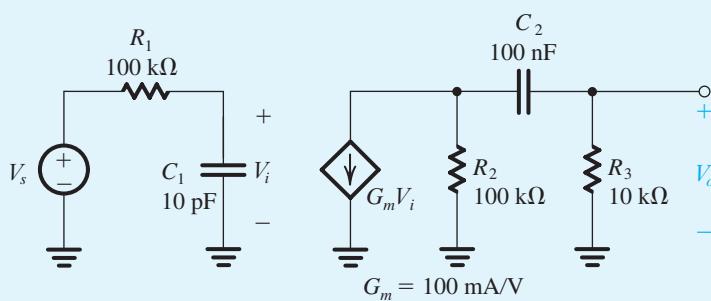


Figure P1.78

**D \*\*1.79** A transconductance amplifier having the equivalent circuit shown in Table 1.1 is fed with a voltage source  $V_s$  having a source resistance  $R_s$ , and its output is connected to a load consisting of a resistance  $R_L$  in parallel with a capacitance  $C_L$ . For given values of  $R_s$ ,  $R_L$ , and  $C_L$ , it is required to specify the values of the amplifier parameters  $R_i$ ,  $G_m$ , and  $R_o$  to meet the following design constraints:

- At most,  $x\%$  of the input signal is lost in coupling the signal source to the amplifier (i.e.,  $V_i \geq [1 - (x/100)]V_s$ ).
- The 3-dB frequency of the amplifier is equal to or greater than a specified value  $f_{3 \text{ dB}}$ .
- The dc gain  $V_o/V_s$  is equal to or greater than a specified value  $A_0$ .

Show that these constraints can be met by selecting

$$R_i \geq \left( \frac{100}{x} - 1 \right) R_s$$

$$R_o \leq \frac{1}{2\pi f_{3 \text{ dB}} C_L - (1/R_L)}$$

$$G_m \geq \frac{A_0/[1 - (x/100)]}{(R_L \parallel R_o)}$$

Find  $R_i$ ,  $R_o$ , and  $G_m$  for  $R_s = 10 \text{ k}\Omega$ ,  $x = 10\%$ ,  $A_0 = 100 \text{ V/V}$ ,  $R_L = 10 \text{ k}\Omega$ ,  $C_L = 20 \text{ pF}$ , and  $f_{3 \text{ dB}} = 2 \text{ MHz}$ .

**\*1.80** Use the voltage-divider rule to find the transfer function  $V_o(s)/V_i(s)$  of the circuit in Fig. P1.80. Show that the transfer function can be made independent of frequency if the condition  $C_1 R_1 = C_2 R_2$  applies. Under this condition

the circuit is called a **compensated attenuator** and is frequently employed in the design of oscilloscope probes. Find the transmission of the compensated attenuator in terms of  $R_1$  and  $R_2$ .

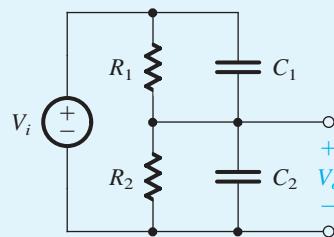


Figure P1.80

**\*1.81** An amplifier with a frequency response of the type shown in Fig. 1.21 is specified to have a phase shift of magnitude no greater than  $5.7^\circ$  over the amplifier bandwidth, which extends from 100 Hz to 1 kHz. It has been found that the gain falloff at the low-frequency end is determined by the response of a high-pass STC circuit and that at the high-frequency end it is determined by a low-pass STC circuit. What do you expect the corner frequencies of these two circuits to be? What is the drop in gain in decibels (relative to the maximum gain) at the two frequencies that define the amplifier bandwidth? What are the frequencies at which the drop in gain is 3 dB? (Hint: Refer to Figs. 1.23 and 1.24.)

## CHAPTER 2

# Operational Amplifiers

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## IN THIS CHAPTER YOU WILL LEARN

1. The terminal characteristics of the ideal op amp.
2. How to analyze circuits containing op amps, resistors, and capacitors.
3. How to use op amps to design amplifiers having precise characteristics.
4. How to design more sophisticated op-amp circuits, including summing amplifiers, instrumentation amplifiers, integrators, and differentiators.
5. Important nonideal characteristics of op amps and how these limit the performance of basic op-amp circuits.

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## Introduction

Having learned basic amplifier concepts and terminology, we are now ready to undertake the study of a circuit building block of universal importance: the operational amplifier (op amp). Op amps have been in use for a long time, their initial applications being primarily in the areas of analog computation and sophisticated instrumentation. Early op amps were constructed from discrete components (vacuum tubes and then transistors, and resistors), and their cost was prohibitively high (tens of dollars). In the mid-1960s the first integrated-circuit (IC) op amp was produced. This unit (the  $\mu$ A 709) was made up of a relatively large number of transistors and resistors all on the same silicon chip. Although its characteristics were poor (by today's standards) and its price was still quite high, its appearance signaled a new era in electronic circuit design. Electronics engineers started using op amps in large quantities, which caused their price to drop dramatically. They also demanded better-quality op amps. Semiconductor manufacturers responded quickly, and within the span of a few years, high-quality op amps became available at extremely low prices (tens of cents) from a large number of suppliers.

One of the reasons for the popularity of the op amp is its versatility. As we will shortly see, one can do almost anything with op amps! Equally important is the fact that the IC op amp has characteristics that closely approach the assumed ideal. This implies that it is quite easy to design circuits using the IC op amp. Also, op-amp circuits work at performance levels that are quite close to those predicted theoretically. It is for this reason that we are studying op amps at this early stage. It is expected that by the end of this chapter the reader should be able to successfully design nontrivial circuits using op amps.

As already implied, an IC op amp is made up of a large number (about 20) of transistors together with resistors, and (usually) one capacitor connected in a rather complex circuit. Since

we have not yet studied transistor circuits, the circuit inside the op amp will not be discussed in this chapter. Rather, we will treat the op amp as a circuit building block and study its terminal characteristics and its applications. This approach is quite satisfactory in many op-amp applications. Nevertheless, for the more difficult and demanding applications it is quite useful to know what is inside the op-amp package. This topic will be studied in Chapter 13. More advanced applications of op amps will appear in later chapters.

## 2.1 The Ideal Op Amp

### 2.1.1 The Op-Amp Terminals

From a signal point of view the op amp has three terminals: two input terminals and one output terminal. Figure 2.1 shows the symbol we shall use to represent the op amp. Terminals 1 and 2 are input terminals, and terminal 3 is the output terminal. As explained in Section 1.4, amplifiers require dc power to operate. Most IC op amps require two dc power supplies, as shown in Fig. 2.2. Two terminals, 4 and 5, are brought out of the op-amp package and connected to a positive voltage  $V_{CC}$  and a negative voltage  $-V_{EE}$ , respectively. In Fig. 2.2(b) we explicitly show the two dc power supplies as batteries with a common ground. It is interesting to note that the reference grounding point in op-amp circuits is just the common terminal of the two power supplies; that is, no terminal of the op-amp package is physically connected to ground. In what follows we will not, for simplicity, explicitly show the op-amp power supplies.

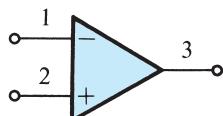


Figure 2.1 Circuit symbol for the op amp.

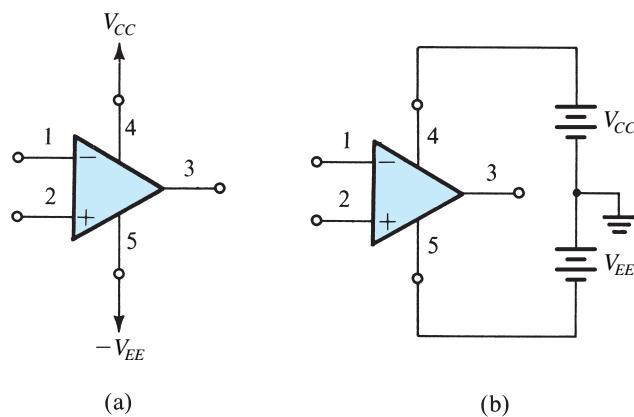


Figure 2.2 The op amp shown connected to dc power supplies.

In addition to the three signal terminals and the two power-supply terminals, an op amp may have other terminals for specific purposes. These other terminals can include terminals for frequency compensation and terminals for offset nulling; both functions will be explained in later sections.

### EXERCISE

- 2.1** What is the minimum number of terminals required by a single op amp? What is the minimum number of terminals required on an integrated-circuit package containing four op amps (called a quad op amp)?

**Ans.** 5; 14

### 2.1.2 Function and Characteristics of the Ideal Op Amp

We now consider the circuit function of the op amp. The op amp is designed to sense the difference between the voltage signals applied at its two input terminals (i.e., the quantity  $v_2 - v_1$ ), multiply this by a number  $A$ , and cause the resulting voltage  $A(v_2 - v_1)$  to appear at output terminal 3. Thus  $v_3 = A(v_2 - v_1)$ . Here it should be emphasized that when we talk about the voltage at a terminal we mean the voltage between that terminal and ground; thus  $v_1$  means the voltage applied between terminal 1 and ground.

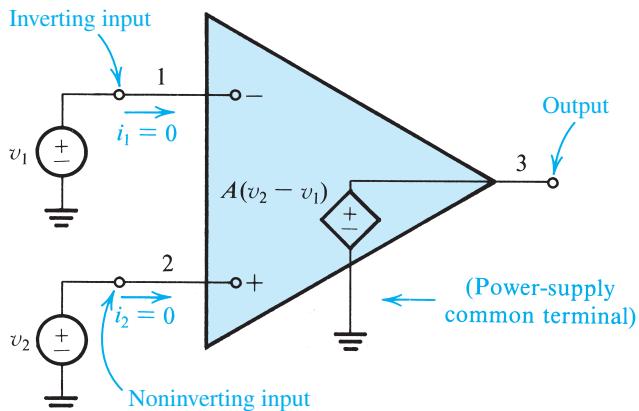
The ideal op amp is not supposed to draw any input current; that is, the signal current into terminal 1 and the signal current into terminal 2 are both zero. In other words, *the input impedance of an ideal op amp is supposed to be infinite*.

How about the output terminal 3? This terminal is supposed to act as the output terminal of an ideal voltage source. That is, the voltage between terminal 3 and ground will always be equal to  $A(v_2 - v_1)$ , independent of the current that may be drawn from terminal 3 into a load impedance. In other words, *the output impedance of an ideal op amp is supposed to be zero*.

Putting together all of the above, we arrive at the equivalent circuit model shown in Fig. 2.3. Note that the output is in phase with (has the same sign as)  $v_2$  and is out of phase with (has the opposite sign of)  $v_1$ . For this reason, input terminal 1 is called the **inverting input terminal** and is distinguished by a “−” sign, while input terminal 2 is called the **noninverting input terminal** and is distinguished by a “+” sign.

As can be seen from the above description, the op amp responds only to the *difference* signal  $v_2 - v_1$  and hence ignores any signal *common* to both inputs. That is, if  $v_1 = v_2 = 1\text{ V}$ , then the output will (ideally) be zero. We call this property **common-mode rejection**, and we conclude that an ideal op amp has zero common-mode gain or, equivalently, infinite common-mode rejection. We will have more to say about this point later. For the time being note that the op amp is a **differential-input, single-ended-output** amplifier, with the latter term referring to the fact that the output appears between terminal 3 and ground.<sup>1</sup>

<sup>1</sup>Some op amps are designed to have differential outputs. This topic will not be discussed in this book. Rather, we confine ourselves here to single-ended-output op amps, which constitute the vast majority of commercially available op amps.



**Figure 2.3** Equivalent circuit of the ideal op amp.

Furthermore, gain  $A$  is called the **differential gain**, for obvious reasons. Perhaps not so obvious is another name that we will attach to  $A$ : the **open-loop gain**. The reason for this name will become obvious later on when we “close the loop” around the op amp and define another gain, the closed-loop gain.

An important characteristic of op amps is that they are **direct-coupled** or **dc amplifiers**, where dc stands for direct-coupled (it could equally well stand for direct current, since a direct-coupled amplifier is one that amplifies signals whose frequency is as low as zero). The fact that op amps are direct-coupled devices will allow us to use them in many important applications. Unfortunately, though, the direct-coupling property can cause some serious practical problems, as will be discussed in a later section.

How about bandwidth? The ideal op amp has a gain  $A$  that remains constant down to zero frequency and up to infinite frequency. That is, ideal op amps will amplify signals of any frequency with equal gain, and are thus said to have *infinite bandwidth*.

We have discussed all of the properties of the ideal op amp except for one, which in fact is the most important. This has to do with the value of  $A$ . *The ideal op amp should have a gain  $A$  whose value is very large and ideally infinite*. One may justifiably ask: If the gain  $A$  is infinite, how are we going to use the op amp? The answer is very simple: In almost all applications the op amp will *not* be used alone in a so-called open-loop configuration. Rather, we will use other components to apply feedback to close the loop around the op amp, as will be illustrated in detail in Section 2.2.

For future reference, Table 2.1 lists the characteristics of the ideal op amp.

**Table 2.1** Characteristics of the Ideal Op Amp

1. Infinite input impedance
2. Zero output impedance
3. Zero common-mode gain or, equivalently, infinite common-mode rejection
4. Infinite open-loop gain  $A$
5. Infinite bandwidth

### 2.1.3 Differential and Common-Mode Signals

The differential input signal  $v_{Id}$  is simply the difference between the two input signals  $v_1$  and  $v_2$ ; that is,

$$v_{Id} = v_2 - v_1 \quad (2.1)$$

The common-mode input signal  $v_{Icm}$  is the average of the two input signals  $v_1$  and  $v_2$ ; namely,

$$v_{Icm} = \frac{1}{2}(v_1 + v_2) \quad (2.2)$$

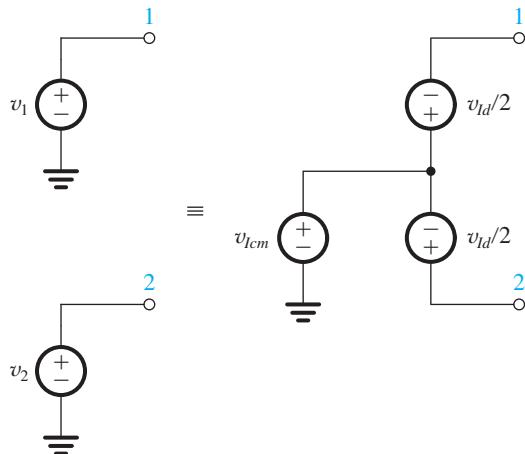
Equations (2.1) and (2.2) can be used to express the input signals  $v_1$  and  $v_2$  in terms of their differential and common-mode components as follows:

$$v_1 = v_{Icm} - v_{Id}/2 \quad (2.3)$$

and

$$v_2 = v_{Icm} + v_{Id}/2 \quad (2.4)$$

These equations can in turn lead to the pictorial representation in Fig. 2.4.



**Figure 2.4** Representation of the signal sources  $v_1$  and  $v_2$  in terms of their differential and common-mode components.

### EXERCISES

- 2.2** Consider an op amp that is ideal except that its open-loop gain  $A = 10^3$ . The op amp is used in a feedback circuit, and the voltages appearing at two of its three signal terminals are measured. In each of the following cases, use the measured values to find the expected value of the voltage at the third terminal. Also give the differential and common-mode input signals in each case. (a)  $v_2 = 0$  V and  $v_3 = 2$  V; (b)  $v_2 = +5$  V and  $v_3 = -10$  V; (c)  $v_1 = 1.002$  V and  $v_2 = 0.998$  V; (d)  $v_1 = -3.6$  V and  $v_3 = -3.6$  V.

**Ans.** (a)  $v_1 = -0.002$  V,  $v_{Id} = 2$  mV,  $v_{Icm} = -1$  mV; (b)  $v_1 = +5.01$  V,  $v_{Id} = -10$  mV,  $v_{Icm} = 5.005 \approx 5$  V; (c)  $v_3 = -4$  V,  $v_{Id} = -4$  mV,  $v_{Icm} = 1$  V; (d)  $v_2 = -3.6036$  V,  $v_{Id} = -3.6$  mV,  $v_{Icm} \approx -3.6$  V

- 2.3** The internal circuit of a particular op amp can be modeled by the circuit shown in Fig. E2.3. Express  $v_3$  as a function of  $v_1$  and  $v_2$ . For the case  $G_m = 10 \text{ mA/V}$ ,  $R = 10 \text{ k}\Omega$ , and  $\mu = 100$ , find the value of the open-loop gain  $A$ .

**Ans.**  $v_3 = \mu G_m R (v_2 - v_1)$ ;  $A = 10,000 \text{ V/V}$  or  $80 \text{ dB}$

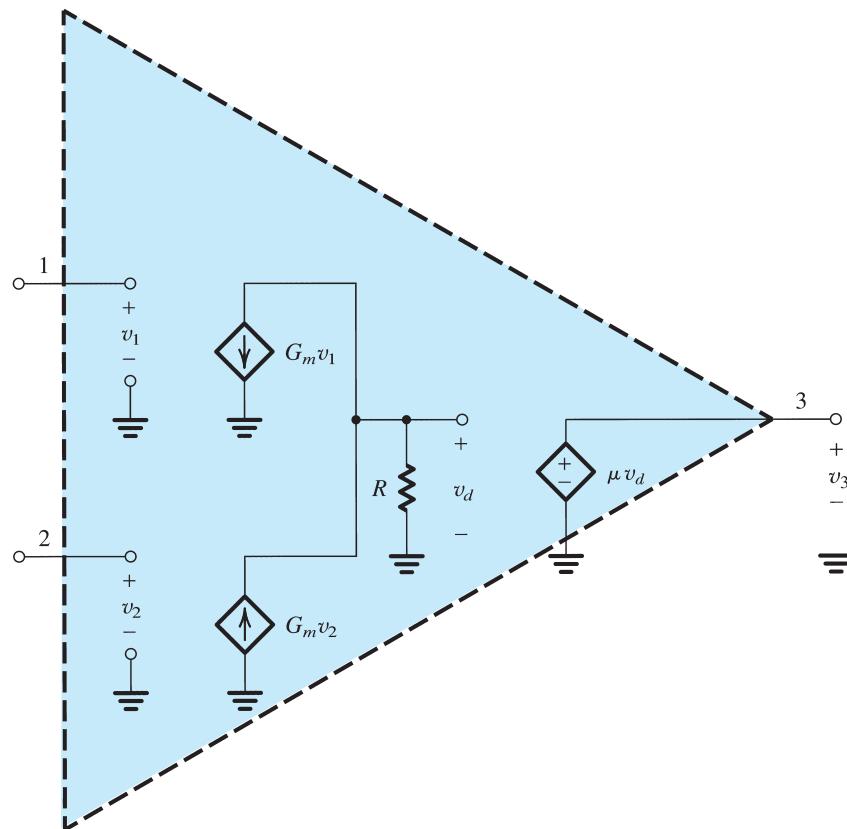
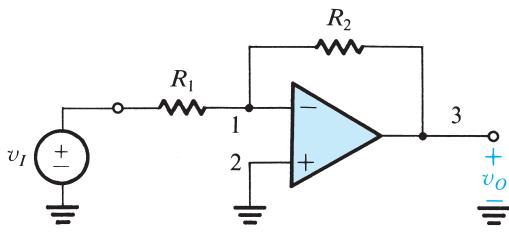


Figure E2.3

## 2.2 The Inverting Configuration

As mentioned above, op amps are not used alone; rather, the op amp is connected to passive components in a feedback circuit. There are two such basic circuit configurations employing an op amp and two resistors: the inverting configuration, which is studied in this section, and the noninverting configuration, which we shall study in the next section.

Figure 2.5 shows the inverting configuration. It consists of one op amp and two resistors  $R_1$  and  $R_2$ . Resistor  $R_2$  is connected from the output terminal of the op amp, terminal 3, back to the *inverting* or *negative* input terminal, terminal 1. We speak of  $R_2$  as applying **negative feedback**; if  $R_2$  were connected between terminals 3 and 2 we would have called this **positive feedback**. Note also that  $R_2$  *closes the loop* around the op amp. In addition to adding  $R_2$ , we have grounded terminal 2 and connected a resistor  $R_1$  between terminal 1 and an input signal source



**Figure 2.5** The inverting closed-loop configuration.

with a voltage  $v_I$ . The output of the overall circuit is taken at terminal 3 (i.e., between terminal 3 and ground). Terminal 3 is, of course, a convenient point from which to take the output, since the impedance level there is ideally zero. Thus the voltage  $v_O$  will not depend on the value of the current that might be supplied to a load impedance connected between terminal 3 and ground.

### 2.2.1 The Closed-Loop Gain

We now wish to analyze the circuit in Fig. 2.5 to determine the **closed-loop gain**  $G$ , defined as

$$G \equiv \frac{v_O}{v_I}$$

We will do so assuming the op amp to be ideal. Figure 2.6(a) shows the equivalent circuit, and the analysis proceeds as follows: The gain  $A$  is very large (ideally infinite). If we assume that the circuit is “working” and producing a finite output voltage at terminal 3, then the voltage between the op-amp input terminals should be negligibly small and ideally zero. Specifically, if we call the output voltage  $v_O$ , then, by definition,

$$v_2 - v_1 = \frac{v_O}{A} = 0$$

It follows that the voltage at the inverting input terminal ( $v_1$ ) is given by  $v_1 = v_2$ . That is, because the gain  $A$  approaches infinity, the voltage  $v_1$  approaches and ideally equals  $v_2$ . We speak of this as the two input terminals “tracking each other in potential.” We also speak of a “virtual short circuit” that exists between the two input terminals. Here the word *virtual* should be emphasized, and one should *not* make the mistake of physically shorting terminals 1 and 2 together while analyzing a circuit. A **virtual short circuit** means that whatever voltage is at 2 will automatically appear at 1 because of the infinite gain  $A$ . But terminal 2 happens to be connected to ground; thus  $v_2 = 0$  and  $v_1 = 0$ . We speak of terminal 1 as being a **virtual ground**—that is, having zero voltage but not physically connected to ground.

Now that we have determined  $v_1$  we are in a position to apply Ohm’s law and find the current  $i_1$  through  $R_1$  (see Fig. 2.6) as follows:

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

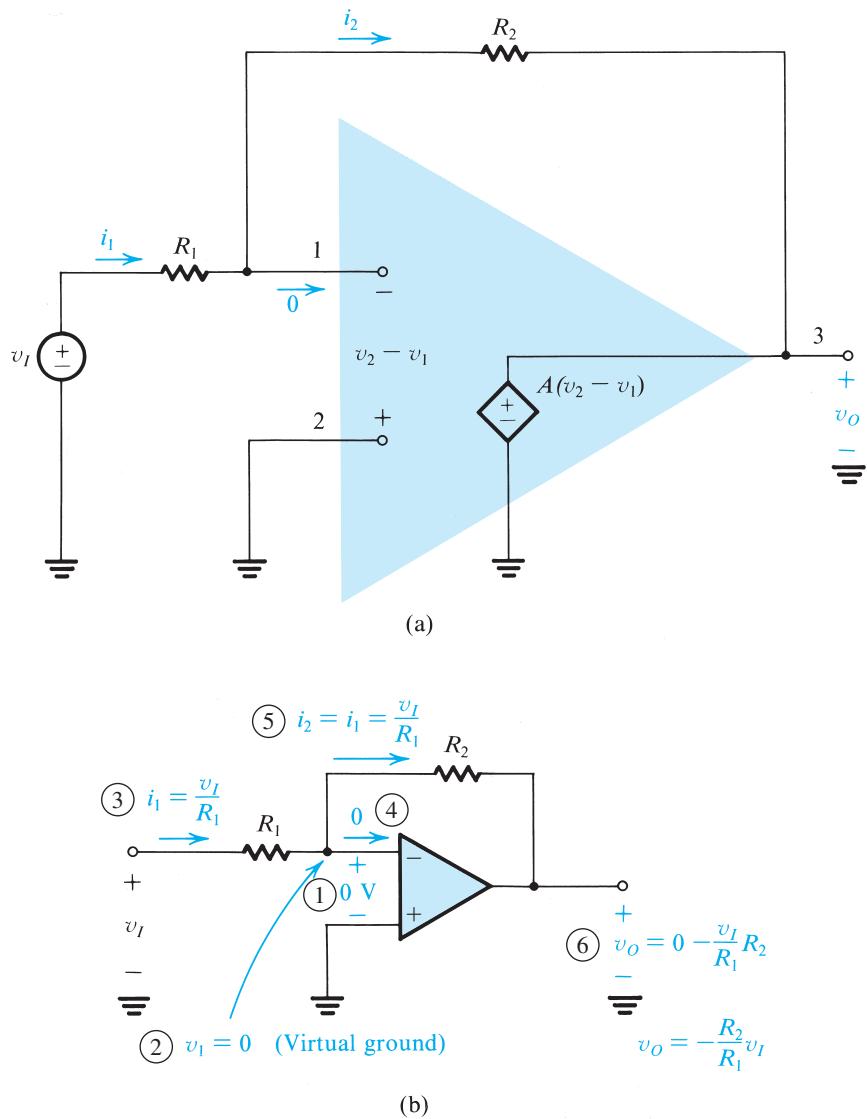
Where will this current go? It cannot go into the op amp, since the ideal op amp has an infinite input impedance and hence draws zero current. It follows that  $i_1$  will have to flow through  $R_2$  to the low-impedance terminal 3. We can then apply Ohm’s law to  $R_2$  and determine  $v_O$ ; that is,

$$\begin{aligned} v_O &= v_1 - i_1 R_2 \\ &= 0 - \frac{v_I}{R_1} R_2 \end{aligned}$$

Thus,

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1}$$





**Figure 2.6** Analysis of the inverting configuration. The circled numbers indicate the order of the analysis steps.

which is the required closed-loop gain. Figure 2.6(b) illustrates these steps and indicates by the circled numbers the order in which the analysis is performed.

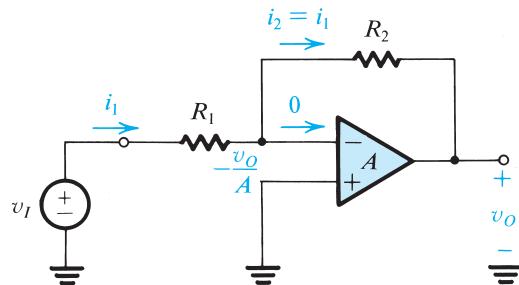
We thus see that the closed-loop gain is simply the ratio of the two resistances  $R_2$  and  $R_1$ . The minus sign means that the closed-loop amplifier provides signal inversion. Thus if  $R_2/R_1 = 10$  and we apply at the input ( $v_I$ ) a sine-wave signal of 1 V peak-to-peak, then the output  $v_O$  will be a sine wave of 10 V peak-to-peak and phase-shifted  $180^\circ$  with respect to the input sine wave. Because of the minus sign associated with the closed-loop gain, this configuration is called the **inverting configuration**.

The fact that the closed-loop gain depends entirely on external passive components (resistors  $R_1$  and  $R_2$ ) is very significant. It means that we can make the closed-loop gain as accurate as we want by selecting passive components of appropriate accuracy. It also means that the closed-loop gain is (ideally) independent of the op-amp gain. This is a dramatic illustration of negative feedback: We started out with an amplifier having very large gain  $A$ , and through applying negative feedback we have obtained a closed-loop gain  $R_2/R_1$  that is much smaller than  $A$  but is stable and predictable. That is, we are trading gain for accuracy.

## 2.2.2 Effect of Finite Open-Loop Gain

The points just made are more clearly illustrated by deriving an expression for the closed-loop gain under the assumption that the op-amp open-loop gain  $A$  is finite. Figure 2.7 shows the analysis. If we denote the output voltage  $v_o$ , then the voltage between the two input terminals of the op amp will be  $v_o/A$ . Since the positive input terminal is grounded, the voltage at the negative input terminal must be  $-v_o/A$ . The current  $i_1$  through  $R_1$  can now be found from

$$i_1 = \frac{v_I - (-v_o/A)}{R_1} = \frac{v_I + v_o/A}{R_1}$$



**Figure 2.7** Analysis of the inverting configuration taking into account the finite open-loop gain of the op amp.

The infinite input impedance of the op amp forces the current  $i_1$  to flow entirely through  $R_2$ . The output voltage  $v_o$  can thus be determined from

$$\begin{aligned} v_o &= -\frac{v_o}{A} - i_1 R_2 \\ &= -\frac{v_o}{A} - \left( \frac{v_I + v_o/A}{R_1} \right) R_2 \end{aligned}$$

Collecting terms, the closed-loop gain  $G$  is found as

$$G \equiv \frac{v_o}{v_I} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A} \quad (2.5)$$

We note that as  $A$  approaches  $\infty$ ,  $G$  approaches the ideal value of  $-R_2/R_1$ . Also, from Fig. 2.7 we see that as  $A$  approaches  $\infty$ , the voltage at the inverting input terminal approaches zero. This is the virtual-ground assumption we used in our earlier analysis when the op amp was

assumed to be ideal. Finally, note that Eq. (2.5) in fact indicates that to minimize the dependence of the closed-loop gain  $G$  on the value of the open-loop gain  $A$ , we should make

$$1 + \frac{R_2}{R_1} \ll A$$

### Example 2.1

Consider the inverting configuration with  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 100 \text{ k}\Omega$ , that is, having an ideal closed-loop gain of  $-100$ .

- (a) Find the closed-loop gain for the cases  $A = 10^3, 10^4$ , and  $10^5$ . In each case determine the percentage error in the magnitude of  $G$  relative to the ideal value of  $R_2/R_1$  (obtained with  $A = \infty$ ). Also determine the voltage  $v_1$  that appears at the inverting input terminal when  $v_i = 0.1 \text{ V}$ .
- (b) If the open-loop gain  $A$  changes from 100,000 to 50,000 (i.e., drops by 50%), what is the corresponding percentage change in the magnitude of the closed-loop gain  $G$ ?

#### Solution

- (a) Substituting the given values in Eq. (2.5), we obtain the values given in the following table, where the percentage error  $\epsilon$  is defined as

$$\epsilon \equiv \frac{|G| - (R_2/R_1)}{(R_2/R_1)} \times 100$$

The values of  $v_1$  are obtained from  $v_1 = -v_o/A = Gv_i/A$  with  $v_i = -0.1 \text{ V}$ .

$A$	$ G $	$\epsilon$	$v_1$
$10^3$	90.83	-9.17%	-9.08 mV
$10^4$	99.00	-1.00%	-0.99 mV
$10^5$	99.90	-0.10%	-0.10 mV

- (b) Using Eq. (2.5), we find that for  $A = 50,000$ ,  $|G| = 99.80$ . Thus a -50% change in the open-loop gain results in a change in  $|G|$  from 99.90 to 99.80, which is only -0.1%!

### 2.2.3 Input and Output Resistances

Assuming an ideal op amp with infinite open-loop gain, the input resistance of the closed-loop inverting amplifier of Fig. 2.5 is simply equal to  $R_1$ . This can be seen from Fig. 2.6(b), where

$$R_i \equiv \frac{v_i}{i_1} = \frac{v_i}{v_i/R_1} = R_1$$

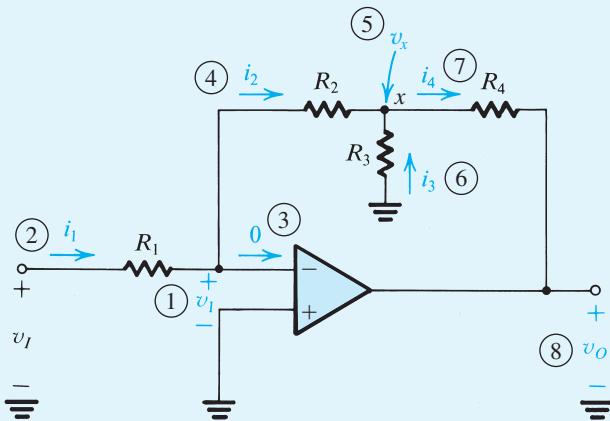
Now recall that in Section 1.5 we learned that the amplifier input resistance forms a voltage divider with the resistance of the source that feeds the amplifier. Thus, to avoid the loss of signal strength, voltage amplifiers are required to have high input resistance. In the case of the inverting op-amp configuration we are studying, to make  $R_i$  high we should select a high value for  $R_1$ . However, if the required gain  $R_2/R_1$  is also high, then  $R_2$  could become impractically large

(e.g., greater than a few megohms). We may conclude that the inverting configuration suffers from a low input resistance. A solution to this problem is discussed in Example 2.2 below.

Since the output of the inverting configuration is taken at the terminals of the ideal voltage source  $A(v_2 - v_1)$  (see Fig. 2.6a), it follows that the output resistance of the closed-loop amplifier is zero.

### Example 2.2

Assuming the op amp to be ideal, derive an expression for the closed-loop gain  $v_o/v_i$  of the circuit shown in Fig. 2.8. Use this circuit to design an inverting amplifier with a gain of 100 and an input resistance of  $1 \text{ M}\Omega$ . Assume that for practical reasons it is required not to use resistors greater than  $1 \text{ M}\Omega$ . Compare your design with that based on the inverting configuration of Fig. 2.5.



**Figure 2.8** Circuit for Example 2.2. The circled numbers indicate the sequence of the steps in the analysis.

### Solution

The analysis begins at the inverting input terminal of the op amp, where the voltage is

$$v_1 = \frac{-v_o}{A} = \frac{-v_o}{\infty} = 0$$

Here we have assumed that the circuit is “working” and producing a finite output voltage  $v_o$ . Knowing  $v_1$ , we can determine the current  $i_1$  as follows:

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

Since zero current flows into the inverting input terminal, all of  $i_1$  will flow through  $R_2$ , and thus

$$i_2 = i_1 = \frac{v_I}{R_1}$$

Now we can determine the voltage at node  $x$ :

$$v_x = v_1 - i_2 R_2 = 0 - \frac{v_I}{R_1} R_2 = -\frac{R_2}{R_1} v_I$$

**Example 2.2** *continued*

This in turn enables us to find the current  $i_3$ :

$$i_3 = \frac{0 - v_x}{R_3} = \frac{R_2}{R_1 R_3} v_I$$

Next, a node equation at  $x$  yields  $i_4$ :

$$i_4 = i_2 + i_3 = \frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I$$

Finally, we can determine  $v_O$  from

$$\begin{aligned} v_O &= v_x - i_4 R_4 \\ &= -\frac{R_2}{R_1} v_I - \left( \frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I \right) R_4 \end{aligned}$$

Thus the voltage gain is given by

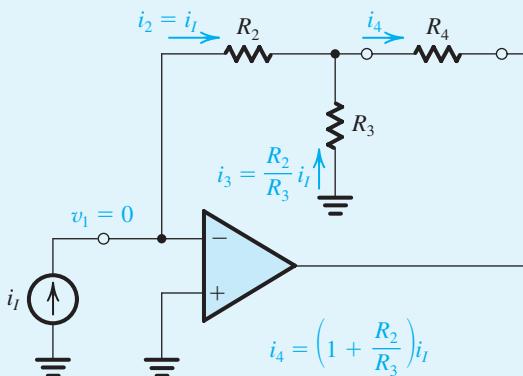
$$\frac{v_O}{v_I} = -\left[ \frac{R_2}{R_1} + \frac{R_4}{R_1} \left( 1 + \frac{R_2}{R_3} \right) \right]$$

which can be written in the form

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1} \left( 1 + \frac{R_4}{R_2} + \frac{R_4}{R_3} \right)$$

Now, since an input resistance of  $1 \text{ M}\Omega$  is required, we select  $R_1 = 1 \text{ M}\Omega$ . Then, with the limitation of using resistors no greater than  $1 \text{ M}\Omega$ , the maximum value possible for the first factor in the gain expression is 1 and is obtained by selecting  $R_2 = 1 \text{ M}\Omega$ . To obtain a gain of  $-100$ ,  $R_3$  and  $R_4$  must be selected so that the second factor in the gain expression is 100. If we select the maximum allowed (in this example) value of  $1 \text{ M}\Omega$  for  $R_4$ , then the required value of  $R_3$  can be calculated to be  $10.2 \text{ k}\Omega$ . Thus this circuit utilizes three  $1\text{-M}\Omega$  resistors and a  $10.2\text{-k}\Omega$  resistor. In comparison, if the inverting configuration were used with  $R_1 = 1 \text{ M}\Omega$  we would have required a feedback resistor of  $100 \text{ M}\Omega$ , an impractically large value!

Before leaving this example it is insightful to inquire into the mechanism by which the circuit is able to realize a large voltage gain without using large resistances in the feedback path. Toward that end, observe that because of the virtual ground at the inverting input terminal of the op amp,  $R_2$  and  $R_3$  are in effect in parallel. Thus, by making  $R_3$  lower than  $R_2$  by, say, a factor  $k$  (i.e., where  $k > 1$ ),  $R_3$  is forced to carry a current  $k$ -times that in  $R_2$ . Thus, while  $i_2 = i_I$ ,  $i_3 = ki_I$  and  $i_4 = (k+1)i_I$ . It is the current multiplication by a factor of  $(k+1)$  that enables a large voltage drop to develop across  $R_4$  and hence a large  $v_O$  without using a large value for  $R_4$ . Notice also that the current through  $R_4$  is independent of the value of  $R_4$ . It follows that the circuit can be used as a current amplifier as shown in Fig. 2.9.



**Figure 2.9** A current amplifier based on the circuit of Fig. 2.8. The amplifier delivers its output current to  $R_4$ . It has a current gain of  $(1 + R_2/R_3)$ , a zero input resistance, and an infinite output resistance. The load ( $R_4$ ), however, must be floating (i.e., neither of its two terminals can be connected to ground).

## EXERCISES

- D2.4** Use the circuit of Fig. 2.5 to design an inverting amplifier having a gain of  $-10$  and an input resistance of  $100 \text{ k}\Omega$ . Give the values of  $R_1$  and  $R_2$ .

**Ans.**  $R_1 = 100 \text{ k}\Omega$ ;  $R_2 = 1 \text{ M}\Omega$

- 2.5** The circuit shown in Fig. E2.5(a) can be used to implement a transresistance amplifier (see Table 1.1 in Section 1.5). Find the value of the input resistance  $R_i$ , the transresistance  $R_m$ , and the output resistance  $R_o$  of the transresistance amplifier. If the signal source shown in Fig. E2.5(b) is connected to the input of the transresistance amplifier, find the amplifier output voltage.

**Ans.**  $R_i = 0$ ;  $R_m = -10 \text{ k}\Omega$ ;  $R_o = 0$ ;  $v_o = -5 \text{ V}$

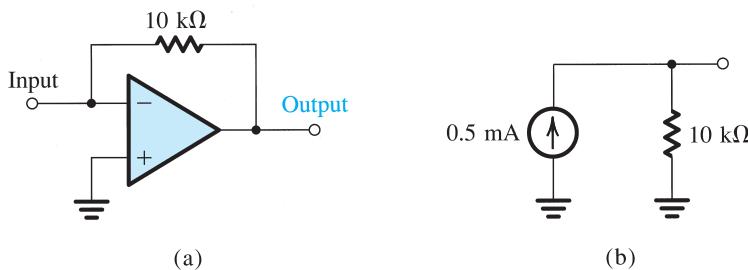


Figure E2.5

- 2.6** For the circuit in Fig. E2.6 determine the values of  $v_1, i_1, i_2, v_o, i_L$ , and  $i_o$ . Also determine the voltage gain  $v_o/v_1$ , current gain  $i_L/i_1$ , and power gain  $P_o/P_I$ .

**Ans.**  $0 \text{ V}$ ;  $1 \text{ mA}$ ;  $1 \text{ mA}$ ;  $-10 \text{ V}$ ;  $-10 \text{ mA}$ ;  $-11 \text{ mA}$ ;  $-10 \text{ V/V}$  (20 dB);  $-10 \text{ A/A}$  (20 dB);  $100 \text{ W/W}$  (20 dB)

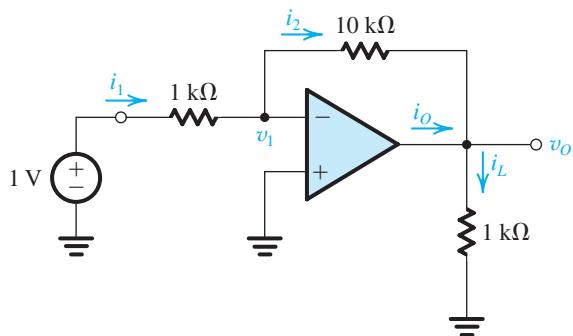


Figure E2.6

## 2.2.4 An Important Application—The Weighted Summer

A very important application of the inverting configuration is the weighted-summer circuit shown in Fig. 2.10. Here we have a resistance  $R_f$  in the negative-feedback path (as before), but we have a number of input signals  $v_1, v_2, \dots, v_n$  each applied to a corresponding resistor

$R_1, R_2, \dots, R_n$ , which are connected to the inverting terminal of the op amp. From our previous discussion, the ideal op amp will have a virtual ground appearing at its negative input terminal. Ohm's law then tells us that the currents  $i_1, i_2, \dots, i_n$  are given by

$$i_1 = \frac{v_1}{R_1}, \quad i_2 = \frac{v_2}{R_2}, \quad \dots, \quad i_n = \frac{v_n}{R_n}$$

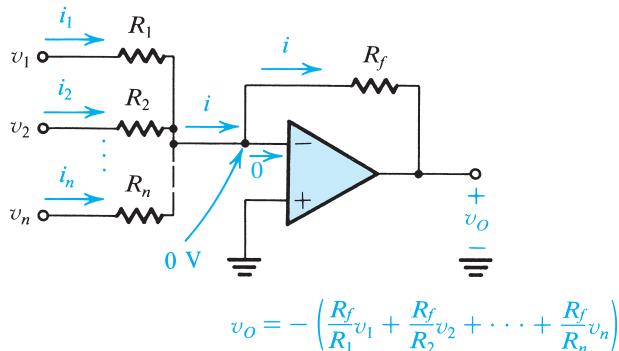


Figure 2.10 A weighted summer.

All these currents sum together to produce the current  $i$ ,

$$i = i_1 + i_2 + \dots + i_n \quad (2.6)$$

which will be forced to flow through  $R_f$  (since no current flows into the input terminals of an ideal op amp). The output voltage  $v_o$  may now be determined by another application of Ohm's law,

$$v_o = 0 - iR_f = -iR_f$$

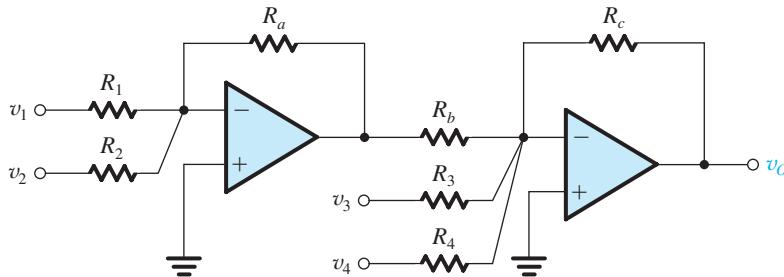
Thus,

$$\rightarrow v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \dots + \frac{R_f}{R_n}v_n\right) \quad (2.7)$$

That is, the output voltage is a weighted sum of the input signals  $v_1, v_2, \dots, v_n$ . This circuit is therefore called a **weighted summer**. Note that each summing coefficient may be independently adjusted by adjusting the corresponding "feed-in" resistor ( $R_1$  to  $R_n$ ). This nice property, which greatly simplifies circuit adjustment, is a direct consequence of the virtual ground that exists at the inverting op-amp terminal. As the reader will soon come to appreciate, virtual grounds are extremely "handy." In the weighted summer of Fig. 2.10 all the summing coefficients must be of the same sign. The need occasionally arises for summing signals with opposite signs. Such a function can be implemented, however, using two op amps as shown in Fig. 2.11. Assuming ideal op amps, it can be easily shown that the output voltage is given by

$$v_o = v_1\left(\frac{R_a}{R_1}\right)\left(\frac{R_c}{R_b}\right) + v_2\left(\frac{R_a}{R_2}\right)\left(\frac{R_c}{R_b}\right) - v_3\left(\frac{R_c}{R_3}\right) - v_4\left(\frac{R_c}{R_4}\right) \quad (2.8)$$

Weighted summers are utilized in a variety of applications including in the design of audio systems, where they can be used in mixing signals originating from different musical instruments.



**Figure 2.11** A weighted summer capable of implementing summing coefficients of both signs.

## EXERCISES

- D2.7** Design an inverting op-amp circuit to form the weighted sum  $v_o$  of two inputs  $v_1$  and  $v_2$ . It is required that  $v_o = -(v_1 + 5v_2)$ . Choose values for  $R_1$ ,  $R_2$ , and  $R_f$  so that for a maximum output voltage of 10 V the current in the feedback resistor will not exceed 1 mA.  
**Ans.** A possible choice:  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ , and  $R_f = 10 \text{ k}\Omega$
- D2.8** Use the idea presented in Fig. 2.11 to design a weighted summer that provides

$$v_o = 2v_1 + v_2 - 4v_3$$

**Ans.** A possible choice:  $R_1 = 5 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $R_a = 10 \text{ k}\Omega$ ,  $R_b = 10 \text{ k}\Omega$ ,  $R_3 = 2.5 \text{ k}\Omega$ ,  $R_c = 10 \text{ k}\Omega$

## 2.3 The Noninverting Configuration

The second closed-loop configuration we shall study is shown in Fig. 2.12. Here the input signal  $v_I$  is applied directly to the positive input terminal of the op amp while one terminal of  $R_1$  is connected to ground.

### 2.3.1 The Closed-Loop Gain

Analysis of the noninverting circuit to determine its closed-loop gain ( $v_o/v_I$ ) is illustrated in Fig. 2.13. Again the order of the steps in the analysis is indicated by circled numbers. Assuming that the op amp is ideal with infinite gain, a virtual short circuit exists between its two input terminals. Hence the difference input signal is

$$v_{Id} = \frac{v_o}{A} = 0 \quad \text{for } A = \infty$$

Thus the voltage at the inverting input terminal will be equal to that at the noninverting input terminal, which is the applied voltage  $v_I$ . The current through  $R_1$  can then be determined as  $v_I/R_1$ . Because of the infinite input impedance of the op amp, this current will flow through  $R_2$ , as shown in Fig. 2.13. Now the output voltage can be determined from

$$v_o = v_I + \left( \frac{v_I}{R_1} \right) R_2$$

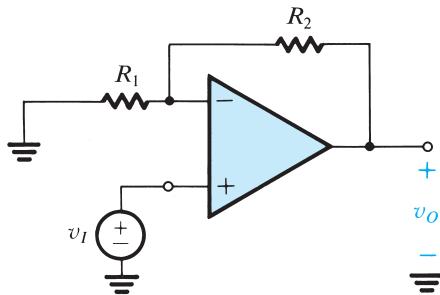


Figure 2.12 The noninverting configuration.

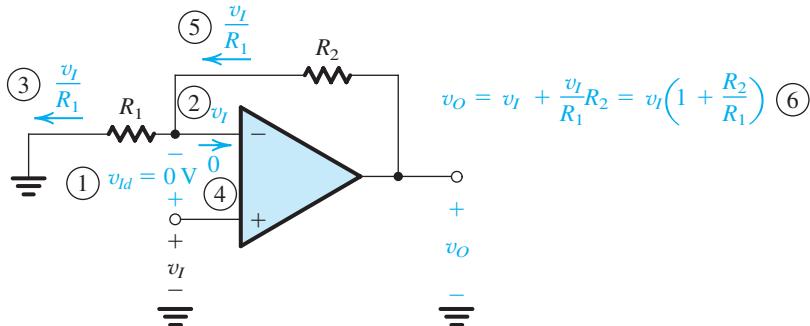


Figure 2.13 Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers.

which yields

$$\frac{v_O}{v_I} = 1 + \frac{R_2}{R_1} \quad (2.9)$$

Further insight into the operation of the noninverting configuration can be obtained by considering the following: Since the current into the op-amp inverting input is zero, the circuit composed of  $R_1$  and  $R_2$  acts in effect as a voltage divider feeding a fraction of the output voltage back to the inverting input terminal of the op amp; that is,

$$v_I = v_O \left( \frac{R_1}{R_1 + R_2} \right) \quad (2.10)$$

Then the infinite op-amp gain and the resulting virtual short circuit between the two input terminals of the op amp forces this voltage to be equal to that applied at the positive input terminal; thus,

$$v_O \left( \frac{R_1}{R_1 + R_2} \right) = v_I$$

which yields the gain expression given in Eq. (2.9).

This is an appropriate point to reflect further on the action of the negative feedback present in the noninverting circuit of Fig. 2.12. Let  $v_I$  increase. Such a change in  $v_I$  will cause  $v_{ld}$  to increase, and  $v_O$  will correspondingly increase as a result of the high (ideally infinite) gain of the op amp. However, a fraction of the increase in  $v_O$  will be fed back to the inverting input terminal of the op amp through the  $(R_1, R_2)$  voltage divider. The result of this feedback will be to counteract the increase in  $v_{ld}$ , driving  $v_{ld}$  back to zero, albeit at a higher value of  $v_O$  that corresponds to the increased value of  $v_I$ . This *degenerative* action of negative feedback gives it the alternative name **degenerative feedback**. Finally, note that the argument above applies equally well if  $v_I$  decreases. A formal and detailed study of feedback is presented in Chapter 11.

### 2.3.2 Effect of Finite Open-Loop Gain

As we have done for the inverting configuration, we now consider the effect of the finite op-amp open-loop gain  $A$  on the gain of the noninverting configuration. Assuming the op amp to be ideal except for having a finite open-loop gain  $A$ , it can be shown that the closed-loop gain of the noninverting amplifier circuit of Fig. 2.12 is given by

$$G \equiv \frac{v_o}{v_i} = \frac{1 + (R_2/R_1)}{1 + \frac{1 + (R_2/R_1)}{A}} \quad (2.11)$$

Observe that the denominator is identical to that for the case of the inverting configuration (Eq. 2.5). This is no coincidence; it is a result of the fact that both the inverting and the noninverting configurations have the same feedback loop, which can be readily seen if the input signal source is eliminated (i.e., short-circuited). The numerators, however, are different, for the numerator gives the ideal or nominal closed-loop gain ( $-R_2/R_1$  for the inverting configuration, and  $1 + R_2/R_1$  for the noninverting configuration). Finally, we note (with reassurance) that the gain expression in Eq. (2.11) reduces to the ideal value for  $A = \infty$ . In fact, it approximates the ideal value for

$$A \gg 1 + \frac{R_2}{R_1}$$

This is the same condition as in the inverting configuration, except that here the quantity on the right-hand side is the nominal closed-loop gain. The expressions for the actual and ideal values of the closed-loop gain  $G$  in Eqs. (2.11) and (2.9), respectively, can be used to determine the percentage error in  $G$  resulting from the finite op-amp gain  $A$  as

$$\text{Percent gain error} = -\frac{1 + (R_2/R_1)}{A + 1 + (R_2/R_1)} \times 100 \quad (2.12)$$

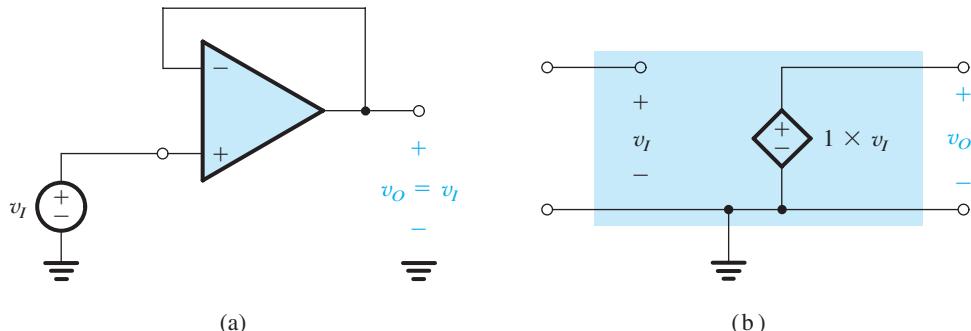
Thus, as an example, if an op amp with an open-loop gain of 1000 is used to design a noninverting amplifier with a nominal closed-loop gain of 10, we would expect the closed-loop gain to be about 1% below the nominal value.

### 2.3.3 Input and Output Resistance

The gain of the noninverting configuration is positive—hence the name *noninverting*. The input impedance of this closed-loop amplifier is ideally infinite, since no current flows into the positive input terminal of the op amp. The output of the noninverting amplifier is taken at the terminals of the ideal voltage source  $A(v_2 - v_1)$  (see the op-amp equivalent circuit in Fig. 2.3), and thus the output resistance of the noninverting configuration is zero.

### 2.3.4 The Voltage Follower

The property of high input impedance is a very desirable feature of the noninverting configuration. It enables using this circuit as a buffer amplifier to connect a source with a high impedance to a low-impedance load. We discussed the need for buffer amplifiers in Section 1.5. In many applications the buffer amplifier is not required to provide any voltage gain; rather, it is used mainly as an impedance transformer or a power amplifier. In such cases we may make  $R_2 = 0$  and  $R_1 = \infty$  to obtain the **unity-gain amplifier** shown in Fig. 2.14(a). This circuit is commonly referred to as a **voltage follower**, since the output “follows” the input. In the ideal case,  $v_o = v_i, R_{in} = \infty, R_{out} = 0$ , and the follower has the equivalent circuit shown in Fig. 2.14(b).



**Figure 2.14** (a) The unity-gain buffer or follower amplifier. (b) Its equivalent circuit model.

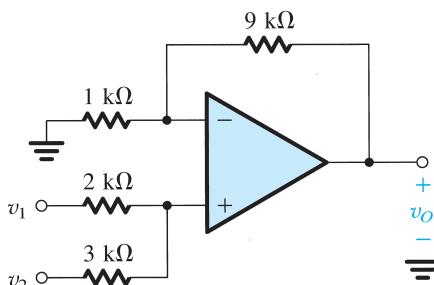
Since in the voltage-follower circuit the entire output is fed back to the inverting input, the circuit is said to have 100% negative feedback. The infinite gain of the op amp then acts to make  $v_{ld} = 0$  and hence  $v_o = v_i$ . Observe that the circuit is elegant in its simplicity!

Since the noninverting configuration has a gain greater than or equal to unity, depending on the choice of  $R_2/R_1$ , some prefer to call it "a follower with gain."

## EXERCISES

- 2.9** Use the superposition principle to find the output voltage of the circuit shown in Fig. E2.9.

**Ans.**  $v_0 = 6v_1 + 4v_2$



## Figure E2.9

- 2.10** If in the circuit of Fig. E2.9 the 1-k $\Omega$  resistor is disconnected from ground and connected to a third signal source  $v_3$ , use superposition to determine  $v_o$  in terms of  $v_1$ ,  $v_2$ , and  $v_3$ .

**Ans.**  $v_0 = 6v_1 + 4v_2 - 9v_3$

- D2.11** Design a noninverting amplifier with a gain of 2. At the maximum output voltage of 10 V the current in the voltage divider is to be 10  $\mu$ A.

**Ans.**  $R_1 = R_2 = 0.5 \text{ M}\Omega$

- 2.12** (a) Show that if the op amp in the circuit of Fig. 2.12 has a finite open-loop gain  $A$ , then the closed-loop gain is given by Eq. (2.11). (b) For  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 9 \text{ k}\Omega$  find the percentage deviation  $\epsilon$  of the closed-loop gain from the ideal value of  $(1 + R_2/R_1)$  for the cases  $A = 10^3, 10^4$ , and  $10^5$ . For  $v_i = 1 \text{ V}$ , find in each case the voltage between the two input terminals of the op amp.

**Ans.**  $\epsilon = -1\%, -0.1\%, -0.01\%$ ;  $v_2 - v_1 = 9.9 \text{ mV}, 1 \text{ mV}, 0.1 \text{ mV}$

- 2.13** For the circuit in Fig. E2.13 find the values of  $i_L$ ,  $v_1$ ,  $i_1$ ,  $i_2$ ,  $v_o$ ,  $i_L$ , and  $i_o$ . Also find the voltage gain  $v_o/v_I$ , the current gain  $i_L/i_I$ , and the power gain  $P_L/P_I$ .

**Ans.** 0; 1 V; 1 mA; 10 V; 10 mA; 11 mA; 10 V/V (20 dB);  $\infty$ ;  $\infty$

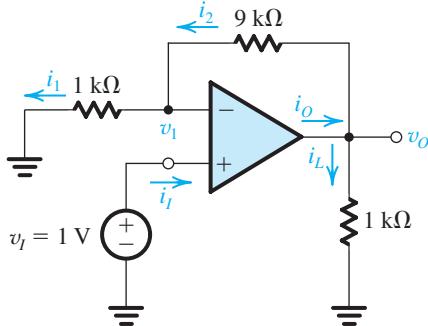


Figure E2.13

- 2.14** It is required to connect a transducer having an open-circuit voltage of 1 V and a source resistance of  $1 \text{ M}\Omega$  to a load of  $1\text{-k}\Omega$  resistance. Find the load voltage if the connection is done (a) directly, and (b) through a unity-gain voltage follower.

**Ans.** (a) 1 mV; (b) 1 V

## 2.4 Difference Amplifiers

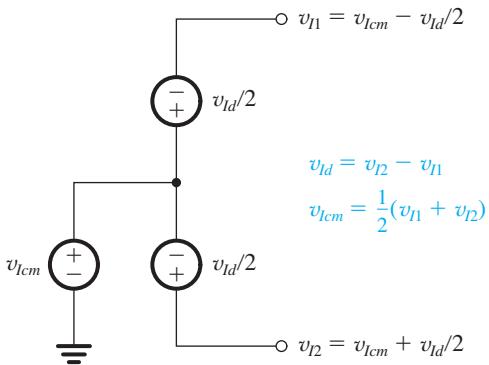
Having studied the two basic configurations of op-amp circuits together with some of their direct applications, we are now ready to consider a somewhat more involved but very important application. Specifically, we shall study the use of op amps to design difference or differential amplifiers.<sup>2</sup> A difference amplifier is one that responds to the difference between the two signals applied at its input and ideally rejects signals that are common to the two inputs. The representation of signals in terms of their differential and common-mode components was given in Fig. 2.4. It is repeated here in Fig. 2.15 with slightly different symbols to serve as the input signals for the difference amplifiers we are about to design. Although ideally the difference amplifier will amplify only the differential input signal  $v_{Id}$  and reject completely the common-mode input signal  $v_{Icm}$ , practical circuits will have an output voltage  $v_O$  given by

$$v_O = A_d v_{Id} + A_{cm} v_{Icm} \quad (2.13)$$

where  $A_d$  denotes the amplifier differential gain and  $A_{cm}$  denotes its common-mode gain (ideally zero). The efficacy of a differential amplifier is measured by the degree of its rejection of common-mode signals in preference to differential signals. This is usually quantified by a measure known as the **common-mode rejection ratio (CMRR)**, defined as

$$\text{CMRR} = 20 \log \frac{|A_d|}{|A_{cm}|} \quad (2.14)$$

<sup>2</sup>The terms *difference* and *differential* are usually used to describe somewhat different amplifier types. For our purposes at this point, the distinction is not sufficiently significant. We will be more precise near the end of this section.



**Figure 2.15** Representing the input signals to a differential amplifier in terms of their differential and common-mode components.

The need for difference amplifiers arises frequently in the design of electronic systems, especially those employed in instrumentation. As a common example, consider a transducer providing a small (e.g., 1 mV) signal between its two output terminals while each of the two wires leading from the transducer terminals to the measuring instrument may have a large interference signal (e.g., 1 V) relative to the circuit ground. The instrument front end obviously needs a difference amplifier.

Before we proceed any further we should address a question that the reader might have: The op amp is itself a difference amplifier; why not just use an op amp? The answer is that the very high (ideally infinite) gain of the op amp makes it impossible to use by itself. Rather, as we did before, we have to devise an appropriate feedback network to connect to the op amp to create a circuit whose closed-loop gain is finite, predictable, and stable.

### 2.4.1 A Single-Op-Amp Difference Amplifier

Our first attempt at designing a difference amplifier is motivated by the observation that the gain of the noninverting amplifier configuration is positive,  $(1 + R_2/R_1)$ , while that of the inverting configuration is negative,  $(-R_2/R_1)$ . Combining the two configurations together is then a step in the right direction—namely, getting the difference between two input signals. Of course, we have to make the two gain magnitudes equal in order to reject common-mode signals. This, however, can be easily achieved by attenuating the positive input signal to reduce the gain of the positive path from  $(1 + R_2/R_1)$  to  $(R_2/R_1)$ . The resulting circuit would then look like that shown in Fig. 2.16, where the attenuation in the positive input path is achieved by the voltage divider  $(R_3, R_4)$ . The proper ratio of this voltage divider can be determined from

$$\frac{R_4}{R_4 + R_3} \left( 1 + \frac{R_2}{R_1} \right) = \frac{R_2}{R_1}$$

which can be put in the form

$$\frac{R_4}{R_4 + R_3} = \frac{R_2}{R_2 + R_1}$$

This condition is satisfied by selecting

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} \quad (2.15)$$

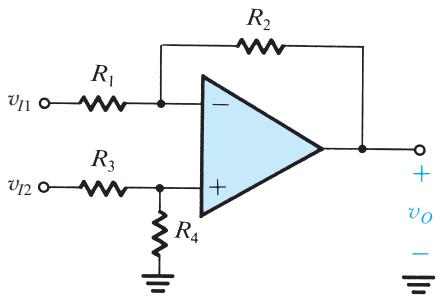


Figure 2.16 A difference amplifier.

This completes our work. However, we have perhaps proceeded a little too fast! Let's step back and verify that the circuit in Fig. 2.16 with  $R_3$  and  $R_4$  selected according to Eq. (2.15) does in fact function as a difference amplifier. Specifically, we wish to determine the output voltage  $v_O$  in terms of  $v_{I1}$  and  $v_{I2}$ . Toward that end, we observe that the circuit is linear, and thus we can use superposition.

To apply superposition, we first reduce  $v_{I2}$  to zero—that is, ground the terminal to which  $v_{I2}$  is applied—and then find the corresponding output voltage, which will be due entirely to  $v_{I1}$ . We denote this output voltage  $v_{O1}$ . Its value may be found from the circuit in Fig. 2.17(a), which we recognize as that of the inverting configuration. The existence of  $R_3$  and  $R_4$  does not affect the gain expression, since no current flows through either of them. Thus,

$$v_{O1} = -\frac{R_2}{R_1}v_{I1}$$

Next, we reduce  $v_{I1}$  to zero and evaluate the corresponding output voltage  $v_{O2}$ . The circuit will now take the form shown in Fig. 2.17(b), which we recognize as the noninverting configuration with an additional voltage divider, made up of  $R_3$  and  $R_4$ , connected to the input  $v_{I2}$ . The output voltage  $v_{O2}$  is therefore given by

$$v_{O2} = v_{I2} \frac{R_4}{R_3 + R_4} \left(1 + \frac{R_2}{R_1}\right) = \frac{R_2}{R_1} v_{I2}$$

where we have utilized Eq. (2.15).

The superposition principle tells us that the output voltage  $v_O$  is equal to the sum of  $v_{O1}$  and  $v_{O2}$ . Thus we have

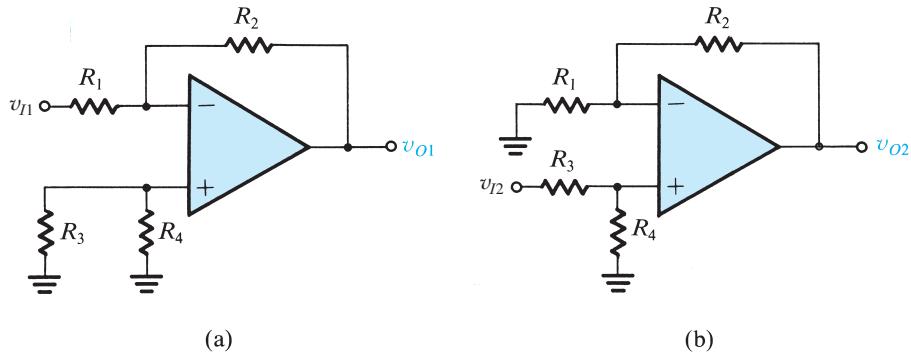
$$v_O = \frac{R_2}{R_1}(v_{I2} - v_{I1}) = \frac{R_2}{R_1}v_{Id} \quad (2.16)$$

Thus, as expected, the circuit acts as a difference amplifier with a differential gain  $A_d$  of

$$A_d = \frac{R_2}{R_1} \quad (2.17)$$

Of course this is predicated on the op amp being ideal and furthermore on the selection of  $R_3$  and  $R_4$  so that their ratio matches that of  $R_1$  and  $R_2$  (Eq. 2.15). To make this matching requirement a little easier to satisfy, we usually select

$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$



**Figure 2.17** Application of superposition to the analysis of the circuit of Fig. 2.16.

Let's next consider the circuit with only a common-mode signal applied at the input, as shown in Fig. 2.18. The figure also shows some of the analysis steps. Thus,

$$\begin{aligned} i_1 &= \frac{1}{R_1} \left[ v_{Icm} - \frac{R_4}{R_4 + R_3} v_{Icm} \right] \\ &= v_{Icm} \frac{R_3}{R_4 + R_3} \frac{1}{R_1} \end{aligned} \quad (2.18)$$

The output voltage can now be found from

$$v_o = \frac{R_4}{R_4 + R_3} v_{Icm} - i_2 R_2$$

Substituting \$i\_2 = i\_1\$ and for \$i\_1\$ from Eq. (2.18),

$$\begin{aligned} v_o &= \frac{R_4}{R_4 + R_3} v_{Icm} - \frac{R_2}{R_1} \frac{R_3}{R_4 + R_3} v_{Icm} \\ &= \frac{R_4}{R_4 + R_3} \left( 1 - \frac{R_2 R_3}{R_1 R_4} \right) v_{Icm} \end{aligned}$$

Thus,

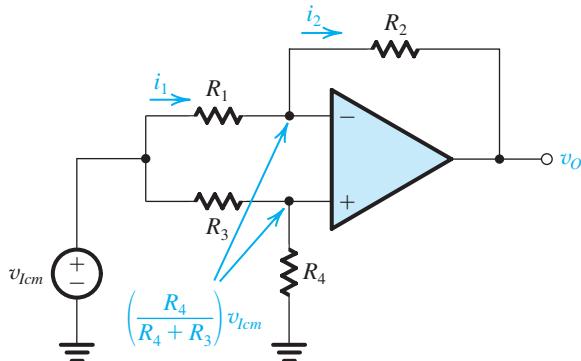
$$A_{cm} \equiv \frac{v_o}{v_{Icm}} = \left( \frac{R_4}{R_4 + R_3} \right) \left( 1 - \frac{R_2 R_3}{R_1 R_4} \right) \quad (2.19)$$

For the design with the resistor ratios selected according to Eq. (2.15), we obtain

$$A_{cm} = 0$$

as expected. Note, however, that any mismatch in the resistance ratios can make \$A\_{cm}\$ nonzero, and hence CMRR finite.

In addition to rejecting common-mode signals, a difference amplifier is usually required to have a high input resistance. To find the input resistance between the two input terminals



**Figure 2.18** Analysis of the difference amplifier to determine its common-mode gain  $A_{cm} \equiv v_o/v_{icm}$ .

(i.e., the resistance seen by  $v_{id}$ ), called the **differential input resistance**  $R_{id}$ , consider Fig. 2.19. Here we have assumed that the resistors are selected so that

$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$

Now

$$R_{id} \equiv \frac{v_{id}}{i_I}$$

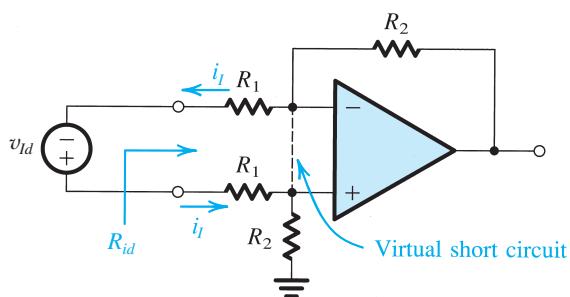
Since the two input terminals of the op amp track each other in potential, we may write a loop equation and obtain

$$v_{id} = R_1 i_I + 0 + R_1 i_I$$

Thus,

$$R_{id} = 2R_1 \quad (2.20)$$

Note that if the amplifier is required to have a large differential gain ( $R_2/R_1$ ), then  $R_1$  of necessity will be relatively small and the input resistance will be correspondingly low, a drawback of this circuit. Another drawback of the circuit is that it is not easy to vary the differential gain of the amplifier. Both of these drawbacks are overcome in the instrumentation amplifier discussed next.



**Figure 2.19** Finding the input resistance of the difference amplifier for the case  $R_3 = R_1$  and  $R_4 = R_2$ .

## EXERCISES

**2.15** Consider the difference-amplifier circuit of Fig. 2.16 for the case  $R_1 = R_3 = 2 \text{ k}\Omega$  and  $R_2 = R_4 = 200 \text{ k}\Omega$ .

(a) Find the value of the differential gain  $A_d$ . (b) Find the value of the differential input resistance  $R_{id}$  and the output resistance  $R_o$ . (c) If the resistors have 1% tolerance (i.e., each can be within  $\pm 1\%$  of its nominal value), use Eq. (2.19) to find the worst-case common-mode gain  $A_{cm}$  and hence the corresponding value of CMRR.

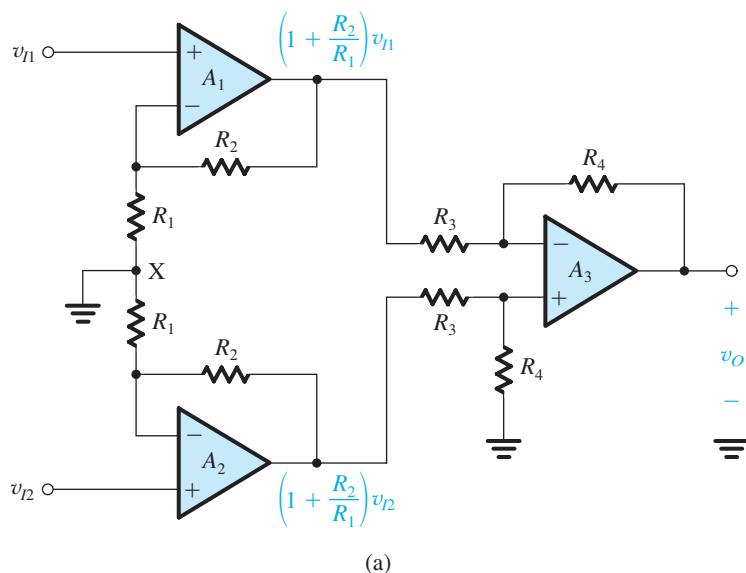
**Ans.** (a) 100 V/V (40 dB); (b) 4 k $\Omega$ , 0  $\Omega$ ; (c) 0.04 V/V, 68 dB

**D2.16** Find values for the resistances in the circuit of Fig. 2.16 so that the circuit behaves as a difference amplifier with an input resistance of 20 k $\Omega$  and a gain of 10.

**Ans.**  $R_1 = R_3 = 10 \text{ k}\Omega$ ;  $R_2 = R_4 = 100 \text{ k}\Omega$

### 2.4.2 A Superior Circuit—The Instrumentation Amplifier

The low-input-resistance problem of the difference amplifier of Fig. 2.16 can be solved by using voltage followers to buffer the two input terminals; that is, a voltage follower of the type in Fig. 2.14 is connected between each input terminal and the corresponding input terminal of the difference amplifier. However, if we are going to use two additional op amps, we should ask the question: Can we get more from them than just impedance buffering? An obvious answer would be that we should try to get some voltage gain. It is especially interesting that



**Figure 2.20** A popular circuit for an instrumentation amplifier. (a) Initial approach to the circuit. (b) The circuit in (a) with the connection between node X and ground removed and the two resistors  $R_1$  and  $R_1'$  lumped together. This simple wiring change dramatically improves performance. (c) Analysis of the circuit in (b) assuming ideal op amps.

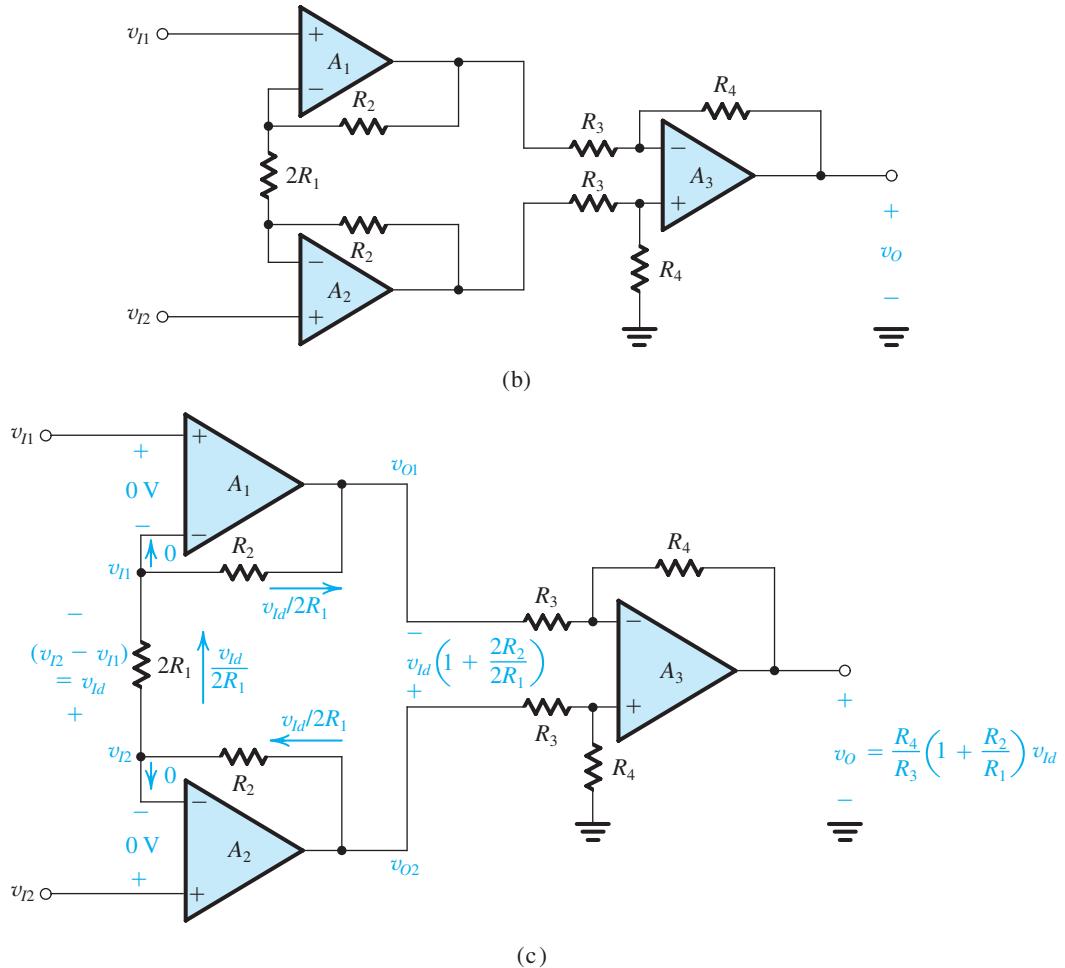


Figure 2.20 continued

we can achieve this without compromising the high input resistance simply by using followers with gain rather than unity-gain followers. Achieving some or indeed the bulk of the required gain in this new first stage of the differential amplifier eases the burden on the difference amplifier in the second stage, leaving it to its main task of implementing the differencing function and thus rejecting common-mode signals.

The resulting circuit is shown in Fig. 2.20(a). It consists of two stages in cascade. The first stage is formed by op amps  $A_1$  and  $A_2$  and their associated resistors, and the second stage is the by-now-familiar difference amplifier formed by op amp  $A_3$  and its four associated resistors. Observe that as we set out to do, each of  $A_1$  and  $A_2$  is connected in the noninverting configuration and thus realizes a gain of  $(1 + R_2/R_1)$ . It follows that each of  $v_{I1}$  and  $v_{I2}$  is amplified by this factor, and the resulting amplified signals appear at the outputs of  $A_1$  and  $A_2$ , respectively.

The difference amplifier in the second stage operates on the difference signal  $(1 + R_2/R_1)(v_{I2} - v_{I1}) = (1 + R_2/R_1)v_{Id}$  and provides at its output

$$v_O = \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1}\right) v_{Id}$$

Thus the differential gain realized is

$$A_d = \left( \frac{R_4}{R_3} \right) \left( 1 + \frac{R_2}{R_1} \right) \quad (2.21)$$

The common-mode gain will be zero because of the differencing action of the second-stage amplifier.

The circuit in Fig. 2.20(a) has the advantage of very high (ideally infinite) input resistance and high differential gain. Also, provided  $A_1$  and  $A_2$  and their corresponding resistors are matched, the two signal paths are symmetric—a definite advantage in the design of a differential amplifier. The circuit, however, has three major disadvantages:

1. The input common-mode signal  $v_{lcm}$  is amplified in the first stage by a gain equal to that experienced by the differential signal  $v_{ld}$ . This is a very serious issue, for it could result in the signals at the outputs of  $A_1$  and  $A_3$  being of such large magnitudes that the op amps saturate (more on op-amp saturation in Section 2.8). But even if the op amps do not saturate, the difference amplifier of the second stage will now have to deal with much larger common-mode signals, with the result that the CMRR of the overall amplifier will inevitably be reduced.
2. The two amplifier channels in the first stage have to be perfectly matched, otherwise a spurious signal may appear between their two outputs. Such a signal would get amplified by the difference amplifier in the second stage.
3. To vary the differential gain  $A_d$ , two resistors have to be varied simultaneously, say the two resistors labeled  $R_1$ . At each gain setting the two resistors have to be perfectly matched: a difficult task.

All three problems can be solved with a very simple wiring change: Simply disconnect the node between the two resistors labeled  $R_1$ , node X, from ground. The circuit with this small but functionally profound change is redrawn in Fig. 2.20(b), where we have lumped the two resistors ( $R_1$  and  $R_1$ ) together into a single resistor ( $2R_1$ ).

Analysis of the circuit in Fig. 2.20(b), assuming ideal op amps, is straightforward, as is illustrated in Fig. 2.20(c). The key point is that the virtual short circuits at the inputs of op amps  $A_1$  and  $A_2$  cause the input voltages  $v_{l1}$  and  $v_{l2}$  to appear at the two terminals of resistor ( $2R_1$ ). Thus the differential input voltage  $v_{l2} - v_{l1} \equiv v_{ld}$  appears across  $2R_1$  and causes a current  $i = v_{ld}/2R_1$  to flow through  $2R_1$  and the two resistors labeled  $R_2$ . This current in turn produces a voltage difference between the output terminals of  $A_1$  and  $A_2$  given by

$$v_{o2} - v_{o1} = \left( 1 + \frac{2R_2}{2R_1} \right) v_{ld}$$

The difference amplifier formed by op amp  $A_3$  and its associated resistors senses the voltage difference ( $v_{o2} - v_{o1}$ ) and provides a proportional output voltage  $v_o$ :

$$\begin{aligned} v_o &= \frac{R_4}{R_3} (v_{o2} - v_{o1}) \\ &= \frac{R_4}{R_3} \left( 1 + \frac{R_2}{R_1} \right) v_{ld} \end{aligned}$$

Thus the overall differential voltage-gain is given by

$$A_d \equiv \frac{v_o}{v_{ld}} = \frac{R_4}{R_3} \left( 1 + \frac{R_2}{R_1} \right) \quad (2.22)$$

Observe that proper differential operation does *not* depend on the matching of the two resistors labeled  $R_2$ . Indeed, if one of the two is of different value, say  $R'_2$ , the expression for  $A_d$  becomes

$$A_d = \frac{R_4}{R_3} \left( 1 + \frac{R_2 + R'_2}{2R_1} \right) \quad (2.23)$$

Consider next what happens when the two input terminals are connected together to a common-mode input voltage  $v_{lcm}$ . It is easy to see that an equal voltage appears at the negative input terminals of  $A_1$  and  $A_2$ , causing the current through  $2R_1$  to be zero. Thus there will be no current flowing in the  $R_2$  resistors, and the voltages at the output terminals of  $A_1$  and  $A_2$  will be equal to the input (i.e.,  $v_{lcm}$ ). Thus the first stage no longer amplifies  $v_{lcm}$ ; it simply propagates  $v_{lcm}$  to its two output terminals, where they are subtracted to produce a zero common-mode output by  $A_3$ . The difference amplifier in the second stage, however, now has a much improved situation at its input: The difference signal has been amplified by  $(1 + R_2/R_1)$  while the common-mode voltage remained unchanged.

Finally, we observe from the expression in Eq. (2.22) that the gain can be varied by changing only one resistor,  $2R_1$ . We conclude that this is an excellent differential amplifier circuit and is widely employed as an instrumentation amplifier, that is, as the input amplifier used in a variety of electronic instruments.

### INTEGRATED INSTRUMENTATION AMPLIFIERS:

The conventional combination of three op amps and a number of precision resistors to form an instrumentation amplifier is an extremely powerful tool for the design of instruments for many applications. While the earliest applications used separate op amps and discrete resistors, fully integrated versions incorporating most required components in a single integrated-circuit package are increasingly available from many manufacturers. Low-power versions of these units are extremely important in the design of portable, wearable, and implantable medical monitoring devices, such as wristband activity monitors.

### Example 2.3

Design the instrumentation amplifier circuit in Fig. 2.20(b) to provide a gain that can be varied over the range of 2 to 1000 utilizing a 100-k $\Omega$  variable resistance (a potentiometer, or “pot” for short).

#### Solution

It is usually preferable to obtain all the required gain in the first stage, leaving the second stage to perform the task of taking the difference between the outputs of the first stage and thereby rejecting the common-mode signal. In other words, the second stage is usually designed for a gain of 1. Adopting this approach, we select

**Example 2.3** *continued*

all the second-stage resistors to be equal to a practically convenient value, say  $10\text{ k}\Omega$ . The problem then reduces to designing the first stage to realize a gain adjustable over the range of 2 to 1000. Implementing  $2R_1$  as the series combination of a fixed resistor  $R_{lf}$  and the variable resistor  $R_{lv}$ , obtained using the  $100\text{-k}\Omega$  pot (Fig. 2.21), we can write

$$1 + \frac{2R_2}{R_{lf} + R_{lv}} = 2 \text{ to } 1000$$

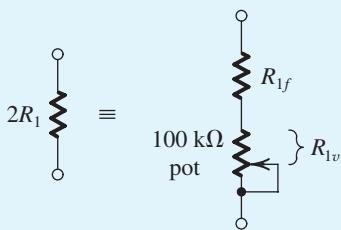
Thus,

$$1 + \frac{2R_2}{R_{lf}} = 1000$$

and

$$1 + \frac{2R_2}{R_{lf} + 100\text{ k}\Omega} = 2$$

These two equations yield  $R_{lf} = 100.2\ \Omega$  and  $R_2 = 50.050\text{ k}\Omega$ . Other practical values may be selected; for instance,  $R_{lf} = 100\ \Omega$  and  $R_2 = 49.9\text{ k}\Omega$  (both values are available as standard 1%-tolerance metal-film resistors; see Appendix J) results in a gain covering approximately the required range.



**Figure 2.21** To make the gain of the circuit in Fig. 2.20(b) variable,  $2R_1$  is implemented as the series combination of a fixed resistor  $R_{lf}$  and a variable resistor  $R_{lv}$ . Resistor  $R_{lf}$  ensures that the maximum available gain is limited.

### EXERCISE

- 2.17** Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of  $+5\text{ V}$  (dc) and a differential input signal of  $10\text{-mV-peak}$  sine wave. Let  $(2R_1) = 1\text{ k}\Omega$ ,  $R_2 = 0.5\text{ M}\Omega$ , and  $R_3 = R_4 = 10\text{ k}\Omega$ . Find the voltage at every node in the circuit.

**Ans.**  $v_{I1} = 5 - 0.005 \sin \omega t$ ;  $v_{I2} = 5 + 0.005 \sin \omega t$ ;  $v_{-}(\text{op amp } A_1) = 5 - 0.005 \sin \omega t$ ;  $v_{-}(\text{op amp } A_2) = 5 + 0.005 \sin \omega t$ ;  $v_{O1} = 5 - 5.005 \sin \omega t$ ;  $v_{O2} = 5 + 5.005 \sin \omega t$ ;  $v_{-}(A_3) = v_{+}(A_3) = 2.5 + 2.5025 \sin \omega t$ ;  $v_o = 10.01 \sin \omega t$  (all in volts)

## 2.5 Integrators and Differentiators

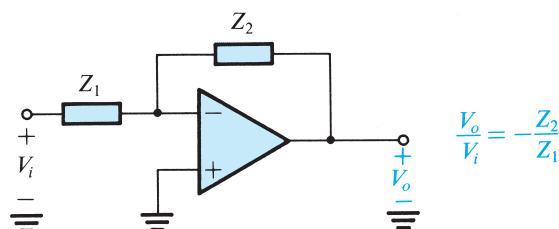
The op-amp circuit applications we have studied thus far utilized resistors in the op-amp feedback path and in connecting the signal source to the circuit, that is, in the feed-in path. As a result, circuit operation has been (ideally) independent of frequency. By allowing the use of capacitors together with resistors in the feedback and feed-in paths of op-amp circuits, we open the door to a very wide range of useful and exciting applications of the op amp. We begin our study of op-amp- $RC$  circuits by considering two basic applications, namely, signal integrators and differentiators.<sup>3</sup>

### 2.5.1 The Inverting Configuration with General Impedances

To begin with, consider the inverting closed-loop configuration with impedances  $Z_1(s)$  and  $Z_2(s)$  replacing resistors  $R_1$  and  $R_2$ , respectively. The resulting circuit is shown in Fig. 2.22 and, for an ideal op amp, has the closed-loop gain or, more appropriately, the closed-loop transfer function

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)} \quad (2.24)$$

As explained in Section 1.6, replacing  $s$  by  $j\omega$  provides the transfer function for physical frequencies  $\omega$ , that is, the transmission magnitude and phase for a sinusoidal input signal of frequency  $\omega$ .



**Figure 2.22** The inverting configuration with general impedances in the feedback and the feed-in paths.

<sup>3</sup>At this point, a review of Section 1.6 would be helpful. Also, an important fact to remember: Passing a constant current  $I$  through a capacitor  $C$  for a time  $t$  causes a change of  $It$  to accumulate on the capacitor. Thus the capacitor voltage changes by  $\Delta V = \Delta Q/C = It/C$ ; that is, the capacitor voltage increases linearly with time.

## EARLY OP AMPS AND ANALOG COMPUTATION:

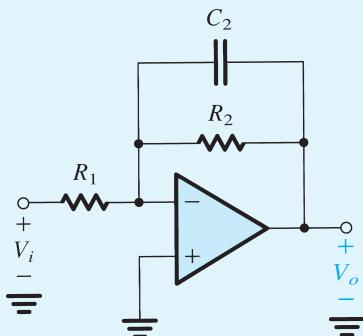
In 1941, Karl D. Swartzel Jr. of Bell Labs patented “the summing amplifier,” a high-gain dc inverting amplifier, intended to be used with negative feedback. This precursor of the op amp used three vacuum tubes (the predecessor of the transistor) and  $\pm 350\text{-V}$  power supplies to achieve a gain of 90 dB. Though lacking a differential input, it provided the usual applications of summation, integration, and general filtering using convenient passive resistive and capacitive components.

Soon after (1942), Loebe Julie, working with Professor John R. Regazzini at Columbia University, created a differential version, still using vacuum tubes. During World War II, these units were used extensively to provide analog computational functions in association with radar-directed antiaircraft firing control involving aircraft speed projection.

In the early 1950s, driven by the demonstrated wartime success of op-amp-based computation, general-purpose commercial systems called “analog computers” began to appear. They consisted of a few dozen op amps and associated passive components, including potentiometers; the interconnections required for programming were achieved with plug boards. These computers were used to solve differential equations.

### Example 2.4

For the circuit in Fig. 2.23, derive an expression for the transfer function  $V_o(s)/V_i(s)$ . Show that the transfer function is that of a low-pass STC circuit. By expressing the transfer function in the standard form shown in Table 1.2 on page 36, find the dc gain and the 3-dB frequency. Design the circuit to obtain a dc gain of 40 dB, a 3-dB frequency of 1 kHz, and an input resistance of  $1\text{ k}\Omega$ . At what frequency does the magnitude of transmission become unity? What is the phase angle at this frequency?



**Figure 2.23** Circuit for Example 2.4.

### Solution

To obtain the transfer function of the circuit in Fig. 2.23, we substitute in Eq. (2.24),  $Z_1 = R_1$  and  $Z_2 = R_2 \parallel (1/sC_2)$ . Since  $Z_2$  is the parallel connection of two components, it is more convenient to work in terms of  $Y_2$ ; that is, we use the following alternative form of the transfer function:

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{Z_1(s)Y_2(s)}$$

and substitute  $Z_1 = R_1$  and  $Y_2(s) = (1/R_2) + sC_2$  to obtain

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{\frac{R_1}{R_2} + sC_2R_1}$$

This transfer function is of first order, has a finite dc gain (at  $s = 0, V_o/V_i = -R_2/R_1$ ), and has zero gain at infinite frequency. Thus it is the transfer function of a low-pass STC network and can be expressed in the standard form of Table 1.2 as follows:

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + sC_2R_2}$$

from which we find the dc gain  $K$  to be

$$K = -\frac{R_2}{R_1}$$

and the 3-dB frequency  $\omega_0$  as

$$\omega_0 = \frac{1}{C_2R_2}$$

We could have found all this from the circuit in Fig. 2.23 by inspection. Specifically, note that the capacitor behaves as an open circuit at dc; thus at dc the gain is simply  $(-R_2/R_1)$ . Furthermore, because there is a virtual ground at the inverting input terminal, the resistance seen by the capacitor is  $R_2$ , and thus the time constant of the STC network is  $C_2R_2$ .

Now to obtain a dc gain of 40 dB, that is, 100 V/V, we select  $R_2/R_1 = 100$ . For an input resistance of 1 k $\Omega$ , we select  $R_1 = 1$  k $\Omega$ , and thus  $R_2 = 100$  k $\Omega$ . Finally, for a 3-dB frequency  $f_0 = 1$  kHz, we select  $C_2$  from

$$2\pi \times 1 \times 10^3 = \frac{1}{C_2 \times 100 \times 10^3}$$

which yields  $C_2 = 1.59$  nF.

The circuit has gain and phase Bode plots of the standard form in Fig. 1.23. As the gain falls off at the rate of  $-20$  dB/decade, it will reach 0 dB in two decades, that is, at  $f = 100f_0 = 100$  kHz. As Fig. 1.23(b) indicates, at such a frequency, which is much greater than  $f_0$ , the phase is approximately  $-90^\circ$ . To this, however, we must add the  $180^\circ$  arising from the inverting nature of the amplifier (i.e., the negative sign in the transfer function expression). Thus at 100 kHz, the total phase shift will be  $-270^\circ$  or, equivalently,  $+90^\circ$ .

## 2.5.2 The Inverting Integrator

By placing a capacitor in the feedback path (i.e., in place of  $Z_2$  in Fig. 2.22) and a resistor at the input (in place of  $Z_1$ ), we obtain the circuit of Fig. 2.24(a). We shall now show that this circuit realizes the mathematical operation of integration. Let the input be a time-varying function  $v_i(t)$ . The virtual ground at the inverting op-amp input causes  $v_i(t)$  to appear in effect

across  $R$ , and thus the current  $i_1(t)$  will be  $v_i(t)/R$ . This current flows through the capacitor  $C$ , causing charge to accumulate on  $C$ . If we assume that the circuit begins operation at time  $t = 0$ , then at an arbitrary time  $t$  the current  $i_1(t)$  will have deposited on  $C$  a charge equal to  $\int_0^t i_1(t)dt$ . Thus the capacitor voltage  $v_C(t)$  will change by  $\frac{1}{C} \int_0^t i_1(t)dt$ . If the initial voltage on  $C$  (at  $t = 0$ ) is denoted  $V_C$ , then

$$v_C(t) = V_C + \frac{1}{C} \int_0^t i_1(t)dt$$

Now the output voltage  $v_o(t) = -v_C(t)$ ; thus,

$$\rightarrow v_o(t) = -\frac{1}{CR} \int_0^t v_i(t)dt - V_C \quad (2.25)$$

Thus the circuit provides an output voltage that is proportional to the time integral of the input, with  $V_C$  being the initial condition of integration and  $CR$  the **integrator time constant**. Note that, as expected, there is a negative sign attached to the output voltage, and thus this integrator circuit is said to be an **inverting integrator**. It is also known as a **Miller integrator** after an early worker in this field.

The operation of the integrator circuit can be described alternatively in the frequency domain by substituting  $Z_1(s) = R$  and  $Z_2(s) = 1/sC$  in Eq. (2.24) to obtain the transfer function

$$\rightarrow \frac{V_o(s)}{V_i(s)} = -\frac{1}{sCR} \quad (2.26)$$

For physical frequencies,  $s = j\omega$  and

$$\rightarrow \frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR} \quad (2.27)$$

Thus the integrator transfer function has magnitude

$$\rightarrow \left| \frac{V_o}{V_i} \right| = \frac{1}{\omega CR} \quad (2.28)$$

and phase

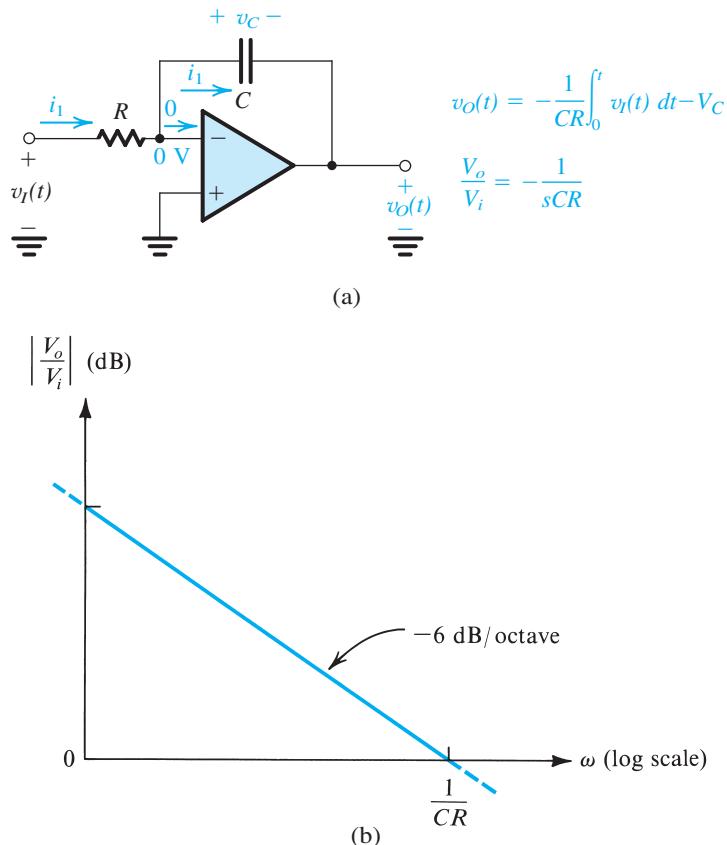
$$\rightarrow \phi = +90^\circ \quad (2.29)$$

The Bode plot for the integrator magnitude response can be obtained by noting from Eq. (2.28) that as  $\omega$  doubles (increases by an octave) the magnitude is halved (decreased by 6 dB). Thus the Bode plot is a straight line of slope  $-6$  dB/octave (or, equivalently,  $-20$  dB/decade). This line (shown in Fig. 2.24b) intercepts the 0-dB line at the frequency that makes  $|V_o/V_i| = 1$ , which from Eq. (2.28) is

$$\rightarrow \omega_{int} = \frac{1}{CR} \quad (2.30)$$

The frequency  $\omega_{int}$  is known as the **integrator frequency** and is simply the inverse of the integrator time constant.

Comparison of the frequency response of the integrator to that of an STC low-pass network indicates that the integrator behaves as a low-pass filter with a corner frequency of zero. Observe also that at  $\omega = 0$ , the magnitude of the integrator transfer function is infinite. This

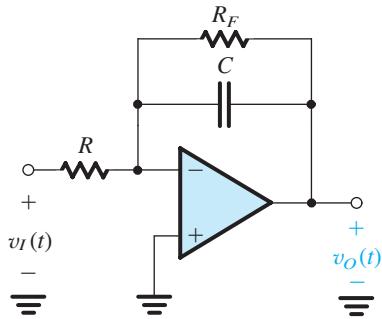


**Figure 2.24** (a) The Miller or inverting integrator. (b) Frequency response of the integrator.

indicates that at dc the op amp is operating with an open loop. This should also be obvious from the integrator circuit itself. Reference to Fig. 2.24(a) shows that the feedback element is a capacitor, and thus at dc, where the capacitor behaves as an open circuit, there is no negative feedback! This is a very significant observation and one that indicates a source of problems with the integrator circuit: Any tiny dc component in the input signal will theoretically produce an infinite output. Of course, no infinite output voltage results in practice; rather, the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply ( $L_+$  or  $L_-$ ), depending on the polarity of the input dc signal.

The dc problem of the integrator circuit can be alleviated by connecting a resistor  $R_F$  across the integrator capacitor  $C$ , as shown in Fig. 2.25, and thus the gain at dc will be  $-R_F/R$  rather than infinite. Such a resistor provides a dc feedback path. Unfortunately, however, the integration is no longer ideal, and the lower the value of  $R_F$ , the less ideal the integrator circuit becomes. This is because  $R_F$  causes the frequency of the integrator pole to move from its ideal location at  $\omega = 0$  to one determined by the corner frequency of the STC network ( $R_F, C$ ). Specifically, the integrator transfer function becomes

$$\frac{V_o(s)}{V_i(s)} = -\frac{R_F/R}{1 + sCR_F}$$



**Figure 2.25** The Miller integrator with a large resistance  $R_F$  connected in parallel with  $C$  in order to provide negative feedback and hence finite gain at dc.

as opposed to the ideal function of  $-1/sCR$ . The lower the value we select for  $R_F$ , the higher the corner frequency ( $1/CR_F$ ) will be and the more nonideal the integrator becomes. Thus selecting a value for  $R_F$  presents the designer with a trade-off between dc performance and signal performance. The effect of  $R_F$  on integrator performance is investigated further in Example 2.5.

### Example 2.5

Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width [Fig. 2.26(a)]. Let  $R = 10 \text{ k}\Omega$  and  $C = 10 \text{ nF}$ . If the integrator capacitor is shunted by a  $1\text{-M}\Omega$  resistor, how will the response be modified? The op amp is specified to saturate at  $\pm 13 \text{ V}$ .

#### Solution

In response to a 1-V, 1-ms input pulse, the integrator output will be

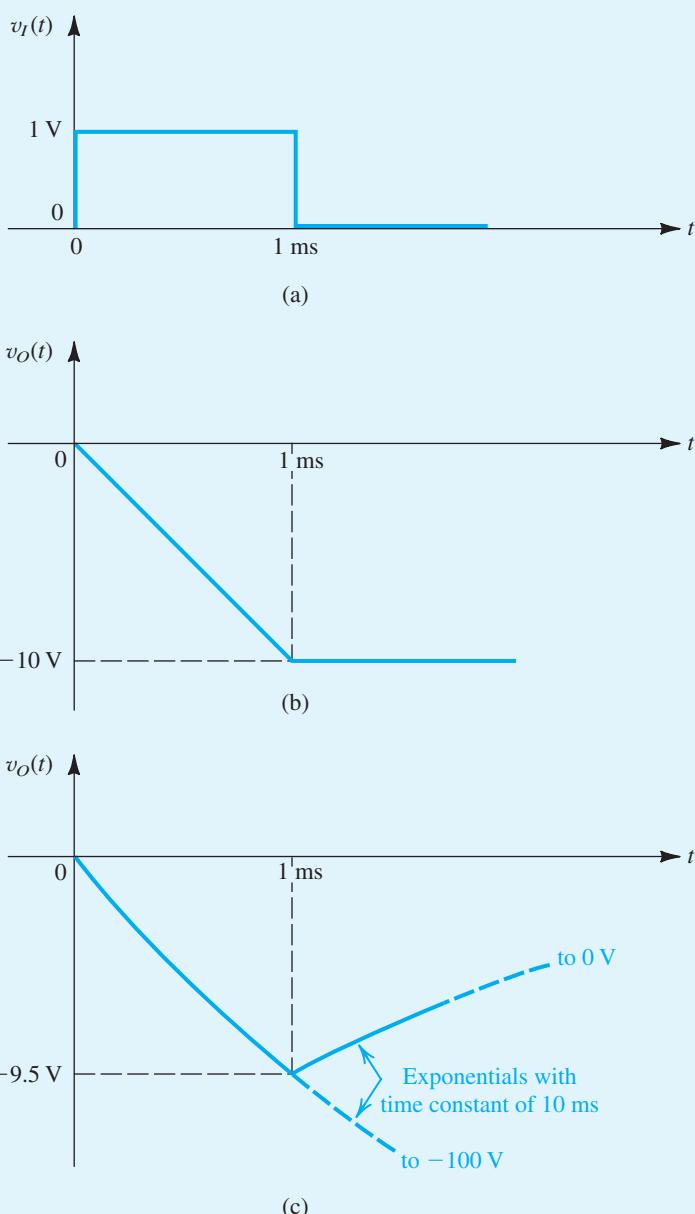
$$v_o(t) = -\frac{1}{CR} \int_0^t 1 dt, \quad 0 \leq t \leq 1 \text{ ms}$$

where we have assumed that the initial voltage on the integrator capacitor is 0. For  $C = 10 \text{ nF}$  and  $R = 10 \text{ k}\Omega$ ,  $CR = 0.1 \text{ ms}$ , and

$$v_o(t) = -10t, \quad 0 \leq t \leq 1 \text{ ms}$$

which is the linear ramp shown in Fig. 2.26(b). It reaches a magnitude of  $-10 \text{ V}$  at  $t = 1 \text{ ms}$  and remains constant thereafter.

That the output is a linear ramp should also be obvious from the fact that the 1-V input pulse produces a constant current through the capacitor of  $1 \text{ V}/10 \text{ k}\Omega = 0.1 \text{ mA}$ . This constant current  $I = 0.1 \text{ mA}$  supplies the capacitor with a charge  $It$ , and thus the capacitor voltage changes linearly as  $(It/C)$ , resulting in  $v_o = -(I/C)t$ . It is worth remembering that charging a capacitor with a constant current produces a linear voltage across it.



**Figure 2.26** Waveforms for Example 2.5: (a) Input pulse. (b) Output linear ramp of ideal integrator with time constant of 0.1 ms. (c) Output exponential ramp with resistor  $R_F$  connected across integrator capacitor.

Next consider the situation with resistor  $R_F = 1 \text{ M}\Omega$  connected across  $C$ . As before, the 1-V pulse will provide a constant current  $I = 0.1 \text{ mA}$ . Now, however, this current is supplied to an STC network composed of  $R_F$  in parallel with  $C$ . Thus, the output will be an exponential heading toward  $-100 \text{ V}$  with

**Example 2.5** *continued*

a time constant of  $CR_F = 10 \times 10^{-9} \times 1 \times 10^6 = 10 \text{ ms}$ ,

$$v_o(t) = -100(1 - e^{-t/10}), \quad 0 \leq t \leq 1 \text{ ms}$$

Of course, the exponential will be interrupted at the end of the pulse, that is, at  $t = 1 \text{ ms}$ , and the output will reach the value

$$v_o(1 \text{ ms}) = -100(1 - e^{-1/10}) = -9.5 \text{ V}$$

The output waveform is shown in Fig. 2.26(c), from which we see that including  $R_F$  causes the ramp to be slightly rounded such that the output reaches only  $-9.5 \text{ V}$ ,  $0.5 \text{ V}$  short of the ideal value of  $-10 \text{ V}$ . Furthermore, for  $t > 1 \text{ ms}$ , the capacitor discharges through  $R_F$  with the relatively long time constant of  $10 \text{ ms}$ . Finally, we note that op-amp saturation, specified to occur at  $\pm 13 \text{ V}$ , has no effect on the operation of this circuit.

The preceding example hints at an important application of integrators, namely, their use in providing triangular waveforms in response to square-wave inputs. This application is explored in Exercise 2.18. Integrators have many other applications, including their use in the design of filters (Chapter 17).

### 2.5.3 The Op-Amp Differentiator

Interchanging the location of the capacitor and the resistor of the integrator circuit results in the circuit in Fig. 2.27(a), which performs the mathematical function of differentiation. To see how this comes about, let the input be the time-varying function  $v_i(t)$ , and note that the virtual ground at the inverting input terminal of the op amp causes  $v_i(t)$  to appear in effect across the capacitor  $C$ . Thus the current through  $C$  will be  $C(dv_i/dt)$ , and this current flows through the feedback resistor  $R$  providing at the op-amp output a voltage  $v_o(t)$ ,

➤

$$v_o(t) = -CR \frac{dv_i(t)}{dt} \quad (2.31)$$

The frequency-domain transfer function of the differentiator circuit can be found by substituting in Eq. (2.24),  $Z_1(s) = 1/sC$  and  $Z_2(s) = R$  to obtain

➤

$$\frac{V_o(s)}{V_i(s)} = -sCR \quad (2.32)$$

which for physical frequencies  $s = j\omega$  yields

➤

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega CR \quad (2.33)$$

Thus the transfer function has magnitude

➤

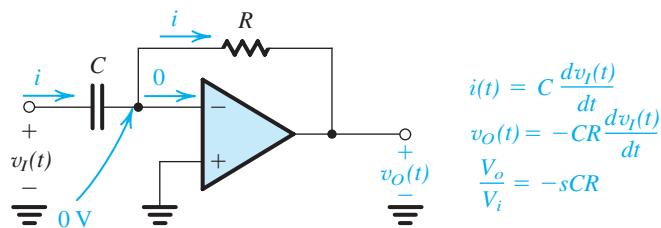
$$\left| \frac{V_o}{V_i} \right| = \omega CR \quad (2.34)$$

and phase

$$\phi = -90^\circ \quad (2.35) \quad \text{◀}$$

The Bode plot of the magnitude response can be found from Eq. (2.34) by noting that for an octave increase in  $\omega$ , the magnitude doubles (increases by 6 dB). Thus the plot is simply a straight line of slope +6 dB/octave (or, equivalently, +20 dB/decade) intersecting the 0-dB line (where  $|V_o/V_i| = 1$ ) at  $\omega = 1/CR$ , where  $CR$  is the **differentiator time constant** [see Fig. 2.27(b)].

The frequency response of the differentiator can be thought of as the response of an STC high-pass filter with a corner frequency at infinity (refer to Fig. 1.24). Finally, we should note that the very nature of a differentiator circuit causes it to be a “noise magnifier.” This is due to the spike introduced at the output every time there is a sharp change in  $v_I(t)$ ; such a change could be interference coupled electromagnetically (“picked up”) from adjacent signal sources. For this reason and because they suffer from stability problems (Chapter 11), differentiator circuits are generally avoided in practice. When the circuit of Fig. 2.27(a) is used, it is usually necessary to connect a small-valued resistor in series with the capacitor. This modification, unfortunately, turns the circuit into a nonideal differentiator.

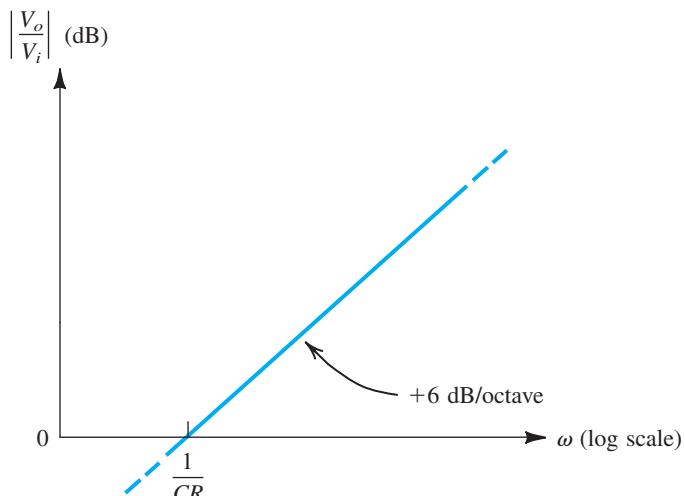


(a)

$$i(t) = C \frac{dv_I(t)}{dt}$$

$$v_O(t) = -CR \frac{dv_I(t)}{dt}$$

$$\frac{V_o}{V_i} = -sCR$$



(b)

**Figure 2.27** (a) A differentiator. (b) Frequency response of a differentiator with a time constant  $CR$ .

## EXERCISES

- 2.18** Consider a symmetrical square wave of 20-V peak-to-peak, 0 average, and 2-ms period applied to a Miller integrator. Find the value of the time constant  $CR$  such that the triangular waveform at the output has a 20-V peak-to-peak amplitude.

**Ans.** 0.5 ms

- D2.19** Use an ideal op amp to design an inverting integrator with an input resistance of 10 k $\Omega$  and an integration time constant of  $10^{-3}$  s. What is the gain magnitude and phase angle of this circuit at 10 rad/s and at 1 rad/s? What is the frequency at which the gain magnitude is unity?

**Ans.**  $R = 10 \text{ k}\Omega$ ,  $C = 0.1 \mu\text{F}$ ; at  $\omega = 10 \text{ rad/s}$ :  $|V_o/V_i| = 100 \text{ V/V}$  and  $\phi = +90^\circ$ ; at  $\omega = 1 \text{ rad/s}$ :  $|V_o/V_i| = 1000 \text{ V/V}$  and  $\phi = +90^\circ$ ; 1000 rad/s

- D2.20** Design a differentiator to have a time constant of  $10^{-2}$  s and an input capacitance of 0.01  $\mu\text{F}$ . What is the gain magnitude and phase of this circuit at 10 rad/s, and at  $10^3$  rad/s? In order to limit the high-frequency gain of the differentiator circuit to 100, a resistor is added in series with the capacitor. Find the required resistor value.

**Ans.**  $C = 0.01 \mu\text{F}$ ;  $R = 1 \text{ M}\Omega$ ; at  $\omega = 10 \text{ rad/s}$ :  $|V_o/V_i| = 0.1 \text{ V/V}$  and  $\phi = -90^\circ$ ; at  $\omega = 1000 \text{ rad/s}$ :  $|V_o/V_i| = 10 \text{ V/V}$  and  $\phi = -90^\circ$ ; 10 k $\Omega$

## 2.6 DC Imperfections

Thus far we have considered the op amp to be ideal. The only exception has been a brief discussion of the effect of the op-amp finite gain  $A$  on the closed-loop gain of the inverting and noninverting configurations. Although in many applications the assumption of an ideal op amp is not a bad one, a circuit designer has to be thoroughly familiar with the characteristics of practical op amps and the effects of such characteristics on the performance of op-amp circuits. Only then will the designer be able to use the op amp intelligently, especially if the application at hand is not a straightforward one. The nonideal properties of op amps will, of course, limit the range of operation of the circuits analyzed in the previous examples.

In this and the two sections that follow, we consider some of the important nonideal properties of the op amp.<sup>4</sup> We do this by treating one nonideality at a time, beginning in this section with the dc problems to which op amps are susceptible.

### 2.6.1 Offset Voltage

Because op amps are direct-coupled devices with large gains at dc, they are prone to dc problems. The first such problem is the dc offset voltage. To understand this problem consider

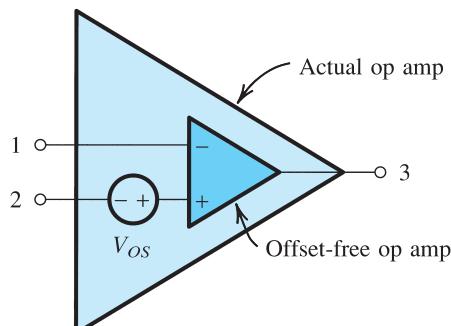
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<sup>4</sup>We should note that real op amps have nonideal effects additional to those discussed in this chapter. These include finite (nonzero) common-mode gain or, equivalently, noninfinite CMRR, noninfinite input resistance, and nonzero output resistance. The effect of these, however, on the performance of most of the closed-loop circuits studied here is not very significant, and their study will be postponed to later chapters (in particular, Chapters 9, 10, and 13).

the following *conceptual* experiment: If the two input terminals of the op amp are tied together and connected to ground, it will be found that despite the fact that  $v_{Id} = 0$ , a finite dc voltage exists at the output. In fact, if the op amp has a high dc gain, the output will be at either the positive or negative saturation level. The op-amp output can be brought back to its ideal value of 0 V by connecting a dc voltage source of appropriate polarity and magnitude between the two input terminals of the op amp. This external source balances out the input offset voltage of the op amp. It follows that the **input offset voltage** ( $V_{os}$ ) must be of equal magnitude and of opposite polarity to the voltage we applied externally.

The input offset voltage arises as a result of the unavoidable mismatches present in the input differential stage inside the op amp. In later chapters (in particular Chapters 9 and 13) we shall study this topic in detail. Here, however, our concern is to investigate the effect of  $V_{os}$  on the operation of closed-loop op-amp circuits. Toward that end, we note that general-purpose op amps exhibit  $V_{os}$  in the range of 1 mV to 5 mV. Also, the value of  $V_{os}$  depends on temperature. The op-amp data sheets usually specify typical and maximum values for  $V_{os}$  at room temperature as well as the temperature coefficient of  $V_{os}$  (usually in  $\mu\text{V}/^\circ\text{C}$ ). They do not, however, specify the polarity of  $V_{os}$  because the component mismatches that give rise to  $V_{os}$  are obviously not known *a priori*; different units of the same op-amp type may exhibit either a positive or a negative  $V_{os}$ .

To analyze the effect of  $V_{os}$  on the operation of op-amp circuits, we need a circuit model for the op amp with input offset voltage. Such a model is shown in Fig. 2.28. It consists of a dc source of value  $V_{os}$  placed in series with the positive input lead of an offset-free op amp. The justification for this model follows from the description above.



**Figure 2.28** Circuit model for an op amp with input offset voltage  $V_{os}$ .

### EXERCISE

- 2.21** Use the model of Fig. 2.28 to sketch the transfer characteristic  $v_o$  versus  $v_{id}$  ( $v_o \equiv v_3$  and  $v_{id} \equiv v_2 - v_1$ ) of an op amp having an open-loop dc gain  $A_0 = 10^4$  V/V, output saturation levels of  $\pm 10$  V, and  $V_{os}$  of +5 mV.

**Ans.** See Fig. E2.21. Observe that true to its name, the input offset voltage causes an offset in the voltage-transfer characteristic; rather than passing through the origin it is now shifted to the left by  $V_{os}$ .

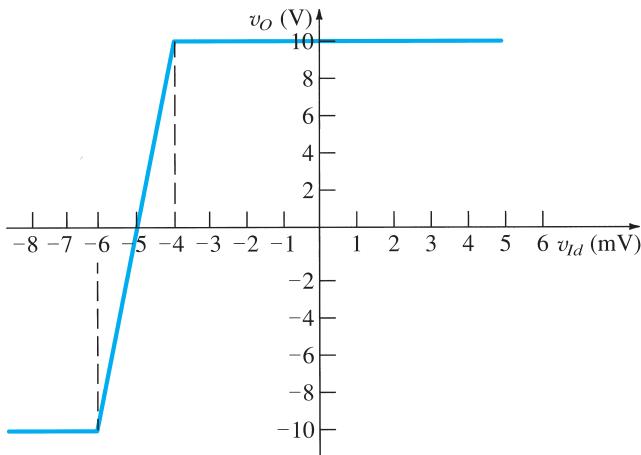


Figure E2.21 Transfer characteristic of an op amp with  $V_{os} = 5 \text{ mV}$ .

Analysis of op-amp circuits to determine the effect of the op-amp  $V_{os}$  on their performance is straightforward: The input voltage signal source is short-circuited and the op amp is replaced with the model of Fig. 2.28. (Eliminating the input signal, done to simplify matters, is based on the principle of superposition.) Following this procedure, we find that both the inverting and the noninverting amplifier configurations result in the same circuit, that shown in Fig. 2.29, from which the output dc voltage due to  $V_{os}$  is found to be

$$V_o = V_{os} \left[ 1 + \frac{R_2}{R_1} \right] \quad (2.36)$$

This output dc voltage can have a large magnitude. For instance, a noninverting amplifier with a closed-loop gain of 1000, when constructed from an op amp with a 5-mV input offset voltage, will have a dc output voltage of +5 V or -5 V (depending on the polarity of  $V_{os}$ ) rather than the ideal value of 0 V. Now, when an input signal is applied to the amplifier, the corresponding signal output will be superimposed on the 5-V dc. Obviously then, the

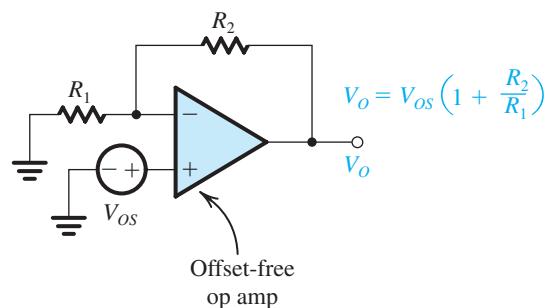
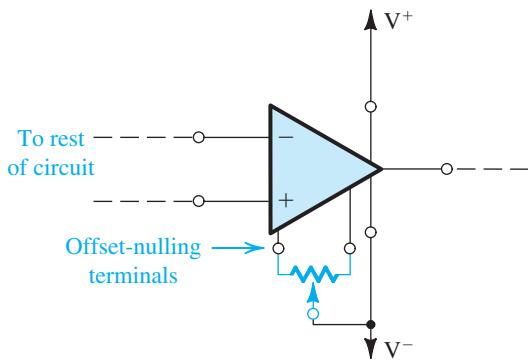
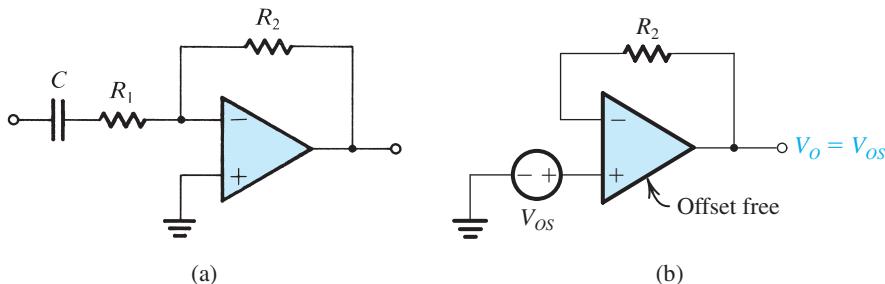


Figure 2.29 Evaluating the output dc offset voltage due to  $V_{os}$  in a closed-loop amplifier.



**Figure 2.30** The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.



**Figure 2.31** (a) A capacitively coupled inverting amplifier. (b) The equivalent circuit for determining its dc output offset voltage  $V_o$ .

allowable signal swing at the output will be reduced. Even worse, if the signal to be amplified is dc, we would not know whether the output is due to  $V_{os}$  or to the signal!

Some op amps are provided with two additional terminals to which a specified circuit can be connected to trim to zero the output dc voltage due to  $V_{os}$ . Figure 2.30 shows such an arrangement that is typically used with general-purpose op amps. A potentiometer is connected between the offset-nulling terminals with the wiper of the potentiometer connected to the op-amp negative supply. Moving the potentiometer wiper introduces an imbalance that counteracts the asymmetry present in the internal op-amp circuitry and that gives rise to  $V_{os}$ . We shall return to this point in the context of our study of the internal circuitry of op amps in Chapter 13. It should be noted, however, that even though the dc output offset can be trimmed to zero, the problem remains of the variation (or drift) of  $V_{os}$  with temperature.

One way to overcome the dc offset problem is by capacitively coupling the amplifier. This, however, will be possible only in applications where the closed-loop amplifier is not required to amplify dc or very-low-frequency signals. Figure 2.31(a) shows a capacitively coupled amplifier. Because of its infinite impedance at dc, the coupling capacitor will cause the gain to be zero at dc. As a result, the equivalent circuit for determining the dc output voltage resulting from the op-amp input offset voltage  $V_{os}$  will be that shown in Fig. 2.31(b). Thus  $V_{os}$  sees in effect a unity-gain voltage follower, and the dc output voltage  $V_o$  will be equal to  $V_{os}$  rather than  $V_{os}(1 + R_2/R_1)$ , which is the case without the coupling capacitor. As far as input signals are concerned, the coupling capacitor  $C$  forms together with  $R_1$  an STC high-pass circuit with a corner frequency of  $\omega_0 = 1/CR_1$ . Thus the gain of the capacitively

coupled amplifier will fall off at the low-frequency end [from a magnitude of  $(1 + R_2/R_1)$  at high frequencies] and will be 3 dB down at  $\omega_0$ .

## EXERCISES

- 2.22** Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of  $\pm 10$  V. (a) What is (approximately) the peak sine-wave input signal that can be applied without output clipping? (b) If the effect of  $V_{os}$  is nulled at room temperature ( $25^\circ\text{C}$ ), how large an input can one now apply if: (i) the circuit is to operate at a constant temperature? (ii) the circuit is to operate at a temperature in the range  $0^\circ\text{C}$  to  $75^\circ\text{C}$  and the temperature coefficient of  $V_{os}$  is  $10 \mu\text{V}/^\circ\text{C}$ ?

**Ans.** (a) 7 mV; (b) 10 mV, 9.5 mV

- 2.23** Consider the same amplifier as in Exercise 2.22—that is, an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of  $\pm 10$  V—except here let the amplifier be capacitively coupled as in Fig. 2.31(a). (a) What is the dc offset voltage at the output, and what (approximately) is the peak sine-wave signal that can be applied at the input without output clipping? Is there a need for offset trimming? (b) If  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 1 \text{ M}\Omega$ , find the value of the coupling capacitor  $C_1$  that will ensure that the gain will be greater than 57 dB down to 100 Hz.

**Ans.** (a) 3 mV, 10 mV, no need for offset trimming; (b)  $1.6 \mu\text{F}$

### 2.6.2 Input Bias and Offset Currents

The second dc problem encountered in op amps is illustrated in Fig. 2.32. In order for the op amp to operate, its two input terminals have to be supplied with dc currents, termed the **input bias currents**.<sup>5</sup> In Fig. 2.32 these two currents are represented by two current sources,  $I_{B1}$  and  $I_{B2}$ , connected to the two input terminals. It should be emphasized that the input bias currents are independent of the fact that a real op amp has finite (though large) input resistance (not shown in Fig. 2.32). The op-amp manufacturer usually specifies the average value of  $I_{B1}$  and  $I_{B2}$  as well as their expected difference. The average value  $I_B$  is called the **input bias current**,



$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

and the difference is called the **input offset current** and is given by

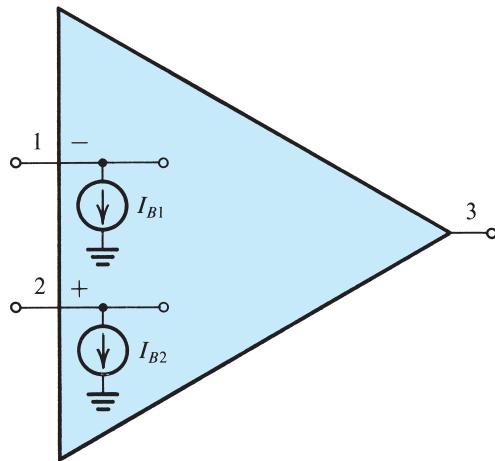


$$I_{OS} = |I_{B1} - I_{B2}|$$

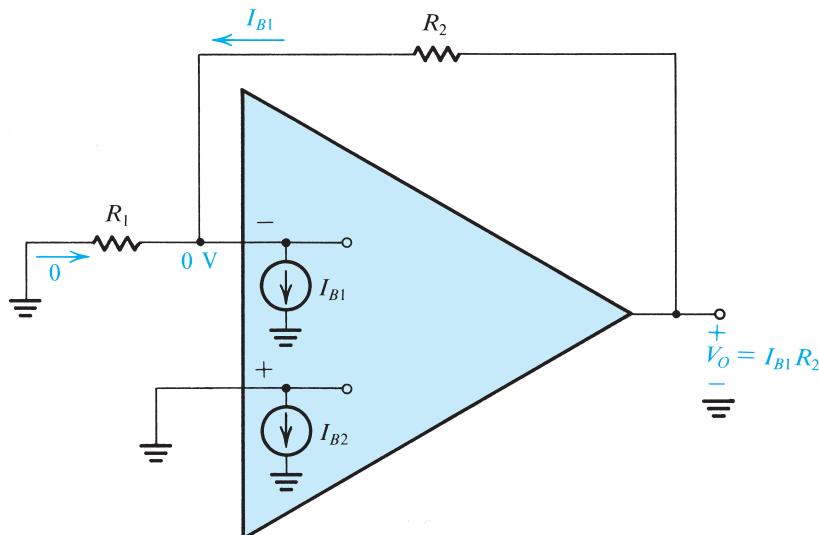
Typical values for general-purpose op amps that use bipolar transistors are  $I_B = 100 \text{ nA}$  and  $I_{OS} = 10 \text{ nA}$ .

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<sup>5</sup>This is the case for op amps constructed using bipolar junction transistors (BJTs). Those using MOSFETs in the first (input) stage do not draw an appreciable input bias current; nevertheless, the input terminals should have continuous dc paths to ground. More on this in later chapters.



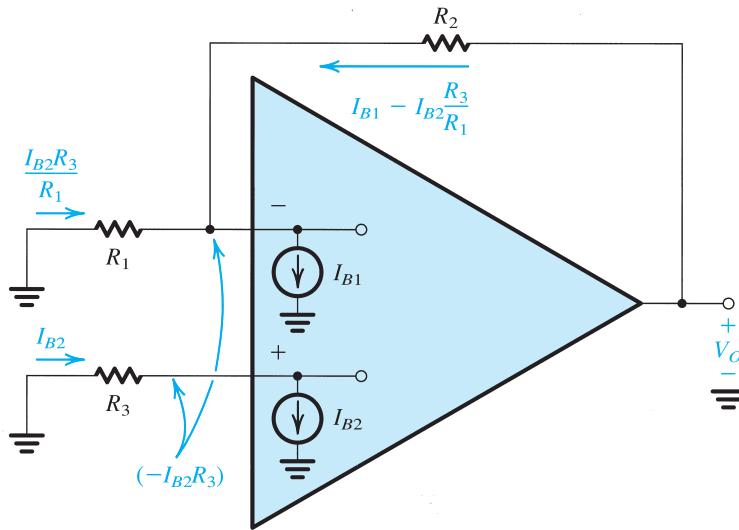
**Figure 2.32** The op-amp input bias currents represented by two current sources  $I_{B1}$  and  $I_{B2}$ .



**Figure 2.33** Analysis of the closed-loop amplifier, taking into account the input bias currents.

We now wish to find the dc output voltage of the closed-loop amplifier due to the input bias currents. To do this we ground the signal source and obtain the circuit shown in Fig. 2.33 for both the inverting and noninverting configurations. As shown in Fig. 2.33, the output dc voltage is given by

$$V_o = I_{B1}R_2 \simeq I_B R_2 \quad (2.37)$$



**Figure 2.34** Reducing the effect of the input bias currents by introducing a resistor  $R_3$ .

This obviously places an upper limit on the value of  $R_2$ . Fortunately, however, a technique exists for reducing the value of the output dc voltage due to the input bias currents. The method consists of introducing a resistance  $R_3$  in series with the noninverting input lead, as shown in Fig. 2.34. From a signal point of view,  $R_3$  has a negligible effect (ideally no effect). The appropriate value for  $R_3$  can be determined by analyzing the circuit in Fig. 2.34, where analysis details are shown, and the output voltage is given by

$$V_O = -I_{B2}R_3 + R_2(I_{B1} - I_{B2}R_3/R_1) \quad (2.38)$$

Consider first the case  $I_{B1} = I_{B2} = I_B$ , which results in

$$V_O = I_B[R_2 - R_3(1 + R_2/R_1)]$$

Thus we can reduce  $V_O$  to zero by selecting  $R_3$  such that

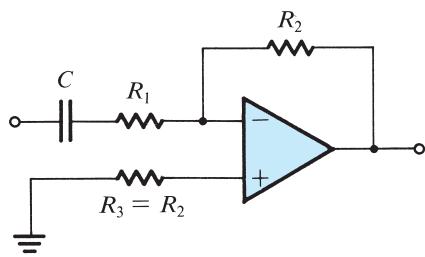
$$R_3 = \frac{R_2}{1 + R_2/R_1} = \frac{R_1R_2}{R_1 + R_2} \quad (2.39)$$

That is,  $R_3$  should be made equal to the parallel equivalent of  $R_1$  and  $R_2$ .

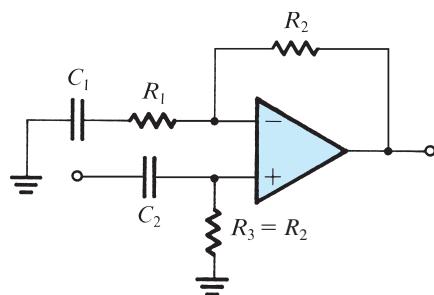
Having selected  $R_3$  as above, let us evaluate the effect of a finite offset current  $I_{OS}$ . Let  $I_{B1} = I_B + I_{OS}/2$  and  $I_{B2} = I_B - I_{OS}/2$ , and substitute in Eq. (2.38). The result is

$$V_O = I_{OS}R_2 \quad (2.40)$$

which is usually about an order of magnitude smaller than the value obtained without  $R_3$  (Eq. 2.37). We conclude that to minimize the effect of the input bias currents, one should place in the positive lead a resistance equal to the equivalent dc resistance seen by the inverting terminal. We emphasize the word *dc* in the last statement; note that if the amplifier is ac-coupled, we should select  $R_3 = R_2$ , as shown in Fig. 2.35.



**Figure 2.35** In an ac-coupled amplifier the dc resistance seen by the inverting terminal is  $R_2$ ; hence  $R_3$  is chosen equal to  $R_2$ .



**Figure 2.36** Illustrating the need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will *not* work without resistor  $R_3$ .

While we are on the subject of ac-coupled amplifiers, we should note that one must always provide a continuous dc path between each of the input terminals of the op amp and ground. This is the case no matter how small  $I_B$  is. For this reason the ac-coupled noninverting amplifier of Fig. 2.36 will *not* work without the resistance  $R_3$  to ground. Unfortunately, including  $R_3$  lowers considerably the input resistance of the closed-loop amplifier.

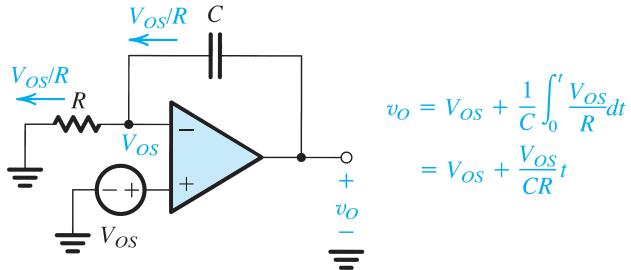
### EXERCISE

- 2.24** Consider an inverting amplifier circuit designed using an op amp and two resistors,  $R_1 = 10\text{ k}\Omega$  and  $R_2 = 1\text{ M}\Omega$ . If the op amp is specified to have an input bias current of  $100\text{ nA}$  and an input offset current of  $10\text{ nA}$ , find the output dc offset voltage resulting and the value of a resistor  $R_3$  to be placed in series with the positive input lead in order to minimize the output offset voltage. What is the new value of  $V_o$ ?

**Ans.**  $0.1\text{ V}$ ;  $9.9\text{ k}\Omega$  ( $\approx 10\text{ k}\Omega$ );  $0.01\text{ V}$

### 2.6.3 Effect of $V_{os}$ and $I_{os}$ on the Operation of the Inverting Integrator

Our discussion of the inverting integrator circuit in Section 2.5.2 mentioned the susceptibility of this circuit to saturation in the presence of small dc voltages or currents. It behooves us therefore to consider the effect of the op-amp dc offsets on its operation. As will be seen, these effects can be quite dramatic.



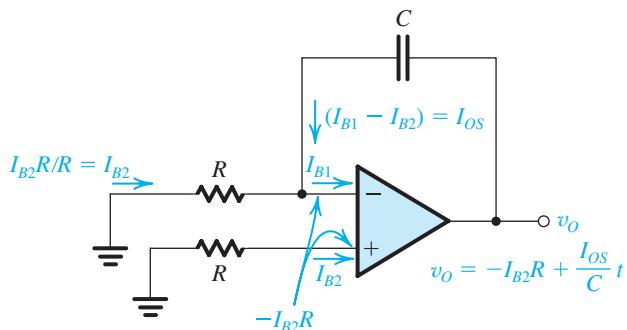
**Figure 2.37** Determining the effect of the op-amp input offset voltage  $V_{os}$  on the Miller integrator circuit. Note that since the output rises with time, the op amp eventually saturates.

To see the effect of the input dc offset voltage  $V_{os}$ , consider the integrator circuit in Fig. 2.37, where for simplicity we have short-circuited the input signal source. Analysis of the circuit is straightforward and is shown in Fig. 2.37. Assuming for simplicity that at time  $t = 0$  the voltage across the capacitor is zero, the output voltage as a function of time is given by

$$v_o = V_{os} + \frac{V_{os}}{CR} t \quad (2.41)$$

Thus  $v_o$  increases linearly with time until the op amp saturates—clearly an unacceptable situation! As should be expected, the dc input offset current  $I_{os}$  produces a similar problem. Figure 2.38 illustrates the situation. Observe that we have added a resistance  $R$  in the op-amp positive-input lead in order to keep the input bias current  $I_B$  from flowing through  $C$ . Nevertheless, the offset current  $I_{os}$  will flow through  $C$  and cause  $v_o$  to ramp linearly with time until the op amp saturates.

As mentioned in Section 2.5.2 the dc problem of the integrator circuit can be alleviated by connecting a resistor  $R_F$  across the integrator capacitor  $C$ , as shown in Fig. 2.25. Such a resistor provides a dc path through which the dc currents ( $V_{os}/R$ ) and  $I_{os}$  can flow (assuming a resistance equal to  $R \parallel R_F$  is connected in the positive op-amp lead), with the result that  $v_o$  will now have a dc component [ $V_{os}(1 + R_F/R) + I_{os}R_F$ ] instead of rising linearly. To keep the dc offset at the output small, one would select a low value for  $R_F$ . Unfortunately, however, the lower the value of  $R_F$ , the less ideal the integrator circuit becomes.



**Figure 2.38** Effect of the op-amp input bias and offset currents on the performance of the Miller integrator circuit.

**EXERCISE**

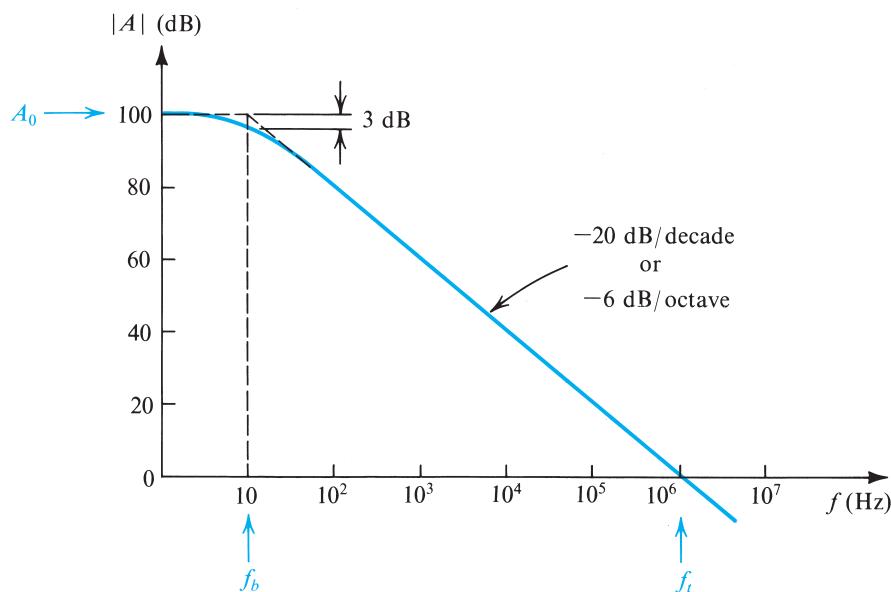
- 2.25** Consider a Miller integrator with a time constant of 1 ms and an input resistance of  $10\text{ k}\Omega$ . Let the op amp have  $V_{os} = 2\text{ mV}$  and output saturation voltages of  $\pm 12\text{ V}$ . (a) Assuming that when the power supply is turned on the capacitor voltage is zero, how long does it take for the amplifier to saturate? (b) Select the largest possible value for a feedback resistor  $R_F$  so that at least  $\pm 10\text{ V}$  of output signal swing remains available. What is the corner frequency of the resulting STC network?

**Ans.** (a) 6 s; (b)  $10\text{ M}\Omega$ , 0.16 Hz

## 2.7 Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance

### 2.7.1 Frequency Dependence of the Open-Loop Gain

The differential open-loop gain  $A$  of an op amp is not infinite; rather, it is finite and decreases with frequency. Figure 2.39 shows a plot for  $|A|$ , with the numbers typical of some commercially available general-purpose op amps (such as the popular 741-type op amp, available from many semiconductor manufacturers; its internal circuit is studied in Chapter 13).



**Figure 2.39** Open-loop gain of a typical general-purpose, internally compensated op amp.

Note that although the gain is quite high at dc and low frequencies, it starts to fall off at a rather low frequency (10 Hz in our example). The uniform -20-dB/decade gain rolloff shown is typical of **internally compensated** op amps. These are units that have a network (usually a single capacitor) included within the same IC chip whose function is to cause the op-amp gain to have the single-time-constant (STC) low-pass response shown. This process of modifying the open-loop gain is termed **frequency compensation**, and its purpose is to ensure that op-amp circuits will be stable (as opposed to oscillatory). The subject of stability of op-amp circuits—or, more generally, of feedback amplifiers—will be studied in Chapter 11.

By analogy to the response of low-pass STC circuits (see Section 1.6 and, for more detail, Appendix E), the gain  $A(s)$  of an internally compensated op amp may be expressed as

$$\Rightarrow A(s) = \frac{A_0}{1 + s/\omega_b} \quad (2.42)$$

which for physical frequencies,  $s = j\omega$ , becomes

$$\Rightarrow A(j\omega) = \frac{A_0}{1 + j\omega/\omega_b} \quad (2.43)$$

where  $A_0$  denotes the dc gain and  $\omega_b$  is the 3-dB frequency (corner frequency or “break” frequency). For the example shown in Fig. 2.39,  $A_0 = 10^5$  and  $\omega_b = 2\pi \times 10$  rad/s. For frequencies  $\omega \gg \omega_b$  (about 10 times and higher) Eq. (2.43) may be approximated by

$$A(j\omega) \approx \frac{A_0 \omega_b}{j\omega} \quad (2.44)$$

Thus,

$$|A(j\omega)| = \frac{A_0 \omega_b}{\omega} \quad (2.45)$$

from which it can be seen that the gain  $|A|$  reaches unity (0 dB) at a frequency denoted by  $\omega_t$  and given by

$$\Rightarrow \omega_t = A_0 \omega_b \quad (2.46)$$

Substituting in Eq. (2.44) gives

$$\Rightarrow A(j\omega) \approx \frac{\omega_t}{j\omega} \quad (2.47)$$

The frequency  $f_t = \omega_t/2\pi$  is usually specified on the data sheets of commercially available op amps and is known as the **unity-gain bandwidth**.<sup>6</sup> Also note that for  $\omega \gg \omega_b$  the open-loop gain in Eq. (2.42) becomes

$$\Rightarrow A(s) \approx \frac{\omega_t}{s} \quad (2.48)$$

---

<sup>6</sup>Since  $f_t$  is the product of the dc gain  $A_0$  and the 3-dB bandwidth  $f_b$  (where  $f_b = \omega_b/2\pi$ ), it is also known as the **gain-bandwidth product** (GB). The reader is cautioned, however, that in some amplifiers (those that do not have an STC response), the unity-gain frequency and the gain-bandwidth product are *not* equal.

The gain magnitude can be obtained from Eq. (2.47) as

$$|A(j\omega)| \simeq \frac{\omega_t}{\omega} = \frac{f_t}{f} \quad (2.49)$$

Thus if  $f_t$  is known ( $10^6$  Hz in our example), one can easily determine the magnitude of the op-amp gain at a given frequency  $f$ . Furthermore, observe that this relationship correlates with the Bode plot in Fig. 2.39. Specifically, for  $f \gg f_b$ , doubling  $f$  (an octave increase) results in halving the gain (a 6-dB reduction). Similarly, increasing  $f$  by a factor of 10 (a decade increase) results in reducing  $|A|$  by a factor of 10 (20 dB).

As a matter of practical importance, we note that the production spread in the value of  $f_t$  between op-amp units of the same type is usually much smaller than that observed for  $A_0$  and  $f_b$ . For this reason  $f_t$  is preferred as a specification parameter. Finally, it should be mentioned that an op amp having this uniform  $-6$ -dB/octave (or equivalently  $-20$ -dB/decade) gain rolloff is said to have a **single-pole model**. Also, since this single pole *dominates* the amplifier frequency response, it is called a *dominant pole*. For more on poles (and zeros), the reader may wish to consult Appendix F.

### EXERCISE

- 2.26** An internally compensated op amp is specified to have an open-loop dc gain of 106 dB and a unity-gain bandwidth of 3 MHz. Find  $f_b$  and the open-loop gain (in dB) at  $f_b$ , 300 Hz, 3 kHz, 12 kHz, and 60 kHz.

**Ans.** 15 Hz; 103 dB; 80 dB; 60 dB; 48 dB; 34 dB

## 2.7.2 Frequency Response of Closed-Loop Amplifiers

We next consider the effect of limited op-amp gain and bandwidth on the closed-loop transfer functions of the two basic configurations: the inverting circuit of Fig. 2.5 and the noninverting circuit of Fig. 2.12. The closed-loop gain of the inverting amplifier, assuming a finite op-amp open-loop gain  $A$ , was derived in Section 2.2 and given in Eq. (2.5), which we repeat here as

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A} \quad (2.50)$$

Substituting for  $A$  from Eq. (2.42) and using Eq. (2.46) gives

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + \frac{1}{A_0} \left( 1 + \frac{R_2}{R_1} \right) + \frac{s}{\omega_t/(1 + R_2/R_1)}} \quad (2.51)$$

For  $A_0 \gg 1 + R_2/R_1$ , which is usually the case,

$$\frac{V_o(s)}{V_i(s)} \simeq \frac{-R_2/R_1}{1 + \frac{s}{\omega_t/(1 + R_2/R_1)}} \quad (2.52)$$

which is of the same form as that for a low-pass STC network (see Table 1.2, page 36). Thus the inverting amplifier has an STC low-pass response with a dc gain of magnitude equal to  $R_2/R_1$ . The closed-loop gain rolls off at a uniform –20-dB/decade slope with a corner frequency (3-dB frequency) given by

$$\gg \quad \omega_{3\text{dB}} = \frac{\omega_t}{1 + R_2/R_1} \quad (2.53)$$

Similarly, analysis of the noninverting amplifier of Fig. 2.12, assuming a finite open-loop gain  $A$ , yields the closed-loop transfer function

$$\gg \quad \frac{V_o}{V_i} = \frac{1 + R_2/R_1}{1 + (1 + R_2/R_1)/A} \quad (2.54)$$

Substituting for  $A$  from Eq. (2.42) and making the approximation  $A_0 \gg 1 + R_2/R_1$  results in

$$\gg \quad \frac{V_o(s)}{V_i(s)} \simeq \frac{1 + R_2/R_1}{1 + \frac{s}{\omega_t/(1 + R_2/R_1)}} \quad (2.55)$$

Thus the noninverting amplifier has an STC low-pass response with a dc gain of  $(1 + R_2/R_1)$  and a 3-dB frequency given also by Eq. (2.53).

### Example 2.6

Consider an op amp with  $f_t = 1 \text{ MHz}$ . Find the 3-dB frequency of closed-loop amplifiers with nominal gains of  $+1000, +100, +10, +1, -1, -10, -100$ , and  $-1000$ . Sketch the magnitude frequency response for the amplifiers with closed-loop gains of  $+10$  and  $-10$ .

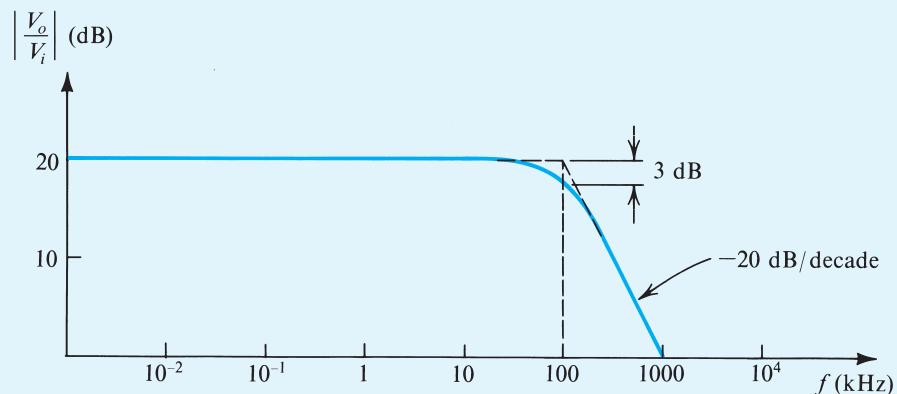
#### Solution

We use Eq. (2.53) to obtain the results given in the following table.

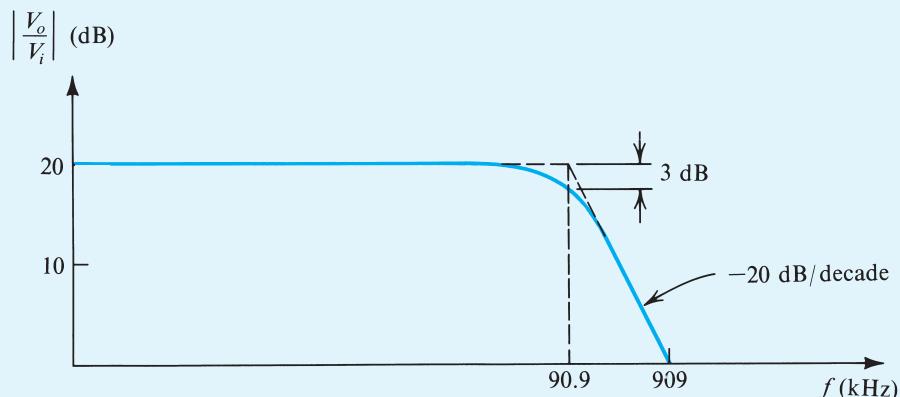
Closed-Loop Gain	$R_2/R_1$	$f_{3 \text{ dB}} = f_t/(1 + R_2/R_1)$
+1000	999	1 kHz
+100	99	10 kHz
+10	9	100 kHz
+1	0	1 MHz
-1	1	0.5 MHz
-10	10	90.9 kHz
-100	100	9.9 kHz
-1000	1000	$\simeq 1 \text{ kHz}$

Figure 2.40 shows the frequency response for the amplifier whose nominal dc gain is  $+10$  (20 dB), and Fig. 2.41 shows the frequency response for the  $-10$  (also 20 dB) case. An interesting observation follows

from the table above: The unity-gain inverting amplifier has a 3-dB frequency of  $f_t/2$  as compared to  $f_t$  for the unity-gain noninverting amplifier (the unity-gain voltage follower).



**Figure 2.40** Frequency response of an amplifier with a nominal gain of +10 V/V.



**Figure 2.41** Frequency response of an amplifier with a nominal gain of -10 V/V.

The table in Example 2.6 above clearly illustrates the trade-off between gain and bandwidth: For a given op amp, the lower the closed-loop gain required, the wider the bandwidth achieved. Indeed, the noninverting configuration exhibits a constant **gain-bandwidth product** equal to  $f_t$  of the op amp. An interpretation of these results in terms of feedback theory will be given in Chapter 11.

## EXERCISES

- 2.27** An internally compensated op amp has a dc open-loop gain of  $10^6$  V/V and an open-loop gain of 40 dB at 10 kHz. Estimate its 3-dB frequency, its unity-gain frequency, its gain-bandwidth product, and its expected gain at 1 kHz.

**Ans.** 1 Hz; 1 MHz; 1 MHz; 60 dB

- 2.28** An op amp having a 106-dB gain at dc and a single-pole frequency response with  $f_i = 2$  MHz is used to design a noninverting amplifier with nominal dc gain of 100. Find the 3-dB frequency of the closed-loop gain.

**Ans.** 20 kHz

## 2.8 Large-Signal Operation of Op Amps

In this section, we study the limitations on the performance of op-amp circuits when large output signals are present.

### 2.8.1 Output Voltage Saturation

Similar to all other amplifiers, op amps operate linearly over a limited range of output voltages. Specifically, the op-amp output saturates in the manner shown in Fig. 1.14 with  $L_+$  and  $L_-$  within 1 V or so of the positive and negative power supplies, respectively. Thus, an op amp that is operating from  $\pm 15$ -V supplies will saturate when the output voltage reaches about +13 V in the positive direction and -13 V in the negative direction. For this particular op amp the **rated output voltage** is said to be  $\pm 13$  V. To avoid clipping off the peaks of the output waveform, and the resulting waveform distortion, the input signal must be kept correspondingly small.

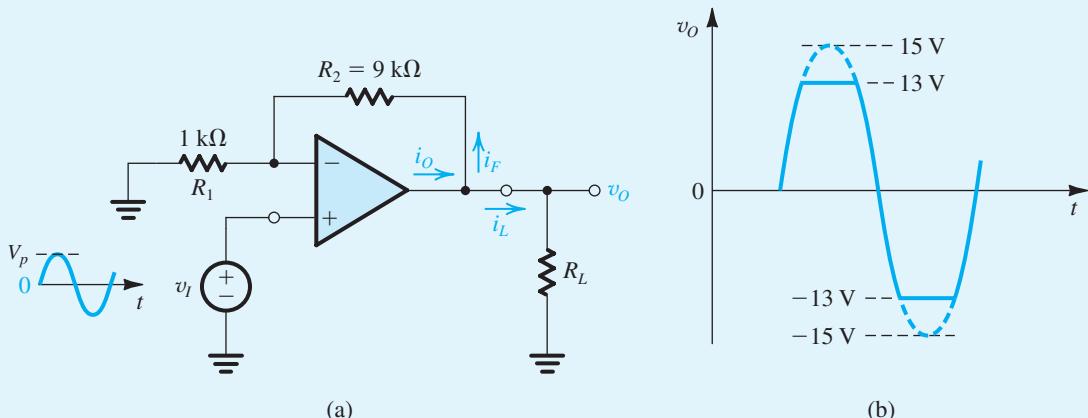
### 2.8.2 Output Current Limits

Another limitation on the operation of op amps is that their output current is limited to a specified maximum. For instance, the popular 741 op amp is specified to have a maximum output current of  $\pm 20$  mA. Thus, in designing closed-loop circuits utilizing the 741, the designer has to ensure that under no condition will the op amp be required to supply an output current, in either direction, exceeding 20 mA. This, of course, has to include both the current in the feedback circuit as well as the current supplied to a load resistor. If the circuit requires a larger current, the op-amp output voltage will saturate at the level corresponding to the maximum allowed output current.

### Example 2.7

Consider the noninverting amplifier circuit shown in Fig. 2.42. As shown, the circuit is designed for a nominal gain ( $1 + R_2/R_1$ ) = 10 V/V. It is fed with a low-frequency sine-wave signal of peak voltage  $V_p$  and is connected to a load resistor  $R_L$ . The op amp is specified to have output saturation voltages of  $\pm 13$  V and output current limits of  $\pm 20$  mA.

- For  $V_p = 1$  V and  $R_L = 1$  k $\Omega$ , specify the signal resulting at the output of the amplifier.
- For  $V_p = 1.5$  V and  $R_L = 1$  k $\Omega$ , specify the signal resulting at the output of the amplifier.
- For  $R_L = 1$  k $\Omega$ , what is the maximum value of  $V_p$  for which an undistorted sine-wave output is obtained?
- For  $V_p = 1$  V, what is the lowest value of  $R_L$  for which an undistorted sine-wave output is obtained?



**Figure 2.42** (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at  $\pm 13$ -V output voltage and has  $\pm 20$ -mA output current limits. (b) When the input sine wave has a peak of 1.5 V, the output is clipped off at  $\pm 13$  V.

### Solution

- For  $V_p = 1$  V and  $R_L = 1$  k $\Omega$ , the output will be a sine wave with peak value of 10 V. This is lower than output saturation levels of  $\pm 13$  V, and thus the amplifier is not limited that way. Also, when the output is at its peak (10 V), the current in the load will be  $10\text{ V}/1\text{ k}\Omega = 10\text{ mA}$ , and the current in the feedback network will be  $10\text{ V}/(9 + 1)\text{ k}\Omega = 1\text{ mA}$ , for a total op-amp output current of 11 mA, well under its limit of 20 mA.
- Now if  $V_p$  is increased to 1.5 V, ideally the output would be a sine wave of 15-V peak. The op amp, however, will saturate at  $\pm 13$  V, thus clipping the sine-wave output at these levels. Let's next check on the op-amp output current: At 13-V output and  $R_L = 1\text{ k}\Omega$ ,  $i_L = 13\text{ mA}$  and  $i_F = 1.3\text{ mA}$ ; thus  $i_O = 14.3\text{ mA}$ , again under the 20-mA limit. Thus the output will be a sine wave with its peaks clipped off at  $\pm 13$  V, as shown in Fig. 2.42(b).
- For  $R_L = 1$  k $\Omega$ , the maximum value of  $V_p$  for undistorted sine-wave output is 1.3 V. The output will be a 13-V peak sine wave, and the op-amp output current at the peaks will be 14.3 mA.

**Example 2.7** *continued*

- (d) For  $V_p = 1$  V and  $R_L$  reduced, the lowest value possible for  $R_L$  while the output is remaining an undistorted sine wave of 10-V peak can be found from

$$i_{O\max} = 20 \text{ mA} = \frac{10 \text{ V}}{R_{L\min}} + \frac{10 \text{ V}}{9 \text{ k}\Omega + 1 \text{ k}\Omega}$$

which results in

$$R_{L\min} = 526 \text{ }\Omega$$

### 2.8.3 Slew Rate

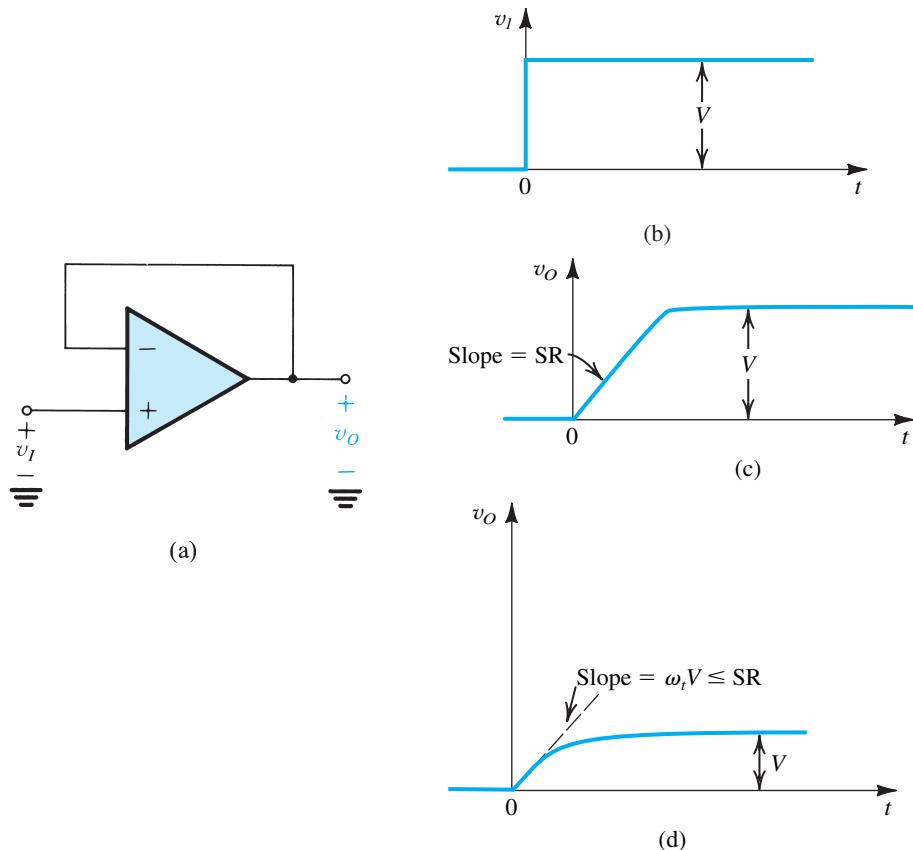
Another phenomenon that can cause nonlinear distortion when large output signals are present is slew-rate limiting. The name refers to the fact that there is a specific *maximum rate of change* possible at the output of a real op amp. This maximum is known as the **slew rate** (SR) of the op amp and is defined as

➤  $\text{SR} = \left. \frac{dv_o}{dt} \right|_{\max}$  (2.56)

and is usually specified on the op-amp data sheet in units of  $\text{V}/\mu\text{s}$ . It follows that if the input signal applied to an op-amp circuit is such that it demands an output response that is faster than the specified value of SR, the op amp will not comply. Rather, its output will change at the maximum possible rate, which is equal to its SR. As an example, consider an op amp connected in the unity-gain voltage-follower configuration shown in Fig. 2.43(a), and let the input signal be the step voltage shown in Fig. 2.43(b). The output of the op amp will not be able to rise instantaneously to the ideal value  $V$ ; rather, the output will be the linear ramp of slope equal to SR, shown in Fig. 2.43(c). The amplifier is then said to be **slewing**, and its output is **slew-rate limited**.

In order to understand the origin of the slew-rate phenomenon, we need to know about the internal circuit of the op amp, and we will study it in Chapter 13. For the time being, however, it is sufficient to know about the phenomenon and to note that it is distinct from the finite op-amp bandwidth that limits the frequency response of the closed-loop amplifiers, studied in the previous section. The limited bandwidth is a linear phenomenon and does not result in a change in the shape of an input sinusoid; that is, it does not lead to nonlinear distortion. The slew-rate limitation, on the other hand, can cause nonlinear distortion to an input sinusoidal signal when its frequency and amplitude are such that the corresponding ideal output would require  $v_o$  to change at a rate greater than SR. This is the origin of another related op-amp specification, its full-power bandwidth, to be explained later.

Before leaving the example in Fig. 2.43, however, we should point out that if the step input voltage  $V$  is sufficiently small, the output can be the exponentially rising ramp shown



**Figure 2.43** (a) Unity-gain follower. (b) Input step waveform. (c) Linearly rising output waveform obtained when the amplifier is slew-rate limited. (d) Exponentially rising output waveform obtained when  $V$  is sufficiently small so that the initial slope ( $\omega_t V$ ) is smaller than or equal to SR.

in Fig. 2.43(d). Such an output would be expected from the follower if the only limitation on its dynamic performance were the finite op-amp bandwidth. Specifically, the transfer function of the follower can be found by substituting  $R_1 = \infty$  and  $R_2 = 0$  in Eq. (2.55) to obtain

$$\frac{V_o}{V_i} = \frac{1}{1 + s/\omega_t} \quad (2.57)$$

which is a low-pass STC response with a time constant  $1/\omega_t$ . Its step response would therefore be (see Appendix E)

$$v_o(t) = V(1 - e^{-\omega_t t}) \quad (2.58)$$

The initial slope of this exponentially rising function is  $(\omega_t V)$ . Thus, as long as  $V$  is sufficiently small so that  $\omega_t V \leq SR$ , the output will be as in Fig. 2.43(d).

## EXERCISE

- 2.29** An op amp that has a slew rate of  $1 \text{ V}/\mu\text{s}$  and a unity-gain bandwidth  $f_t$  of 1 MHz is connected in the unity-gain follower configuration. Find the largest possible input voltage step for which the output waveform will still be given by the exponential ramp of Eq. (2.58). For this input voltage, what is the 10% to 90% rise time of the output waveform? If an input step 10 times as large is applied, find the 10% to 90% rise time of the output waveform.

**Ans.** 0.16 V;  $0.35 \mu\text{s}$ ;  $1.28 \mu\text{s}$

### 2.8.4 Full-Power Bandwidth

Op-amp slew-rate limiting can cause nonlinear distortion in sinusoidal waveforms. Consider once more the unity-gain follower with a sine-wave input given by

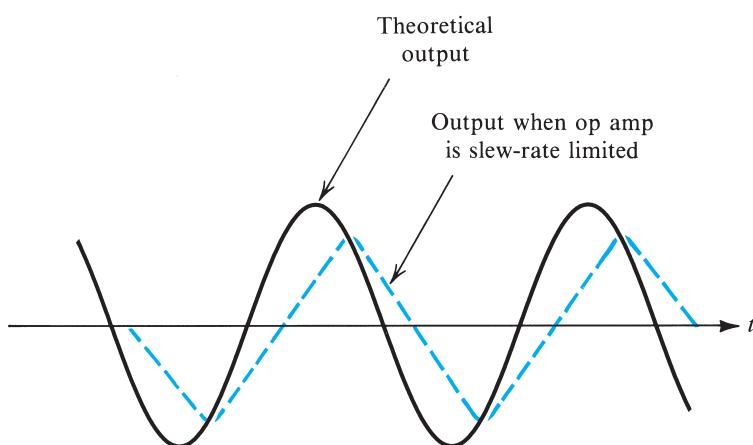
$$v_I = \hat{V}_i \sin \omega t$$

The rate of change of this waveform is given by

$$\frac{dv_I}{dt} = \omega \hat{V}_i \cos \omega t$$

with a maximum value of  $\omega \hat{V}_i$ . This maximum occurs at the zero crossings of the input sinusoid. Now if  $\omega \hat{V}_i$  exceeds the slew rate of the op amp, the output waveform will be distorted in the manner shown in Fig. 2.44. Observe that the output cannot keep up with the large rate of change of the sinusoid at its zero crossings, and the op amp slews.

The op-amp data sheets usually specify a frequency  $f_M$  called the **full-power bandwidth**. It is the frequency at which an output sinusoid with amplitude equal to the rated output voltage of the op amp begins to show distortion due to slew-rate limiting. If we denote the rated output



**Figure 2.44** Effect of slew-rate limiting on output sinusoidal waveforms.

voltage  $V_{o\max}$ , then  $f_M$  is related to SR as follows:

$$\omega_M V_{o\max} = \text{SR}$$

Thus,

$$f_M = \frac{\text{SR}}{2\pi V_{o\max}} \quad (2.59)$$

It should be obvious that output sinusoids of amplitudes smaller than  $V_{o\max}$  will show slew-rate distortion at frequencies higher than  $\omega_M$ . In fact, at a frequency  $\omega$  higher than  $\omega_M$ , the maximum amplitude of the undistorted output sinusoid is given by

$$V_o = V_{o\max} \left( \frac{\omega_M}{\omega} \right) \quad (2.60)$$

### EXERCISE

- 2.30** An op amp has a rated output voltage of  $\pm 10$  V and a slew rate of  $1 \text{ V}/\mu\text{s}$ . What is its full-power bandwidth? If an input sinusoid with frequency  $f = 5f_M$  is applied to a unity-gain follower constructed using this op amp, what is the maximum possible amplitude that can be accommodated at the output without incurring SR distortion?

**Ans.** 15.9 kHz; 2 V (peak)

## Summary

- The IC op amp is a versatile circuit building block. It is easy to apply, and the performance of op-amp circuits closely matches theoretical predictions.
- The op-amp terminals are the inverting input terminal (1), the noninverting input terminal (2), the output terminal (3), the positive-supply terminal (4) to be connected to the positive power supply ( $V_{CC}$ ), and the negative-supply terminal (5) to be connected to the negative supply ( $-V_{EE}$ ). The common terminal of the two supplies is the circuit ground.
- The ideal op amp responds only to the difference input signal, that is,  $(v_2 - v_1)$ ; it provides at the output, between terminal 3 and ground, a signal  $A(v_2 - v_1)$ , where  $A$ , the open-loop gain, is very large ( $10^4$  to  $10^6$ ) and ideally infinite; and it has an infinite input resistance and a zero output resistance. (See Table 2.1.)
- Negative feedback is applied to an op amp by connecting a passive component between its output terminal and its inverting (negative) input terminal. Negative feedback causes the voltage between the two input terminals to become very small and ideally zero. Correspondingly, a virtual short circuit is said to exist between the two input terminals. If the positive input terminal is connected to ground, a virtual ground appears on the negative input terminal.
- The two most important assumptions in the analysis of op-amp circuits, presuming negative feedback exists and the op amps are ideal, are as follows: the two input terminals of the op amp are at the same voltage, and zero current flows into the op-amp input terminals.
- With negative feedback applied and the loop closed, the closed-loop gain is almost entirely determined by external components: For the inverting configuration,  $V_o/V_i = -R_2/R_1$ ; and for the noninverting configuration,  $V_o/V_i = 1 + R_2/R_1$ .
- The noninverting closed-loop configuration features a very high input resistance. A special case is the unity-gain

follower, frequently employed as a buffer amplifier to connect a high-resistance source to a low-resistance load.

- The difference amplifier of Fig. 2.16 is designed with  $R_4/R_3 = R_2/R_1$ , resulting in  $v_o = (R_2/R_1)(v_{I2} - v_{I1})$ .
- The instrumentation amplifier of Fig. 2.20(b) is a very popular circuit. It provides  $v_o = (1 + R_2/R_1)(R_4/R_3)(v_{I2} - v_{I1})$ . It is usually designed with  $R_3 = R_4$ , and  $R_1$  and  $R_2$  selected to provide the required gain. If an adjustable gain is needed, part of  $R_1$  can be made variable.
- The inverting Miller integrator of Fig. 2.24(a) is a popular circuit, frequently employed in analog signal-processing functions such as filters (Chapter 17) and oscillators (Chapter 18).
- The input offset voltage,  $V_{os}$ , is the magnitude of dc voltage that when applied between the op-amp input terminals, with appropriate polarity, reduces the dc offset voltage at the output to zero.
- The effect of  $V_{os}$  on performance can be evaluated by including in the analysis a dc source  $V_{os}$  in series with the op-amp positive input lead. For both the inverting and the noninverting configurations,  $V_{os}$  results in a dc offset voltage at the output of  $V_{os}(1 + R_2/R_1)$ .
- Capacitively coupling an op amp reduces the dc offset voltage at the output considerably.
- The average of the two dc currents,  $I_{B1}$  and  $I_{B2}$ , that flow in the input terminals of the op amp, is called the

input bias current,  $I_B$ . In a closed-loop amplifier,  $I_B$  gives rise to a dc offset voltage at the output of magnitude  $I_B R_2$ . This voltage can be reduced to  $I_{os} R_2$  by connecting a resistance in series with the positive input terminal equal to the total dc resistance seen by the negative input terminal.  $I_{os}$  is the input offset current; that is,  $I_{os} = |I_{B1} - I_{B2}|$ .

- Connecting a large resistance in parallel with the capacitor of an op-amp inverting integrator prevents op-amp saturation (due to the effect of  $V_{os}$  and  $I_B$ ).
- For most internally compensated op amps, the open-loop gain falls off with frequency at a rate of  $-20 \text{ dB/decade}$ , reaching unity at a frequency  $f_t$  (the unity-gain bandwidth). Frequency  $f_t$  is also known as the gain-bandwidth product of the op amp:  $f_t = A_0 f_b$ , where  $A_0$  is the dc gain, and  $f_b$  is the 3-dB frequency of the open-loop gain. At any frequency  $f$  ( $f \gg f_b$ ), the op-amp gain  $|A| \approx f_t/f$ .
- For both the inverting and the noninverting closed-loop configurations, the 3-dB frequency is equal to  $f_t/(1 + R_2/R_1)$ .
- The maximum rate at which the op-amp output voltage can change is called the slew rate. The slew rate, SR, is usually specified in  $\text{V}/\mu\text{s}$ . Op-amp slewing can result in nonlinear distortion of output signal waveforms.
- The full-power bandwidth,  $f_M$ , is the maximum frequency at which an output sinusoid with an amplitude equal to the op-amp rated output voltage ( $V_{o\max}$ ) can be produced without distortion:  $f_M = \text{SR}/2\pi V_{o\max}$ .

## PROBLEMS

### Computer Simulation Problems

**SIM** Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSPice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified

in the problem statement, you are to make a reasonable assumption.

### Section 2.1: The Ideal Op Amp

**2.1** What is the minimum number of pins required for a so-called dual-op-amp IC package, one containing two op amps? What is the number of pins required for a so-called quad-op-amp package, one containing four op-amps?

- 2.2** The circuit of Fig. P2.2 uses an op amp that is ideal except for having a finite gain  $A$ . Measurements indicate  $v_o = 4.0$  V when  $v_i = 1.0$  V. What is the op-amp gain  $A$ ?

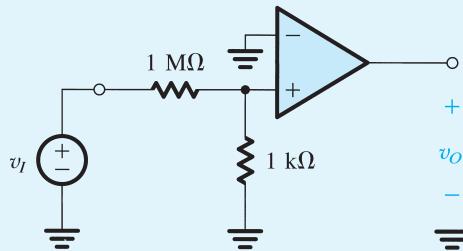


Figure P2.2

- 2.3** Measurement of a circuit incorporating what is thought to be an ideal op amp shows the voltage at the op-amp output to be  $-2.000$  V and that at the negative input to be  $-1.000$  V. For the amplifier to be ideal, what would you expect the voltage at the positive input to be? If the measured voltage at the positive input is  $-1.005$  V, what is likely to be the actual gain of the amplifier?

- 2.4** A set of experiments is run on an op amp that is ideal except for having a finite gain  $A$ . The results are tabulated below. Are the results consistent? If not, are they reasonable, in view of the possibility of experimental error? What do they show the gain to be? Using this value, predict values of the measurements that were accidentally omitted (the blank entries).

Experiment #	$v_1$	$v_2$	$v_o$
1	0.00	0.00	0.00
2	1.00	1.00	0.00
3		1.00	1.00
4	1.00	1.10	10.1
5	2.01	2.00	-0.99
6	1.99	2.00	1.00
7	5.10		-5.10

- 2.5** Refer to Exercise 2.3. This problem explores an alternative internal structure for the op amp. In particular, we wish to model the internal structure of a particular op amp using two transconductance amplifiers and one transresistance amplifier. Suggest an appropriate topology.

For equal transconductances  $G_m$  and a transresistance  $R_m$ , find an expression for the open-loop gain  $A$ . For  $G_m = 40$  mA/V and  $R_m = 1 \times 10^6 \Omega$ , what value of  $A$  results?

- 2.6** The two wires leading from the output terminals of a transducer pick up an interference signal that is a 60-Hz, 2-V sinusoid. The output signal of the transducer is sinusoidal of 5-mV amplitude and 1000-Hz frequency. Give expressions for  $v_{cm}$ ,  $v_d$ , and the total signal between each wire and the system ground.

- 2.7** Nonideal (i.e., real) operational amplifiers respond to both the differential and common-mode components of their input signals (refer to Fig. 2.4 for signal representation). Thus the output voltage of the op amp can be expressed as

$$v_o = A_d v_{ld} + A_{cm} v_{lcm}$$

where  $A_d$  is the differential gain (referred to simply as  $A$  in the text) and  $A_{cm}$  is the common-mode gain (assumed to be zero in the text). The op amp's effectiveness in rejecting common-mode signals is measured by its CMRR, defined as

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

Consider an op amp whose internal structure is of the type shown in Fig. E2.3 except for a mismatch  $\Delta G_m$  between the transconductances of the two channels; that is,

$$G_{m1} = G_m - \frac{1}{2} \Delta G_m$$

$$G_{m2} = G_m + \frac{1}{2} \Delta G_m$$

Find expressions for  $A_d$ ,  $A_{cm}$ , and CMRR. What is the maximum permitted percentage mismatch between the two  $G_m$  values if a minimum CMRR of 60 dB is required?

## Section 2.2: The Inverting Configuration

- 2.8** Assuming ideal op amps, find the voltage gain  $v_o/v_i$  and input resistance  $R_{in}$  of each of the circuits in Fig. P2.8.

- 2.9** A particular inverting circuit uses an ideal op amp and two  $10\text{-k}\Omega$  resistors. What closed-loop gain would you expect? If a dc voltage of  $+1.00$  V is applied at the input, what outputs result? If the  $10\text{-k}\Omega$  resistors are said to be “1% resistors,” having values somewhere in the range  $(1 \pm 0.01)$  times the nominal value, what range of outputs would you expect to actually measure for an input of precisely  $1.00$  V?

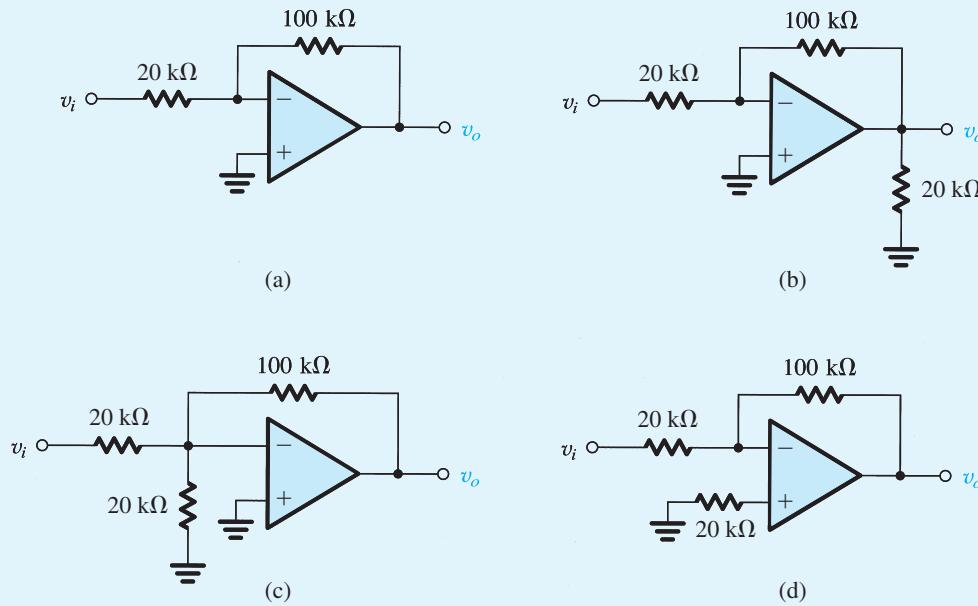


Figure P2.8

**2.10** You are provided with an ideal op amp and three 10-k $\Omega$  resistors. Using series and parallel resistor combinations, how many different inverting-amplifier circuit topologies are possible? What is the largest (noninfinite) available voltage gain magnitude? What is the smallest (nonzero) available gain magnitude? What are the input resistances in these two cases?

**SIM 2.11** For ideal op amps operating with the following feedback networks in the inverting configuration, what closed-loop gain results?

- (a)  $R_1 = 10 \text{ k}\Omega, R_2 = 10 \text{ k}\Omega$
- (b)  $R_1 = 10 \text{ k}\Omega, R_2 = 100 \text{ k}\Omega$
- (c)  $R_1 = 10 \text{ k}\Omega, R_2 = 1 \text{ k}\Omega$
- (d)  $R_1 = 100 \text{ k}\Omega, R_2 = 10 \text{ M}\Omega$
- (e)  $R_1 = 100 \text{ k}\Omega, R_2 = 1 \text{ M}\Omega$

**D 2.12** Given an ideal op amp, what are the values of the resistors  $R_1$  and  $R_2$  to be used to design amplifiers with the closed-loop gains listed below? In your designs, use at least one 10-k $\Omega$  resistor and another equal or larger resistor.

- (a)  $-1 \text{ V/V}$
- (b)  $-2 \text{ V/V}$

- (c)  $-5 \text{ V/V}$
- (d)  $-100 \text{ V/V}$

**D 2.13** Design an inverting op-amp circuit for which the gain is  $-10 \text{ V/V}$  and the total resistance used is 110 k $\Omega$ .

**D 2.14** Using the circuit of Fig. 2.5 and assuming an ideal op amp, design an inverting amplifier with a gain of 46 dB having the largest possible input resistance under the constraint of having to use resistors no larger than 1 M $\Omega$ . What is the input resistance of your design?

**2.15** An ideal op amp is connected as shown in Fig. 2.5 with  $R_1 = 10 \text{ k}\Omega$  and  $R_2 = 100 \text{ k}\Omega$ . A symmetrical square-wave signal with levels of 0 V and  $-1 \text{ V}$  is applied at the input. Sketch and clearly label the waveform of the resulting output voltage. What is its average value? What is its highest value? What is its lowest value?

**2.16** For the circuit in Fig. P2.16, assuming an ideal op amp, find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?

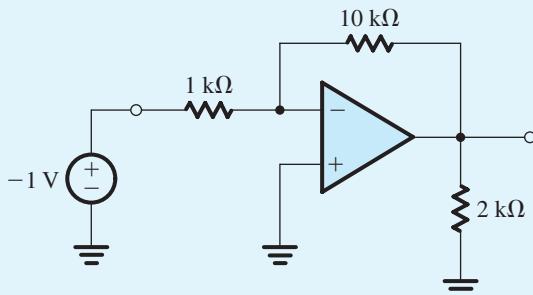


Figure P2.16

**2.17** An inverting op-amp circuit is fabricated with the resistors  $R_1$  and  $R_2$  having  $x\%$  tolerance (i.e., the value of each resistance can deviate from the nominal value by as much as  $\pm x\%$ ). What is the tolerance on the realized closed-loop gain? Assume the op amp to be ideal. If the nominal closed-loop gain is  $-100 \text{ V/V}$  and  $x = 1$ , what is the range of gain values expected from such a circuit?

**2.18** An ideal op amp with  $5\text{-k}\Omega$  and  $15\text{-k}\Omega$  resistors is used to create a  $+5\text{-V}$  supply from a  $-15\text{-V}$  reference. Sketch the circuit. What are the voltages at the ends of the  $5\text{-k}\Omega$  resistor? If these resistors are so-called  $1\%$  resistors, whose actual values are the range bounded by the nominal value  $\pm 1\%$ , what are the limits of the output voltage produced? If the  $-15\text{-V}$  supply can also vary by  $\pm 1\%$ , what is the range of the output voltages that might be found?

**2.19** An inverting op-amp circuit for which the required gain is  $-50 \text{ V/V}$  uses an op amp whose open-loop gain is only  $500 \text{ V/V}$ . If the larger resistor used is  $100 \text{k}\Omega$ , to what must the smaller be adjusted? With what resistor must a  $2\text{-k}\Omega$  resistor connected to the input be shunted to achieve this goal? (Note that a resistor  $R_a$  is said to be shunted by resistor  $R_b$  when  $R_b$  is placed in parallel with  $R_a$ .)

- D 2.20** (a) Design an inverting amplifier with a closed-loop gain of  $-200 \text{ V/V}$  and an input resistance of  $1 \text{k}\Omega$ .  
 (b) If the op amp is known to have an open-loop gain of  $5000 \text{ V/V}$ , what do you expect the closed-loop gain of your circuit to be (assuming the resistors have precise values)?  
 (c) Give the value of a resistor you can place in parallel (shunt) with  $R_1$  to restore the closed-loop gain to its nominal value. Use the closest standard  $1\%$  resistor value (see Appendix J).

**2.21** An op amp with an open-loop gain of  $5000 \text{ V/V}$  is used in the inverting configuration. If in this application the output

voltage ranges from  $-10 \text{ V}$  to  $+10 \text{ V}$ , what is the maximum voltage by which the “virtual ground node” departs from its ideal value?

**2.22** The circuit in Fig. P2.22 is frequently used to provide an output voltage  $v_o$  proportional to an input signal current  $i_i$ .

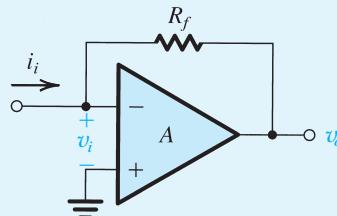


Figure P2.22

Derive expressions for the transresistance  $R_m \equiv v_o/i_i$  and the input resistance  $R_i \equiv v_i/i_i$  for the following cases:

- (a)  $A$  is infinite.  
 (b)  $A$  is finite.

**2.23** Show that for the inverting amplifier if the op-amp gain is  $A$ , the input resistance is given by

$$R_{in} = R_1 + \frac{R_2}{A+1}$$

**2.24** For an inverting amplifier with nominal closed-loop gain  $R_2/R_1$ , find the minimum value that the op-amp open-loop gain  $A$  must have (in terms of  $R_2/R_1$ ) so that the gain error (due to the finite  $A$ ) is limited to  $0.1\%$ ,  $1\%$ , and  $10\%$ . In each case find the value of a resistor  $R_{la}$  such that when it is placed in shunt with  $R_1$ , the gain is restored to its nominal value.

**\*2.25** Figure P2.25 shows an op amp that is ideal except for having a finite open-loop gain and is used to realize an inverting amplifier whose gain has a nominal magnitude  $G = R_2/R_1$ . To compensate for the gain reduction due to

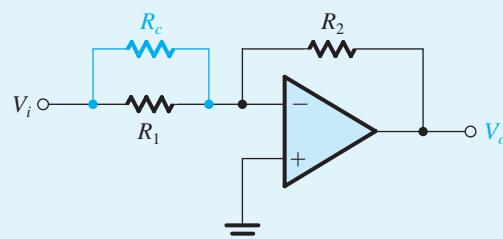


Figure P2.25

the finite  $A$ , a resistor  $R_c$  is shunted across  $R_1$ . Show that perfect compensation is achieved when  $R_c$  is selected according to

$$\frac{R_c}{R_1} = \frac{A - G}{1 + G}$$

**D \*2.26** (a) Use Eq. (2.5) to obtain the amplifier open-loop gain  $A$  required to realize a specified closed-loop gain ( $G_{\text{nominal}} = -R_2/R_1$ ) within a specified gain error  $\epsilon$ ,

$$\epsilon \equiv \left| \frac{G - G_{\text{nominal}}}{G_{\text{nominal}}} \right|$$

(b) Design an inverting amplifier for a nominal closed-loop gain of  $-100$ , an input resistance of  $1 \text{ k}\Omega$ , and a gain error of  $\leq 10\%$ . Specify  $R_1$ ,  $R_2$ , and the minimum  $A$  required.

**\*2.27** (a) Use Eq. (2.5) to show that a reduction  $\Delta A$  in the op-amp gain  $A$  gives rise to a reduction  $\Delta|G|$  in the magnitude of the closed-loop gain  $G$  with  $\Delta|G|$  and  $\Delta A$  related by

$$\frac{\Delta|G|/|G|}{\Delta A/A} \simeq \frac{1 + R_2/R_1}{A}$$

Assume that  $\left(1 + \frac{R_2}{R_1}\right) \ll A$  and  $\frac{\Delta A}{A} \ll 1$ .

(b) If in a closed-loop amplifier with a nominal gain (i.e.,  $R_2/R_1$ ) of  $100$ ,  $A$  decreases by  $10\%$ , what is the minimum nominal  $A$  required to limit the percentage change in  $|G|$  to  $0.1\%$ ?

**2.28** Consider the circuit in Fig. 2.8 with  $R_1 = R_2 = R_4 = 1 \text{ M}\Omega$ , and assume the op amp to be ideal. Find values for  $R_3$  to obtain the following gains:

- (a)  $-100 \text{ V/V}$
- (b)  $-10 \text{ V/V}$
- (c)  $-2 \text{ V/V}$

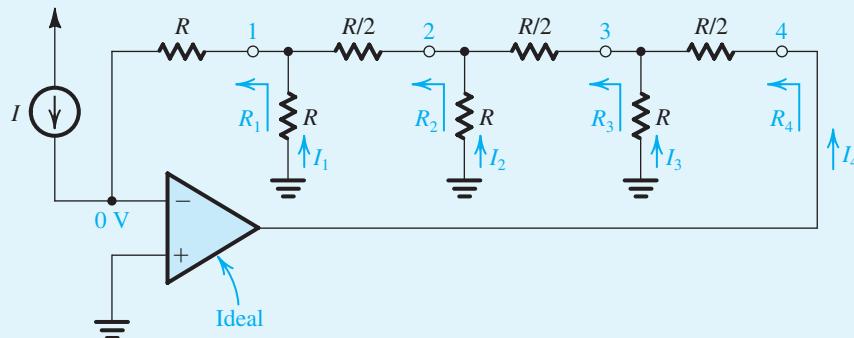


Figure P2.31

**D 2.29** An inverting op-amp circuit using an ideal op amp must be designed to have a gain of  $-500 \text{ V/V}$  using resistors no larger than  $100 \text{ k}\Omega$ .

- (a) For the simple two-resistor circuit, what input resistance would result?
- (b) If the circuit in Fig. 2.8 is used with three resistors of maximum value, what input resistance results? What is the value of the smallest resistor needed?

**2.30** The inverting circuit with the T network in the feedback is redrawn in Fig. P2.30 in a way that emphasizes the observation that  $R_2$  and  $R_3$  in effect are in parallel (because the ideal op amp forces a virtual ground at the inverting input terminal). Use this observation to derive an expression for the gain  $(v_o/v_i)$  by first finding  $(v_x/v_i)$  and  $(v_o/v_x)$ . For the latter use the voltage-divider rule applied to  $R_4$  and  $(R_2 \parallel R_3)$ .

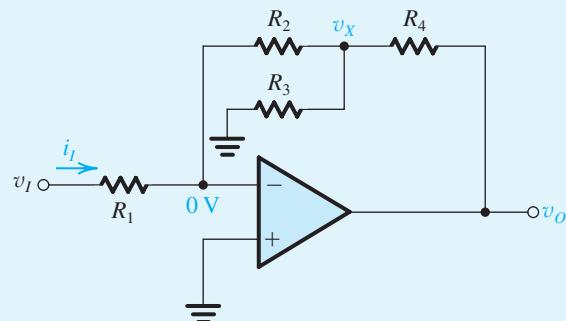


Figure P2.30

**\*2.31** The circuit in Fig. P2.31 can be considered to be an extension of the circuit in Fig. 2.8.

- (a) Find the resistances looking into node 1,  $R_1$ ; node 2,  $R_2$ ; node 3,  $R_3$ ; and node 4,  $R_4$ .

- (b) Find the currents  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_4$ , in terms of the input current  $i_I$ .
- (c) Find the voltages at nodes 1, 2, 3, and 4, that is,  $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$  in terms of  $(IR)$ .

**2.32** The circuit in Fig. P2.32 utilizes an ideal op amp.

- (a) Find  $I_1$ ,  $I_2$ ,  $I_3$ ,  $I_L$ , and  $V_x$ .
- (b) If  $V_o$  is not to be lower than  $-13$  V, find the maximum allowed value for  $R_L$ .
- (c) If  $R_L$  is varied in the range  $100\ \Omega$  to  $1\ k\Omega$ , what is the corresponding change in  $I_L$  and in  $V_o$ ?

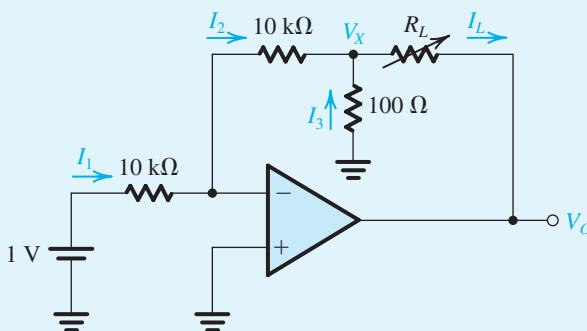


Figure P2.32

**D 2.33** Use the circuit in Fig. P2.32 as an inspiration to design a circuit that supplies a constant current  $I_L$  of  $3.1\text{ mA}$  to a variable resistance  $R_L$ . Assume the availability of a  $1.5\text{-V}$  battery and design so that the current drawn from the battery is  $0.1\text{ mA}$ . For the smallest resistance in the circuit, use  $500\ \Omega$ . If the op amp saturates at  $\pm 10\text{ V}$ , what is the maximum value that  $R_L$  can have while the current source supplying it operates properly?

**D 2.34** Assuming the op amp to be ideal, it is required to design the circuit shown in Fig. P2.34 to implement a current amplifier with gain  $i_L/i_I = 11\text{ A/A}$ .

- (a) Find the required value for  $R$ .
- (b) What are the input and the output resistance of this current amplifier?
- (c) If  $R_L = 1\ k\Omega$  and the op amp operates in an ideal manner as long as  $v_o$  is in the range  $\pm 12\text{ V}$ , what range of  $i_I$  is possible?
- (d) If the amplifier is fed with a current source having a current of  $0.2\text{ mA}$  and a source resistance of  $10\text{k}\Omega$ , find  $i_L$ .

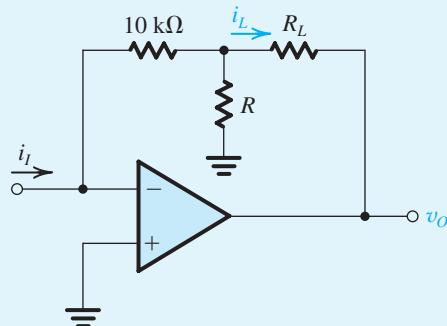


Figure P2.34

**D 2.35** Design the circuit shown in Fig. P2.35 to have an input resistance of  $100\text{ k}\Omega$  and a gain that can be varied from  $-1\text{ V/V}$  to  $-100\text{ V/V}$  using the  $100\text{-k}\Omega$  potentiometer  $R_4$ . What voltage gain results when the potentiometer is set exactly at its middle value?

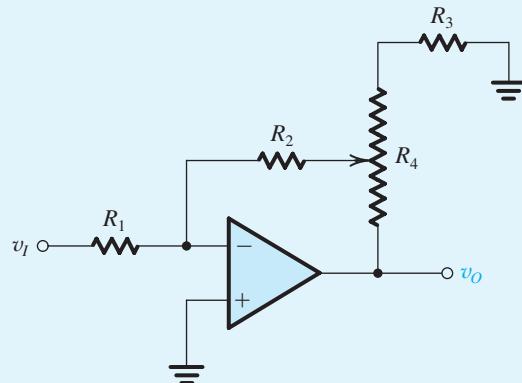


Figure P2.35

**2.36** A weighted summer circuit using an ideal op amp has three inputs using  $10\text{-k}\Omega$  resistors and a feedback resistor of  $50\text{ k}\Omega$ . A signal  $v_1$  is connected to two of the inputs while a signal  $v_2$  is connected to the third. Express  $v_o$  in terms of  $v_1$  and  $v_2$ . If  $v_1 = 1\text{ V}$  and  $v_2 = -1\text{ V}$ , what is  $v_o$ ?

**D 2.37** Design an op-amp circuit to provide an output  $v_o = -[2v_1 + (v_2/2)]$ . Choose relatively low values of resistors but ones for which the input current (from each input signal source) does not exceed  $50\ \mu\text{A}$  for  $1\text{-V}$  input signals.

**D 2.38** Use the scheme illustrated in Fig. 2.10 to design an op-amp circuit with inputs  $v_1$ ,  $v_2$ , and  $v_3$ , whose output is

$v_o = -(2v_1 + 4v_2 + 8v_3)$  using small resistors but no smaller than  $1\text{ k}\Omega$ .

**D 2.39** An ideal op amp is connected in the weighted summer configuration of Fig. 2.10. The feedback resistor  $R_f = 100\text{ k}\Omega$ , and six  $100\text{-k}\Omega$  resistors are connected to the inverting input terminal of the op amp. Show, by sketching the various circuit configurations, how this basic circuit can be used to implement the following functions:

- $v_o = -(v_1 + 2v_2 + 3v_3)$
- $v_o = -(v_1 + v_2 + 2v_3 + 2v_4)$
- $v_o = -(v_1 + 5v_2)$
- $v_o = -6v_1$

In each case find the input resistance seen by each of the signal sources supplying  $v_1$ ,  $v_2$ ,  $v_3$ , and  $v_4$ . Suggest at least two additional summing functions that you can realize with this circuit. How would you realize a summing coefficient that is 0.5?

**D 2.40** Give a circuit, complete with component values, for a weighted summer that shifts the dc level of a sine-wave signal of  $3 \sin(\omega t)$  V from zero to  $-3$  V. Assume that in addition to the sine-wave signal you have a dc reference voltage of  $1.5$  V available. Sketch the output signal waveform.

**D 2.41** Use two ideal op amps and resistors to implement the summing function

$$v_o = v_1 + 2v_2 - 3v_3 - 5v_4$$

**D 2.42** In an instrumentation system, there is a need to take the difference between two signals, one of  $v_1 = 2 \sin(2\pi \times 60t) + 0.01 \sin(2\pi \times 1000t)$  volts and another of  $v_2 = 2 \sin(2\pi \times 60t) - 0.01 \sin(2\pi \times 1000t)$  volts. Draw a circuit that finds the required difference using two op amps and mainly  $100\text{-k}\Omega$  resistors. Since it is desirable to amplify the 1000-Hz component in the process, arrange to provide an overall gain of 100 as well. The op amps available are ideal except that their output voltage swing is limited to  $\pm 10$  V.

**\*2.43** Figure P2.43 shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary word  $a_3a_2a_1a_0$ , where  $a_0$ ,  $a_1$ ,  $a_2$ , and  $a_3$  take the values of 0 or 1, and it provides an analog output voltage  $v_o$  proportional to the value of the digital input. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if  $a_2$  is 0 then switch  $S_2$  connects the  $20\text{-k}\Omega$  resistor to ground, while if  $a_2$  is 1 then  $S_2$  connects the  $20\text{-k}\Omega$  resistor to the  $+5\text{-V}$

power supply. Show that  $v_o$  is given by

$$v_o = -\frac{R_f}{16} [2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3]$$

where  $R_f$  is in kilohms. Find the value of  $R_f$  so that  $v_o$  ranges from 0 to  $-12$  volts.

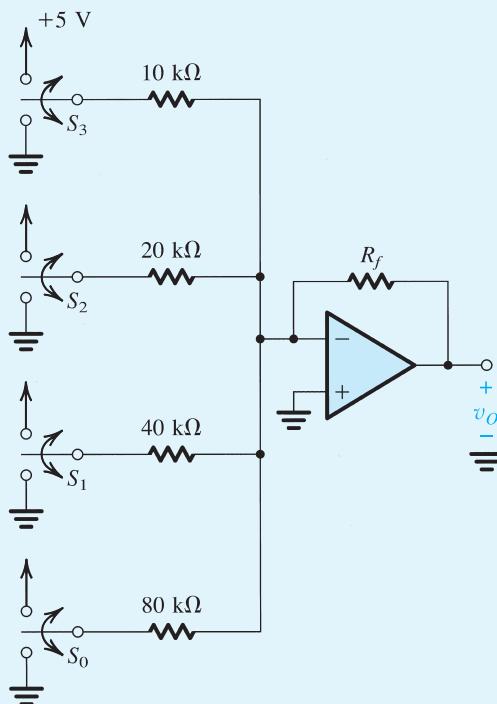


Figure P2.43

### Section 2.3: The Noninverting Configuration

**D 2.44** Given an ideal op amp to implement designs for the following closed-loop gains, what values of resistors ( $R_1$ ,  $R_2$ ) should be used? Where possible, use at least one  $10\text{-k}\Omega$  resistor as the smallest resistor in your design.

- $+1\text{ V/V}$
- $+2\text{ V/V}$
- $+21\text{ V/V}$
- $+100\text{ V/V}$

**D 2.45** Design a circuit based on the topology of the noninverting amplifier to obtain a gain of  $+1.5\text{ V/V}$ , using only  $10\text{-k}\Omega$  resistors. Note that there are two possibilities. Which of these can be easily converted to have a gain of

either +1.0 V/V or +2.0 V/V simply by short-circuiting a single resistor in each case?

**D 2.46** Figure P2.46 shows a circuit for an analog voltmeter of very high input resistance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage  $V$  applied between the op amp's positive-input terminal and ground. Assuming that the moving coil produces full-scale deflection when the current passing through it is  $100 \mu\text{A}$ , find the value of  $R$  such that a full-scale reading is obtained when  $V$  is +10 V. Does the meter resistance shown affect the voltmeter calibration?

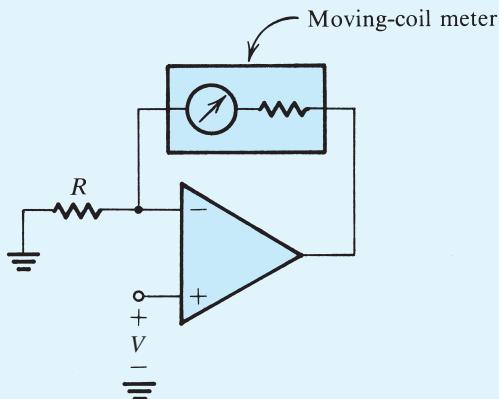


Figure P2.46

**D \*2.47** (a) Use superposition to show that the output of the circuit in Fig. P2.47 is given by

$$v_o = \left[ \frac{R_f}{R_{N1}} v_{N1} + \frac{R_f}{R_{N2}} v_{N2} + \cdots + \frac{R_f}{R_{Nn}} v_{Nn} \right] + \left[ 1 + \frac{R_f}{R_N} \right] \left[ \frac{R_p}{R_{P1}} v_{P1} + \frac{R_p}{R_{P2}} v_{P2} + \cdots + \frac{R_p}{R_{Pn}} v_{Pn} \right]$$

where  $R_N = R_{N1} \parallel R_{N2} \parallel \cdots \parallel R_{Nn}$ , and

$$R_p = R_{P1} \parallel R_{P2} \parallel \cdots \parallel R_{Pn} \parallel R_{P0}$$

(b) Design a circuit to obtain

$$v_o = -4v_{N1} + v_{P1} + 3v_{P2}$$

The smallest resistor used should be  $10 \text{k}\Omega$ .

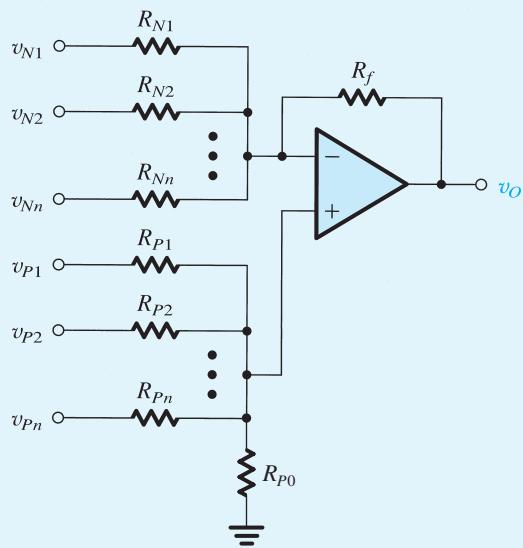


Figure P2.47

**D \*2.48** Design a circuit, using one ideal op amp, whose output is  $v_o = v_{I1} + 2v_{I2} - 9v_{I3} + 4v_{I4}$ . (Hint: Use a structure similar to that shown in general form in Fig. P2.47.)

**2.49** Derive an expression for the voltage gain,  $v_o/v_I$ , of the circuit in Fig. P2.49.

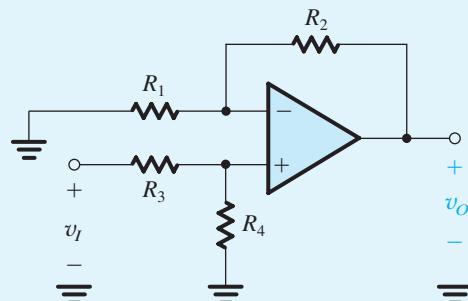


Figure P2.49

**2.50** For the circuit in Fig. P2.50, use superposition to find  $v_o$  in terms of the input voltages  $v_1$  and  $v_2$ . Assume an ideal op amp. For

$$v_1 = 10 \sin(2\pi \times 60t) - 0.1 \sin(2\pi \times 1000t), \text{ volts}$$

$$v_2 = 10 \sin(2\pi \times 60t) + 0.1 \sin(2\pi \times 1000t), \text{ volts}$$

find  $v_o$ .

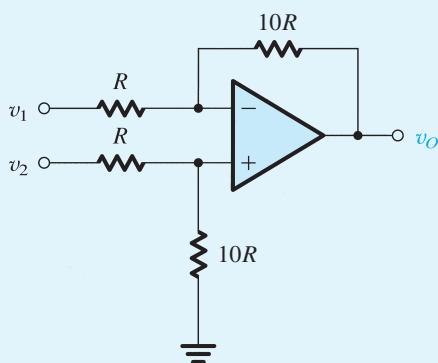


Figure P2.50

**D 2.51** The circuit shown in Fig. P2.51 utilizes a 10-k $\Omega$  potentiometer to realize an adjustable-gain amplifier. Derive an expression for the gain as a function of the potentiometer setting  $x$ . Assume the op amp to be ideal. What is the range of gains obtained? Show how to add a fixed resistor so that the gain range can be 1 to 11 V/V. What should the resistor value be?

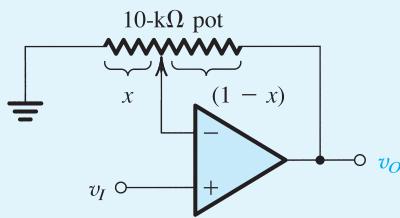


Figure P2.51

**D 2.52** Given the availability of resistors of value 1 k $\Omega$  and 10 k $\Omega$  only, design a circuit based on the noninverting configuration to realize a gain of +10 V/V. What is the input resistance of your amplifier?

**2.53** It is required to connect a 10-V source with a source resistance of 1 M $\Omega$  to a 1-k $\Omega$  load. Find the voltage that will appear across the load if:

- (a) The source is connected directly to the load.
- (b) A unity-gain op-amp buffer is inserted between the source and the load.

In each case find the load current and the current supplied by the source. Where does the load current come from in case (b)?

**2.54** Derive an expression for the gain of the voltage follower of Fig. 2.14, assuming the op amp to be ideal except for having a finite gain  $A$ . Calculate the value of the closed-loop gain for  $A = 1000, 100$ , and  $10$ . In each case find the percentage error in gain magnitude from the nominal value of unity.

**2.55** Complete the following table for feedback amplifiers created using one ideal op amp. Note that  $R_{in}$  signifies input resistance and  $R_1$  and  $R_2$  are feedback-network resistors as labeled in the inverting and noninverting configurations.

Case	Gain	$R_{in}$	$R_1$	$R_2$
a	-10 V/V	10 k $\Omega$		
b	-1 V/V		100 k $\Omega$	
c	-2 V/V			200 k $\Omega$
d	+1 V/V	$\infty$		
e	+2 V/V		100 k $\Omega$	
f	+11 V/V			100 k $\Omega$
g	-0.5 V/V	20 k $\Omega$		

**D 2.56** A noninverting op-amp circuit with nominal gain of 10 V/V uses an op amp with open-loop gain of 100 V/V and a lowest-value resistor of 10 k $\Omega$ . What closed-loop gain actually results? With what value resistor can which resistor be shunted to achieve the nominal gain? If in the manufacturing process, an op amp of gain 200 V/V were used, what closed-loop gain would result in each case (the uncompensated one, and the compensated one)?

**2.57** Use Eq. (2.11) to show that if the reduction in the closed-loop gain  $G$  from the nominal value  $G_0 = 1 + R_2/R_1$  is to be kept less than  $x\%$  of  $G_0$ , then the open-loop gain of the op amp must exceed  $G_0$  by at least a factor  $F = (100/x) - 1 \approx 100/x$ . Find the required  $F$  for  $x = 0.01, 0.1, 1$ , and  $10$ . Utilize these results to find for each value of  $x$  the minimum required open-loop gain to obtain closed-loop gains of 1, 10, 10<sup>2</sup>, 10<sup>3</sup>, and 10<sup>4</sup> V/V.

**2.58** For each of the following combinations of op-amp open-loop gain  $A$  and nominal closed-loop gain  $G_0$ , calculate the actual closed-loop gain  $G$  that is achieved. Also, calculate the percentage by which  $|G|$  falls short of the nominal gain magnitude  $|G_0|$ .

Case	$G_0$ (V/V)	$A$ (V/V)
a	-1	10
b	+1	10
c	-1	100
d	+10	10
e	-10	100
f	-10	1000
g	+1	2

**2.59** Figure P2.59 shows a circuit that provides an output voltage  $v_o$  whose value can be varied by turning the wiper of the 100-k $\Omega$  potentiometer. Find the range over which  $v_o$  can be varied. If the potentiometer is a “20-turn” device, find the change in  $v_o$  corresponding to each turn of the pot.

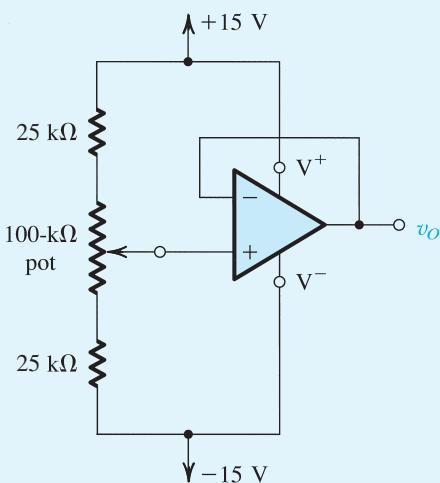


Figure P2.59

### Section 2.4: Difference Amplifiers

**2.60** Find the voltage gain  $v_o/v_{id}$  for the difference amplifier of Fig. 2.16 for the case  $R_1 = R_3 = 5\text{ k}\Omega$  and  $R_2 = R_4 = 100\text{ k}\Omega$ . What is the differential input resistance  $R_{id}$ ? If the two key resistance ratios ( $R_2/R_1$ ) and ( $R_4/R_3$ ) are different from each other by 1%, what do you expect the common-mode gain  $A_{cm}$  to be? Also, find the CMRR in this case. Neglect the effect of the ratio mismatch on the value of  $A_d$ .

**D 2.61** Using the difference amplifier configuration of Fig. 2.16 and assuming an ideal op amp, design the circuit to provide the following differential gains. In each case, the differential input resistance should be 20 k $\Omega$ .

- (a) 1 V/V
- (b) 5 V/V
- (c) 100 V/V
- (d) 0.5 V/V

**2.62** For the circuit shown in Fig. P2.62, express  $v_o$  as a function of  $v_1$  and  $v_2$ . What is the input resistance seen by  $v_1$  alone? By  $v_2$  alone? By a source connected between the two input terminals? By a source connected to both input terminals simultaneously?

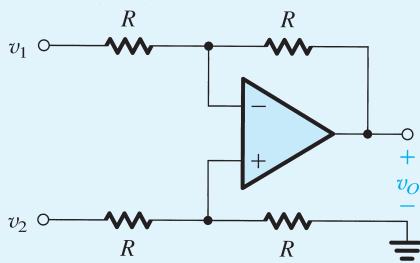


Figure P2.62

**2.63** Consider the difference amplifier of Fig. 2.16 with the two input terminals connected together to an input common-mode signal source. For  $R_2/R_1 = R_4/R_3$ , show that the input common-mode resistance is  $(R_3 + R_4) \parallel (R_1 + R_2)$ .

**2.64** Consider the circuit of Fig. 2.16, and let each of the  $v_{I1}$  and  $v_{I2}$  signal sources have a series resistance  $R_s$ . What condition must apply in addition to the condition in Eq. (2.15) in order for the amplifier to function as an ideal difference amplifier?

**\*2.65** For the difference amplifier shown in Fig. P2.62, let all the resistors be  $10\text{ k}\Omega \pm x\%$ . Find an expression for the worst-case common-mode gain that results. Evaluate this for  $x = 0.1, 1, \text{ and } 5$ . Also, evaluate the resulting CMRR in each case. Neglect the effect of resistor tolerances on  $A_d$ .

**2.66** For the difference amplifier of Fig. 2.16, show that if each resistor has a tolerance of  $\pm 100\epsilon\%$  (i.e., for, say, a 5% resistor,  $\epsilon = 0.05$ ) then the worst-case CMRR is given approximately by

$$\text{CMRR} \simeq 20 \log \left[ \frac{K+1}{4\epsilon} \right]$$

where  $K$  is the nominal (ideal) value of the ratios  $(R_2/R_1)$  and  $(R_4/R_3)$ . Calculate the value of worst-case CMRR for an amplifier designed to have a differential gain of ideally 100 V/V, assuming that the op amp is ideal and that 1% resistors are used. What resistor tolerance is needed if a CMRR of 80 dB is required?

**D \*2.67** Design the difference amplifier circuit of Fig. 2.16 to realize a differential gain of 1000, a differential input resistance of  $2\text{ k}\Omega$ , and a minimum CMRR of 88 dB. Assume the op amp to be ideal. Specify both the resistor values and their required tolerance (e.g., better than  $x\%$ ).

**\*2.68** (a) Find  $A_d$  and  $A_{cm}$  for the difference amplifier circuit shown in Fig. P2.68.

(b) If the op amp is specified to operate properly as long as the common-mode voltage at its positive and negative inputs falls in the range  $\pm 2.5\text{ V}$ , what is the corresponding limitation on the range of the input common-mode signal  $v_{icm}$ ? (This is known as the **common-mode range** of the differential amplifier.)

(c) The circuit is modified by connecting a  $10\text{-k}\Omega$  resistor between node A and ground, and another  $10\text{-k}\Omega$  resistor between node B and ground. What will now be the values of  $A_d$ ,  $A_{cm}$ , and the input common-mode range?

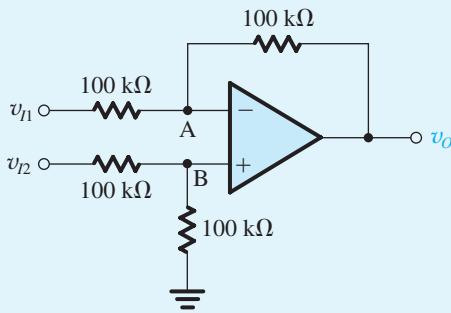


Figure P2.68

**D \*2.69** To obtain a high-gain, high-input-resistance difference amplifier, the circuit in Fig. P2.69 employs positive feedback, in addition to the negative feedback provided by the resistor  $R$  connected from the output to the negative input of the op amp. Specifically, a voltage divider ( $R_5, R_6$ ) connected across the output feeds a fraction  $\beta$  of the output, that is, a voltage  $\beta v_o$ , back to the positive-input terminal of the op amp through a resistor  $R$ . Assume that  $R_5$  and  $R_6$  are much smaller than  $R$  so that the current through  $R$  is much lower than the current in the voltage divider, with the result that

$\beta \simeq R_6/(R_5 + R_6)$ . Show that the differential gain is given by

$$A_d \equiv \frac{v_o}{v_{id}} = \frac{1}{1 - \beta}$$

(Hint: Use superposition.)

Design the circuit to obtain a differential gain of 10 V/V and differential input resistance of  $2\text{ M}\Omega$ . Select values for  $R$ ,  $R_5$ , and  $R_6$ , such that  $(R_5 + R_6) \leq R/100$ .

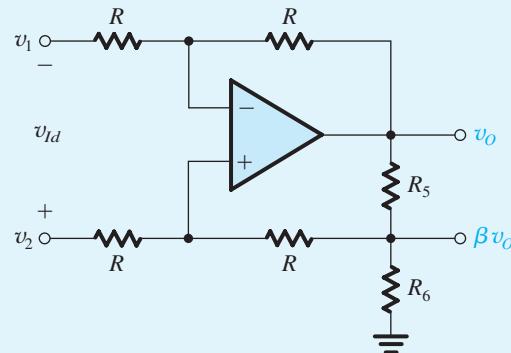


Figure P2.69

**\*2.70** Figure P2.70 shows a modified version of the difference amplifier. The modified circuit includes a resistor  $R_G$ , which can be used to vary the gain. Show that the differential voltage gain is given by

$$\frac{v_o}{v_{id}} = -2 \frac{R_2}{R_1} \left[ 1 + \frac{R_2}{R_G} \right]$$

(Hint: The virtual short circuit at the op-amp input causes the current through the  $R_1$  resistors to be  $v_{id}/2R_1$ ).

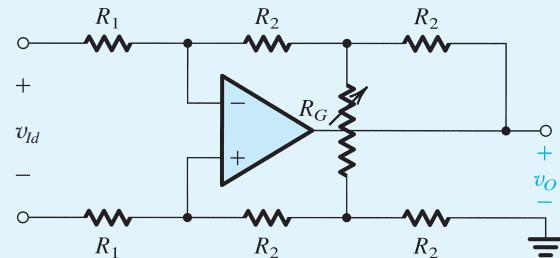


Figure P2.70

**D \*2.71** The circuit shown in Fig. P2.71 is a representation of a versatile, commercially available IC, the INA105, manufactured by Burr-Brown and known as a differential amplifier module. It consists of an op amp and precision, laser-trimmed, metal-film resistors. The circuit can be configured for a variety of applications by the appropriate connection of terminals A, B, C, D, and O.

- (a) Show how the circuit can be used to implement a difference amplifier of unity gain.
- (b) Show how the circuit can be used to implement single-ended amplifiers with gains:
  - (i)  $-1 \text{ V/V}$
  - (ii)  $+1 \text{ V/V}$
  - (iii)  $+2 \text{ V/V}$
  - (iv)  $+1/2 \text{ V/V}$

Avoid leaving a terminal open-circuited, for such a terminal may act as an “antenna,” picking up interference and noise through capacitive coupling. Rather, find a convenient node to connect such a terminal in a redundant way. When more than one circuit implementation is possible, comment on the relative merits of each, taking into account such considerations as dependence on component matching and input resistance.

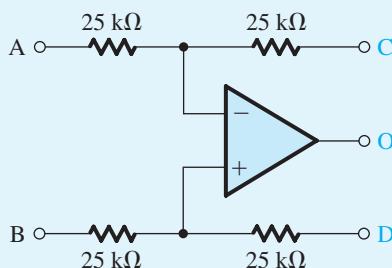


Figure P2.71

**2.72** Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of  $+3 \text{ V}$  (dc) and a differential input signal of  $100\text{-mV}$  peak sine wave. Let  $2R_1 = 2 \text{ k}\Omega$ ,  $R_2 = 50 \text{ k}\Omega$ ,  $R_3 = R_4 = 10 \text{ k}\Omega$ . Find the voltage at every node in the circuit.

**2.73** (a) Consider the instrumentation amplifier circuit of Fig. 2.20(a). If the op amps are ideal except that their outputs saturate at  $\pm 12 \text{ V}$ , in the manner shown in Fig. 1.14, find the maximum allowed input common-mode signal for the case  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 100 \text{ k}\Omega$ .

(b) Repeat (a) for the circuit in Fig. 2.20(b), and comment on the difference between the two circuits.

**2.74** (a) Expressing  $v_{I1}$  and  $v_{I2}$  in terms of differential and common-mode components, find  $v_{O1}$  and  $v_{O2}$  in the circuit in Fig. 2.20(a) and hence find their differential component  $v_{O2} - v_{O1}$  and their common-mode component  $\frac{1}{2}(v_{O1} + v_{O2})$ . Now find the differential gain and the common-mode gain of the first stage of this instrumentation amplifier and hence the CMRR.

(b) Repeat for the circuit in Fig. 2.20(b), and comment on the difference between the two circuits.

**\*2.75** For an instrumentation amplifier of the type shown in Fig. 2.20(b), a designer proposes to make  $R_2 = R_3 = R_4 = 100 \text{ k}\Omega$ , and  $2R_1 = 10 \text{ k}\Omega$ . For ideal components, what difference-mode gain, common-mode gain, and CMRR result? Reevaluate the worst-case values for these for the situation in which all resistors are specified as  $\pm 1\%$  units. Repeat the latter analysis for the case in which  $2R_1$  is reduced to  $1 \text{ k}\Omega$ . What do you conclude about the effect of the gain of the first stage on CMRR? (Hint: Eq. (2.19) can be used to evaluate  $A_{cm}$  of the second stage.)

**D 2.76** Design the instrumentation-amplifier circuit of Fig. 2.20(b) to realize a differential gain, variable in the range 2 to 100, utilizing a  $100\text{-k}\Omega$  pot as variable resistor.

**SIM \*2.77** The circuit shown in Fig. P2.77 is intended to supply a voltage to floating loads (those for which both terminals are ungrounded) while making greatest possible use of the available power supply.

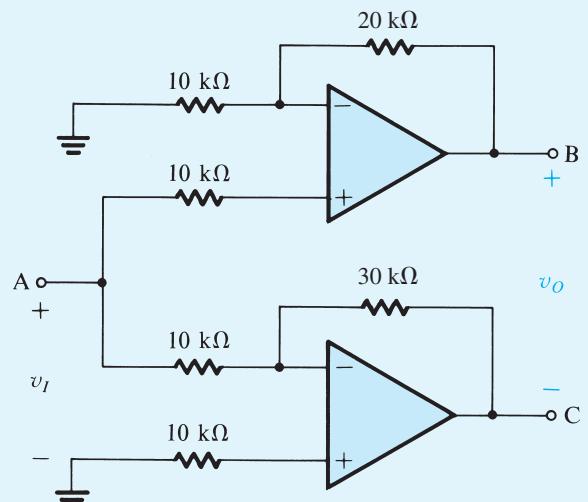


Figure P2.77

- (a) Assuming ideal op amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied at A. Also sketch  $v_o$ .
- (b) What is the voltage gain  $v_o/v_i$ ?
- (c) Assuming that the op amps operate from  $\pm 15$ -V power supplies and that their output saturates at  $\pm 14$  V (in the manner shown in Fig. 1.14), what is the largest sine-wave output that can be accommodated? Specify both its peak-to-peak and rms values.

\*2.78 The two circuits in Fig. P2.78 are intended to function as voltage-to-current converters; that is, they supply the load impedance  $Z_L$  with a current proportional to  $v_i$  and independent of the value of  $Z_L$ . Show that this is indeed the case, and find for each circuit  $i_o$  as a function of  $v_i$ . Comment on the differences between the two circuits.

### Section 2.5: Integrators and Differentiators

2.79 A Miller integrator incorporates an ideal op amp, a resistor  $R$  of  $10\text{ k}\Omega$ , and a capacitor  $C$  of  $1\text{ nF}$ . A sine-wave signal is applied to its input.

- (a) At what frequency (in Hz) are the input and output signals equal in amplitude?
- (b) At that frequency, how does the phase of the output sine wave relate to that of the input?

- (c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?

- (d) What is the phase relation between the input and output in situation (c)?

D 2.80 Design a Miller integrator with a time constant of 1 s and an input resistance of  $100\text{ k}\Omega$ . A dc voltage of  $-1$  volt is applied at the input at time 0, at which moment  $v_o = -10$  V. How long does it take the output to reach 0 V?  $+10$  V?

2.81 An op-amp-based inverting integrator is measured at 10 kHz to have a voltage gain of  $-100\text{ V/V}$ . At what frequency is its gain reduced to  $-1\text{ V/V}$ ? What is the integrator time constant?

D 2.82 Design a Miller integrator that has a unity-gain frequency of 10 krad/s and an input resistance of  $100\text{ k}\Omega$ . Sketch the output you would expect for the situation in which, with output initially at 0 V, a 2-V,  $100\text{-}\mu\text{s}$  pulse is applied to the input. Characterize the output that results when a sine wave  $2 \sin 10^4 t$  is applied to the input.

D 2.83 Design a Miller integrator whose input resistance is  $10\text{ k}\Omega$  and unity-gain frequency is 100 kHz. What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor to limit the dc gain

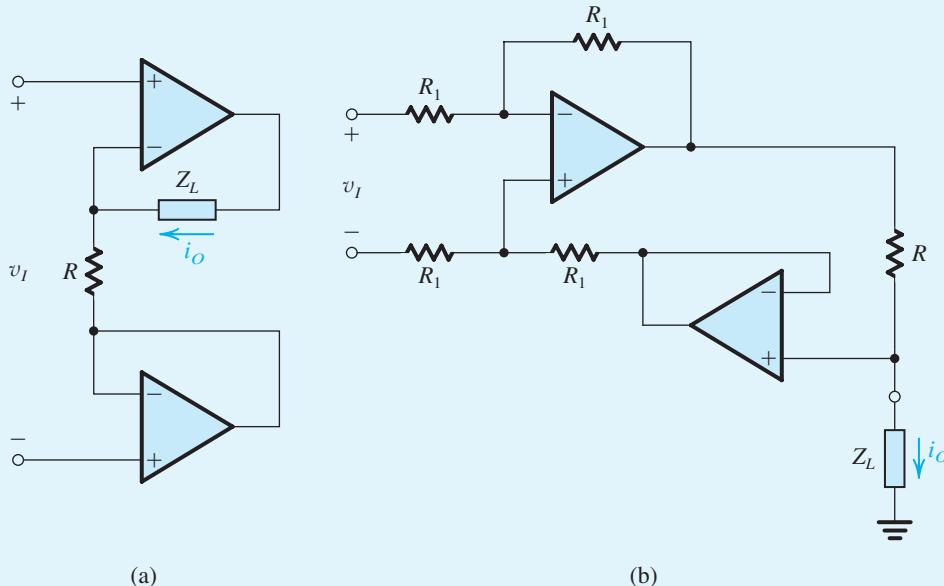


Figure P2.78

to 40 dB. What is its value? What is the associated lower 3-dB frequency? Sketch and label the output that results with a 10- $\mu$ s, 1-V positive-input pulse (initially at 0 V) with (a) no dc stabilization (but with the output initially at 0 V) and (b) the feedback resistor connected.

**\*2.84** A Miller integrator whose input and output voltages are initially zero and whose time constant is 1 ms is driven by the signal shown in Fig. P2.84. Sketch and label the output waveform that results. Indicate what happens if the input levels are  $\pm 2$  V, with the time constant the same (1 ms) and with the time constant raised to 2 ms.

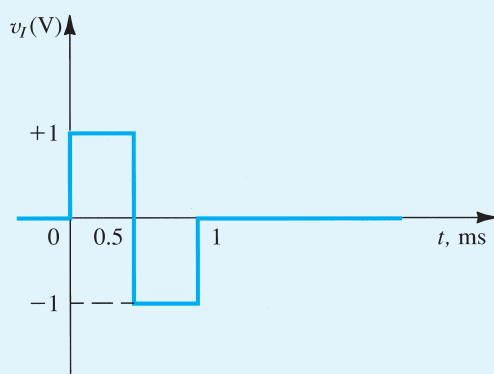


Figure P2.84

**2.85** Consider a Miller integrator having a time constant of 1 ms and an output that is initially zero, when fed with a string of pulses of 10- $\mu$ s duration and 1-V amplitude rising from 0 V (see Fig. P2.85). Sketch and label the output waveform resulting. How many pulses are required for an output voltage change of 1 V?

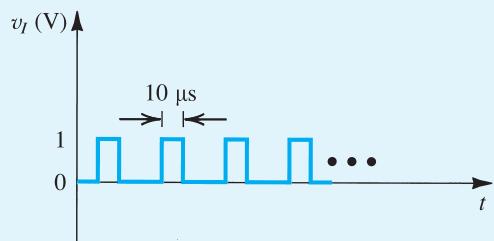


Figure P2.85

**D 2.86** Figure P2.86 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order,

low-pass active filter. Derive the transfer function and show that the dc gain is  $(-R_2/R_1)$  and the 3-dB frequency  $\omega_0 = 1/CR_2$ . Design the circuit to obtain an input resistance of 10 k $\Omega$ , a dc gain of 40 dB, and a 3-dB frequency of 1 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

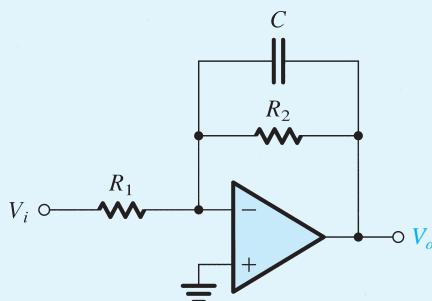


Figure P2.86

**\*2.87** Show that a Miller integrator implemented with an op amp with open-loop gain  $A_0$  has a low-pass STC transfer function. What is the pole frequency of the STC function? How does this compare with the pole frequency of the ideal integrator? If an ideal Miller integrator is fed with a -1-V pulse signal with a width  $T = CR$ , what will the output voltage be at  $t = T$ ? Assume that at  $t = 0, v_o = 0$ . Repeat for an integrator with an op amp having  $A_0 = 1000$ .

**2.88** A differentiator utilizes an ideal op amp, a 10-k $\Omega$  resistor, and a 1-nF capacitor. What is the frequency  $f_0$  (in Hz) at which its input and output sine-wave signals have equal magnitude? What is the output signal for a 1-V peak-to-peak sine-wave input with frequency equal to  $10f_0$ ?

**2.89** An op-amp differentiator with 1-ms time constant is driven by the rate-controlled step shown in Fig. P2.89. Assuming  $v_o$  to be zero initially, sketch and label its waveform.

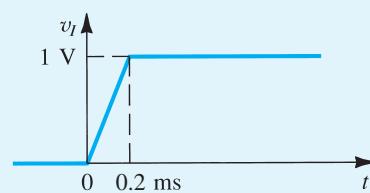


Figure P2.89

**2.90** An op-amp differentiator, employing the circuit shown in Fig. 2.27(a), has  $R = 20\text{ k}\Omega$  and  $C = 0.1\text{ }\mu\text{F}$ . When a triangle wave of  $\pm 1\text{-V}$  peak amplitude at 1 kHz is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of  $R$  is needed to cause the output to have a 12-V peak amplitude?

**2.91** Use an ideal op amp to design a differentiation circuit for which the time constant is  $10^{-3}$  s using a 10-nF capacitor. What are the gains and phase shifts found for this circuit at one-tenth and 10 times the unity-gain frequency? A series input resistor is added to limit the gain magnitude at high frequencies to 100 V/V. What is the associated 3-dB frequency? What gain and phase shift result at 10 times the unity-gain frequency?

**D 2.92** Figure P2.92 shows a circuit that performs the high-pass, single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function and show that the high-frequency gain is  $(-R_2/R_1)$  and the 3-dB frequency  $\omega_0 = 1/CR_1$ . Design the circuit to obtain a high-frequency input resistance of 1 k $\Omega$ , a high-frequency gain of 40 dB, and a 3-dB frequency of 2 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

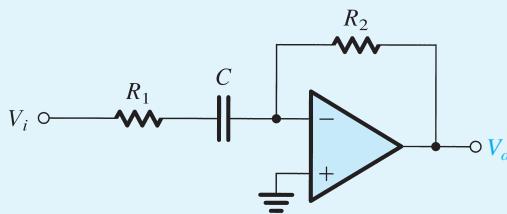


Figure P2.92

**D \*\*2.93** Derive the transfer function of the circuit in Fig. P2.93 (for an ideal op amp) and show that it can be written in the form

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{[1 + (\omega_1/j\omega)][1 + j(\omega/\omega_2)]}$$

where  $\omega_1 = 1/C_1R_1$  and  $\omega_2 = 1/C_2R_2$ . Assuming that the circuit is designed such that  $\omega_2 \gg \omega_1$ , find approximate expressions

for the transfer function in the following frequency regions:

- (a)  $\omega \ll \omega_1$
- (b)  $\omega_1 \ll \omega \ll \omega_2$
- (c)  $\omega \gg \omega_2$

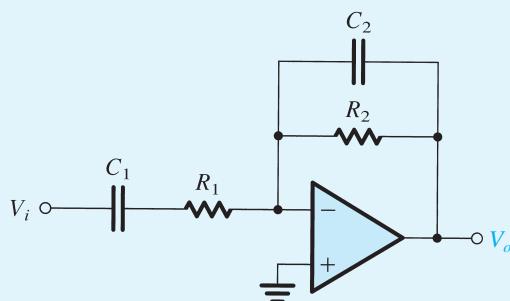


Figure P2.93

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the “middle-frequency range,” a low-frequency 3-dB point at 200 Hz, a high-frequency 3-dB point at 200 kHz, and an input resistance (at  $\omega \gg \omega_1$ ) of 2 k $\Omega$ .

### Section 2.6: DC Imperfections

**2.94** An op amp wired in the inverting configuration with the input grounded, having  $R_2 = 100\text{ k}\Omega$  and  $R_1 = 2\text{ k}\Omega$ , has an output dc voltage of  $-0.2\text{ V}$ . If the input bias current is known to be very small, find the input offset voltage.

**2.95** A noninverting amplifier with a gain of 100 uses an op amp having an input offset voltage of  $\pm 2\text{ mV}$ . Find the output when the input is  $0.01 \sin \omega t$ , volts.

**2.96** A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 3 mV and output saturation levels of  $\pm 12\text{ V}$ . What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping? If the amplifier is

capacitively coupled in the manner indicated in Fig. 2.36, what would the maximum possible amplitude be?

**2.97** An op amp connected in a closed-loop inverting configuration having a gain of 1000 V/V and using relatively small-valued resistors is measured with input grounded to have a dc output voltage of  $-1.8$  V. What is its input offset voltage? Prepare an offset-voltage-source sketch resembling that in Fig. 2.28. Be careful of polarities.

**2.98** A particular inverting amplifier with nominal gain of  $-100$  V/V uses an imperfect op amp in conjunction with  $100\text{-k}\Omega$  and  $10\text{-M}\Omega$  resistors. The output voltage is found to be  $+5.3$  V when measured with the input open and  $+5$  V with the input grounded.

- What is the bias current of this amplifier? In what direction does it flow?
- Estimate the value of the input offset voltage.
- A  $10\text{-M}\Omega$  resistor is connected between the positive-input terminal and ground. With the input left floating (disconnected), the output dc voltage is measured to be  $-0.6$  V. Estimate the input offset current.

**D 2.99** A noninverting amplifier with a gain of  $+10$  V/V using  $100\text{k}\Omega$  as the feedback resistor operates from a  $5\text{-k}\Omega$  source. For an amplifier offset voltage of  $0\text{ mV}$ , but with a bias current of  $2\text{ }\mu\text{A}$  and an offset current of  $0.2\text{ }\mu\text{A}$ , what range of outputs would you expect? Indicate where you would add an additional resistor to compensate for the bias currents. What does the range of possible outputs then become? A designer wishes to use this amplifier with a  $15\text{-k}\Omega$  source. In order to compensate for the bias current in this case, what resistor would you use? And where?

**D 2.100** The circuit of Fig. 2.36 is used to create an ac-coupled noninverting amplifier with a gain of  $100$  V/V using resistors no larger than  $100\text{k}\Omega$ . What values of  $R_1$ ,  $R_2$ , and  $R_3$  should be used? For a break frequency due to  $C_1$  at  $100$  Hz, and that due to  $C_2$  at  $10$  Hz, what values of  $C_1$  and  $C_2$  are needed?

**\*2.101** Consider the difference amplifier circuit in Fig. 2.16. Let  $R_1 = R_3 = 10\text{k}\Omega$  and  $R_2 = R_4 = 1\text{ M}\Omega$ . If the op amp has  $V_{os} = 5\text{ mV}$ ,  $I_B = 1\text{ }\mu\text{A}$ , and  $I_{os} = 0.2\text{ }\mu\text{A}$ , find the worst-case (largest) dc offset voltage at the output.

**\*2.102** The circuit shown in Fig. P2.102 uses an op amp having a  $\pm 3\text{-mV}$  offset. What is its output offset voltage? What does the output offset become with the input ac coupled

through a capacitor  $C$ ? If, instead, a large capacitor is placed in series with a  $1\text{-k}\Omega$  resistor, what does the output offset become?

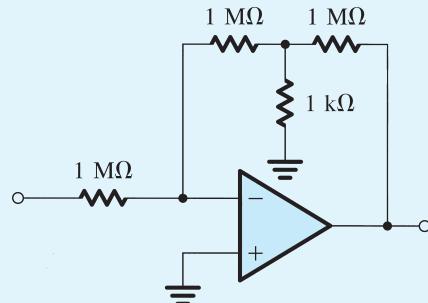


Figure P2.102

**2.103** Using offset-nulling facilities provided for the op amp, a closed-loop amplifier with gain of  $+1000$  is adjusted at  $25^\circ\text{C}$  to produce zero output with the input grounded. If the input offset-voltage drift is specified to be  $20\text{ }\mu\text{V}/^\circ\text{C}$ , what output would you expect at  $0^\circ\text{C}$  and at  $100^\circ\text{C}$ ? While nothing can be said separately about the polarity of the output offset at either  $0$  or  $75^\circ\text{C}$ , what would you expect their relative polarities to be?

**2.104** An op amp is connected in a closed loop with gain of  $+100$  utilizing a feedback resistor of  $1\text{ M}\Omega$ .

- If the input bias current is  $200\text{ nA}$ , what output voltage results with the input grounded?
- If the input offset voltage is  $\pm 2\text{ mV}$  and the input bias current as in (a), what is the largest possible output that can be observed with the input grounded?
- If bias-current compensation is used, what is the value of the required resistor? If the offset current is no more than one-tenth the bias current, what is the resulting output offset voltage (due to offset current alone)?
- With bias-current compensation as in (c) in place, what is the largest dc voltage at the output due to the combined effect of offset voltage and offset current?

**\*2.105** An op amp intended for operation with a closed-loop gain of  $-100$  V/V uses resistors of  $10\text{k}\Omega$  and  $1\text{ M}\Omega$  with a bias-current-compensation resistor  $R_3$ . What should the value of  $R_3$  be? With input grounded, the output offset voltage is found to be  $+0.30$  V. Estimate the input offset current assuming zero input offset voltage. If the input offset voltage

can be as large as 1 mV of unknown polarity, what range of offset current is possible?

**2.106** A Miller integrator with  $R = 10 \text{ k}\Omega$  and  $C = 10 \text{ nF}$  is implemented by using an op amp with  $V_{os} = 2 \text{ mV}$ ,  $I_B = 0.1 \mu\text{A}$ , and  $I_{os} = 20 \text{ nA}$ . To provide a finite dc gain, a  $1-\text{M}\Omega$  resistor is connected across the capacitor.

- To compensate for the effect of  $I_B$ , a resistor is connected in series with the positive-input terminal of the op amp. What should its value be?
- With the resistor of (a) in place, find the worst-case dc output voltage of the integrator when the input is grounded.

### Section 2.7: Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance

**2.107** The data in the following table apply to internally compensated op amps. Fill in the blank entries.

$A_0$	$f_b$ (Hz)	$f_t$ (Hz)
$10^5$	$10^2$	
$10^6$	$10^3$	$10^6$
	$10^{-1}$	$10^8$
$2 \times 10^5$	10	$10^6$

**2.108** A measurement of the open-loop gain of an internally compensated op amp at very low frequencies shows it to be 98 dB; at 100 kHz, this shows it is 40 dB. Estimate values for  $A_0$ ,  $f_b$ , and  $f_t$ .

**2.109** Measurements of the open-loop gain of a compensated op amp intended for high-frequency operation indicate that the gain is  $4 \times 10^3$  at 100 kHz and  $20 \times 10^3$  at 10 kHz. Estimate its 3-dB frequency, its unity-gain frequency, and its dc gain.

**2.110** Measurements made on the internally compensated amplifiers listed below provide the dc gain and the frequency at which the gain has dropped by 20 dB. For each, what are the 3 dB and unity-gain frequencies?

- $2 \times 10^5 \text{ V/V}$  and  $5 \times 10^2 \text{ Hz}$
- $20 \times 10^5 \text{ V/V}$  and  $10 \text{ Hz}$
- $1800 \text{ V/V}$  and  $0.1 \text{ MHz}$
- $100 \text{ V/V}$  and  $0.1 \text{ GHz}$
- $25 \text{ V/mV}$  and  $250 \text{ kHz}$

**2.111** An inverting amplifier with nominal gain of  $-50 \text{ V/V}$  employs an op amp having a dc gain of  $10^4$  and a unity-gain frequency of  $10^6 \text{ Hz}$ . What is the 3-dB frequency  $f_{3dB}$  of the closed-loop amplifier? What is its gain at  $0.1f_{3dB}$  and at  $10f_{3dB}$ ?

**2.112** A particular op amp, characterized by a gain-bandwidth product of 20 MHz, is operated with a closed-loop gain of  $+100 \text{ V/V}$ . What 3-dB bandwidth results? At what frequency does the closed-loop amplifier exhibit a  $-6^\circ$  phase shift? A  $-84^\circ$  phase shift?

**2.113** Find the  $f_t$  required for internally compensated op amps to be used in the implementation of closed-loop amplifiers with the following nominal dc gains and 3-dB bandwidths:

- $-50 \text{ V/V}$ ; 100 kHz
- $+50 \text{ V/V}$ ; 100 kHz
- $+2 \text{ V/V}$ ; 5 MHz
- $-2 \text{ V/V}$ ; 5 MHz
- $-1000 \text{ V/V}$ ; 10 kHz
- $+1 \text{ V/V}$ ; 1 MHz
- $-1 \text{ V/V}$ ; 1 MHz

**2.114** A noninverting op-amp circuit with a gain of 96 V/V is found to have a 3-dB frequency of 8 kHz. For a particular system application, a bandwidth of 32 kHz is required. What is the highest gain available under these conditions?

**2.115** Consider a unity-gain follower utilizing an internally compensated op amp with  $f_t = 2 \text{ MHz}$ . What is the 3-dB frequency of the follower? At what frequency is the gain of the follower 1% below its low-frequency magnitude? If the input to the follower is a 1-V step, find the 10% to 90% rise time of the output voltage. (Note: The step response of STC low-pass networks is discussed in Appendix E. Specifically, note that the 10%–90% rise time of a low-pass STC circuit with a time constant  $\tau$  is  $2.2\tau$ .)

**D \*2.116** It is required to design a noninverting amplifier with a dc gain of 10. When a step voltage of 100 mV is applied at the input, it is required that the output be within 1% of its final value of 1 V in at most 200 ns. What must the  $f_t$  of the op amp be? (Note: The step response of STC low-pass networks is discussed in Appendix E.)

**D \*2.117** This problem illustrates the use of cascaded closed-loop amplifiers to obtain an overall bandwidth greater than can be achieved using a single-stage amplifier with the same overall gain.

- (a) Show that cascading two identical amplifier stages, each having a low-pass STC frequency response with a 3-dB frequency  $f_1$ , results in an overall amplifier with a 3-dB frequency given by

$$f_{3\text{dB}} = \sqrt{\sqrt{2}-1}f_1$$

- (b) It is required to design a noninverting amplifier with a dc gain of 40 dB utilizing a single internally compensated op amp with  $f_t = 2$  MHz. What is the 3-dB frequency obtained?  
 (c) Redesign the amplifier of (b) by cascading two identical noninverting amplifiers each with a dc gain of 20 dB. What is the 3-dB frequency of the overall amplifier? Compare this to the value obtained in (b) above.

**D \*\*2.118** A designer, wanting to achieve a stable gain of 100 V/V at 5 MHz, considers her choice of amplifier topologies. What unity-gain frequency would a single operational amplifier require to satisfy her need? Unfortunately, the best available amplifier has an  $f_t$  of 40 MHz. How many such amplifiers connected in a cascade of identical noninverting stages would she need to achieve her goal? What is the 3-dB frequency of each stage she can use? What is the overall 3-dB frequency?

**2.119** Consider the use of an op amp with a unity-gain frequency  $f_t$  in the realization of:

- (a) An inverting amplifier with dc gain of magnitude  $K$ .  
 (b) A noninverting amplifier with a dc gain of  $K$ .

In each case find the 3-dB frequency and the gain-bandwidth product ( $\text{GBP} \equiv |\text{Gain}| \times f_{3\text{dB}}$ ). Comment on the results.

**\*2.120** Consider an inverting summer with two inputs  $V_1$  and  $V_2$  and with  $V_o = -(V_1 + 3V_2)$ . Find the 3-dB frequency of each of the gain functions  $V_o/V_1$  and  $V_o/V_2$  in terms of the op amp  $f_t$ . (Hint: In each case, the other input to the summer can be set to zero—an application of superposition.)

## Section 2.8: Large-Signal Operation of Op Amps

**2.121** A particular op amp using  $\pm 15$ -V supplies operates linearly for outputs in the range  $-14$  V to  $+14$  V. If used in an inverting amplifier configuration of gain  $-100$ , what is the rms value of the largest possible sine wave that can be applied at the input without output clipping?

**2.122** Consider an op amp connected in the inverting configuration to realize a closed-loop gain of  $-100$  V/V utilizing resistors of  $1\text{ k}\Omega$  and  $100\text{ k}\Omega$ . A load resistance  $R_L$

is connected from the output to ground, and a low-frequency sine-wave signal of peak amplitude  $V_p$  is applied to the input. Let the op amp be ideal except that its output voltage saturates at  $\pm 10$  V and its output current is limited to the range  $\pm 20$  mA.

- (a) For  $R_L = 1\text{ k}\Omega$ , what is the maximum possible value of  $V_p$  while an undistorted output sinusoid is obtained?  
 (b) Repeat (a) for  $R_L = 200\text{ }\Omega$ .  
 (c) If it is desired to obtain an output sinusoid of 10-V peak amplitude, what minimum value of  $R_L$  is allowed?

**2.123** An op amp having a slew rate of  $10\text{ V}/\mu\text{s}$  is to be used in the unity-gain follower configuration, with input pulses that rise from 0 to 2 V. What is the shortest pulse that can be used while ensuring full-amplitude output? For such a pulse, describe the output resulting.

**2.124** For operation with 10-V output pulses with the requirement that the sum of the rise and fall times represent only 20% of the pulse width (at half-amplitude), what is the slew-rate requirement for an op amp to handle pulses  $2\text{ }\mu\text{s}$  wide? (Note: The rise and fall times of a pulse signal are usually measured between the 10%- and 90%-height points.)

**2.125** What is the highest frequency of a triangle wave of 10-V peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is  $20\text{ V}/\mu\text{s}$ ? For a sine wave of the same frequency, what is the maximum amplitude of output signal that remains undistorted?

**2.126** For an amplifier having a slew rate of  $40\text{ V}/\mu\text{s}$ , what is the highest frequency at which a 20-V peak-to-peak sine wave can be produced at the output?

**D \*2.127** In designing with op amps one has to check the limitations on the voltage and frequency ranges of operation of the closed-loop amplifier, imposed by the op-amp finite bandwidth ( $f_t$ ), slew rate (SR), and output saturation ( $V_{o\text{max}}$ ). This problem illustrates the point by considering the use of an op amp with  $f_t = 20$  MHz, SR =  $10\text{ V}/\mu\text{s}$ , and  $V_{o\text{max}} = 10$  V in the design of a noninverting amplifier with a nominal gain of 10. Assume a sine-wave input with peak amplitude  $V_i$ .

- (a) If  $V_i = 0.5$  V, what is the maximum frequency before the output distorts?  
 (b) If  $f = 200$  kHz, what is the maximum value of  $V_i$  before the output distorts?  
 (c) If  $V_i = 50$  mV, what is the useful frequency range of operation?  
 (d) If  $f = 50$  kHz, what is the useful input voltage range?

## CHAPTER 3

# Semiconductors

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**3.3 Current Flow in Semiconductors 142**

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**3.5 The *pn* Junction with an Applied Voltage 155**

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## IN THIS CHAPTER YOU WILL LEARN

1. The basic properties of semiconductors and in particular silicon, which is the material used to make most of today's electronic circuits.
2. How doping a pure silicon crystal dramatically changes its electrical conductivity, which is the fundamental idea underlying the use of semiconductors in the implementation of electronic devices.
3. The two mechanisms by which current flows in semiconductors: drift and diffusion of charge carriers.
4. The structure and operation of the *pn* junction; a basic semiconductor structure that implements the diode and plays a dominant role in transistors.

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## Introduction

Thus far we have dealt with electronic circuits, and notably amplifiers, as system building blocks. For instance, in Chapter 2 we learned how to use op amps to design interesting and useful circuits, taking advantage of the terminal characteristics of the op amp and without any knowledge of what is inside the op-amp package. Though interesting and motivating, this approach has its limitations. Indeed, to achieve our goal of preparing the reader to become a proficient circuit designer, we have to go beyond this black-box or system-level abstraction and learn about the basic devices from which electronic circuits are assembled, namely, diodes (Chapter 4) and transistors (Chapters 5 and 6). These solid-state devices are made using semiconductor materials, predominantly silicon.

In this chapter, we briefly introduce the properties and physics of semiconductors. The objective is to provide a basis for understanding the physical operation of diodes and transistors in order to enable their effective use in the design of circuits. Although many of the concepts studied in this chapter apply to semiconductor materials in general, our treatment is heavily biased toward silicon, simply because it is the material used in the vast majority of microelectronic circuits. To complement the material presented here, Appendix A provides a description of the integrated-circuit fabrication process. As discussed in Appendix A, whether our circuit consists of a single transistor or is an **integrated circuit** containing more than 2 billion transistors, it is fabricated in a single silicon crystal, which gives rise to the name **monolithic circuit**. This chapter therefore begins with a study of the crystal structure of semiconductors and introduces the two types of charge carriers available for current conduction: electrons and holes. The most significant property of semiconductors is that their conductivity can be varied over a very wide range through the introduction of

controlled amounts of impurity atoms into the semiconductor crystal in a process called **doping**. Doped semiconductors are discussed in Section 3.2. This is followed by the study in Section 3.3 of the two mechanisms for current flow in semiconductors, namely, carrier drift and carrier diffusion.

Armed with these basic semiconductor concepts, we spend the remainder of the chapter on the study of an important semiconductor structure: the *pn* junction. In addition to being essentially a diode, the *pn* junction is the basic element of the bipolar junction transistor (BJT, Chapter 6) and plays an important role in the operation of field-effect transistors (FETs, Chapter 5).

### 3.1 Intrinsic Semiconductors

As their name implies, semiconductors are materials whose conductivity lies between that of conductors, such as copper, and insulators, such as glass. There are two kinds of semiconductors: single-element semiconductors, such as germanium and silicon, which are in group IV in the periodic table; and compound semiconductors, such as gallium-arsenide, which are formed by combining elements from groups III and V or groups II and VI. Compound semiconductors are useful in special electronic circuit applications as well as in applications that involve light, such as light-emitting diodes (LEDs). Of the two elemental semiconductors, germanium was used in the fabrication of very early transistors (late 1940s, early 1950s). It was quickly supplanted, however, with silicon, on which today's integrated-circuit technology is almost entirely based. For this reason, we will deal mostly with silicon devices throughout this book.<sup>1</sup>

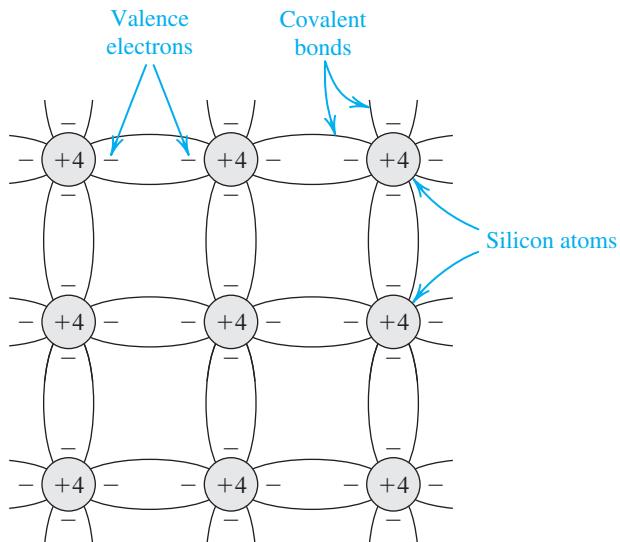
A silicon atom has four valence electrons, and thus it requires another four to complete its outermost shell. This is achieved by sharing one of its valence electrons with each of its four neighboring atoms. Each pair of shared electrons forms a **covalent bond**. The result is that a crystal of pure or intrinsic silicon has a regular lattice structure, where the atoms are held in their position by the covalent bonds. Figure 3.1 shows a two-dimensional representation of such a structure.

At sufficiently low temperatures, approaching absolute zero (0 K), all the covalent bonds are intact and no electrons are available to conduct electric current. Thus, at such low temperatures, the intrinsic silicon crystal behaves as an insulator.

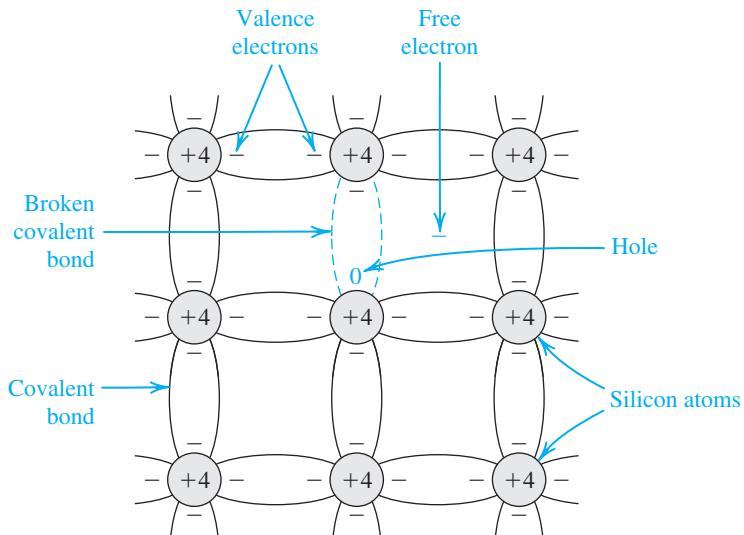
At room temperature, sufficient thermal energy exists to break some of the covalent bonds, a process known as thermal generation. As shown in Fig. 3.2, when a covalent bond is broken, an electron is freed. The **free electron** can wander away from its parent atom, and it becomes available to conduct electric current if an electric field is applied to the crystal. As the electron leaves its parent atom, it leaves behind a net positive charge, equal to the magnitude of the electron charge. Thus, an electron from a neighboring atom may be attracted to this positive charge, and leaves its parent atom. This action fills up the “hole” that existed in the ionized atom but creates a new hole in the other atom. This process may repeat itself, with the result that we effectively have a positively charged carrier, or **hole**, moving through the silicon crystal structure and being available to conduct electric current. The charge of a hole is equal in magnitude to the charge of an electron. We can thus see that as temperature increases, more covalent bonds are broken and electron–hole pairs are generated. The increase in the numbers of free electrons and holes results in an increase in the conductivity of silicon.

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<sup>1</sup>An exception is the subject of gallium arsenide (GaAs) circuits, which though not covered in this edition of the book, is studied in some detail in material provided on the text website.



**Figure 3.1** Two-dimensional representation of the silicon crystal. The circles represent the inner core of silicon atoms, with +4 indicating its positive charge of  $+4q$ , which is neutralized by the charge of the four valence electrons. Observe how the covalent bonds are formed by sharing of the valence electrons. At 0 K, all bonds are intact and no free electrons are available for current conduction.



**Figure 3.2** At room temperature, some of the covalent bonds are broken by thermal generation. Each broken bond gives rise to a free electron and a hole, both of which become available for current conduction.

Thermal generation results in free electrons and holes in equal numbers and hence equal concentrations, where concentration refers to the number of charge carriers per unit volume ( $\text{cm}^3$ ). The free electrons and holes move randomly through the silicon crystal structure, and in the process some electrons may fill some of the holes. This process, called **recombination**, results in the disappearance of free electrons and holes. The recombination rate is

proportional to the number of free electrons and holes, which in turn is determined by the thermal **generation** rate. The latter is a strong function of temperature. In thermal equilibrium, the recombination rate is equal to the generation rate, and one can conclude that the concentration of free electrons  $n$  is equal to the concentration of holes  $p$ ,

$$n = p = n_i \quad (3.1)$$

where  $n_i$  denotes the number of free electrons and holes in a unit volume ( $\text{cm}^3$ ) of intrinsic silicon at a given temperature. Results from semiconductor physics gives  $n_i$  as



$$n_i = BT^{3/2} e^{-E_g/2kT} \quad (3.2)$$

where  $B$  is a material-dependent parameter that is  $7.3 \times 10^{15} \text{ cm}^{-3} \text{ K}^{-3/2}$  for silicon;  $T$  is the temperature in  $K$ ;  $E_g$ , a parameter known as the **bandgap energy**, is 1.12 electron volt (eV) for silicon<sup>2</sup>; and  $k$  is Boltzmann's constant ( $8.62 \times 10^{-5} \text{ eV/K}$ ). It is interesting to know that the bandgap energy  $E_g$  is the minimum energy required to break a covalent bond and thus generate an electron-hole pair.

### Example 3.1

Calculate the value of  $n_i$  for silicon at room temperature ( $T \simeq 300 \text{ K}$ ).

#### Solution

Substituting the values given above in Eq. (3.2) provides

$$\begin{aligned} n_i &= 7.3 \times 10^{15} (300)^{3/2} e^{-1.12/(2 \times 8.62 \times 10^{-5} \times 300)} \\ &= 1.5 \times 10^{10} \text{ carriers/cm}^3 \end{aligned}$$

Although this number seems large, to place it into context note that silicon has  $5 \times 10^{22}$  atoms/ $\text{cm}^3$ . Thus at room temperature only one in about  $5 \times 10^{12}$  atoms is ionized and contributing a free electron and a hole!

Finally, it is useful for future purposes to express the product of the hole and free-electron concentration as

$$pn = n_i^2 \quad (3.3)$$

where for silicon at room temperature,  $n_i \simeq 1.5 \times 10^{10}/\text{cm}^3$ . As will be seen shortly, this relationship extends to extrinsic or doped silicon as well.

---

<sup>2</sup>Note that  $1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}$ .

### LCDs, THE FACE OF ELECTRONICS:

The existence of liquid crystals whose color could be changed by means of an external heat source was first reported in 1888 by an Austrian botanical physiologist. The LC idea lay dormant until the late 1940s, however. Subsequent developments in the field of solid-state electronics provided the technology to harness the technique in display media, with the first LCDs being demonstrated by RCA beginning in 1962. Today, LCDs are an essential component in every mobile device as the interface to the world of electronics within. At the other end of the scale, large LCDs are used in flat-panel TVs, and very large LCDs are appearing as “dynamic” wallpaper in museum display settings.

### EXERCISE

- 3.1** Calculate the intrinsic carrier density  $n_i$  for silicon at  $T = 50$  K and  $350$  K.

**Ans.**  $9.6 \times 10^{-39}/\text{cm}^3$ ;  $4.15 \times 10^{11}/\text{cm}^3$

## 3.2 Doped Semiconductors

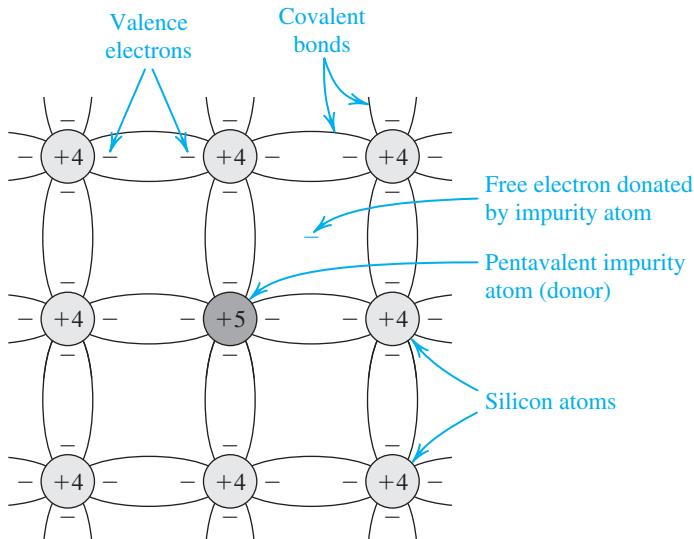
The intrinsic silicon crystal described above has equal concentrations of free electrons and holes, generated by thermal generation. These concentrations are far too small for silicon to conduct appreciable current at room temperature. Also, the carrier concentrations and hence the conductivity are strong functions of temperature, not a desirable property in an electronic device. Fortunately, a method was developed to change the carrier concentration in a semiconductor crystal substantially and in a precisely controlled manner. This process is known as **doping**, and the resulting silicon is referred to as **doped silicon**.

Doping involves introducing impurity atoms into the silicon crystal in sufficient numbers to substantially increase the concentration of either free electrons or holes but with little or no change in the crystal properties of silicon. To increase the concentration of free electrons,  $n$ , silicon is doped with an element with a valence of 5, such as phosphorus. The resulting doped silicon is then said to be of ***n* type**. To increase the concentration of holes,  $p$ , silicon is doped with an element having a valence of 3, such as boron, and the resulting doped silicon is said to be of ***p* type**.

Figure 3.3 shows a silicon crystal doped with phosphorus impurity. The dopant (phosphorus) atoms replace some of the silicon atoms in the crystal structure. Since the phosphorus atom has five electrons in its outer shell, four of these electrons form covalent bonds with the neighboring atoms, and the fifth electron becomes a free electron. Thus each phosphorus atom *donates* a free electron to the silicon crystal, and the phosphorus impurity is called a **donor**. It should be clear, though, that no holes are generated by this process. The net positive charge associated with the phosphorus atom is a **bound charge** that does not move through the crystal.

If the concentration of donor atoms is  $N_D$ , where  $N_D$  is usually much greater than  $n_i$ , the concentration of free electrons in the *n*-type silicon will be

$$n_n \simeq N_D \quad (3.4)$$



**Figure 3.3** A silicon crystal doped by a pentavalent element. Each dopant atom donates a free electron and is thus called a donor. The doped semiconductor becomes  $n$  type.

where the subscript  $n$  denotes  $n$ -type silicon. Thus  $n_n$  is determined by the doping concentration and not by temperature. This is not the case, however, for the hole concentration. All the holes in the  $n$ -type silicon are those generated by thermal ionization. Their concentration  $p_n$  can be found by noting that the relationship in Eq. (3.3) applies equally well for doped silicon, provided thermal equilibrium is achieved. Thus for  $n$ -type silicon

$$p_n n_n = n_i^2$$

Substituting for  $n_n$  from Eq. (3.4), we obtain for  $p_n$

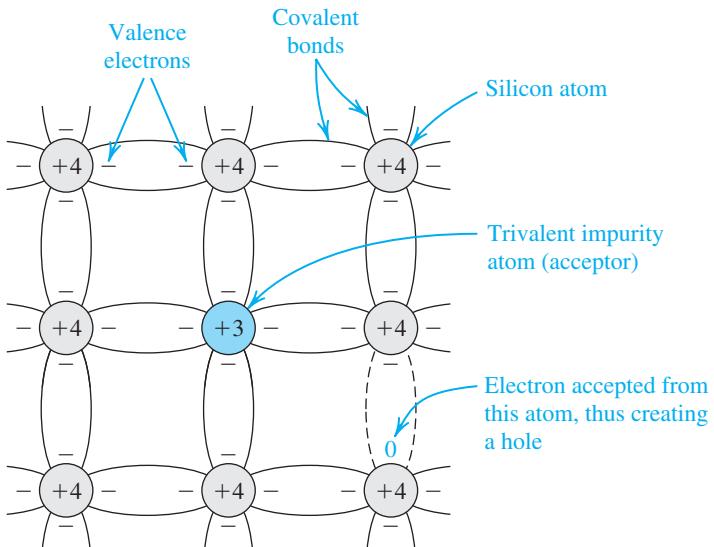
$$p_n \simeq \frac{n_i^2}{N_D} \quad (3.5)$$

Thus  $p_n$  will have the same dependence on temperature as that of  $n_i^2$ . Finally, we note that in  $n$ -type silicon the concentration of free electrons  $n_n$  will be much larger than that of holes. Hence electrons are said to be the **majority** charge carriers and holes the **minority** charge carriers in  $n$ -type silicon.

To obtain  $p$ -type silicon in which holes are the majority charge carriers, a trivalent impurity such as boron is used. Figure 3.4 shows a silicon crystal doped with boron. Note that the boron atoms replace some of the silicon atoms in the silicon crystal structure. Since each boron atom has three electrons in its outer shell, it **accepts** an electron from a neighboring atom, thus forming covalent bonds. The result is a hole in the neighboring atom and a bound negative charge at the **acceptor** (boron) atom. It follows that each acceptor atom provides a hole. If the acceptor doping concentration is  $N_A$ , where  $N_A \gg n_i$ , the hole concentration becomes

$$p_p \simeq N_A \quad (3.6)$$

where the subscript  $p$  denotes  $p$ -type silicon. Thus, here the majority carriers are holes and their concentration is determined by  $N_A$ . The concentration of minority electrons can be found



**Figure 3.4** A silicon crystal doped with boron, a trivalent impurity. Each dopant atom gives rise to a hole, and the semiconductor becomes *p* type.

by using the relationship

$$p_p n_p = n_i^2$$

and substituting for  $p_p$  from Eq. (3.6),

$$n_p \simeq \frac{n_i^2}{N_A} \quad (3.7)$$

Thus, the concentration of the minority electrons will have the same temperature dependence as that of  $n_i^2$ .

It should be emphasized that a piece of *n*-type or *p*-type silicon is electrically neutral; the charge of the majority free carriers (electrons in the *n*-type and holes in the *p*-type silicon) are neutralized by the bound charges associated with the impurity atoms.

### Example 3.2

Consider an *n*-type silicon for which the dopant concentration  $N_D = 10^{17}/\text{cm}^3$ . Find the electron and hole concentrations at  $T = 300 \text{ K}$ .

#### Solution

The concentration of the majority electrons is

$$n_n \simeq N_D = 10^{17}/\text{cm}^3$$

**Example 3.2** *continued*

The concentration of the minority holes is

$$p_n \simeq \frac{n_i^2}{N_D}$$

In Example 3.1 we found that at  $T = 300$  K,  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ . Thus,

$$\begin{aligned} p_n &= \frac{(1.5 \times 10^{10})^2}{10^{17}} \\ &= 2.25 \times 10^3/\text{cm}^3 \end{aligned}$$

Observe that  $n_n \gg n_i$  and that  $n_n$  is vastly higher than  $p_n$ .

## EXERCISES

- 3.2** For the situation in Example 3.2, find the electron and hole concentrations at 350 K. You may use the value of  $n_i$  at  $T = 350$  K found in Exercise 3.1.

**Ans.**  $n_n = 10^{17}/\text{cm}^3$ ,  $p_n = 1.72 \times 10^6/\text{cm}^3$

- 3.3** For a silicon crystal doped with boron, what must  $N_A$  be if at  $T = 300$  K the electron concentration drops below the intrinsic level by a factor of  $10^6$ ?

**Ans.**  $N_A = 1.5 \times 10^{16}/\text{cm}^3$

## 3.3 Current Flow in Semiconductors

There are two distinctly different mechanisms for the movement of charge carriers and hence for current flow in semiconductors: drift and diffusion.

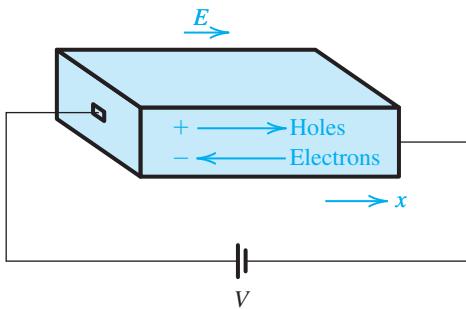
### 3.3.1 Drift Current

When an electrical field  $E$  is established in a semiconductor crystal, holes are accelerated in the direction of  $E$ , and free electrons are accelerated in the direction opposite to that of  $E$ . This situation is illustrated in Fig. 3.5. The holes acquire a velocity  $v_{p\text{-drift}}$  given by



$$v_{p\text{-drift}} = \mu_p E \quad (3.8)$$

where  $\mu_p$  is a constant called the **hole mobility**: It represents the degree of ease by which holes move through the silicon crystal in response to the electrical field  $E$ . Since velocity has the units of centimeters per second and  $E$  has the units of volts per centimeter, we see from Eq. (3.8) that the mobility  $\mu_p$  must have the units of centimeters squared per volt-second ( $\text{cm}^2/\text{V} \cdot \text{s}$ ). For intrinsic silicon  $\mu_p = 480 \text{ cm}^2/\text{V} \cdot \text{s}$ .



**Figure 3.5** An electric field  $E$  established in a bar of silicon causes the holes to drift in the direction of  $E$  and the free electrons to drift in the opposite direction. Both the hole and electron drift currents are in the direction of  $E$ .

The free electrons acquire a drift velocity  $v_{n\text{-drift}}$  given by

$$v_{n\text{-drift}} = -\mu_n E \quad (3.9)$$

where the result is negative because the electrons move in the direction opposite to  $E$ . Here  $\mu_n$  is the **electron mobility**, which for intrinsic silicon is about  $1350 \text{ cm}^2/\text{V}\cdot\text{s}$ . Note that  $\mu_n$  is about 2.5 times  $\mu_p$ , signifying that electrons move with much greater ease through the silicon crystal than do holes.

Let's now return to the single-crystal silicon bar shown in Fig. 3.5. Let the concentration of holes be  $p$  and that of free electrons  $n$ . We wish to calculate the current component due to the flow of holes. Consider a plane perpendicular to the  $x$  direction. In one second, the hole charge that crosses that plane will be  $(Aqp v_{p\text{-drift}})$  coulombs, where  $A$  is the cross-sectional area of the silicon bar and  $q$  is the magnitude of electron charge. This then must be the hole component of the drift current flowing through the bar,

$$I_p = Aqp v_{p\text{-drift}} \quad (3.10)$$

Substituting for  $v_{p\text{-drift}}$  from Eq. (3.8), we obtain

$$I_p = Aqp\mu_p E$$

We are usually interested in the current density  $J_p$ , which is the current per unit cross-sectional area,

$$J_p = \frac{I_p}{A} = qp\mu_p E \quad (3.11)$$

The current component due to the drift of free electrons can be found in a similar manner. Note, however, that electrons drifting from right to left result in a current component from left to right. This is because of the convention of taking the direction of current flow as the direction of flow of positive charge and opposite to the direction of flow of negative charge. Thus,

$$I_n = -Aqn v_{n\text{-drift}}$$

Substituting for  $v_{n\text{-drift}}$  from Eq. (3.9), we obtain the current density  $J_n = I_n/A$  as

$$J_n = qn\mu_n E \quad (3.12)$$

The total drift current density can now be found by summing  $J_p$  and  $J_n$  from Eqs. (3.11) and (3.12),

$$J = J_p + J_n = q(p\mu_p + n\mu_n)E \quad (3.13)$$

This relationship can be written as

$$J = \sigma E \quad (3.14)$$

or

$$J = E/\rho \quad (3.15)$$

where the **conductivity**  $\sigma$  is given by

$$\sigma = q(p\mu_p + n\mu_n) \quad (3.16)$$

and the **resistivity**  $\rho$  is given by

$$\rho \equiv \frac{1}{\sigma} = \frac{1}{q(p\mu_p + n\mu_n)} \quad (3.17)$$

Observe that Eq. (3.15) is a form of Ohm's law and can be written alternately as

$$\rho = \frac{E}{J} \quad (3.18)$$

Thus the units of  $\rho$  are obtained from:  $\frac{\text{V}/\text{cm}}{\text{A}/\text{cm}^2} = \Omega \cdot \text{cm}$ .

### Example 3.3

Find the resistivity of (a) intrinsic silicon and (b) *p*-type silicon with  $N_A = 10^{16}/\text{cm}^3$ . Use  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ , and assume that for intrinsic silicon  $\mu_n = 1350 \text{ cm}^2/\text{V} \cdot \text{s}$  and  $\mu_p = 480 \text{ cm}^2/\text{V} \cdot \text{s}$ , and for the doped silicon  $\mu_n = 1110 \text{ cm}^2/\text{V} \cdot \text{s}$  and  $\mu_p = 400 \text{ cm}^2/\text{V} \cdot \text{s}$ . (Note that doping results in reduced carrier mobilities.)

#### Solution

(a) For intrinsic silicon,

$$p = n = n_i = 1.5 \times 10^{10}/\text{cm}^3$$

Thus,

$$\begin{aligned} \rho &= \frac{1}{q(p\mu_p + n\mu_n)} \\ &= \frac{1}{1.6 \times 10^{-19} (1.5 \times 10^{10} \times 480 + 1.5 \times 10^{10} \times 1350)} \\ &= 2.28 \times 10^5 \Omega \cdot \text{cm} \end{aligned}$$

(b) For the *p*-type silicon

$$p_p \simeq N_A = 10^{16}/\text{cm}^3$$

$$n_p \simeq \frac{n_i^2}{N_A} = \frac{(1.5 \times 10^{10})^2}{10^{16}} = 2.25 \times 10^4/\text{cm}^3$$

Thus,

$$\begin{aligned}\rho &= \frac{1}{q(p\mu_p + n\mu_n)} \\ &= \frac{1}{1.6 \times 10^{-19} (10^{16} \times 400 + 2.25 \times 10^4 \times 1110)} \\ &\approx \frac{1}{1.6 \times 10^{-19} \times 10^{16} \times 400} = 1.56 \Omega \cdot \text{cm}\end{aligned}$$

Observe that the resistivity of the *p*-type silicon is determined almost entirely by the doping concentration. Also observe that doping the silicon reduces its resistivity by a factor of about  $10^4$ , a truly remarkable change.

### EXERCISE

- 3.4** A uniform bar of *n*-type silicon of 2-μm length has a voltage of 1 V applied across it. If  $N_D = 10^{16}/\text{cm}^3$  and  $\mu_n = 1350 \text{ cm}^2/\text{V} \cdot \text{s}$ , find (a) the electron drift velocity, (b) the time it takes an electron to cross the 2-μm length, (c) the drift-current density, and (d) the drift current in the case that the silicon bar has a cross-sectional area of  $0.25 \mu\text{m}^2$ .

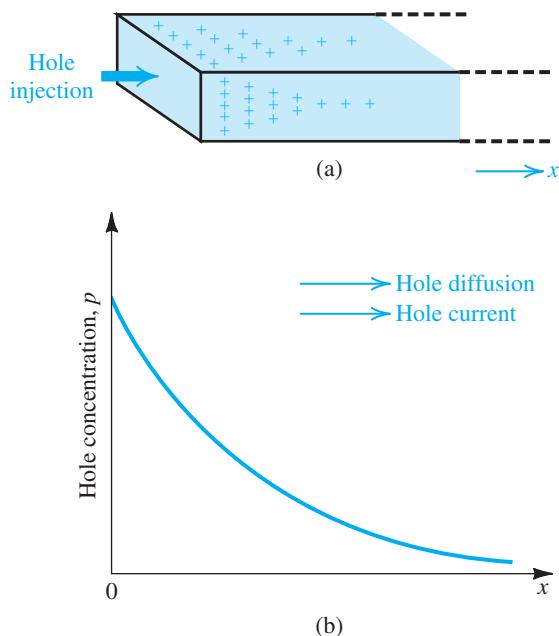
**Ans.**  $6.75 \times 10^6 \text{ cm/s}$ ;  $30 \text{ ps}$ ;  $1.08 \times 10^4 \text{ A/cm}^2$ ;  $27 \mu\text{A}$

### 3.3.2 Diffusion Current

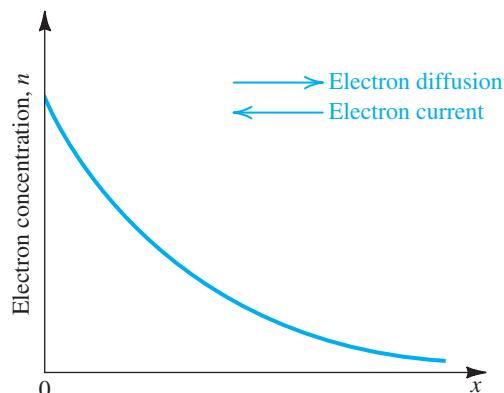
Carrier diffusion occurs when the density of charge carriers in a piece of semiconductor is not uniform. For instance, if by some mechanism the concentration of, say, holes, is made higher in one part of a piece of silicon than in another, then holes will diffuse from the region of high concentration to the region of low concentration. Such a diffusion process is like that observed if one drops a few ink drops in a water-filled tank. The diffusion of charge carriers gives rise to a net flow of charge, or **diffusion current**.

As an example, consider the bar of silicon shown in Fig. 3.6(a): By some unspecified process, we have arranged to inject holes into its left side. This continuous hole injection gives rise to and maintains a hole **concentration profile** such as that shown in Fig. 3.6(b). This profile in turn causes holes to diffuse from left to right along the silicon bar, resulting in a hole current in the *x* direction. The magnitude of the current at any point is proportional to the slope of the concentration profile, or the **concentration gradient**, at that point,

$$J_p = -qD_p \frac{dp(x)}{dx} \quad (3.19)$$



**Figure 3.6** A bar of silicon (a) into which holes are injected, thus creating the hole concentration profile along the  $x$  axis, shown in (b). The holes diffuse in the positive direction of  $x$  and give rise to a hole diffusion current in the same direction. Note that we are not showing the circuit to which the silicon bar is connected.



**Figure 3.7** If the electron concentration profile shown is established in a bar of silicon, electrons diffuse in the  $x$  direction, giving rise to an electron diffusion current in the negative- $x$  direction.

where  $J_p$  is the hole-current density ( $\text{A}/\text{cm}^2$ ),  $q$  is the magnitude of electron charge,  $D_p$  is a constant called the **diffusion constant** or **diffusivity** of holes; and  $p(x)$  is the hole concentration at point  $x$ . Note that the gradient ( $dp/dx$ ) is negative, resulting in a positive current in the  $x$  direction, as should be expected.

In the case of electron diffusion resulting from an electron concentration gradient (see Fig. 3.7), a similar relationship applies, giving the electron-current density,

$$J_n = qD_n \frac{dn(x)}{dx} \quad (3.20)$$

where  $D_n$  is the diffusion constant or diffusivity of electrons. Observe that a negative ( $dn/dx$ ) gives rise to a negative current, a result of the convention that the positive direction of current is taken to be that of the flow of positive charge (and opposite to that of the flow of negative

charge). For holes and electrons diffusing in intrinsic silicon, typical values for the diffusion constants are  $D_p = 12 \text{ cm}^2/\text{s}$  and  $D_n = 35 \text{ cm}^2/\text{s}$ .

At this point the reader is probably wondering where the diffusion current in the silicon bar in Fig. 3.6(a) goes. A good question, as we are not showing how the right-side end of the bar is connected to the rest of the circuit. We will address this and related questions in detail in our discussion of the *pn* junction in later sections.

### Example 3.4

Consider a bar of silicon in which a hole concentration profile described by

$$p(x) = p_0 e^{-x/L_p}$$

is established. Find the hole-current density at  $x = 0$ . Let  $p_0 = 10^{16}/\text{cm}^3$ ,  $L_p = 1 \mu\text{m}$ , and  $D_p = 12 \text{ cm}^2/\text{s}$ . If the cross-sectional area of the bar is  $100 \mu\text{m}^2$ , find the current  $I_p$ .

#### Solution

$$\begin{aligned} J_p &= -qD_p \frac{dp(x)}{dx} \\ &= -qD_p \frac{d}{dx} \left[ p_0 e^{-x/L_p} \right] \\ &= q \frac{D_p}{L_p} p_0 e^{-x/L_p} \end{aligned}$$

Thus,

$$\begin{aligned} J_p(0) &= q \frac{D_p}{L_p} p_0 \\ &= 1.6 \times 10^{-19} \times \frac{12}{1 \times 10^{-4}} \times 10^{16} \\ &= 192 \text{ A/cm}^2 \end{aligned}$$

The current  $I_p$  can be found from

$$\begin{aligned} I_p &= J_p \times A \\ &= 192 \times 100 \times 10^{-8} \\ &= 192 \mu\text{A} \end{aligned}$$

### EXERCISE

- 3.5** The linear electron-concentration profile shown in Fig. E3.5 has been established in a piece of silicon. If  $n_0 = 10^{17}/\text{cm}^3$  and  $W = 1 \mu\text{m}$ , find the electron-current density in microamperes per micron squared ( $\mu\text{A}/\mu\text{m}^2$ ). If a diffusion current of 1 mA is required, what must the cross-sectional area (in a direction perpendicular to the page) be? Recall that  $D_n = 35 \text{ cm}^2/\text{s}$ .

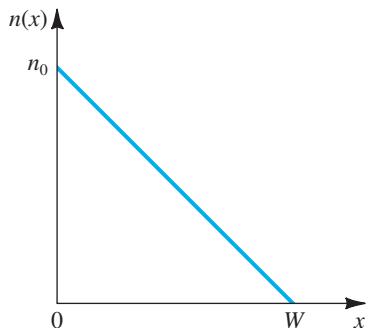


Figure E3.5

**Ans.**  $56 \mu\text{A}/\mu\text{m}^2$ ;  $18 \mu\text{m}^2$

### 3.3.3 Relationship between $D$ and $\mu$

A simple but powerful relationship ties the diffusion constant with the mobility,

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T \quad (3.21)$$

where  $V_T = kT/q$ . The parameter  $V_T$  is known as the **thermal voltage**. At room temperature,  $T \simeq 300 \text{ K}$  and  $V_T = 25.9 \text{ mV}$ . We will encounter  $V_T$  repeatedly throughout this book. The relationship in Eq. (3.21) is known as the **Einstein relationship**.

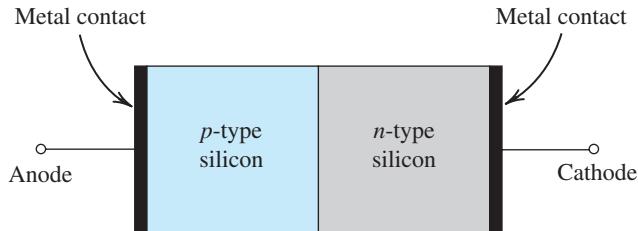
#### EXERCISE

- 3.6 Use the Einstein relationship to find  $D_n$  and  $D_p$  for intrinsic silicon using  $\mu_n = 1350 \text{ cm}^2/\text{V}\cdot\text{s}$  and  $\mu_p = 480 \text{ cm}^2/\text{V}\cdot\text{s}$ .

**Ans.**  $35 \text{ cm}^2/\text{s}$ ;  $12.4 \text{ cm}^2/\text{s}$

## 3.4 The *pn* Junction

Having learned important semiconductor concepts, we are now ready to consider our first practical semiconductor structure—the *pn* junction. As mentioned previously, the *pn* junction implements the diode (Chapter 4) and plays the dominant role in the structure and operation of the bipolar junction transistor (BJT, Chapter 6). As well, understanding *pn* junctions is very important to the study of the MOSFET operation (Chapter 5).



**Figure 3.8** Simplified physical structure of the *pn* junction. (Actual geometries are given in Appendix A.) As the *pn* junction implements the junction diode, its terminals are labeled anode and cathode.

### 3.4.1 Physical Structure

Figure 3.8 shows a simplified physical structure of the *pn* junction. It consists of a *p*-type semiconductor (e.g., silicon) brought into close contact with an *n*-type semiconductor material (also silicon). In actual practice, both the *p* and *n* regions are part of the same silicon crystal; that is, the *pn* junction is formed within a single silicon crystal by creating regions of different dopings (*p* and *n* regions). Appendix A provides a description of the fabrication process of integrated circuits including *pn* junctions. As indicated in Fig. 3.8, external wire connections are made to the *p* and *n* regions through metal (aluminum) contacts. If the *pn* junction is used as a diode, these constitute the diode terminals and are therefore labeled “anode” and “cathode” in keeping with diode terminology.<sup>3</sup>

### 3.4.2 Operation with Open-Circuit Terminals

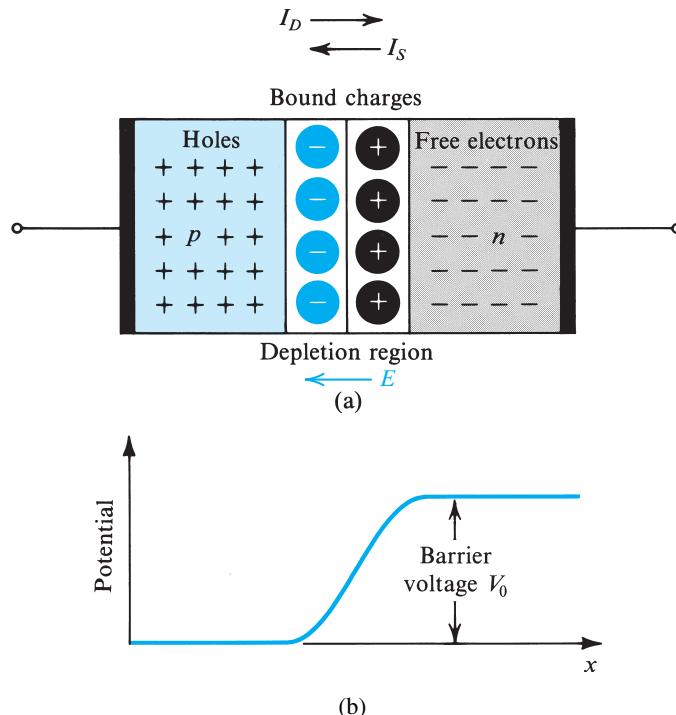
Figure 3.9 shows a *pn* junction under open-circuit conditions—that is, the external terminals are left open. The “+” signs in the *p*-type material denote the majority holes. The charge of these holes is neutralized by an equal amount of bound negative charge associated with the acceptor atoms. For simplicity, these bound charges are not shown in the diagram. Also not shown are the minority electrons generated in the *p*-type material by thermal ionization.

In the *n*-type material the majority electrons are indicated by “−” signs. Here also, the bound positive charge, which neutralizes the charge of the majority electrons, is not shown in order to keep the diagram simple. The *n*-type material also contains minority holes generated by thermal ionization but not shown in the diagram.

**The Diffusion Current  $I_D$**  Because the concentration of holes is high in the *p* region and low in the *n* region, holes diffuse across the junction from the *p* side to the *n* side. Similarly, electrons diffuse across the junction from the *n* side to the *p* side. These two current components add together to form the diffusion current  $I_D$ , whose direction is from the *p* side to the *n* side, as indicated in Fig. 3.9.

**The Depletion Region** The holes that diffuse across the junction into the *n* region quickly recombine with some of the majority electrons present there and thus disappear from the scene. This recombination process results also in the disappearance of some free electrons from the

<sup>3</sup>This terminology in fact is a carryover from that used with vacuum-tube technology, which was the technology for making diodes and other electronic devices until the invention of the transistor in 1947. This event ushered in the era of solid-state electronics, which changed not only electronics, communications, and computers but indeed the world!



**Figure 3.9** (a) The *pn* junction with no applied voltage (open-circuited terminals). (b) The potential distribution along an axis perpendicular to the junction.

*n*-type material. Thus some of the bound positive charge will no longer be neutralized by free electrons, and this charge is said to have been **uncovered**. Since recombination takes place close to the junction, there will be a region close to the junction that is *depleted of free electrons* and contains uncovered bound positive charge, as indicated in Fig. 3.9.

The electrons that diffuse across the junction into the *p* region quickly recombine with some of the majority holes there, and thus disappear from the scene. This results also in the disappearance of some majority holes, causing some of the bound negative charge to be uncovered (i.e., no longer neutralized by holes). Thus, in the *p* material close to the junction, there will be a region *depleted of holes* and containing uncovered bound negative charge, as indicated in Fig. 3.9.

From the above it follows that a **carrier-depletion region** will exist on both sides of the junction, with the *n* side of this region positively charged and the *p* side negatively charged. This carrier-depletion region—or, simply, **depletion region**—is also called the **space-charge region**. The charges on both sides of the depletion region cause an electric field  $E$  to be established across the region in the direction indicated in Fig. 3.9. Hence a potential difference results across the depletion region, with the *n* side at a positive voltage relative to the *p* side, as shown in Fig. 3.9(b). Thus the resulting electric field opposes the diffusion of holes into the *n* region and electrons into the *p* region. In fact, the voltage drop across the depletion region acts as a **barrier** that has to be overcome for holes to diffuse into the *n* region and electrons to diffuse into the *p* region. The larger the barrier voltage  $V_0$ , the smaller the number of carriers that will be able to overcome the barrier, and hence the lower the magnitude of diffusion current. Thus it is the appearance of the barrier voltage  $V_0$  that limits the carrier diffusion process. It follows that the diffusion current  $I_D$  depends strongly on the voltage drop  $V_0$  across the depletion region.

**The Drift Current  $I_s$  and Equilibrium** In addition to the current component  $I_D$  due to majority-carrier diffusion, a component due to minority-carrier drift exists across the junction. Specifically, some of the thermally generated holes in the *n* material move toward the junction and reach the edge of the depletion region. There, they experience the electric field in the depletion region, which sweeps them across that region into the *p* side. Similarly, some of the minority thermally generated electrons in the *p* material move to the edge of the depletion region and get swept by the electric field in the depletion region across that region into the *n* side. These two current components—electrons moved by drift from *p* to *n* and holes moved by drift from *n* to *p*—add together to form the drift current  $I_s$ , whose direction is from the *n* side to the *p* side of the junction, as indicated in Fig. 3.9. Since the current  $I_s$  is carried by thermally generated minority carriers, its value is strongly dependent on temperature; however, it is independent of the value of the depletion-layer voltage  $V_0$ . This is due to the fact that the drift current is determined by the number of minority carriers that make it to the edge of the depletion region; any minority carriers that manage to get to the edge of the depletion region will be swept across by  $E$  irrespective of the value of  $E$  or, correspondingly, of  $V_0$ .

Under open-circuit conditions (Fig. 3.9) no external current exists; thus the two opposite currents across the junction must be equal in magnitude:

$$I_D = I_s$$

This equilibrium condition<sup>4</sup> is maintained by the barrier voltage  $V_0$ . Thus, if for some reason  $I_D$  exceeds  $I_s$ , then more bound charge will be uncovered on both sides of the junction, the depletion layer will widen, and the voltage across it ( $V_0$ ) will increase. This in turn causes  $I_D$  to decrease until equilibrium is achieved with  $I_D = I_s$ . On the other hand, if  $I_s$  exceeds  $I_D$ , then the amount of uncovered charge will decrease, the depletion layer will narrow, and the voltage across it ( $V_0$ ) will decrease. This causes  $I_D$  to increase until equilibrium is achieved with  $I_D = I_s$ .

**The Junction Built-in Voltage** With no external voltage applied, the barrier voltage  $V_0$  across the *pn* junction can be shown to be given by<sup>5</sup>

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (3.22)$$

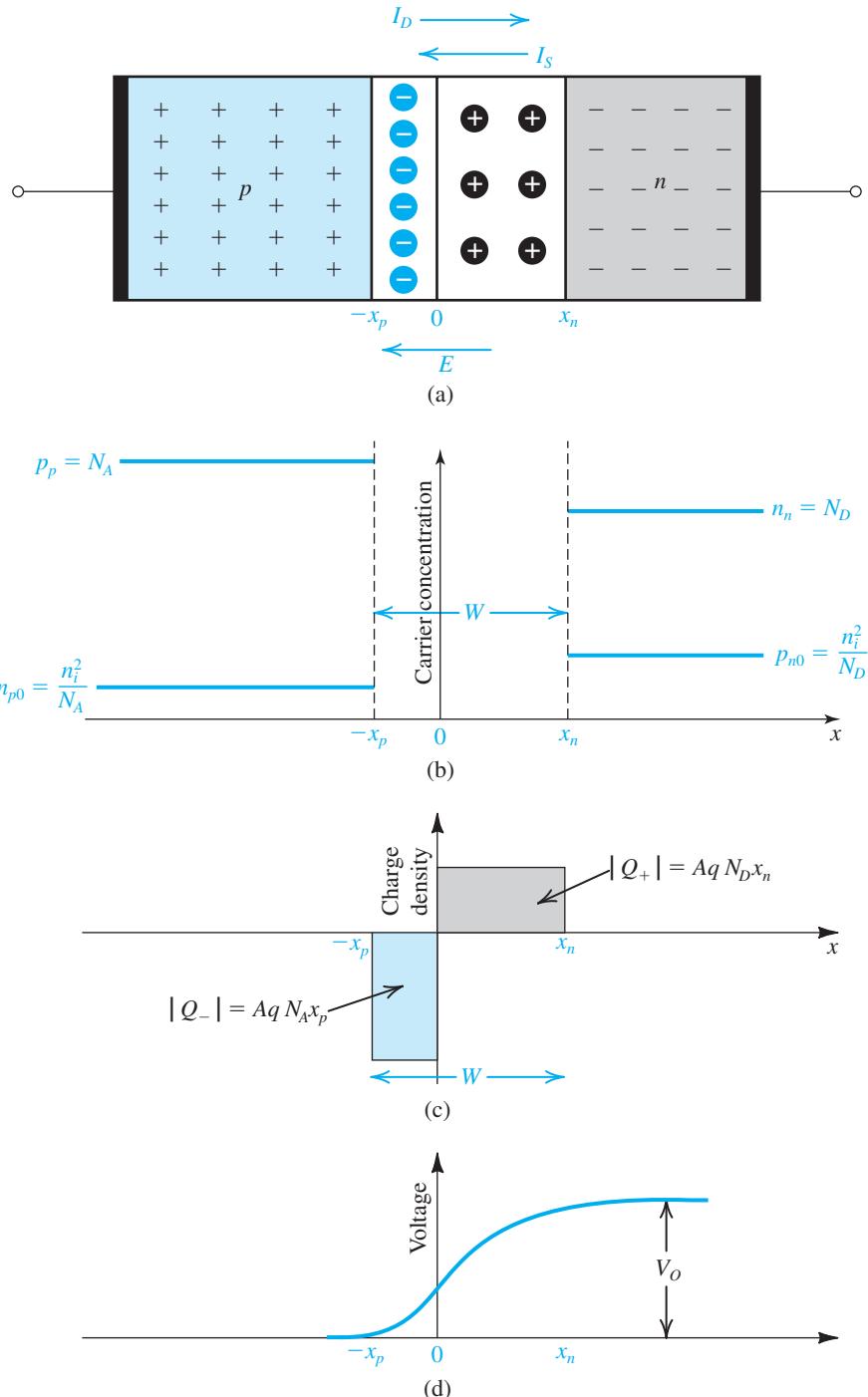
where  $N_A$  and  $N_D$  are the doping concentrations of the *p* side and *n* side of the junction, respectively. Thus  $V_0$  depends both on doping concentrations and on temperature. It is known as the **junction built-in voltage**. Typically, for silicon at room temperature,  $V_0$  is in the range of 0.6 V to 0.9 V.

When the *pn* junction terminals are left open-circuited, the voltage measured between them will be zero. That is, the voltage  $V_0$  across the depletion region *does not* appear between the junction terminals. This is because of the contact voltages existing at the metal–semiconductor junctions at the terminals, which counter and exactly balance the barrier voltage. If this were not the case, we would have been able to draw energy from the isolated *pn* junction, which would clearly violate the principle of conservation of energy.

**Width of and Charge Stored in the Depletion Region** Figure 3.10 provides further illustration of the situation that obtains in the *pn* junction when the junction is in equilibrium.

<sup>4</sup>In fact, in equilibrium the equality of drift and diffusion currents applies not just to the total currents but also to their individual components. That is, the hole drift current must equal the hole diffusion current and, similarly, the electron drift current must equal the electron diffusion current.

<sup>5</sup>The derivation of this formula and of a number of others in this chapter can be found in textbooks dealing with devices, such as that by Streetman and Bannerjee (see the reading list in Appendix I).



**Figure 3.10** (a) A *pn* junction with the terminals open-circuited. (b) Carrier concentrations; note that  $N_A > N_D$ . (c) The charge stored in both sides of the depletion region;  $Q_J = |Q_+| = |Q_-|$ . (d) The built-in voltage  $V_0$ .

In Fig. 3.10(a) we show a junction in which  $N_A > N_D$ , a typical situation in practice. This is borne out by the carrier concentration on both sides of the junction, as shown in Fig. 3.10(b). Note that we have denoted the minority-carrier concentrations in both sides by  $n_{p0}$  and  $p_{n0}$ , with the additional subscript “0” signifying equilibrium (i.e., before external voltages are applied, as will be seen in the next section). Observe that the depletion region extends in both the *p* and *n* materials and that equal amounts of charge exist on both sides ( $Q_+$  and  $Q_-$  in Fig. 3.10c). However, since usually unequal dopings  $N_A$  and  $N_D$  are used, as in the case illustrated in Fig. 3.10, the width of the depletion layer will not be the same on the two sides. Rather, to uncover the same amount of charge, the depletion layer will extend deeper into the more lightly doped material. Specifically, if we denote the width of the depletion region in the *p* side by  $x_p$  and in the *n* side by  $x_n$ , we can express the magnitude of the charge on the *n* side of the junction as

$$|Q_+| = qAx_nN_D \quad (3.23)$$

and that on the *p* side of the junction as

$$|Q_-| = qAx_pN_A \quad (3.24)$$

where  $A$  is the cross-sectional area of the junction in the plane perpendicular to the page. The charge equality condition can now be written as

$$qAx_nN_D = qAx_pN_A$$

which can be rearranged to yield

$$\frac{x_n}{x_p} = \frac{N_A}{N_D} \quad (3.25)$$

In actual practice, it is usual for one side of the junction to be much more heavily doped than the other, with the result that the depletion region exists almost entirely on one side (the lightly doped side).

The width  $W$  of the depletion layer can be shown to be given by

$$W = x_n + x_p = \sqrt{\frac{2\epsilon_s}{q} \left( \frac{1}{N_A} + \frac{1}{N_D} \right) V_0} \quad (3.26)$$

where  $\epsilon_s$  is the electrical permittivity of silicon =  $11.7\epsilon_0 = 11.7 \times 8.85 \times 10^{-14}$  F/cm =  $1.04 \times 10^{-12}$  F/cm. Typically  $W$  is in the range 0.1  $\mu\text{m}$  to 1  $\mu\text{m}$ . Eqs. (3.25) and (3.26) can be used to obtain  $x_n$  and  $x_p$  in terms of  $W$  as

$$x_n = W \frac{N_A}{N_A + N_D} \quad (3.27)$$

$$x_p = W \frac{N_D}{N_A + N_D} \quad (3.28)$$

The charge stored on either side of the depletion region can be expressed in terms of  $W$  by utilizing Eqs. (3.23) and (3.27) to obtain

$$Q_J = |Q_+| = |Q_-| \quad (3.29)$$

$$Q_J = Aq \left( \frac{N_A N_D}{N_A + N_D} \right) W \quad (3.29)$$

Finally, we can substitute for  $W$  from Eq. (3.26) to obtain

$$Q_J = A \sqrt{2\epsilon_s q \left( \frac{N_A N_D}{N_A + N_D} \right) V_0} \quad (3.30)$$

These expressions for  $Q_J$  will prove useful in subsequent sections.

**Example 3.5**

Consider a *pn* junction in equilibrium at room temperature ( $T = 300\text{ K}$ ) for which the doping concentrations are  $N_A = 10^{18}/\text{cm}^3$  and  $N_D = 10^{16}/\text{cm}^3$  and the cross-sectional area  $A = 10^{-4}\text{ cm}^2$ . Calculate  $p_p$ ,  $n_{p0}$ ,  $n_n$ ,  $p_{n0}$ ,  $V_0$ ,  $W$ ,  $x_n$ ,  $x_p$ , and  $Q_J$ . Use  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ .

**Solution**

$$p_p \simeq N_A = 10^{18}\text{ cm}^{-3}$$

$$n_{p0} = \frac{n_i^2}{p_p} \simeq \frac{n_i^2}{N_A} = \frac{(1.5 \times 10^{10})^2}{10^{18}} = 2.25 \times 10^2\text{ cm}^{-3}$$

$$n_n \simeq N_D = 10^{16}\text{ cm}^{-3}$$

$$p_{n0} = \frac{n_i^2}{n_n} \simeq \frac{n_i^2}{N_D} = \frac{(1.5 \times 10^{10})^2}{10^{16}} = 2.25 \times 10^4\text{ cm}^{-3}$$

To find  $V_0$  we use Eq. (3.22),

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

where

$$\begin{aligned} V_T &= \frac{kT}{q} = \frac{8.62 \times 10^{-5} \times 300\text{ (eV)}}{q\text{ (e)}} \\ &= 25.9 \times 10^{-3}\text{ V} \end{aligned}$$

Thus,

$$\begin{aligned} V_0 &= 25.9 \times 10^{-3} \ln\left(\frac{10^{18} \times 10^{16}}{2.25 \times 10^{20}}\right) \\ &= 0.814\text{ V} \end{aligned}$$

To determine  $W$  we use Eq. (3.26):

$$\begin{aligned} W &= \sqrt{\frac{2 \times 1.04 \times 10^{-12}}{1.6 \times 10^{-19}} \left( \frac{1}{10^{18}} + \frac{1}{10^{16}} \right) \times 0.814} \\ &= 3.27 \times 10^{-5}\text{ cm} = 0.327\text{ } \mu\text{m} \end{aligned}$$

To determine  $x_n$  and  $x_p$  we use Eqs. (3.27) and (3.28), respectively:

$$\begin{aligned} x_n &= W \frac{N_A}{N_A + N_D} \\ &= 0.327 \frac{10^{18}}{10^{18} + 10^{16}} = 0.324\text{ } \mu\text{m} \\ x_p &= W \frac{N_D}{N_A + N_D} \\ &= 0.327 \frac{10^{16}}{10^{18} + 10^{16}} = 0.003\text{ } \mu\text{m} \end{aligned}$$

Finally, to determine the charge stored on either side of the depletion region, we use Eq. (3.29):

$$\begin{aligned} Q_J &= 10^{-4} \times 1.6 \times 10^{-19} \left( \frac{10^{18} \times 10^{16}}{10^{18} + 10^{16}} \right) \times 0.327 \times 10^{-4} \\ &= 5.18 \times 10^{-12}\text{ C} = 5.18\text{ pC} \end{aligned}$$

## EXERCISES

**3.7** Show that

$$V_0 = \frac{1}{2} \left( \frac{q}{\epsilon_s} \right) \left( \frac{N_A N_D}{N_A + N_D} \right) W^2$$

**3.8** Show that for a *pn* junction in which the *p* side is much more heavily doped than the *n* side (i.e.,  $N_A \gg N_D$ ), referred to as a  $p^+n$  diode, Eqs. (3.26), (3.27), (3.28), (3.29), and (3.30) can be simplified as follows:

$$W \simeq \sqrt{\frac{2\epsilon_s}{qN_D} V_0} \quad (3.26')$$

$$x_n \simeq W \quad (3.27')$$

$$x_p \simeq W / (N_A / N_D) \quad (3.28')$$

$$Q_J \simeq A q N_D W \quad (3.29')$$

$$Q_J \simeq A \sqrt{2\epsilon_s q N_D V_0} \quad (3.30')$$

**3.9** If in the fabrication of the *pn* junction in Example 3.5, it is required to increase the minority-carrier concentration in the *n* region by a factor of 2, what must be done?

**Ans.** Lower  $N_D$  by a factor of 2.

## 3.5 The *pn* Junction with an Applied Voltage

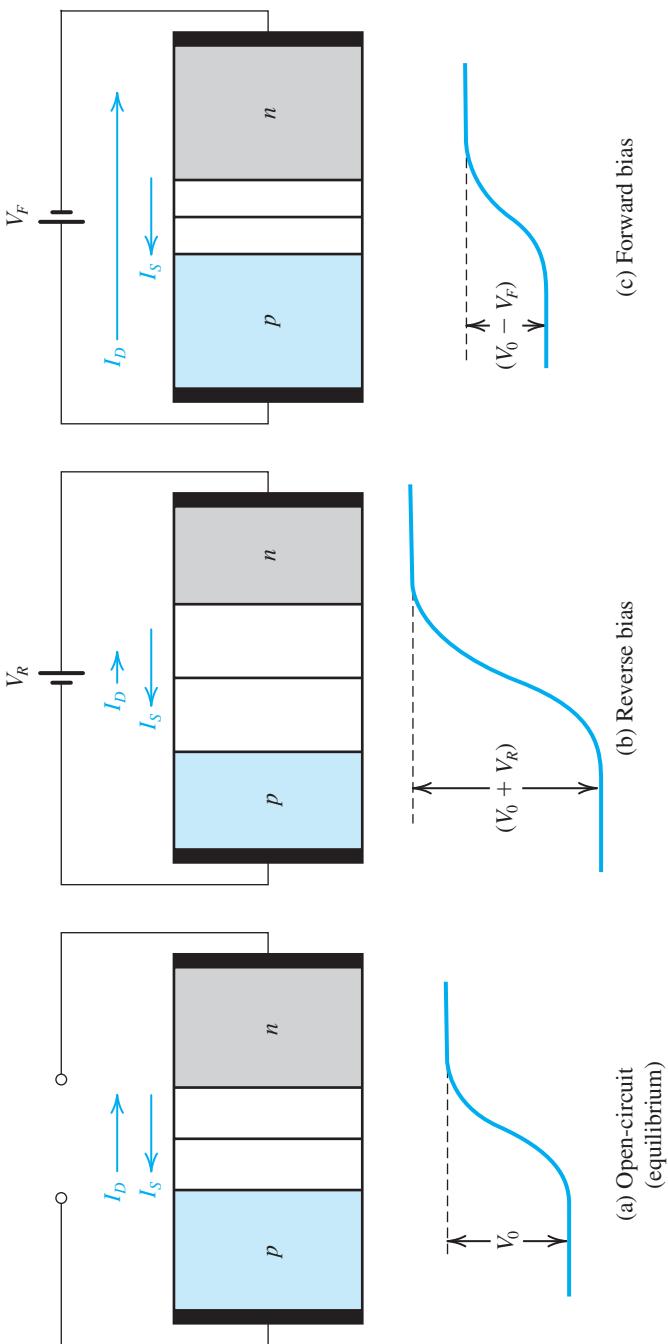
Having studied the open-circuited *pn* junction in detail, we are now ready to apply a dc voltage between its two terminals to find its electrical conduction properties. If the voltage is applied so that the *p* side is made more positive than the *n* side, it is referred to as a forward-bias<sup>6</sup> voltage. Conversely, if our applied dc voltage is such that it makes the *n* side more positive than the *p* side, it is said to be a reverse-bias voltage. As will be seen, the *pn* junction exhibits vastly different conduction properties in its forward and reverse directions.

Our plan is as follows. We begin by a simple qualitative description in Section 3.5.1 and then consider an analytical description of the *i*-*v* characteristic of the junction in Section 3.5.2.

### 3.5.1 Qualitative Description of Junction Operation

Figure 3.11 shows the *pn* junction under three different conditions: (a) the open-circuit or equilibrium condition studied in the previous section; (b) the reverse-bias condition, where a dc voltage  $V_R$  is applied; and (c) the forward-bias condition, where a dc voltage  $V_F$  is applied.

<sup>6</sup>For the time being, we take the term *bias* to refer simply to the application of a dc voltage. We will see in later chapters that it has a deeper meaning in the design of electronic circuits.



**Figure 3.11** The *pn* junction in: (a) equilibrium; (b) reverse bias; (c) forward bias.

Observe that in the open-circuit case, a barrier voltage  $V_0$  develops, making *n* more positive than *p*, and limiting the diffusion current  $I_D$  to a value exactly equal to the drift current  $I_S$ , thus resulting in a zero current at the junction terminals, as should be the case, since the terminals are open-circuited. Also, as mentioned previously, the barrier voltage  $V_0$ , though it establishes the current equilibrium across the junction, does *not* in fact appear between the junction terminals.

Consider now the reverse-bias case in (b). The externally applied reverse-bias voltage  $V_R$  is in the direction to add to the barrier voltage, and it does, thus increasing the effective barrier voltage to  $(V_0 + V_R)$  as shown. This reduces the number of holes that diffuse into the *n* region and the number of electrons that diffuse into the *p* region. The end result is that the diffusion current  $I_D$  is dramatically reduced. As will be seen shortly, a reverse-bias voltage of a volt or so is sufficient to cause  $I_D \simeq 0$ , and the current across the junction and through the external circuit will be equal to  $I_S$ . Recalling that  $I_S$  is the current due to the drift across the depletion region of the thermally generated minority carriers, we expect  $I_S$  to be very small and to be strongly dependent on temperature. We will show this to be the case very shortly. We thus conclude that in the reverse direction, the *pn* junction conducts a very small and almost-constant current equal to  $I_S$ .

Before leaving the reverse-bias case, observe that the increase in barrier voltage will be accompanied by a corresponding increase in the stored uncovered charge on both sides of the depletion region. This in turn means a wider depletion region, needed to uncover the additional charge required to support the larger barrier voltage  $(V_0 + V_R)$ . Analytically, these results can be obtained easily by a simple extension of the results of the equilibrium case. Thus the width of the depletion region can be obtained by replacing  $V_0$  in Eq. (3.26) by  $(V_0 + V_R)$ ,

$$W = x_n + x_p = \sqrt{\frac{2\epsilon_s}{q} \left( \frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 + V_R)} \quad (3.31)$$

and the magnitude of the charge stored on either side of the depletion region can be determined by replacing  $V_0$  in Eq. (3.30) by  $(V_0 + V_R)$ ,

$$Q_J = A \sqrt{2\epsilon_s q \left( \frac{N_A N_D}{N_A + N_D} \right) (V_0 + V_R)} \quad (3.32)$$

We next consider the forward-bias case shown in Fig. 3.11(c). Here the applied voltage  $V_F$  is in the direction that subtracts from the built-in voltage  $V_0$ , resulting in a reduced barrier voltage  $(V_0 - V_F)$  across the depletion region. This reduced barrier voltage will be accompanied by reduced depletion-region charge and correspondingly narrower depletion-region width  $W$ . Most importantly, the lowering of the barrier voltage will enable more holes to diffuse from *p* to *n* and more electrons to diffuse from *n* to *p*. Thus the diffusion current  $I_D$  increases substantially and, as will be seen shortly, can become many orders of magnitude larger than the drift current  $I_S$ . The current  $I$  in the external circuit is of course the difference between  $I_D$  and  $I_S$ ,

$$I = I_D - I_S$$

and it flows in the forward direction of the junction, from *p* to *n*. We thus conclude that the *pn* junction can conduct a substantial current in the forward-bias region and that current is mostly a diffusion current whose value is determined by the forward-bias voltage  $V_F$ .

### 3.5.2 The Current–Voltage Relationship of the Junction

We are now ready to find an analytical expression that describes the current–voltage relationship of the *pn* junction. In the following we consider a junction operating with a forward applied voltage  $V$  and derive an expression for the current  $I$  that flows in the forward direction (from *p* to *n*). However, our derivation is general and will be seen to yield the reverse current when the applied voltage  $V$  is made negative.

From the qualitative description above we know that a forward-bias voltage  $V$  subtracts from the built-in voltage  $V_0$ , thus resulting in a lower barrier voltage ( $V_0 - V$ ). The lowered barrier in turn makes it possible for a greater number of holes to overcome the barrier and diffuse into the *n* region. A similar statement can be made about electrons from the *n* region diffusing into the *p* region.

Let us now consider the holes injected into the *n* region. The concentration of holes in the *n* region at the edge of the depletion region will increase considerably. In fact, an important result from device physics shows that the steady-state concentration at the edge of the depletion region will be

$$p_n(x_n) = p_{n0} e^{V/V_T} \quad (3.33)$$

That is, the concentration of the minority holes increases from the equilibrium value of  $p_{n0}$  (see Fig. 3.10) to the much larger value determined by the value of  $V$ , given by Eq. (3.33).

We describe this situation as follows: The forward-bias voltage  $V$  results in an **excess concentration** of minority holes at  $x = x_n$ , given by

$$\begin{aligned} \text{Excess concentration} &= p_{n0} e^{V/V_T} - p_{n0} \\ &= p_{n0} (e^{V/V_T} - 1) \end{aligned} \quad (3.34)$$

The increase in minority-carrier concentration in Eqs. (3.33) and (3.34) occurs at the edge of the depletion region ( $x = x_n$ ). As the injected holes diffuse into the *n* material, some will recombine with the majority electrons and disappear. Thus, the excess hole concentration will decay exponentially with distance. As a result, the total hole concentration in the *n* material will be given by

$$p_n(x) = p_{n0} + (\text{Excess concentration}) e^{-(x-x_n)/L_p}$$

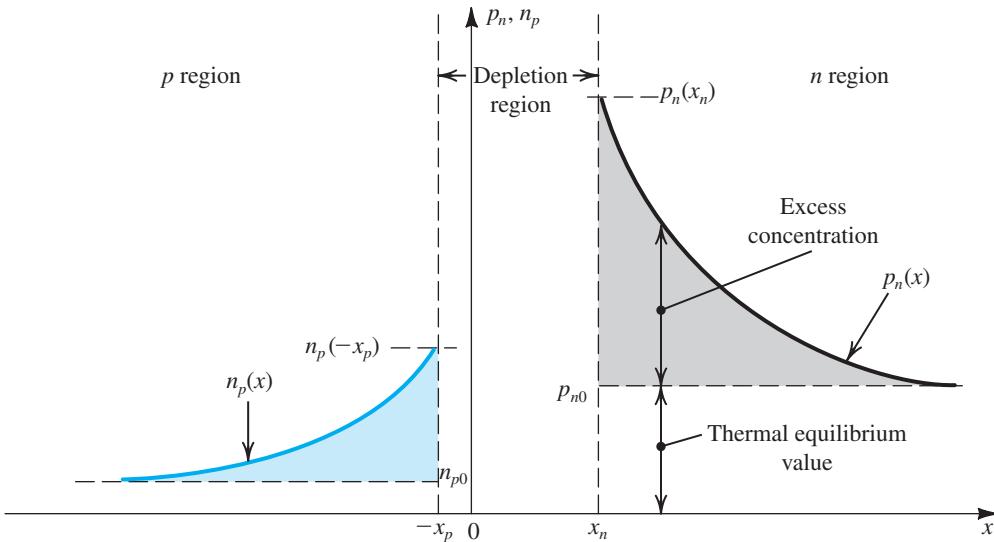
Substituting for the “Excess concentration” from Eq. (3.34) gives

$$p_n(x) = p_{n0} + p_{n0} (e^{V/V_T} - 1) e^{-(x-x_n)/L_p} \quad (3.35)$$

The exponential decay is characterized by the constant  $L_p$ , which is called the **diffusion length** of holes in the *n* material. The smaller the value of  $L_p$ , the faster the injected holes will recombine with the majority electrons, resulting in a steeper decay of minority-carrier concentration.

Figure 3.12 shows the steady-state minority-carrier concentration profiles on both sides of a *pn* junction in which  $N_A \gg N_D$ . Let’s stay a little longer with the diffusion of holes into the *n* region. Note that the shaded region under the exponential represents the excess minority carriers (holes). From our study of diffusion in Section 3.3, we know that the establishment of a carrier concentration profile such as that in Fig. 3.12 is essential to support a steady-state diffusion current. In fact, we can now find the value of the hole–diffusion current density by applying Eq. (3.19),

$$J_p(x) = -qD_p \frac{dp_n(x)}{dx}$$



**Figure 3.12** Minority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* region is more heavily doped than the *n* region;  $N_A \gg N_D$ .

Substituting for  $p_n(x)$  from Eq. (3.35) gives

$$J_p(x) = q \left( \frac{D_p}{L_p} \right) p_{n0} (e^{V/V_T} - 1) e^{-(x-x_n)/L_p} \quad (3.36)$$

As expected,  $J_p(x)$  is highest at  $x = x_n$ ,

$$J_p(x_n) = q \left( \frac{D_p}{L_p} \right) p_{n0} (e^{V/V_T} - 1) \quad (3.37)$$

and decays exponentially for  $x > x_n$ , as the minority holes recombine with the majority electrons. This recombination, however, means that the majority electrons will have to be replenished by a current that injects electrons from the external circuit into the *n* region of the junction. This latter current component has the same direction as the hole current (because electrons moving from right to left give rise to current in the direction from left to right). It follows that as  $J_p(x)$  decreases, the electron current component increases by exactly the same amount, making the total current in the *n* material constant at the value given by Eq. (3.37).

An exactly parallel development can be applied to the electrons that are injected from the *n* to the *p* region, resulting in an electron diffusion current given by a simple adaptation of Eq. (3.37),

$$J_n(-x_p) = q \left( \frac{D_n}{L_n} \right) n_{p0} (e^{V/V_T} - 1) \quad (3.38)$$

Now, although the currents in Eqs. (3.37) and (3.38) are found at the two edges of the depletion region, their values do not change in the depletion region. Thus we can drop the location descriptors  $(x_n)$ ,  $(-x_p)$ , add the two current densities, and multiply by the junction area  $A$  to

obtain the total current  $I$  as

$$I = A(J_p + J_n)$$

$$I = Aq \left( \frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0} \right) (e^{V/V_T} - 1)$$

Substituting for  $p_{n0} = n_i^2/N_D$  and for  $n_{p0} = n_i^2/N_A$  gives

$$I = Aqn_i^2 \left( \frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right) (e^{V/V_T} - 1) \quad (3.39)$$

From this equation we note that for a negative  $V$  (reverse bias) with a magnitude of a few times  $V_T$  (25.9 mV), the exponential term becomes essentially zero, and the current across the junction becomes negative and constant. From our qualitative description in Section 3.5.1, we know that this current must be  $I_S$ . Thus,

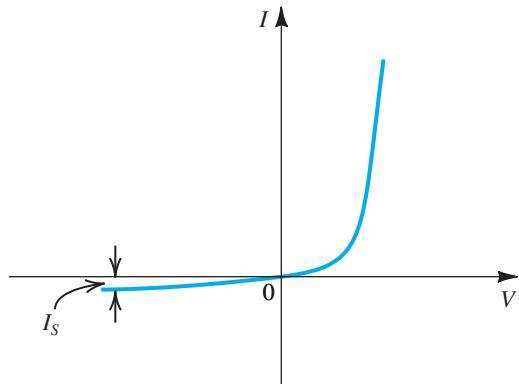
➤  $I = I_S (e^{V/V_T} - 1)$  (3.40)

where

➤  $I_S = Aqn_i^2 \left( \frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right)$  (3.41)

Figure 3.13 shows the  $I$ - $V$  characteristic of the  $pn$  junction (Eq. 3.40). Observe that in the reverse direction the current saturates at a value equal to  $-I_S$ . For this reason,  $I_S$  is given the name **saturation current**. From Eq. (3.41) we see that  $I_S$  is directly proportional to the cross-sectional area  $A$  of the junction. Thus, another name for  $I_S$ , one we prefer to use in this book, is the **junction scale current**. Typical values for  $I_S$ , for junctions of various areas, range from  $10^{-18}$  A to  $10^{-12}$  A.

Besides being proportional to the junction area  $A$ , the expression for  $I_S$  in Eq. (3.41) indicates that  $I_S$  is proportional to  $n_i^2$ , which is a very strong function of temperature (see Eq. 3.2).



**Figure 3.13** The  $pn$  junction  $I$ - $V$  characteristic.

### Example 3.6

For the *pn* junction considered in Example 3.5 for which  $N_A = 10^{18}/\text{cm}^3$ ,  $N_D = 10^{16}/\text{cm}^3$ ,  $A = 10^{-4}\text{cm}^2$ , and  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ , let  $L_p = 5 \mu\text{m}$ ,  $L_n = 10 \mu\text{m}$ ,  $D_p$  (in the *n* region) =  $10 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $D_n$  (in the *p* region) =  $18 \text{ cm}^2/\text{V}\cdot\text{s}$ . The *pn* junction is forward biased and conducting a current  $I = 0.1 \text{ mA}$ . Calculate: (a)  $I_s$ ; (b) the forward-bias voltage  $V$ ; and (c) the component of the current  $I$  due to hole injection and that due to electron injection across the junction.

#### Solution

(a) Using Eq. (3.41), we find  $I_s$  as

$$\begin{aligned} I_s &= 10^{-4} \times 1.6 \times 10^{-19} \times \left(1.5 \times 10^{10}\right)^2 \\ &\quad \times \left(\frac{10}{5 \times 10^{-4} \times 10^{16}} + \frac{18}{10 \times 10^{-4} \times 10^{18}}\right) \\ &= 7.3 \times 10^{-15} \text{ A} \end{aligned}$$

(b) In the forward direction,

$$\begin{aligned} I &= I_s (e^{V/V_T} - 1) \\ &\simeq I_s e^{V/V_T} \end{aligned}$$

Thus,

$$V = V_T \ln\left(\frac{I}{I_s}\right)$$

For  $I = 0.1 \text{ mA}$ ,

$$\begin{aligned} V &= 25.9 \times 10^{-3} \ln\left(\frac{0.1 \times 10^{-3}}{7.3 \times 10^{-15}}\right) \\ &= 0.605 \text{ V} \end{aligned}$$

(c) The hole-injection component of  $I$  can be found using Eq. (3.37)

$$\begin{aligned} I_p &= Aq \frac{D_p}{L_p} p_{n0} (e^{V/V_T} - 1) \\ &= Aq \frac{D_p}{L_p} \frac{n_i^2}{N_D} (e^{V/V_T} - 1) \end{aligned}$$

Similarly,  $I_n$  can be found using Eq. (3.39),

$$I_n = Aq \frac{D_n}{L_n} \frac{n_i^2}{N_A} (e^{V/V_T} - 1)$$

Thus,

$$\frac{I_p}{I_n} = \left(\frac{D_p}{D_n}\right) \left(\frac{L_n}{L_p}\right) \left(\frac{N_A}{N_D}\right)$$

For our case,

$$\frac{I_p}{I_n} = \frac{10}{18} \times \frac{10}{5} \times \frac{10^{18}}{10^{16}} = 1.11 \times 10^2 = 111$$

**Example 3.6** *continued*

Thus most of the current is conducted by holes injected into the *n* region.

Specifically,

$$I_p = \frac{111}{112} \times 0.1 = 0.0991 \text{ mA}$$

$$I_n = \frac{1}{112} \times 0.1 = 0.0009 \text{ mA}$$

This stands to reason, since the *p* material has a doping concentration 100 times that of the *n* material.

## EXERCISES

- 3.10** Show that if  $N_A \gg N_D$ ,

$$I_S \simeq A q n_i^2 \frac{D_p}{L_p N_D}$$

- 3.11** For the *pn* junction in Example 3.6, find the value of  $I_S$  and that of the current  $I$  at  $V = 0.605$  V (same voltage found in Example 3.6 at a current  $I = 0.1$  mA) if  $N_D$  is reduced by a factor of 2.

**Ans.**  $1.46 \times 10^{-14}$  A; 0.2 mA

- 3.12** For the *pn* junction considered in Examples 3.5 and 3.6, find the width of the depletion region  $W$  corresponding to the forward-bias voltage found in Example 3.6. (*Hint:* Use the formula in Eq. (3.31) with  $V_R$  replaced with  $-V_F$ .)

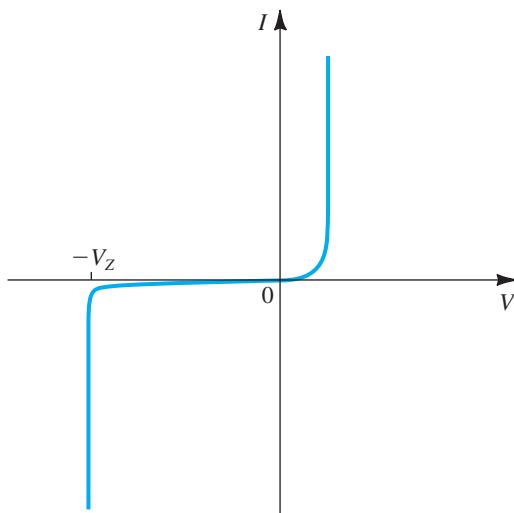
**Ans.** 0.166 μm

- 3.13** For the *pn* junction considered in Examples 3.5 and 3.6, find the width of the depletion region  $W$  and the charge stored in the depletion region  $Q_J$  when a 2-V reverse bias is applied. Also find the value of the reverse current  $I$ .

**Ans.** 0.608 μm; 9.63 pC;  $7.3 \times 10^{-15}$  A

### 3.5.3 Reverse Breakdown

The description of the operation of the *pn* junction in the reverse direction, and the  $I$ – $V$  relationship of the junction in Eq. (3.40), indicate that at a reverse-bias voltage  $-V$ , with  $V \gg V_T$ , the reverse current that flows across the junction is approximately equal to  $I_S$  and thus is very small. However, as the magnitude of the reverse-bias voltage  $V$  is increased, a value is reached at which a very large reverse current flows as shown in Fig. 3.14. Observe that as  $V$  reaches the value  $V_Z$ , the dramatic increase in reverse current is accompanied by a very small increase in the reverse voltage; that is, the reverse voltage across the junction



**Figure 3.14** The  $I-V$  characteristic of the *pn* junction showing the rapid increase in reverse current in the breakdown region.

remains very close to the value  $V_Z$ . The phenomenon that occurs at  $V = V_Z$  is known as **junction breakdown**. It is not a destructive phenomenon. That is, the *pn* junction can be repeatedly operated in the breakdown region without a permanent effect on its characteristics. This, however, is predicated on the assumption that the magnitude of the reverse-breakdown current is limited by the external circuit to a “safe” value. The “safe” value is one that results in the limitation of the power dissipated in the junction to a safe, allowable level.

There are two possible mechanisms for *pn* junction breakdown: the **zener effect**<sup>7</sup> and the **avalanche effect**. If a *pn* junction breaks down with a breakdown voltage  $V_Z < 5$  V, the breakdown mechanism is usually the zener effect. Avalanche breakdown occurs when  $V_Z$  is greater than approximately 7 V. For junctions that break down between 5 V and 7 V, the breakdown mechanism can be either the zener or the avalanche effect or a combination of the two.

Zener breakdown occurs when the electric field in the depletion layer increases to the point of breaking covalent bonds and generating electron–hole pairs. The electrons generated in this way will be swept by the electric field into the *n* side and the holes into the *p* side. Thus these electrons and holes constitute a reverse current across the junction. Once the zener effect starts, a large number of carriers can be generated, with a negligible increase in the junction voltage. Thus the reverse current in the breakdown region will be large and its value must be determined by the external circuit, while the reverse voltage appearing between the diode terminals will remain close to the specified breakdown voltage  $V_Z$ .

The other breakdown mechanism, avalanche breakdown, occurs when the minority carriers that cross the depletion region under the influence of the electric field gain sufficient kinetic energy to be able to break covalent bonds in atoms with which they collide. The carriers liberated by this process may have sufficiently high energy to be able to cause other carriers to be liberated in another ionizing collision. This process keeps repeating in the fashion of an avalanche, with the result that many carriers are created that are able to support any value of

<sup>7</sup> Named after an early worker in the area. Note that the subscript *Z* in  $V_Z$  denotes *zener*. We will use  $V_Z$  to denote the breakdown voltage whether the breakdown mechanism is the zener effect or the avalanche effect.

reverse current, as determined by the external circuit, with a negligible change in the voltage drop across the junction.

As will be seen in Chapter 4, some *pn* junction diodes are fabricated to operate specifically in the breakdown region, where use is made of the nearly constant voltage  $V_z$ .

## 3.6 Capacitive Effects in the *pn* Junction

There are two charge-storage mechanisms in the *pn* junction. One is associated with the charge stored in the depletion region, and the other is associated with the minority-carrier charge stored in the *n* and *p* materials as a result of the concentration profiles established by carrier injection. While the first is easier to see when the *pn* junction is reverse biased, the second is in effect only when the junction is forward biased.

### 3.6.1 Depletion or Junction Capacitance

When a *pn* junction is reverse biased with a voltage  $V_R$ , the charge stored on either side of the depletion region is given by Eq. (3.32),

$$Q_J = A \sqrt{2\epsilon_s q \frac{N_A N_D}{N_A + N_D} (V_0 + V_R)}$$

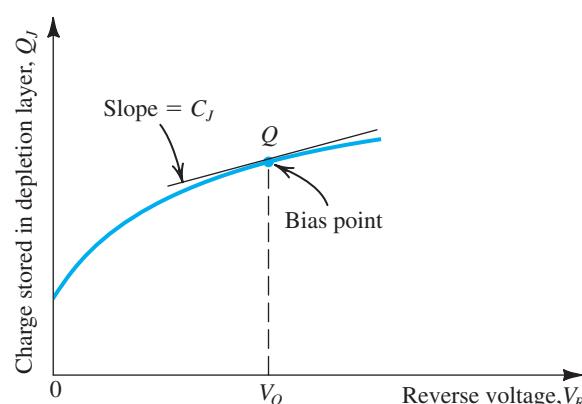
Thus, for a given *pn* junction,

$$Q_J = \alpha \sqrt{V_0 + V_R} \quad (3.42)$$

where  $\alpha$  is given by

$$\alpha = A \sqrt{2\epsilon_s q \frac{N_A N_D}{N_A + N_D}} \quad (3.43)$$

Thus  $Q_J$  is nonlinearly related to  $V_R$ , as shown in Fig. 3.15. This nonlinear relationship makes it difficult to define a capacitance that accounts for the need to change  $Q_J$  whenever  $V_R$  is



**Figure 3.15** The charge stored on either side of the depletion layer as a function of the reverse voltage  $V_R$ .

changed. We can, however, assume that the junction is operating at a point such as  $Q$ , as indicated in Fig. 3.15, and define a capacitance  $C_j$  that relates the change in the charge  $Q_j$  to a change in the voltage  $V_R$ ,

$$C_j = \frac{dQ_j}{dV_R} \Big|_{V_R=V_Q} \quad (3.44)$$

This incremental-capacitance approach turns out to be quite useful in electronic circuit design, as we shall see throughout this book.

Using Eq. (3.44) together with Eq. (3.42) yields

$$C_j = \frac{\alpha}{2\sqrt{V_0 + V_R}} \quad (3.45)$$

The value of  $C_j$  at zero reverse bias can be obtained from Eq. (3.45) as

$$C_{j0} = \frac{\alpha}{2\sqrt{V_0}} \quad (3.46)$$

which enables us to express  $C_j$  as

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_0}}} \quad (3.47)$$

where  $C_{j0}$  is given by Eq. (3.46) or alternatively if we substitute for  $\alpha$  from Eq. (3.43) by

$$C_{j0} = A \sqrt{\left(\frac{\epsilon_s q}{2}\right) \left(\frac{N_A N_D}{N_A + N_D}\right) \left(\frac{1}{V_0}\right)} \quad (3.48)$$

Before leaving the subject of depletion-region or junction capacitance we point out that in the *pn* junction we have been studying, the doping concentration is made to change abruptly at the junction boundary. Such a junction is known as an **abrupt junction**. There is another type of *pn* junction in which the carrier concentration is made to change gradually from one side of the junction to the other. To allow for such a **graded junction**, the formula for the junction capacitance (Eq. 3.47) can be written in the more general form

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{V_0}\right)^m} \quad (3.49)$$

where  $m$  is a constant called the **grading coefficient**, whose value ranges from  $1/3$  to  $1/2$  depending on the manner in which the concentration changes from the *p* to the *n* side.

**EXERCISE**

**3.14** For the *pn* junction considered in Examples 3.5 and 3.6, find  $C_{j0}$  and  $C_j$  at  $V_R = 2$  V. Recall that

$V_0 = 0.814$  V,  $N_A = 10^{18}/\text{cm}^3$ ,  $N_D = 10^{16}/\text{cm}^3$ , and  $A = 10^{-4} \text{ cm}^2$ .

**Ans.** 3.2 pF; 1.7 pF

### 3.6.2 Diffusion Capacitance

Consider a forward-biased *pn* junction. In steady state, minority-carrier distributions in the *p* and *n* materials are established, as shown in Fig. 3.12. Thus a certain amount of excess minority-carrier charge is stored in each of the *p* and *n* bulk regions (outside the depletion region). If the terminal voltage  $V$  changes, this charge will have to change before a new steady state is achieved. This charge-storage phenomenon gives rise to another capacitive effect, distinctly different from that due to charge storage in the depletion region.

To calculate the excess minority-carrier charge, refer to Fig. 3.12. The excess hole charge stored in the *n* region can be found from the shaded area under the exponential as follows:<sup>8</sup>

$$\begin{aligned} Q_p &= Aq \times \text{shaded area under the } p_n(x) \text{ curve} \\ &= Aq[p_n(x_n) - p_{n0}]L_p \end{aligned}$$

Substituting for  $p_n(x_n)$  from Eq. (3.33) and using Eq. (3.37) enables us to express  $Q_p$  as

$$Q_p = \frac{L_p^2}{D_p} I_p \quad (3.50)$$

The factor  $(L_p^2/D_p)$  that relates  $Q_p$  to  $I_p$  is a useful device parameter that has the dimension of time (s) and is denoted  $\tau_p$

➤  $\tau_p = \frac{L_p^2}{D_p} \quad (3.51)$

Thus,

➤  $Q_p = \tau_p I_p \quad (3.52)$

The time constant  $\tau_p$  is known as the excess **minority-carrier (hole) lifetime**. It is the average time it takes for a hole injected into the *n* region to recombine with a majority electron. This definition of  $\tau_p$  implies that the entire charge  $Q_p$  disappears and has to be replenished every  $\tau_p$  seconds. The current that accomplishes the replenishing is  $I_p = Q_p/\tau_p$ . This is an alternate derivation for Eq. (3.52).

---

<sup>8</sup>Recall that the area under an exponential curve  $Ae^{-x/B}$  is equal to  $AB$ .

A relationship similar to that in Eq. (3.52) can be developed for the electron charge stored in the *p* region,

$$Q_n = \tau_n I_n \quad (3.53)$$

where  $\tau_n$  is the electron lifetime in the *p* region. The total excess minority-carrier charge can be obtained by adding together  $Q_p$  and  $Q_n$ ,

$$Q = \tau_p I_p + \tau_n I_n \quad (3.54)$$

This charge can be expressed in terms of the diode current  $I = I_p + I_n$  as

$$Q = \tau_T I \quad (3.55)$$

where  $\tau_T$  is called the **mean transit time** of the junction. Obviously,  $\tau_T$  is related to  $\tau_p$  and  $\tau_n$ . Furthermore, for most practical devices, one side of the junction is much more heavily doped than the other. For instance, if  $N_A \gg N_D$ , one can show that  $I_p \gg I_n$ ,  $I \simeq I_p$ ,  $Q_p \gg Q_n$ ,  $Q \simeq Q_p$ , and thus  $\tau_T \simeq \tau_p$ .

For small changes around a bias point, we can define an **incremental diffusion capacitance**  $C_d$  as

$$C_d = \frac{dQ}{dV} \quad (3.56)$$

and can show that

$$C_d = \left( \frac{\tau_T}{V_T} \right) I \quad (3.57)$$

where  $I$  is the forward-bias current. Note that  $C_d$  is directly proportional to the forward current  $I$  and thus is negligibly small when the diode is reverse biased. Also note that to keep  $C_d$  small, the transit time  $\tau_T$  must be made small, an important requirement for a *pn* junction intended for high-speed or high-frequency operation.

## EXERCISES

- 3.15** Use the definition of  $C_d$  in Eq. (3.56) to derive the expression in Eq. (3.57) by means of Eqs. (3.55) and (3.40).
- 3.16** For the *pn* junction considered in Examples 3.5 and 3.6 for which  $D_p = 10 \text{ cm}^2/\text{V} \cdot \text{s}$ , and  $L_p = 5 \mu\text{m}$ , find  $\tau_p$  and  $C_d$  at a forward-bias current of 0.1 mA. Recall that for this junction,  $I_p \simeq I$ .
- Ans.** 25 ns; 96.5 pF

## Summary

- Today's microelectronics technology is almost entirely based on the semiconductor material silicon. If a circuit is to be fabricated as a monolithic integrated circuit (IC) it is made using a single silicon crystal, no matter how large the circuit is (a recent chip contains 4.31 billion transistors).
- In a crystal of intrinsic or pure silicon, the atoms are held in position by covalent bonds. At very low temperatures, all the bonds are intact, and no charge carriers are available to conduct electrical current. Thus, at such low temperatures, silicon behaves as an insulator.
- At room temperature, thermal energy causes some of the covalent bonds to break, thus generating free electrons and holes that become available for current conduction.
- Current in semiconductors is carried by free electrons and holes. Their numbers are equal and relatively small in intrinsic silicon.
- The conductivity of silicon can be increased dramatically by introducing small amounts of appropriate impurity materials into the silicon crystal in a process called doping.
- There are two kinds of doped semiconductor: *n*-type, in which electrons are abundant, and *p*-type, in which holes are abundant.
- There are two mechanisms for the transport of charge carriers in semiconductors: drift and diffusion.
- Carrier drift results when an electric field  $E$  is applied across a piece of silicon. The electric field accelerates the holes in the direction of  $E$  and the electrons in the direction opposite to  $E$ . These two current components add together to produce a drift current in the direction of  $E$ .
- Carrier diffusion occurs when the concentration of charge carriers is made higher in one part of the silicon crystal than in other parts. To establish a steady-state diffusion current, a carrier concentration gradient must be maintained in the silicon crystal.
- A basic semiconductor structure is the *pn* junction. It is fabricated in a silicon crystal by creating a *p* region in close proximity to an *n* region. The *pn* junction is a diode and plays a dominant role in the structure and operation of transistors.
- When the terminals of the *pn* junction are left open, no current flows externally. However, two equal and opposite currents,  $I_D$  and  $I_S$ , flow across the junction, and equilibrium is maintained by a built-in voltage  $V_0$  that develops across the junction, with the *n* side positive relative to the *p* side. Note, however, that the voltage across an open junction is 0 V, since  $V_0$  is canceled by potentials appearing at the metal-to-semiconductor connection interfaces.
- The voltage  $V_0$  appears across the depletion region, which extends on both sides of the junction.
- The diffusion current  $I_D$  is carried by holes diffusing from *p* to *n* and electrons diffusing from *n* to *p*.  $I_D$  flows from *p* to *n*, which is the forward direction of the junction. Its value depends on  $V_0$ .
- The drift current  $I_S$  is carried by thermally generated minority electrons in the *p* material that are swept across the depletion layer into the *n* side, and by thermally generated minority holes in the *n* side that are swept across the depletion region into the *p* side.  $I_S$  flows from *n* to *p*, in the reverse direction of the junction, and its value is a strong function of temperature but independent of  $V_0$ .
- Forward biasing the *pn* junction, that is, applying an external voltage  $V$  that makes *p* more positive than *n*, reduces the barrier voltage to  $V_0 - V$  and results in an exponential increase in  $I_D$  while  $I_S$  remains unchanged. The net result is a substantial current  $I = I_D - I_S$  that flows across the junction and through the external circuit.
- Applying a negative  $V$  reverse biases the junction and increases the barrier voltage, with the result that  $I_D$  is reduced to almost zero and the net current across the junction becomes the very small reverse current  $I_S$ .
- If the reverse voltage is increased in magnitude to a value  $V_Z$  specific to the particular junction, the junction breaks down, and a large reverse current flows. The value of the reverse current must be limited by the external circuit.
- Whenever the voltage across a *pn* junction is changed, some time has to pass before steady state is reached. This is due to the charge-storage effects in the junction, which are modeled by two capacitances: the junction capacitance  $C_j$  and the diffusion capacitance  $C_d$ .
- For future reference, we present in Table 3.1 a summary of pertinent relationships and the values of physical constants.

**Table 3.1** Summary of Important Equations

Quantity	Relationship	Values of Constants and Parameters (for Intrinsic Si at $T = 300$ K)
Carrier concentration in intrinsic silicon ( $\text{cm}^{-3}$ )	$n_i = BT^{3/2} e^{-E_g/2kT}$	$B = 7.3 \times 10^{15} \text{ cm}^{-3}\text{K}^{-3/2}$ $E_g = 1.12 \text{ eV}$ $k = 8.62 \times 10^{-5} \text{ eV/K}$ $n_i = 1.5 \times 10^{10}/\text{cm}^3$
Diffusion current density ( $\text{A/cm}^2$ )	$J_p = -qD_p \frac{dp}{dx}$ $J_n = qD_n \frac{dn}{dx}$	$q = 1.60 \times 10^{-19} \text{ coulomb}$ $D_p = 12 \text{ cm}^2/\text{s}$ $D_n = 34 \text{ cm}^2/\text{s}$
Drift current density ( $\text{A/cm}^2$ )	$J_{\text{drift}} = q(p\mu_p + n\mu_n)E$	$\mu_p = 480 \text{ cm}^2/\text{V}\cdot\text{s}$ $\mu_n = 1350 \text{ cm}^2/\text{V}\cdot\text{s}$
Resistivity ( $\Omega \cdot \text{cm}$ )	$\rho = 1/[q(p\mu_p + n\mu_n)]$	$\mu_p$ and $\mu_n$ decrease with the increase in doping concentration
Relationship between mobility and diffusivity	$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T$	$V_T = kT/q \simeq 25.9 \text{ mV}$
Carrier concentration in $n$ -type silicon ( $\text{cm}^{-3}$ )	$n_{n0} \simeq N_D$ $p_{n0} = n_i^2/N_D$	
Carrier concentration in $p$ -type silicon ( $\text{cm}^{-3}$ )	$p_{p0} \simeq N_A$ $n_{p0} = n_i^2/N_A$	
Junction built-in voltage (V)	$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$	
Width of depletion region (cm)	$\begin{aligned} \frac{x_n}{x_p} &= \frac{N_A}{N_D} \\ W &= x_n + x_p \\ &= \sqrt{\frac{2\epsilon_s}{q} \left( \frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 + V_R)} \end{aligned}$	$\epsilon_s = 11.7\epsilon_0$ $\epsilon_0 = 8.854 \times 10^{-14} \text{ F/cm}$

**Table 3.1** *continued*

Quantity	Relationship	Values of Constants and Parameters (for Intrinsic Si at $T = 300$ K)
Charge stored in depletion layer (coulomb)	$Q_J = q \frac{N_A N_D}{N_A + N_D} A W$	
Forward current (A)	$I = I_p + I_n$ $I_p = A q n_i^2 \frac{D_p}{L_p N_D} \left( e^{V/V_T} - 1 \right)$ $I_n = A q n_i^2 \frac{D_n}{L_n N_A} \left( e^{V/V_T} - 1 \right)$	
Saturation current (A)	$I_S = A q n_i^2 \left( \frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right)$	
$I$ - $V$ relationship	$I = I_S \left( e^{V/V_T} - 1 \right)$	
Minority-carrier lifetime (s)	$\tau_p = L_p^2 / D_p \quad \tau_n = L_n^2 / D_n$	$L_p, L_n = 1 \text{ } \mu\text{m to } 100 \text{ } \mu\text{m}$ $\tau_p, \tau_n = 1 \text{ ns to } 10^4 \text{ ns}$
Minority-carrier charge storage (coulomb)	$Q_p = \tau_p I_p \quad Q_n = \tau_n I_n$ $Q = Q_p + Q_n = \tau_I I$	
Depletion capacitance (F)	$C_{j0} = A \sqrt{\left( \frac{\epsilon_s q}{2} \right) \left( \frac{N_A N_D}{N_A + N_D} \right) \frac{1}{V_0}}$ $C_j = C_{j0} \left( 1 + \frac{V_R}{V_0} \right)^m$	$m = \frac{1}{3} \text{ to } \frac{1}{2}$
Diffusion capacitance (F)	$C_d = \left( \frac{\tau_T}{V_T} \right) I$	

If in the following problems the need arises for the values of particular parameters or physical constants that are not stated, please consult Table 3.1.

### Section 3.1: Intrinsic Semiconductors

**3.1** Find values of the intrinsic carrier concentration  $n_i$  for silicon at  $-55^\circ\text{C}$ ,  $0^\circ\text{C}$ ,  $20^\circ\text{C}$ ,  $75^\circ\text{C}$ , and  $125^\circ\text{C}$ . At each temperature, what fraction of the atoms is ionized? Recall that a silicon crystal has approximately  $5 \times 10^{22}$  atoms/cm<sup>3</sup>.

**3.2** Calculate the value of  $n_i$  for gallium arsenide (GaAs) at  $T = 300$  K. The constant  $B = 3.56 \times 10^{14}$  cm<sup>-3</sup>K<sup>-3/2</sup> and the bandgap voltage  $E_g = 1.42$  eV.

### Section 3.2: Doped Semiconductors

**3.3** For a *p*-type silicon in which the dopant concentration  $N_A = 5 \times 10^{18}$ /cm<sup>3</sup>, find the hole and electron concentrations at  $T = 300$  K.

**3.4** For a silicon crystal doped with phosphorus, what must  $N_D$  be if at  $T = 300$  K the hole concentration drops below the intrinsic level by a factor of  $10^8$ ?

**3.5** In a phosphorus-doped silicon layer with impurity concentration of  $10^{17}$ /cm<sup>3</sup>, find the hole and electron concentrations at  $27^\circ\text{C}$  and  $125^\circ\text{C}$ .

### Section 3.3: Current Flow in Semiconductors

**3.6** A young designer, aiming to develop intuition concerning conducting paths within an integrated circuit, examines the end-to-end resistance of a connecting bar 10-μm long, 3-μm wide, and 1 μm thick, made of various materials. The designer considers:

- (a) intrinsic silicon
- (b) *n*-doped silicon with  $N_D = 5 \times 10^{16}$ /cm<sup>3</sup>
- (c) *n*-doped silicon with  $N_D = 5 \times 10^{18}$ /cm<sup>3</sup>
- (d) *p*-doped silicon with  $N_A = 5 \times 10^{16}$ /cm<sup>3</sup>
- (e) aluminum with resistivity of 2.8 μΩ·cm

Find the resistance in each case. For intrinsic silicon, use the data in Table 3.1. For doped silicon, assume  $\mu_n = 3\mu_p = 1200$  cm<sup>2</sup>/V·s. (Recall that  $R = \rho L/A$ .)

**3.7** Contrast the electron and hole drift velocities through a 10-μm layer of intrinsic silicon across which a voltage

of 3 V is imposed. Let  $\mu_n = 1350$  cm<sup>2</sup>/V·s and  $\mu_p = 480$  cm<sup>2</sup>/V·s.

**3.8** Find the current that flows in a silicon bar of 10-μm length having a 5-μm × 4-μm cross-section and having free-electron and hole densities of  $10^4$ /cm<sup>3</sup> and  $10^{16}$ /cm<sup>3</sup>, respectively, when a 1 V is applied end-to-end. Use  $\mu_n = 1200$  cm<sup>2</sup>/V·s and  $\mu_p = 500$  cm<sup>2</sup>/V·s.

**3.9** In a 10-μm-long bar of donor-doped silicon, what donor concentration is needed to realize a current density of 2 mA/μm<sup>2</sup> in response to an applied voltage of 1 V? (Note: Although the carrier mobilities change with doping concentration, as a first approximation you may assume  $\mu_n$  to be constant and use 1350 cm<sup>2</sup>/V·s, the value for intrinsic silicon.)

**3.10** Holes are being steadily injected into a region of *n*-type silicon (connected to other devices, the details of which are not important for this question). In the steady state, the excess-hole concentration profile shown in Fig. P3.10 is established in the *n*-type silicon region. Here “excess” means over and above the thermal-equilibrium concentration (in the absence of hole injection), denoted  $p_{n0}$ . If  $N_D = 10^{16}$ /cm<sup>3</sup>,  $n_i = 1.5 \times 10^{10}$ /cm<sup>3</sup>,  $D_p = 12$  cm<sup>2</sup>/s, and  $W = 50$  nm, find the density of the current that will flow in the *x* direction.

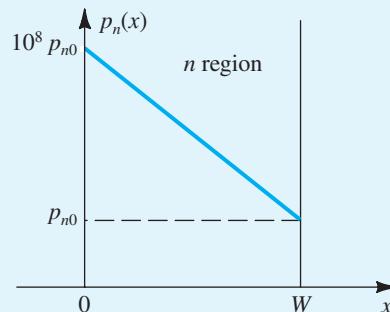


Figure P3.10

**3.11** Both the carrier mobility and the diffusivity decrease as the doping concentration of silicon is increased. Table P3.11 provides a few data points for  $\mu_n$  and  $\mu_p$  versus doping concentration. Use the Einstein relationship to obtain the corresponding values for  $D_n$  and  $D_p$ .

Table P3.11

Doping Concentration (carriers/cm <sup>3</sup> )	$\mu_n$ (cm <sup>2</sup> /V · s)	$\mu_p$ (cm <sup>2</sup> /V · s)	$D_n$ (cm <sup>2</sup> /s)	$D_p$ (cm <sup>2</sup> /s)
Intrinsic	1350	480		
$10^{16}$	1200	400		
$10^{17}$	750	260		
$10^{18}$	380	160		

### Section 3.4: The *pn* Junction

**3.12** Calculate the built-in voltage of a junction in which the *p* and *n* regions are doped equally with  $5 \times 10^{16}$  atoms/cm<sup>3</sup>. Assume  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ . With the terminals left open, what is the width of the depletion region, and how far does it extend into the *p* and *n* regions? If the cross-sectional area of the junction is  $20 \mu\text{m}^2$ , find the magnitude of the charge stored on either side of the junction.

**3.13** If, for a particular junction, the acceptor concentration is  $10^{17}/\text{cm}^3$  and the donor concentration is  $10^{16}/\text{cm}^3$ , find the junction built-in voltage. Assume  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ . Also, find the width of the depletion region ( $W$ ) and its extent in each of the *p* and *n* regions when the junction terminals are left open. Calculate the magnitude of the charge stored on either side of the junction. Assume that the junction area is  $100 \mu\text{m}^2$ .

**3.14** Estimate the total charge stored in a  $0.1\text{-}\mu\text{m}$  depletion layer on one side of a  $10\text{-}\mu\text{m} \times 10\text{-}\mu\text{m}$  junction. The doping concentration on that side of the junction is  $10^{18}/\text{cm}^3$ .

**3.15** In a *pn* junction for which  $N_A \gg N_D$ , and the depletion layer exists mostly on the shallowly doped side with  $W = 0.2 \mu\text{m}$ , find  $V_0$  if  $N_D = 10^{16}/\text{cm}^3$ . Also calculate  $Q_J$  for the case  $A = 10 \mu\text{m}^2$ .

**3.16** By how much does  $V_0$  change if  $N_A$  or  $N_D$  is increased by a factor of 10?

### Section 3.5: The *pn* Junction with an Applied Voltage

**3.17** If a 3-V reverse-bias voltage is applied across the junction specified in Problem 3.13, find  $W$  and  $Q_J$ .

**3.18** Show that for a *pn* junction reverse-biased with a voltage  $V_R$ , the depletion-layer width  $W$  and the

charge stored on either side of the junction,  $Q_J$ , can be expressed as

$$W = W_0 \sqrt{1 + \frac{V_R}{V_0}}$$

$$Q_J = Q_{J0} \sqrt{1 + \frac{V_R}{V_0}}$$

where  $W_0$  and  $Q_{J0}$  are the values in equilibrium.

**3.19** In a forward-biased *pn* junction show that the ratio of the current component due to hole injection across the junction to the component due to electron injection is given by

$$\frac{I_p}{I_n} = \frac{D_p}{D_n} \frac{L_n}{L_p} \frac{N_A}{N_D}$$

Evaluate this ratio for the case  $N_A = 10^{18}/\text{cm}^3$ ,  $N_D = 10^{16}/\text{cm}^3$ ,  $L_p = 5 \mu\text{m}$ ,  $L_n = 10 \mu\text{m}$ ,  $D_p = 10 \text{ cm}^2/\text{s}$ , and  $D_n = 20 \text{ cm}^2/\text{s}$ , and hence find  $I_p$  and  $I_n$  for the case in which the *pn* junction is conducting a forward current  $I = 100 \mu\text{A}$ .

**3.20** Calculate  $I_s$  and the current  $I$  for  $V = 750 \text{ mV}$  for a *pn* junction for which  $N_A = 10^{17}/\text{cm}^3$ ,  $N_D = 10^{16}/\text{cm}^3$ ,  $A = 100 \mu\text{m}^2$ ,  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ ,  $L_p = 5 \mu\text{m}$ ,  $L_n = 10 \mu\text{m}$ ,  $D_p = 10 \text{ cm}^2/\text{s}$ , and  $D_n = 18 \text{ cm}^2/\text{s}$ .

**3.21** Assuming that the temperature dependence of  $I_s$  arises mostly because  $I_s$  is proportional to  $n_i^2$ , use the expression for  $n_i$  in Eq. (3.2) to determine the factor by which  $n_i^2$  changes as  $T$  changes from 300 K to 305 K. This will be approximately the same factor by which  $I_s$  changes for a 5°C rise in temperature. What is the factor?

**3.22** A  $p^+$  $n$  junction is one in which the doping concentration in the  $p$  region is much greater than that in the  $n$  region. In such a junction, the forward current is mostly due to hole injection across the junction. Show that

$$I \simeq I_p = Aq n_i^2 \frac{D_p}{L_p N_D} \left( e^{V/V_T} - 1 \right)$$

For the specific case in which  $N_D = 10^{17}/\text{cm}^3$ ,  $D_p = 10 \text{ cm}^2/\text{s}$ ,  $L_p = 10 \mu\text{m}$ , and  $A = 10^4 \mu\text{m}^2$ , find  $I_s$  and the voltage  $V$  obtained when  $I = 1 \text{ mA}$ . Assume operation at 300 K where  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ .

**3.23** A  $pn$  junction for which the breakdown voltage is 12 V has a rated (i.e., maximum allowable) power dissipation of 0.25 W. What continuous current in the breakdown region will raise the dissipation to half the rated value? If breakdown occurs for only 10 ms in every 20 ms, what average breakdown current is allowed?

### Section 3.6: Capacitive Effects in the $pn$ Junction

**3.24** For the  $pn$  junction specified in Problem 3.13, find  $C_{j0}$  and  $C_j$  at  $V_R = 3 \text{ V}$ .

**3.25** For a particular junction for which  $C_{j0} = 0.4 \text{ pF}$ ,  $V_0 = 0.75 \text{ V}$ , and  $m = 1/3$ , find  $C_j$  at reverse-bias voltages of 1 V and 10 V.

**3.26** The junction capacitance  $C_j$  can be thought of as that of a parallel-plate capacitor and thus given by

$$C_j = \frac{\epsilon A}{W}$$

Show that this approach leads to a formula identical to that obtained by combining Eqs. (3.43) and (3.45) [or equivalently, by combining Eqs. (3.47) and (3.48)].

**3.27** A  $pn$  junction operating in the forward-bias region with a current  $I$  of 1 mA is found to have a diffusion capacitance of 5 pF. What diffusion capacitance do you expect this junction

to have at  $I = 0.1 \text{ mA}$ ? What is the mean transit time for this junction?

**3.28** For the  $p^+$  $n$  junction specified in Problem 3.22, find  $\tau_p$  and calculate the excess minority-carrier charge and the value of the diffusion capacitance at  $I = 0.1 \text{ mA}$ .

**\*3.29** A **short-base diode** is one where the widths of the  $p$  and  $n$  regions are much smaller than  $L_n$  and  $L_p$ , respectively. As a result, the excess minority-carrier distribution in each region is a straight line rather than the exponentials shown in Fig. 3.12.

- (a) For the short-base diode, sketch a figure corresponding to Fig. 3.12 and assume as in Fig. 3.12 that  $N_A \gg N_D$ .
- (b) Following a derivation similar to that given in Section 3.5.2, show that if the widths of the  $p$  and  $n$  regions are denoted  $W_p$  and  $W_n$  then

$$I = A q n_i^2 \left[ \frac{D_p}{(W_n - x_n) N_D} + \frac{D_n}{(W_p - x_p) N_A} \right] \left( e^{V/V_T} - 1 \right)$$

and

$$\begin{aligned} Q_p &= \frac{1}{2} \frac{(W_n - x_n)^2}{D_p} I_p \\ &\simeq \frac{1}{2} \frac{W_n^2}{D_p} I_p, \text{ for } W_n \gg x_n \end{aligned}$$

- (c) Also, assuming  $Q \simeq Q_p$ ,  $I \simeq I_p$ , show that

$$C_d = \frac{\tau_T}{V_T} I$$

where

$$\tau_T = \frac{1}{2} \frac{W_n^2}{D_p}$$

- (d) If a designer wishes to limit  $C_d$  to 8 pF at  $I = 1 \text{ mA}$ , what should  $W_n$  be? Assume  $D_p = 10 \text{ cm}^2/\text{s}$ .

## CHAPTER 4

# Diodes

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## IN THIS CHAPTER YOU WILL LEARN

1. The characteristics of the ideal diode and how to analyze and design circuits containing multiple ideal diodes together with resistors and dc sources to realize useful and interesting nonlinear functions.
2. The details of the  $i-v$  characteristic of the junction diode (which was derived in Chapter 3) and how to use it to analyze diode circuits operating in the various bias regions: forward, reverse, and breakdown.
3. A simple but effective model of the diode  $i-v$  characteristic in the forward direction: the constant-voltage-drop model.
4. A powerful technique for the application and modeling of the diode (and in later chapters, transistors): dc-biasing the diode and modeling its operation for small signals around the dc operating point by means of the small-signal model.
5. The use of a string of forward-biased diodes and of diodes operating in the breakdown region (zener diodes), to provide constant dc voltages (voltage regulators).
6. Application of the diode in the design of rectifier circuits, which convert ac voltages to dc as needed for powering electronic equipment.
7. A number of other practical and important applications of diodes.

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## Introduction

In Chapters 1 and 2 we dealt almost entirely with linear circuits; any nonlinearity, such as that introduced by amplifier output saturation, was treated as a problem to be solved by the circuit designer. However, there are many other signal-processing functions that can be implemented only by nonlinear circuits. Examples include the generation of dc voltages from the ac power supply, and the generation of signals of various waveforms (e.g., sinusoids, square waves, pulses). Also, digital logic and memory circuits constitute a special class of nonlinear circuits.

The simplest and most fundamental nonlinear circuit element is the diode. Just like a resistor, the diode has two terminals; but unlike the resistor, which has a linear (straight-line) relationship between the current flowing through it and the voltage appearing across it, the diode has a nonlinear  $i-v$  characteristic.

This chapter is concerned with the study of diodes. In order to understand the essence of the diode function, we begin with a fictitious element, the ideal diode. We then introduce the silicon junction diode, explain its terminal characteristics, and provide techniques for the

analysis of diode circuits. The latter task involves the important subject of device modeling. Our study of modeling the diode characteristics will lay the foundation for our study of modeling transistor operation in the next three chapters.

Of the many applications of diodes, their use in the design of rectifiers (which convert ac to dc) is the most common. Therefore we shall study rectifier circuits in some detail and briefly look at a number of other diode applications. Further nonlinear circuits that utilize diodes and other devices will be found throughout the book, but particularly in Chapter 18.

The junction diode is nothing more than the *pn* junction we studied in Chapter 3, and most of this chapter is concerned with the study of silicon *pn*-junction diodes. In the last section, however, we briefly consider some specialized diode types, including the photodiode and the light-emitting diode.

## 4.1 The Ideal Diode

### 4.1.1 Current-Voltage Characteristic

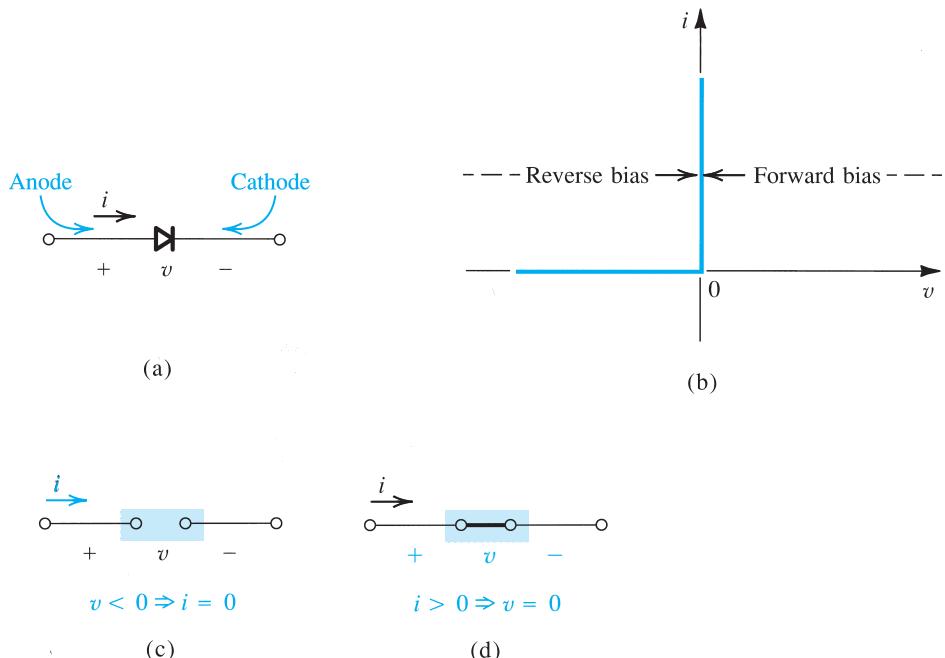
The ideal diode may be considered to be the most fundamental nonlinear circuit element. It is a two-terminal device having the circuit symbol of Fig. 4.1(a) and the  $i-v$  characteristic shown in Fig. 4.1(b). The terminal characteristic of the ideal diode can be interpreted as follows: If a negative voltage (relative to the reference direction indicated in Fig. 4.1a) is applied to the diode, no current flows and the diode behaves as an open circuit (Fig. 4.1c). Diodes operated in this mode are said to be **reverse biased**, or operated in the reverse direction. An ideal diode has zero current when operated in the reverse direction and is said to be **cut off**, or simply **off**.

On the other hand, if a positive current (relative to the reference direction indicated in Fig. 4.1(a) is applied to the ideal diode, zero voltage drop appears across the diode. In other words, the ideal diode behaves as a short circuit in the *forward* direction (Fig. 4.1d); it passes any current with zero voltage drop. A **forward-biased** diode is said to be **turned on**, or simply **on**.

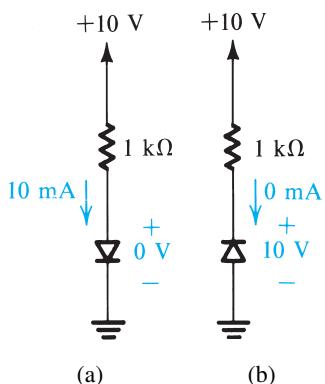
From the above description it should be noted that the external circuit must be designed to limit the forward current through a conducting diode, and the reverse voltage across a cutoff diode, to predetermined values. Figure 4.2 shows two diode circuits that illustrate this point. In the circuit of Fig. 4.2(a) the diode is obviously conducting. Thus its voltage drop will be zero, and the current through it will be determined by the +10-V supply and the 1-k $\Omega$  resistor as 10 mA. The diode in the circuit of Fig. 4.2(b) is obviously cut off, and thus its current will be zero, which in turn means that the entire 10-V supply will appear as reverse bias across the diode.

The positive terminal of the diode is called the **anode** and the negative terminal the **cathode**, a carryover from the days of vacuum-tube diodes. The  $i-v$  characteristic of the ideal diode (conducting in one direction and not in the other) should explain the choice of its arrow-like circuit symbol.

As should be evident from the preceding description, the  $i-v$  characteristic of the ideal diode is highly nonlinear; although it consists of two straight-line segments, they are at 90° to one another. A nonlinear curve that consists of straight-line segments is said to be **piecewise linear**. If a device having a piecewise-linear characteristic is used in a particular application in such a way that the signal across its terminals swings along only one of the linear segments, then the device can be considered a linear circuit element as far as that particular circuit



**Figure 4.1** The ideal diode: (a) diode circuit symbol; (b)  $i$ - $v$  characteristic; (c) equivalent circuit in the reverse direction; (d) equivalent circuit in the forward direction.



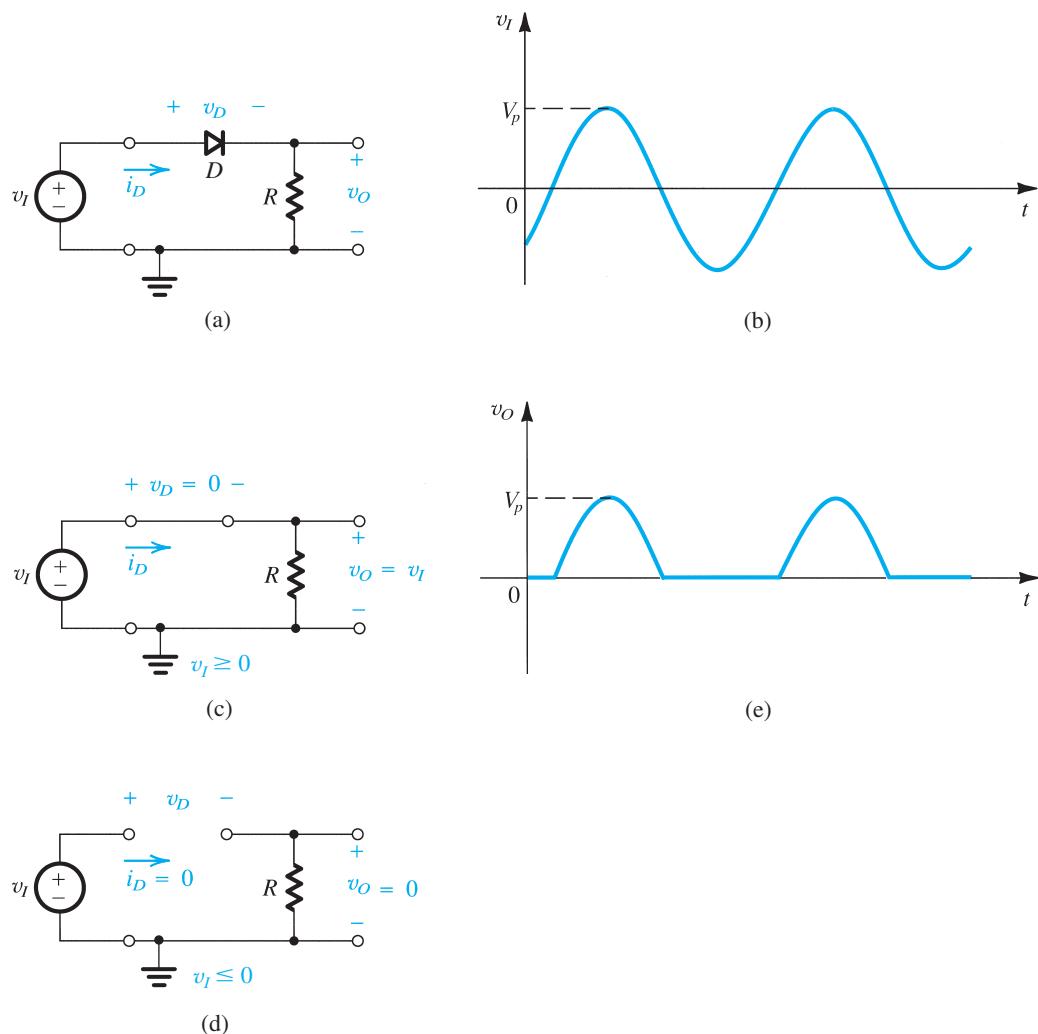
**Figure 4.2** The two modes of operation of ideal diodes and the use of an external circuit to limit (a) the forward current and (b) the reverse voltage.

application is concerned. On the other hand, if signals swing past one or more of the break points in the characteristic, linear analysis is no longer possible.

### 4.1.2 A Simple Application: The Rectifier

A fundamental application of the diode, one that makes use of its severely nonlinear  $i$ - $v$  curve, is the rectifier circuit shown in Fig. 4.3(a). The circuit consists of the series connection of a diode  $D$  and a resistor  $R$ . Let the input voltage  $v_i$  be the sinusoid shown in Fig. 4.3(b), and assume the diode to be ideal. During the positive half-cycles of the input sinusoid, the positive

$v_I$  will cause current to flow through the diode in its forward direction. It follows that the diode voltage  $v_D$  will be very small—ideally zero. Thus the circuit will have the equivalent shown in Fig. 4.3(c), and the output voltage  $v_O$  will be equal to the input voltage  $v_I$ . On the other hand, during the negative half-cycles of  $v_I$ , the diode will not conduct. Thus the circuit will have the equivalent shown in Fig. 4.3(d), and  $v_O$  will be zero. Thus the output voltage will have the waveform shown in Fig. 4.3(e). Note that while  $v_I$  alternates in polarity and has a zero average value,  $v_O$  is unidirectional and has a finite average value or a *dc component*. Thus the circuit of Fig. 4.3(a) **rectifies** the signal and hence is called a **rectifier**. It can be used to generate dc from ac. We will study rectifier circuits in Section 4.5.



**Figure 4.3** (a) Rectifier circuit. (b) Input waveform. (c) Equivalent circuit when  $v_I \geq 0$ . (d) Equivalent circuit when  $v_I \leq 0$ . (e) Output waveform.

## EXERCISES

- 4.1** For the circuit in Fig. 4.3(a), sketch the transfer characteristic  $v_o$  versus  $v_i$ .

**Ans.** See Fig. E4.1

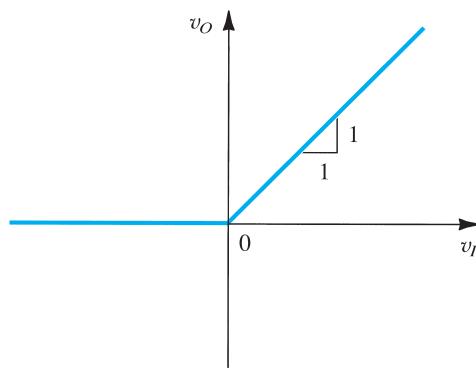


Figure E4.1

- 4.2** For the circuit in Fig. 4.3(a), sketch the waveform of  $v_D$ .

**Ans.**  $v_D = v_i - v_o$ , resulting in the waveform in Fig. E4.2

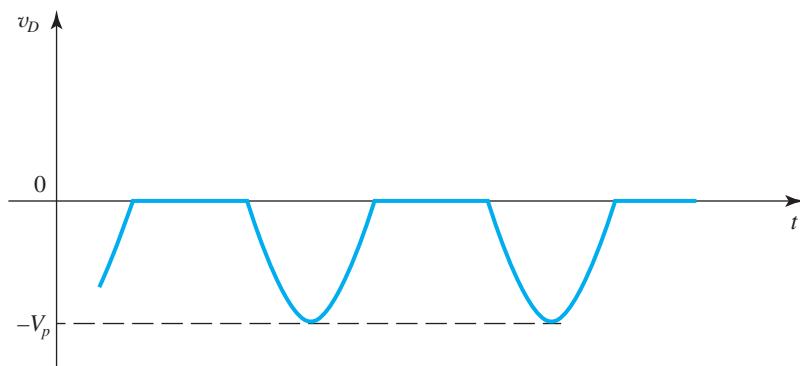


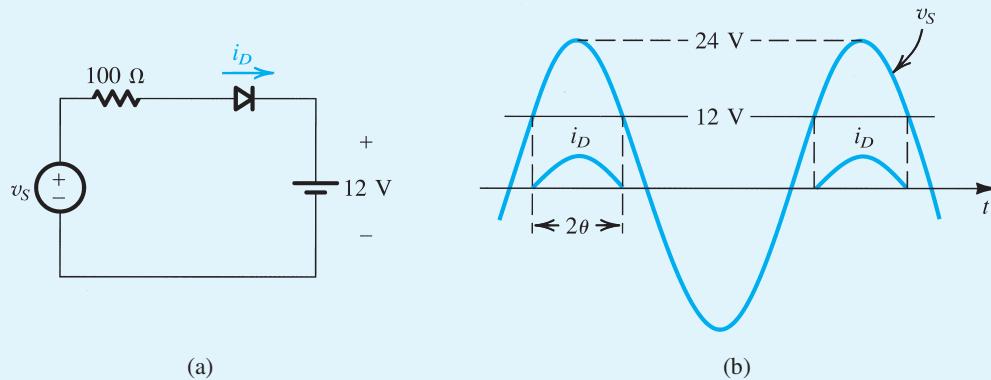
Figure E4.2

- 4.3** In the circuit of Fig. 4.3(a), let  $v_i$  have a peak value of 10 V and  $R = 1 \text{ k}\Omega$ . Find the peak value of  $i_D$  and the dc component of  $v_o$ . (Hint: The average value of half-sine waves is  $V_p/\pi$ .)

**Ans.** 10 mA; 3.18 V

**Example 4.1**

Figure 4.4(a) shows a circuit for charging a 12-V battery. If  $v_s$  is a sinusoid with 24-V peak amplitude, find the fraction of each cycle during which the diode conducts. Also, find the peak value of the diode current and the maximum reverse-bias voltage that appears across the diode.



**Figure 4.4** Circuit and waveforms for Example 4.1.

### Solution

The diode conducts when  $v_s$  exceeds 12 V, as shown in Fig. 4.4(b). The conduction angle is  $2\theta$ , where  $\theta$  is given by

$$24 \cos \theta = 12$$

Thus  $\theta = 60^\circ$  and the conduction angle is  $120^\circ$ , or one-third of a cycle.

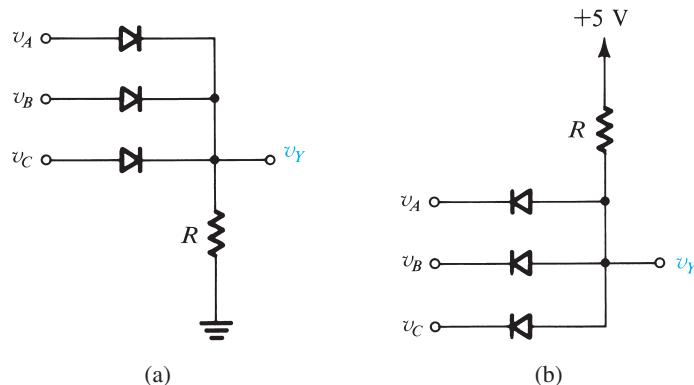
The peak value of the diode current is given by

$$I_d = \frac{24 - 12}{100} = 0.12 \text{ A}$$

The maximum reverse voltage across the diode occurs when  $v_s$  is at its negative peak and is equal to  $24 + 12 = 36$  V.

### 4.1.3 Another Application: Diode Logic Gates

Diodes together with resistors can be used to implement digital logic functions. Figure 4.5 shows two diode logic gates. To see how these circuits function, consider a positive-logic system in which voltage values close to 0 V correspond to logic 0 (or low) and voltage values close to +5 V correspond to logic 1 (or high). The circuit in Fig. 4.5(a) has three inputs,  $v_A$ ,  $v_B$ , and  $v_C$ . It is easy to see that diodes connected to +5-V inputs will conduct, thus clamping the output  $v_Y$  to a value equal to +5 V. This positive voltage at the output will keep the diodes whose inputs are low (around 0 V) cut off. Thus *the output will be high if one or more of the inputs are high*. The circuit therefore implements the **logic OR function**, which in Boolean



**Figure 4.5** Diode logic gates: (a) OR gate; (b) AND gate (in a positive-logic system).

notation is expressed as

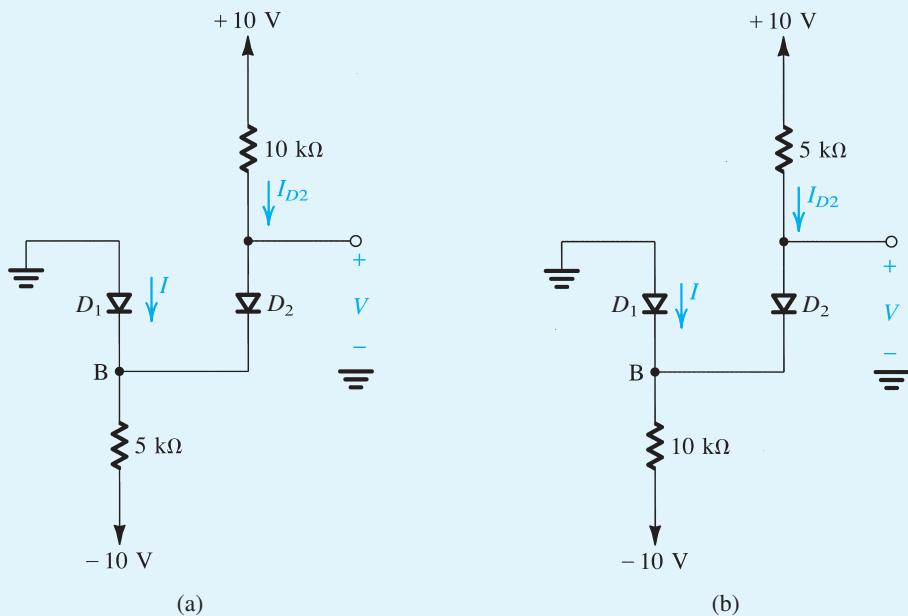
$$Y = A + B + C$$

Similarly, the reader is encouraged to show that using the same logic system mentioned above, the circuit of Fig. 4.5(b) implements the **logic AND function**,

$$Y = A \cdot B \cdot C$$

## Example 4.2

Assuming the diodes to be ideal, find the values of  $I$  and  $V$  in the circuits of Fig. 4.6.



**Figure 4.6** Circuits for Example 4.2.

**Example 4.2** *continued***Solution**

In these circuits it might not be obvious at first sight whether none, one, or both diodes are conducting. In such a case, *we make a plausible assumption, proceed with the analysis, and then check whether we end up with a consistent solution*. For the circuit in Fig. 4.6(a), we shall assume that both diodes are conducting. It follows that  $V_B = 0$  and  $V = 0$ . The current through  $D_2$  can now be determined from

$$I_{D2} = \frac{10 - 0}{10} = 1 \text{ mA}$$

Writing a node equation at B,

$$I + 1 = \frac{0 - (-10)}{5}$$

results in  $I = 1$  mA. Thus  $D_1$  is conducting as originally assumed, and the final result is  $I = 1$  mA and  $V = 0$  V.

For the circuit in Fig. 4.6(b), if we assume that both diodes are conducting, then  $V_B = 0$  and  $V = 0$ . The current in  $D_2$  is obtained from

$$I_{D2} = \frac{10 - 0}{5} = 2 \text{ mA}$$

The node equation at B is

$$I + 2 = \frac{0 - (-10)}{10}$$

which yields  $I = -1$  mA. Since this is not possible, our original assumption is *not* correct. We start again, assuming that  $D_1$  is off and  $D_2$  is on. The current  $I_{D2}$  is given by

$$I_{D2} = \frac{10 - (-10)}{15} = 1.33 \text{ mA}$$

and the voltage at node B is

$$V_B = -10 + 10 \times 1.33 = +3.3 \text{ V}$$

Thus  $D_1$  is reverse biased as assumed, and the final result is  $I = 0$  and  $V = 3.3$  V.

## EXERCISES

**4.4** Find the values of  $I$  and  $V$  in the circuits shown in Fig. E4.4.

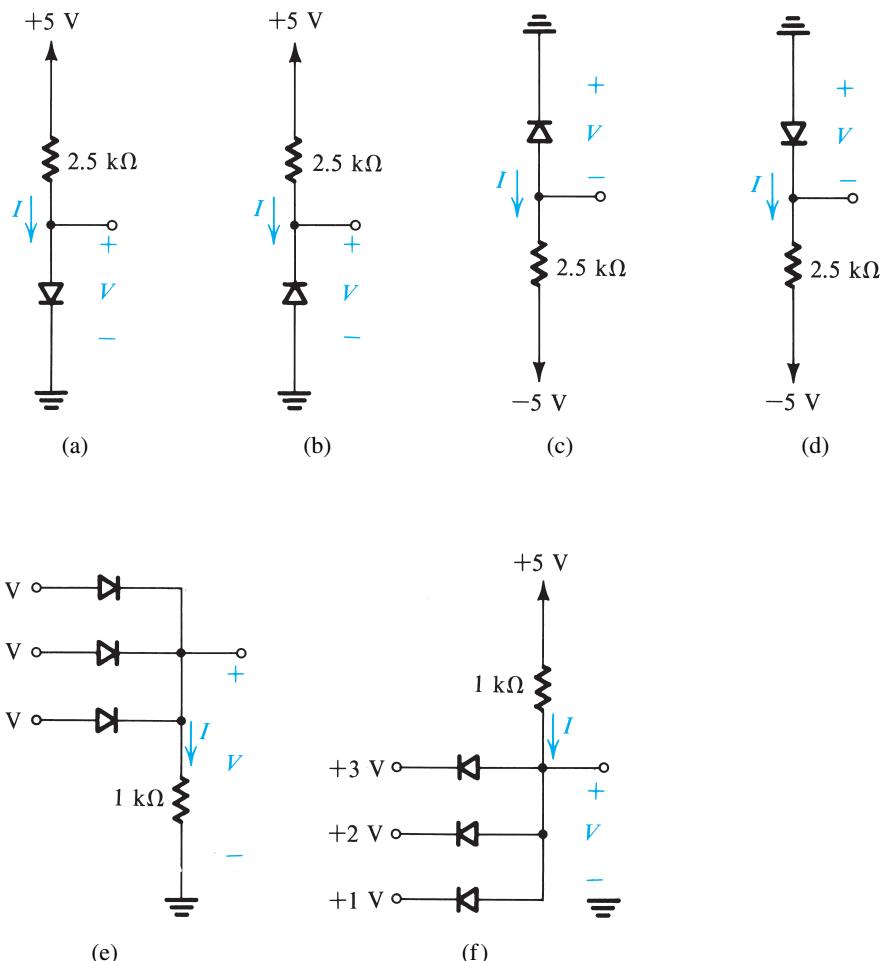


Figure E4.4

**Ans.** (a) 2 mA, 0 V; (b) 0 mA, 5 V; (c) 0 mA, 5 V; (d) 2 mA, 0 V; (e) 3 mA, +3 V; (f) 4 mA, +1 V

**4.5** Figure E4.5 shows a circuit for an ac voltmeter. It utilizes a moving-coil meter that gives a full-scale reading when the *average* current flowing through it is 1 mA. The moving-coil meter has a  $50\text{-}\Omega$  resistance.

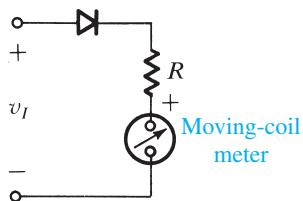


Figure E4.5

Find the value of  $R$  that results in the meter indicating a full-scale reading when the input sine-wave voltage  $v_I$  is 20 V peak-to-peak. (Hint: The average value of half-sine waves is  $V_p/\pi$ .)

**Ans.** 3.133 k $\Omega$

## 4.2 Terminal Characteristics of Junction Diodes

The most common implementation of the diode utilizes a *pn* junction. We have studied the physics of the *pn* junction and derived its  $i-v$  characteristic in Chapter 3. That the *pn* junction is used to implement the diode function should come as no surprise: the *pn* junction can conduct substantial current in the forward direction and almost no current in the reverse direction. In this section we study the  $i-v$  characteristic of the *pn* junction diode in detail in order to prepare ourselves for diode circuit applications.

Figure 4.7 shows the  $i-v$  characteristic of a silicon junction diode. The same characteristic is shown in Fig. 4.8 with some scales expanded and others compressed to reveal details. Note that the scale changes have resulted in the apparent discontinuity at the origin.

As indicated, the characteristic curve consists of three distinct regions:

1. The forward-bias region, determined by  $v > 0$
2. The reverse-bias region, determined by  $v < 0$
3. The breakdown region, determined by  $v < -V_{ZK}$

These three regions of operation are described in the following sections.

### 4.2.1 The Forward-Bias Region

The forward-bias—or simply forward—region of operation is entered when the terminal voltage  $v$  is positive. In the forward region the  $i-v$  relationship is closely approximated by

$$i = I_S(e^{v/V_T} - 1) \quad (4.1)$$

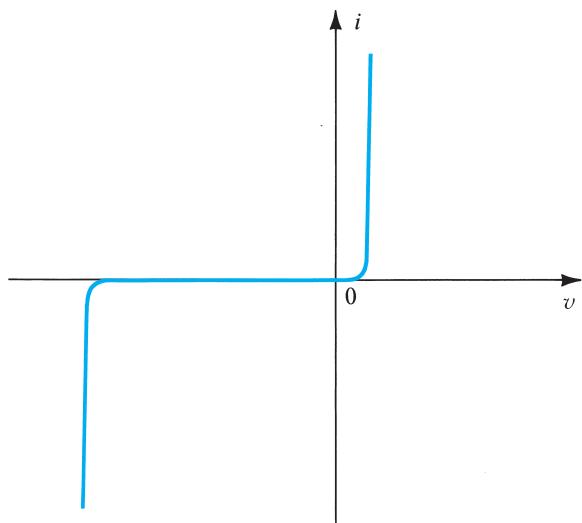
In this equation<sup>1</sup>  $I_S$  is a constant for a given diode at a given temperature. A formula for  $I_S$  in terms of the diode's physical parameters and temperature was given in Eq. (3.41). The current

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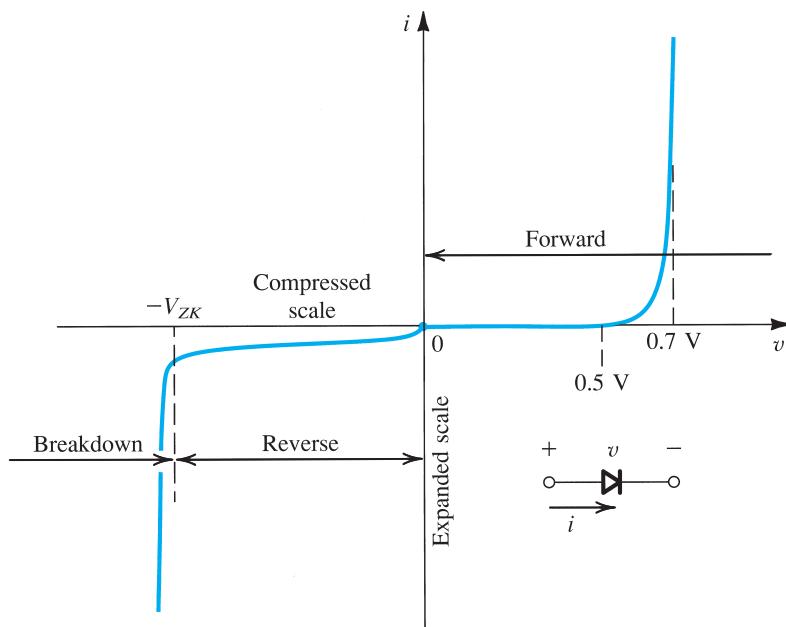
<sup>1</sup>Equation (4.1), the diode equation, is sometimes written to include a constant  $n$  in the exponential,

$$i = I_S(e^{\phi n V_T} - 1)$$

with  $n$  having a value between 1 and 2, depending on the material and the physical structure of the diode. Diodes using the standard integrated-circuit fabrication process exhibit  $n = 1$  when operated under normal conditions. For simplicity, we shall use  $n = 1$  throughout this book, unless otherwise specified.



**Figure 4.7** The  $i$ - $v$  characteristic of a silicon junction diode.



**Figure 4.8** The diode  $i$ - $v$  relationship with some scales expanded and others compressed in order to reveal details.

$I_s$  is usually called the **saturation current** (for reasons that will become apparent shortly). Another name for  $I_s$ , and one that we will occasionally use, is the **scale current**. This name arises from the fact that  $I_s$  is directly proportional to the cross-sectional area of the diode. Thus doubling of the junction area results in a diode with double the value of  $I_s$  and, as the diode equation indicates, double the value of current  $i$  for a given forward voltage  $v$ . For “small-signal” diodes, which are small-size diodes intended for low-power applications,  $I_s$  is on the order of  $10^{-15}$  A. The value of  $I_s$  is, however, a very strong function of temperature. As a rule of thumb,  $I_s$  doubles in value for every  $5^\circ\text{C}$  rise in temperature.

The voltage  $V_T$  in Eq. (4.1) is a constant called the **thermal voltage** and is given by

➤ 
$$V_T = \frac{kT}{q} \quad (4.2)$$

where

$k$  = Boltzmann’s constant =  $8.62 \times 10^{-5}$  eV/K =  $1.38 \times 10^{-23}$  joules/kelvin

$T$  = the absolute temperature in kelvins =  $273 + \text{temperature in } {}^\circ\text{C}$

$q$  = the magnitude of electronic charge =  $1.60 \times 10^{-19}$  coulomb

Substituting  $k = 8.62 \times 10^{-5}$  eV/K into Eq. (4.2) gives

$$V_T = 0.0862T, \text{ mV} \quad (4.2a)$$

Thus, at room temperature ( $20^\circ\text{C}$ ) the value of  $V_T$  is 25.3 mV. In rapid approximate circuit analysis we shall use  $V_T \approx 25$  mV at room temperature.<sup>2</sup>

For appreciable current  $i$  in the forward direction, specifically for  $i \gg I_s$ , Eq. (4.1) can be approximated by the exponential relationship

➤ 
$$i \approx I_s e^{v/V_T} \quad (4.3)$$

This relationship can be expressed alternatively in the logarithmic form

➤ 
$$v = V_T \ln \frac{i}{I_s} \quad (4.4)$$

where  $\ln$  denotes the natural (base  $e$ ) logarithm.

The exponential relationship of the current  $i$  to the voltage  $v$  holds over many decades of current (a span of as many as seven decades—i.e., a factor of  $10^7$ —can be found). This is quite a remarkable property of junction diodes, one that is also found in bipolar junction transistors and that has been exploited in many interesting applications.

Let us consider the forward  $i-v$  relationship in Eq. (4.3) and evaluate the current  $I_1$  corresponding to a diode voltage  $V_1$ :

$$I_1 = I_s e^{V_1/V_T}$$

Similarly, if the voltage is  $V_2$ , the diode current  $I_2$  will be

$$I_2 = I_s e^{V_2/V_T}$$

---

<sup>2</sup>A slightly higher ambient temperature ( $25^\circ\text{C}$  or so) is usually assumed for electronic equipment operating inside a cabinet. At this temperature,  $V_T \approx 25.8$  mV. Nevertheless, for the sake of simplicity and to promote rapid circuit analysis, we shall use the more arithmetically convenient value of  $V_T \approx 25$  mV throughout this book.

These two equations can be combined to produce

$$\frac{I_2}{I_1} = e^{(V_2 - V_1)/V_T}$$

which can be rewritten as

$$V_2 - V_1 = V_T \ln \frac{I_2}{I_1}$$

or, in terms of base-10 logarithms,

$$V_2 - V_1 = 2.3 V_T \log \frac{I_2}{I_1} \quad (4.5)$$



This equation simply states that for a decade (factor of 10) change in current, the diode voltage drop changes by  $2.3V_T$ , which is approximately 60 mV. This also suggests that the diode  $i-v$  relationship is most conveniently plotted on semilog paper. Using the vertical, linear axis for  $v$  and the horizontal, log axis for  $i$ , one obtains a straight line with a slope of 60 mV per decade of current.

A glance at the  $i-v$  characteristic in the forward region (Fig. 4.8) reveals that the current is negligibly small for  $v$  smaller than about 0.5 V. This value is usually referred to as the **cut-in voltage**. It should be emphasized, however, that this apparent threshold in the characteristic is simply a consequence of the exponential relationship. Another consequence of this relationship is the rapid increase of  $i$ . Thus, for a “fully conducting” diode, the voltage drop lies in a narrow range, approximately 0.6 V to 0.8 V. This gives rise to a simple “model” for the diode where it is assumed that a conducting diode has approximately a 0.7-V drop across it. Diodes with different current ratings (i.e., different areas and correspondingly different  $I_S$ ) will exhibit the 0.7-V drop at different currents. For instance, a small-signal diode may be considered to have a 0.7-V drop at  $i = 1 \text{ mA}$ , while a higher-power diode may have a 0.7-V drop at  $i = 1 \text{ A}$ . We will study the topics of diode-circuit analysis and diode models in the next section.

### Example 4.3

A silicon diode said to be a 1-mA device displays a forward voltage of 0.7 V at a current of 1 mA. Evaluate the junction scaling constant  $I_S$ . What scaling constants would apply for a 1-A diode of the same manufacture that conducts 1 A at 0.7 V?

#### Solution

Since

$$i = I_S e^{v/V_T}$$

then

$$I_S = i e^{-v/V_T}$$

**Example 4.3** *continued*

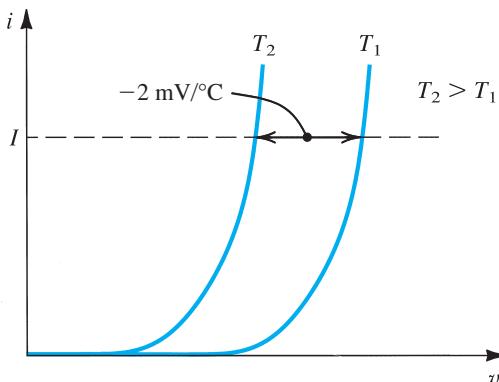
For the 1-mA diode:

$$I_s = 10^{-3} e^{-700/25} = 6.9 \times 10^{-16} \text{ A}$$

The diode conducting 1 A at 0.7 V corresponds to one-thousand 1-mA diodes in parallel with a total junction area 1000 times greater. Thus  $I_s$  is also 1000 times greater,

$$I_s = 6.9 \times 10^{-13} \text{ A}$$

Since both  $I_s$  and  $V_T$  are functions of temperature, the forward  $i-v$  characteristic varies with temperature, as illustrated in Fig. 4.9. At a given constant diode current, the voltage drop across the diode decreases by approximately 2 mV for every 1°C increase in temperature. The change in diode voltage with temperature has been exploited in the design of electronic thermometers.



**Figure 4.9** Temperature dependence of the diode forward characteristic. At a constant current, the voltage drop decreases by approximately 2 mV for every 1°C increase in temperature.

## EXERCISES

- 4.6** Find the change in diode voltage if the current changes from 0.1 mA to 10 mA.

**Ans.** 120 mV

- 4.7** A silicon junction diode has  $v = 0.7$  V at  $i = 1$  mA. Find the voltage drop at  $i = 0.1$  mA and  $i = 10$  mA.

**Ans.** 0.64 V; 0.76 V

- 4.8** Using the fact that a silicon diode has  $I_s = 10^{-14}$  A at 25°C and that  $I_s$  increases by 15% per °C rise in temperature, find the value of  $I_s$  at 125°C.

**Ans.**  $1.17 \times 10^{-8}$  A

### 4.2.2 The Reverse-Bias Region

The reverse-bias region of operation is entered when the diode voltage  $v$  is made negative. Equation (4.1) predicts that if  $v$  is negative and a few times larger than  $V_T$  (25 mV) in magnitude, the exponential term becomes negligibly small compared to unity, and the diode current becomes

$$i \simeq -I_S$$

That is, the current in the reverse direction is constant and equal to  $I_S$ . This constancy is the reason behind the term *saturation current*.

Real diodes exhibit reverse currents that, though quite small, are much larger than  $I_S$ . For instance, a small-signal diode whose  $I_S$  is on the order of  $10^{-14}$  A to  $10^{-15}$  A could show a reverse current on the order of 1 nA. The reverse current also increases somewhat with the increase in magnitude of the reverse voltage. Note that because of the very small magnitude of the current, these details are not clearly evident on the diode  $i-v$  characteristic of Fig. 4.8.

A large part of the reverse current is due to leakage effects. These leakage currents are proportional to the junction area, just as  $I_S$  is. Their dependence on temperature, however, is different from that of  $I_S$ . Thus, whereas  $I_S$  doubles for every  $5^\circ\text{C}$  rise in temperature, the corresponding rule of thumb for the temperature dependence of the reverse current is that it doubles for every  $10^\circ\text{C}$  rise in temperature.

#### EXERCISE

- 4.9** The diode in the circuit of Fig. E4.9 is a large high-current device whose reverse leakage is reasonably independent of voltage. If  $V = 1$  V at  $20^\circ\text{C}$ , find the value of  $V$  at  $40^\circ\text{C}$  and at  $0^\circ\text{C}$ .

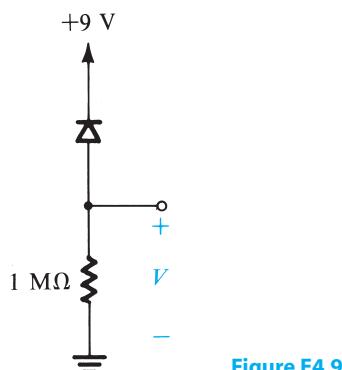


Figure E4.9

**Ans.** 4 V; 0.25 V

### 4.2.3 The Breakdown Region

The third distinct region of diode operation is the breakdown region, which can be easily identified on the diode  $i-v$  characteristic in Fig. 4.8. The breakdown region is entered when the magnitude of the reverse voltage exceeds a threshold value that is specific to the particular diode, called the **breakdown voltage**. This is the voltage at the “knee” of the  $i-v$  curve in Fig. 4.8 and is denoted  $V_{ZK}$ , where the subscript Z stands for zener (see Section 3.5.3) and K denotes knee.

As can be seen from Fig. 4.8, in the breakdown region the reverse current increases rapidly, with the associated increase in voltage drop being very small. Diode breakdown is normally not destructive, provided the power dissipated in the diode is limited by external circuitry to a “safe” level. This safe value is normally specified on the device data sheets. It therefore is necessary to limit the reverse current in the breakdown region to a value consistent with the permissible power dissipation.

The fact that the diode  $i-v$  characteristic in breakdown is almost a vertical line enables it to be used in voltage regulation. This subject will be studied in Section 4.5.

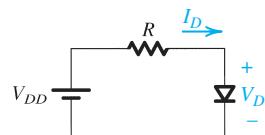
## 4.3 Modeling the Diode Forward Characteristic

Having studied the diode terminal characteristics we are now ready to consider the analysis of circuits employing forward-conducting diodes. Figure 4.10 shows such a circuit. It consists of a dc source  $V_{DD}$ , a resistor  $R$ , and a diode. We wish to analyze this circuit to determine the diode voltage  $V_D$  and current  $I_D$ . To aid in our analysis, we need to represent the diode with a model. There are a variety of diode models, of which we now know two: the ideal-diode model and the exponential model. In the following discussion we shall assess the suitability of these two models in various analysis situations. Also, we shall develop and comment on other models. This material, besides being useful in the analysis and design of diode circuits, establishes a foundation for the modeling of transistor operation that we will study in the next three chapters.

### 4.3.1 The Exponential Model

The most accurate description of the diode operation in the forward region is provided by the exponential model. Unfortunately, however, its severely nonlinear nature makes this model the most difficult to use. To illustrate, let’s analyze the circuit in Fig. 4.10 using the exponential diode model.

Assuming that  $V_{DD}$  is greater than 0.5 V or so, the diode current will be much greater than  $I_s$ , and we can represent the diode  $i-v$  characteristic by the exponential relationship,



**Figure 4.10** A simple circuit used to illustrate the analysis of circuits in which the diode is forward conducting.

resulting in

$$I_D = I_S e^{V_D/V_T} \quad (4.6)$$

The other equation that governs circuit operation is obtained by writing a Kirchhoff loop equation, resulting in

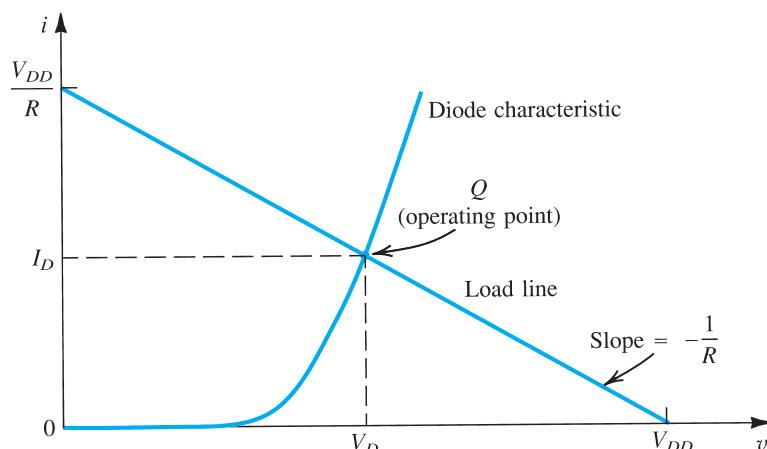
$$I_D = \frac{V_{DD} - V_D}{R} \quad (4.7)$$

Assuming that the diode parameter  $I_S$  is known, Eqs. (4.6) and (4.7) are two equations in the two unknown quantities  $I_D$  and  $V_D$ . Two alternative ways for obtaining the solution are graphical analysis and iterative analysis.

### 4.3.2 Graphical Analysis Using the Exponential Model

Graphical analysis is performed by plotting the relationships of Eqs. (4.6) and (4.7) on the  $i-v$  plane. The solution can then be obtained as the coordinates of the point of intersection of the two graphs. A sketch of the graphical construction is shown in Fig. 4.11. The curve represents the exponential diode equation (Eq. 4.6), and the straight line represents Eq. (4.7). Such a straight line is known as the **load line**, a name that will become more meaningful in later chapters. The load line intersects the diode curve at point  $Q$ , which represents the **operating point** of the circuit. Its coordinates give the values of  $I_D$  and  $V_D$ .

Graphical analysis aids in the visualization of circuit operation. However, the effort involved in performing such an analysis, particularly for complex circuits, is too great to be justified in practice.



**Figure 4.11** Graphical analysis of the circuit in Fig. 4.10 using the exponential diode model.

### 4.3.3 Iterative Analysis Using the Exponential Model

Equations (4.6) and (4.7) can be solved using a simple iterative procedure, as illustrated in the following example.

### Example 4.4

Determine the current  $I_D$  and the diode voltage  $V_D$  for the circuit in Fig. 4.10 with  $V_{DD} = 5$  V and  $R = 1 \text{ k}\Omega$ . Assume that the diode has a current of 1 mA at a voltage of 0.7 V.

#### Solution

To begin the iteration, we assume that  $V_D = 0.7$  V and use Eq. (4.7) to determine the current,

$$\begin{aligned} I_D &= \frac{V_{DD} - V_D}{R} \\ &= \frac{5 - 0.7}{1} = 4.3 \text{ mA} \end{aligned}$$

We then use the diode equation to obtain a better estimate for  $V_D$ . This can be done by employing Eq. (4.5), namely,

$$V_2 - V_1 = 2.3V_T \log \frac{I_2}{I_1}$$

Substituting  $2.3V_T = 60$  mV, we have

$$V_2 = V_1 + 0.06 \log \frac{I_2}{I_1}$$

Substituting  $V_1 = 0.7$  V,  $I_1 = 1$  mA, and  $I_2 = 4.3$  mA results in  $V_2 = 0.738$  V. Thus the results of the first iteration are  $I_D = 4.3$  mA and  $V_D = 0.738$  V. The second iteration proceeds in a similar manner:

$$\begin{aligned} I_D &= \frac{5 - 0.738}{1} = 4.262 \text{ mA} \\ V_2 &= 0.738 + 0.06 \log \left[ \frac{4.262}{4.3} \right] \\ &= 0.738 \text{ V} \end{aligned}$$

Thus the second iteration yields  $I_D = 4.262$  mA and  $V_D = 0.738$  V. Since these values are very close to the values obtained after the first iteration, no further iterations are necessary, and the solution is  $I_D = 4.262$  mA and  $V_D = 0.738$  V.

#### 4.3.4 The Need for Rapid Analysis

The iterative analysis procedure utilized in the example above is simple and yields accurate results after two or three iterations. Nevertheless, there are situations in which the effort and time required are still greater than can be justified. Specifically, if one is doing a pencil-and-paper design of a relatively complex circuit, rapid circuit analysis is a necessity.

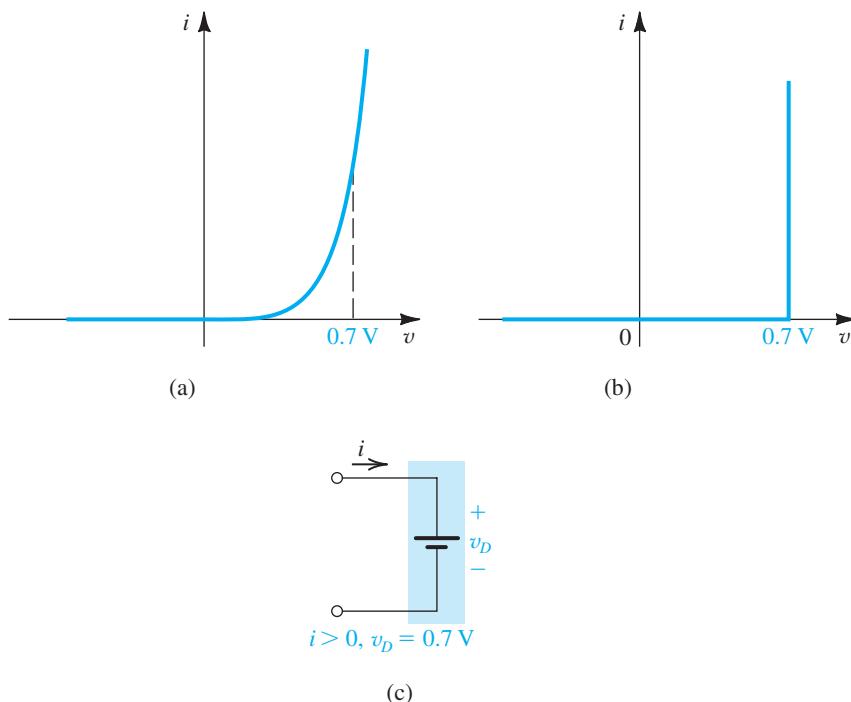
Through quick analysis, the designer is able to evaluate various possibilities before deciding on a suitable circuit design. To speed up the analysis process, one must be content with less precise results. This, however, is seldom a problem, because the more accurate analysis can be postponed until a final or almost-final design is obtained. Accurate analysis of the almost-final design can be performed with the aid of a computer circuit-analysis program such as SPICE (see Appendix B and the website). The results of such an analysis can then be used to further refine or “fine-tune” the design.

To speed up the analysis process, we must find a simpler model for the diode forward characteristic.

### 4.3.5 The Constant-Voltage-Drop Model

The simplest and most widely used diode model is the constant-voltage-drop model. This model is based on the observation that a forward-conducting diode has a voltage drop that varies in a relatively narrow range, say, 0.6 to 0.8 V. The model assumes this voltage to be constant at a value, say, 0.7 V. This development is illustrated in Fig. 4.12.

The constant-voltage-drop model is the one most frequently employed in the initial phases of analysis and design. This is especially true if at these stages one does not have detailed information about the diode characteristics, which is often the case.



**Figure 4.12** Development of the diode constant-voltage-drop model: (a) the exponential characteristic; (b) approximating the exponential characteristic by a constant voltage, usually about 0.7 V; (c) the resulting model of the forward-conducting diodes.

Finally, note that if we employ the constant-voltage-drop model to solve the problem in Example 4.4, we obtain

$$V_D = 0.7 \text{ V}$$

and

$$\begin{aligned} I_D &= \frac{V_{DD} - 0.7}{R} \\ &= \frac{5 - 0.7}{1} = 4.3 \text{ mA} \end{aligned}$$

which are not very different from the values obtained before with the more elaborate exponential model.

### 4.3.6 The Ideal-Diode Model

In applications that involve voltages much greater than the diode voltage drop (0.6 V–0.8 V), we may neglect the diode voltage drop altogether while calculating the diode current. The result is the ideal-diode model, which we studied in Section 4.1. For the circuit in Example 4.4 (i.e., Fig. 4.10 with  $V_{DD} = 5 \text{ V}$  and  $R = 1 \text{ k}\Omega$ ), utilization of the ideal-diode model leads to

$$V_D = 0 \text{ V}$$

$$I_D = \frac{5 - 0}{1} = 5 \text{ mA}$$

which for a very quick analysis would not be bad as a gross estimate. However, with almost no additional work, the 0.7-V-drop model yields much more realistic results. We note, however, that the greatest utility of the ideal-diode model is in determining which diodes are on and which are off in a multidiode circuit, such as those considered in Section 4.1.

## EXERCISES

- 4.10** For the circuit in Fig. 4.10, find  $I_D$  and  $V_D$  for the case  $V_{DD} = 5 \text{ V}$  and  $R = 10 \text{ k}\Omega$ . Assume that the diode has a voltage of 0.7 V at 1-mA current. Use (a) iteration and (b) the constant-voltage-drop model with  $V_D = 0.7 \text{ V}$ .

**Ans.** (a) 0.43 mA, 0.68 V; (b) 0.43 mA, 0.7 V

- D4.11** Design the circuit in Fig. E4.11 to provide an output voltage of 2.4 V. Assume that the diodes available have 0.7-V drop at 1 mA.

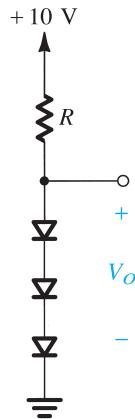


Figure E4.11

**Ans.**  $R = 139 \Omega$

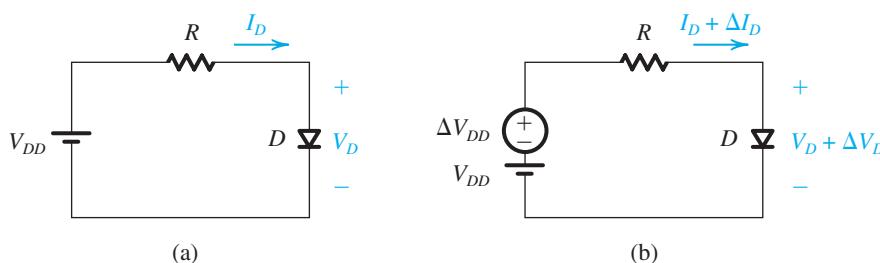
- 4.12** Repeat Exercise 4.4 using the 0.7-V-drop model to obtain better estimates of  $I$  and  $V$  than those found in Exercise 4.4 (using the ideal-diode model).

**Ans.** (a) 1.72 mA, 0.7 V; (b) 0 mA, 5 V; (c) 0 mA, 5 V; (d) 1.72 mA, 0.7 V; (e) 2.3 mA, +2.3 V; (f) 3.3 mA, +1.7 V

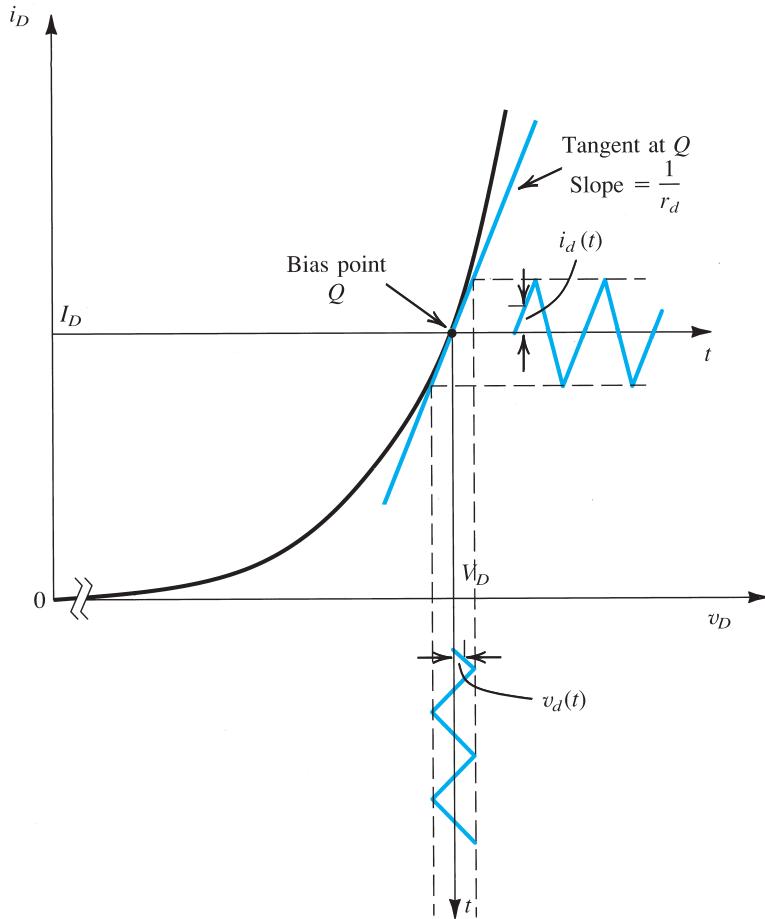
### 4.3.7 The Small-Signal Model

Consider the situation in Fig. 4.13(a), where a dc voltage  $V_{DD}$  establishes a dc current  $I_D$  through the series combination of a resistance  $R$  and a diode  $D$ . The resulting diode voltage is denoted  $V_D$ . As mentioned above, values of  $I_D$  and  $V_D$  can be obtained by solving the circuit using the diode exponential characteristic or, much more quickly, approximate values can be found using the diode constant-voltage-drop model.

Next, consider the situation of  $V_{DD}$  undergoing a small change  $\Delta V_{DD}$ , as shown in Fig. 4.13(b). As indicated, the current  $I_D$  changes by an increment  $\Delta I_D$ , and the diode voltage  $V_D$  changes by an increment  $\Delta V_D$ . We wish to find a quick way to determine the values of these incremental changes. Toward that end, we develop a “small-signal” model for the diode.



**Figure 4.13** (a) A simple diode circuit; (b) the situation when  $V_{DD}$  changes by  $\Delta V_{DD}$ .



**Figure 4.14** Development of the diode small-signal model.

Here the word *signal* emphasizes that in general,  $\Delta V_{DD}$  can be a time-varying quantity. The qualifier “small” indicates that this diode model applies only when  $\Delta V_D$  is kept sufficiently small, with “sufficiently” to be quantified shortly.

To develop the diode small-signal model, refer to Fig. 4.14. We express the voltage across the diode as the sum of the dc voltage  $V_D$  and the time-varying signal  $v_d(t)$ ,

$$v_D(t) = V_D + v_d(t) \quad (4.8)$$

Correspondingly, the total instantaneous diode current  $i_D(t)$  will be

$$i_D(t) = I_S e^{V_D/V_T} \quad (4.9)$$

Substituting for  $v_D$  from Eq. (4.8) gives

$$i_D(t) = I_S e^{(V_D+v_d)/V_T}$$

which can be rewritten

$$i_D(t) = I_S e^{V_D/V_T} e^{v_d/V_T} \quad (4.10)$$

In the absence of the signal  $v_d(t)$ , the diode voltage is equal to  $V_D$ , and the diode current is  $I_D$ , given by

$$I_D = I_S e^{V_D/V_T} \quad (4.11)$$

Thus,  $i_D(t)$  in Eq. (4.10) can be expressed as

$$i_D(t) = I_D e^{v_d/V_T} \quad (4.12)$$

Now if the amplitude of the signal  $v_d(t)$  is kept sufficiently small such that

$$\frac{v_d}{V_T} \ll 1 \quad (4.13)$$

then we may expand the exponential of Eq. (4.12) in a series and truncate the series after the first two terms to obtain the approximate expression

$$i_D(t) \simeq I_D \left( 1 + \frac{v_d}{V_T} \right) \quad (4.14)$$

This is the **small-signal approximation**. It is valid for signals whose amplitudes are smaller than about 5 mV (see Eq. 4.13, and recall that  $V_T = 25$  mV).<sup>3</sup>

From Eq. (4.14) we have

$$i_D(t) = I_D + \frac{I_D}{V_T} v_d \quad (4.15)$$

Thus, superimposed on the dc current  $I_D$ , we have a signal current component directly proportional to the signal voltage  $v_d$ . That is,

$$i_d = I_D + i_d \quad (4.16)$$

where

$$i_d = \frac{I_D}{V_T} v_d \quad (4.17)$$

The quantity relating the signal current  $i_d$  to the signal voltage  $v_d$  has the dimensions of conductance, mhos ( $\Omega$ ), and is called the **diode small-signal conductance**. The inverse of this parameter is the **diode small-signal resistance**, or **incremental resistance**,  $r_d$ ,

$$r_d = \frac{V_T}{I_D} \quad (4.18)$$

Note that the value of  $r_d$  is inversely proportional to the bias current  $I_D$ .

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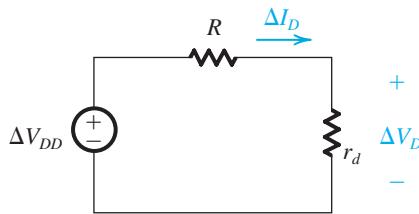
<sup>3</sup>For  $v_d = 5$  mV,  $v_d/V_T = 0.2$ . Thus the next term in the series expansion of the exponential will be  $\frac{1}{2} \times 0.2^2 = 0.02$ , a factor of 10 lower than the linear term we kept.

Additional insight into the small-signal approximation and the small-signal diode model can be obtained by considering again the graphical construction in Fig. 4.14. Here the diode is seen to be operating at a dc bias point  $Q$  characterized by the dc voltage  $V_D$  and the corresponding dc current  $I_D$ . Superimposed on  $V_D$  we have a signal  $v_d(t)$ , assumed (arbitrarily) to have a triangular waveform.

It is easy to see that using the small-signal approximation is equivalent to assuming that *the signal amplitude is sufficiently small such that the excursion along the  $i$ - $v$  curve is limited to a short almost-linear segment*. The slope of this segment, which is equal to the slope of the tangent to the  $i$ - $v$  curve at the operating point  $Q$ , is equal to the small-signal conductance. The reader is encouraged to prove that the slope of the  $i$ - $v$  curve at  $i = I_D$  is equal to  $I_D/V_T$ , which is  $1/r_d$ ; that is,

➤  $r_d = 1 \left/ \left[ \frac{\partial i_D}{\partial v_D} \right] \right|_{i_D=I_D}$  (4.19)

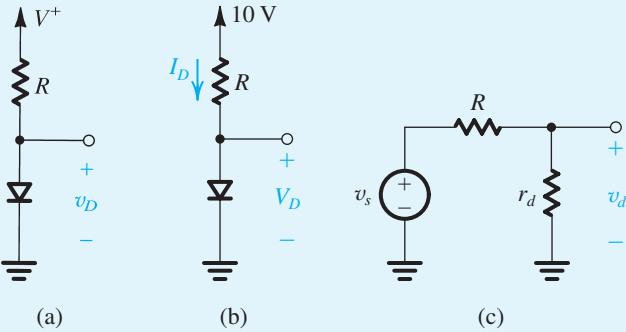
From the preceding we conclude that superimposed on the quantities  $V_D$  and  $I_D$  that define the dc bias point, or **quiescent point**, of the diode will be the small-signal quantities  $v_d(t)$  and  $i_d(t)$ , which are related by the diode small-signal resistance  $r_d$  evaluated at the bias point (Eq. 4.18). Thus the small-signal analysis can be performed separately from the dc bias analysis, a great convenience that results from the linearization of the diode characteristics inherent in the small-signal approximation. Specifically, after the dc analysis is performed, the small-signal equivalent circuit is obtained by eliminating all dc sources (i.e., short-circuiting dc voltage sources and open-circuiting dc current sources) and replacing the diode by its small-signal resistance. Thus, for the circuit in Fig. 4.13(b), the dc analysis is obtained by using the circuit in Fig. 4.13(a), while the incremental quantities  $\Delta I_D$  and  $\Delta V_D$  can be determined by using the small-signal equivalent circuit shown in Fig. 4.15. The following example should further illustrate the application of the small-signal model.



**Figure 4.15** Circuit for determining the incremental quantities  $\Delta I_D$  and  $\Delta V_D$  for the circuit in Figure 4.13(b). Note that replacing the diode with its small-signal resistance  $r_d$  results in a linear circuit.

### Example 4.5

Consider the circuit shown in Fig. 4.16(a) for the case in which  $R = 10 \text{ k}\Omega$ . The power supply  $V^+$  has a dc value of 10 V on which is superimposed a 60-Hz sinusoid of 1-V peak amplitude. (This “signal” component of the power-supply voltage is an imperfection in the power-supply design. It is known as the **power-supply ripple**. More on this later.) Calculate both the dc voltage of the diode and the amplitude of the sine-wave signal appearing across it. Assume the diode to have a 0.7-V drop at 1-mA current.



**Figure 4.16** (a) Circuit for Example 4.5. (b) Circuit for calculating the dc operating point. (c) Small-signal equivalent circuit.

### Solution

Considering dc quantities only, we assume \$V\_D \simeq 0.7\text{ V}\$ and calculate the diode dc current

$$I_D = \frac{10 - 0.7}{10} = 0.93\text{ mA}$$

Since this value is very close to \$1\text{ mA}\$, the diode voltage will be very close to the assumed value of \$0.7\text{ V}\$. At this operating point, the diode incremental resistance \$r\_d\$ is

$$r_d = \frac{V_T}{I_D} = \frac{25}{0.93} = 26.9\Omega$$

The signal voltage across the diode can be found from the small-signal equivalent circuit in Fig. 4.16(c). Here \$v\_s\$ denotes the 60-Hz 1-V peak sinusoidal component of \$V^+\$, and \$v\_d\$ is the corresponding signal across the diode. Using the voltage divider rule provides the peak amplitude of \$v\_d\$ as follows:

$$\begin{aligned} v_d(\text{peak}) &= \hat{V}_s \frac{r_d}{R + r_d} \\ &= 1 \frac{0.0269}{10 + 0.0269} = 2.68\text{ mV} \end{aligned}$$

Finally, we note that since this value is quite small, our use of the small-signal model of the diode is justified.

From the above we see that for a diode circuit that involves both dc and signal quantities, a small-signal equivalent circuit can be obtained by eliminating the dc sources and replacing each diode with its small-signal resistance \$r\_d\$. Such a circuit is linear and can be solved using linear circuit analysis.

Finally, we note that while \$r\_d\$ models the small-signal operation of the diode at low frequencies, its dynamic operation is modeled by the capacitances \$C\_j\$ and \$C\_d\$, which we

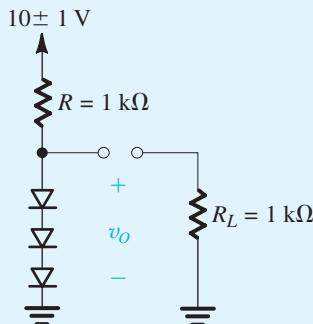
studied in Section 3.6 and which also are small-signal parameters. A complete model of the diode includes  $C_j$  and  $C_d$  in parallel with  $r_d$ .

### 4.3.8 Use of the Diode Forward Drop in Voltage Regulation

A further application of the diode small-signal model is found in a popular diode application, namely, the use of diodes to create a regulated voltage. A **voltage regulator** is a circuit whose purpose is to provide a constant dc voltage between its output terminals. The output voltage is required to remain as constant as possible in spite of (a) changes in the load current drawn from the regulator output terminal and (b) changes in the dc power-supply voltage that feeds the regulator circuit. Since the forward-voltage drop of the diode remains almost constant at approximately 0.7 V while the current through it varies by relatively large amounts, a forward-biased diode can make a simple voltage regulator. For instance, we have seen in Example 4.5 that while the 10-V dc supply voltage had a ripple of 2 V peak-to-peak (a  $\pm 10\%$  variation), the corresponding ripple in the diode voltage was only about  $\pm 2.7$  mV (a  $\pm 0.4\%$  variation). Regulated voltages greater than 0.7 V can be obtained by connecting a number of diodes in series. For example, the use of three forward-biased diodes in series provides a voltage of about 2 V. One such circuit is investigated in the following example, which utilizes the diode small-signal model to quantify the efficacy of the voltage regulator that is realized.

#### Example 4.6

Consider the circuit shown in Fig. 4.17. A string of three diodes is used to provide a constant voltage of about 2.1 V. We want to calculate the percentage change in this regulated voltage caused by (a) a  $\pm 10\%$  change in the power-supply voltage, and (b) connection of a  $1-k\Omega$  load resistance.



**Figure 4.17** Circuit for Example 4.6.

#### Solution

With no load, the nominal value of the current in the diode string is given by

$$I = \frac{10 - 2.1}{1} = 7.9 \text{ mA}$$

Thus each diode will have an incremental resistance of

$$r_d = \frac{V_T}{I}$$

Thus,

$$r_d = \frac{25}{7.9} = 3.2 \Omega$$

The three diodes in series will have a total incremental resistance of

$$r = 3r_d = 9.6 \Omega$$

This resistance, along with the resistance  $R$ , forms a voltage divider whose ratio can be used to calculate the change in output voltage due to a  $\pm 10\%$  (i.e.,  $\pm 1\text{-V}$ ) change in supply voltage. Thus the peak-to-peak change in output voltage will be

$$\Delta v_o = 2 \frac{r}{r+R} = 2 \frac{0.0096}{0.0096 + 1} = 19 \text{ mV peak-to-peak}$$

That is, corresponding to the  $\pm 1\text{-V}$  ( $\pm 10\%$ ) change in supply voltage, the output voltage will change by  $\pm 9.5 \text{ mV}$  or  $\pm 0.5\%$ . Since this implies a change of about  $\pm 3.2 \text{ mV}$  per diode, our use of the small-signal model is justified.

When a load resistance of  $1 \text{ k}\Omega$  is connected across the diode string, it draws a current of approximately  $2.1 \text{ mA}$ . Thus the current in the diodes decreases by  $2.1 \text{ mA}$ , resulting in a decrease in voltage across the diode string given by

$$\Delta v_o = -2.1 \times r = -2.1 \times 9.6 = -20 \text{ mV}$$

Since this implies that the voltage across each diode decreases by about  $6.7 \text{ mV}$ , our use of the small-signal model is not entirely justified. Nevertheless, a detailed calculation of the voltage change using the exponential model results in  $\Delta v_o = -23 \text{ mV}$ , which is not too different from the approximate value obtained using the incremental model.

## EXERCISES

- 4.13** Find the value of the diode small-signal resistance  $r_d$  at bias currents of  $0.1 \text{ mA}$ ,  $1 \text{ mA}$ , and  $10 \text{ mA}$ .

**Ans.**  $250 \Omega$ ;  $25 \Omega$ ;  $2.5 \Omega$

- 4.14** Consider a diode biased at  $1 \text{ mA}$ . Find the change in current as a result of changing the voltage by (a)  $-10 \text{ mV}$ , (b)  $-5 \text{ mV}$ , (c)  $+5 \text{ mV}$ , and (d)  $+10 \text{ mV}$ . In each case, do the calculations (i) using the small-signal model and (ii) using the exponential model.

**Ans.** (a)  $-0.40$ ,  $-0.33 \text{ mA}$ ; (b)  $-0.20$ ,  $-0.18 \text{ mA}$ ; (c)  $+0.20$ ,  $+0.22 \text{ mA}$ ; (d)  $+0.40$ ,  $+0.49 \text{ mA}$

- D4.15** Design the circuit of Fig. E4.15 so that  $V_o = 3 \text{ V}$  when  $I_L = 0$ , and  $V_o$  changes by  $20 \text{ mV}$  per  $1 \text{ mA}$  of load current.

- Use the small-signal model of the diode to find the value of  $R$ .
- Specify the value of  $I_s$  of each of the diodes.

- (c) For this design, use the diode exponential model to determine the actual change in  $V_o$  when a current  $I_L = 1 \text{ mA}$  is drawn from the regulator.

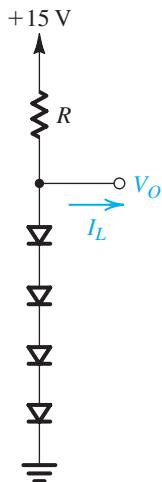


Figure E4.15

**Ans.** (a)  $R = 2.4 \text{ k}\Omega$ ; (b)  $I_S = 4.7 \times 10^{-16} \text{ A}$ ; (c)  $-23 \text{ mV}$

## 4.4 Operation in the Reverse Breakdown Region—Zener Diodes

The very steep  $i-v$  curve that the diode exhibits in the breakdown region (Fig. 4.8) and the almost-constant voltage drop that this indicates suggest that diodes operating in the breakdown region can be used in the design of voltage regulators. From the previous section, the reader will recall that voltage regulators are circuits that provide a constant dc output voltage in the face of changes in their load current and in the system power-supply voltage. This in fact turns out to be an important application of diodes operating in the reverse breakdown region, and special diodes are manufactured to operate specifically in the breakdown region. Such diodes are called **breakdown diodes** or, more commonly, as noted earlier, **zener diodes**.

Figure 4.18 shows the circuit symbol of the zener diode. In normal applications of zener diodes, current flows into the cathode, and the cathode is positive with respect to the anode. Thus  $I_Z$  and  $V_Z$  in Fig. 4.18 have positive values.

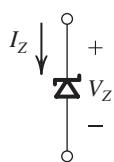


Figure 4.18 Circuit symbol for a zener diode.

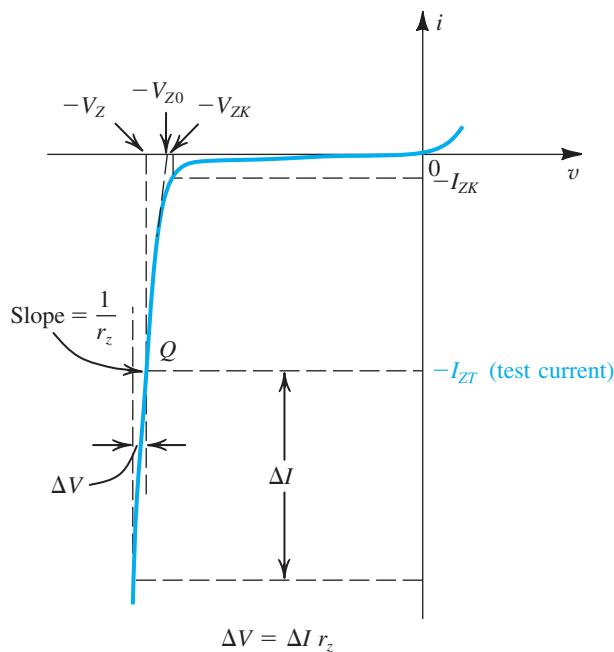
### 4.4.1 Specifying and Modeling the Zener Diode

Figure 4.19 shows details of the diode  $i-v$  characteristic in the breakdown region. We observe that for currents greater than the **knee current**  $I_{ZK}$  (specified on the data sheet of the zener diode), the  $i-v$  characteristic is almost a straight line. The manufacturer usually specifies the voltage across the zener diode  $V_Z$  at a specified test current,  $I_{ZT}$ . We have indicated these parameters in Fig. 4.19 as the coordinates of the point labeled  $Q$ . Thus a 6.8-V zener diode will exhibit a 6.8-V drop at a specified test current of, say, 10 mA. As the current through the zener deviates from  $I_{ZT}$ , the voltage across it will change, though only slightly. Figure 4.19 shows that corresponding to current change  $\Delta I$  the zener voltage changes by  $\Delta V$ , which is related to  $\Delta I$  by

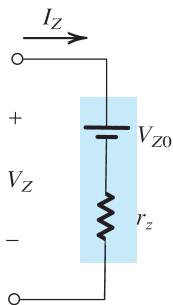
$$\Delta V = r_z \Delta I$$

where  $r_z$  is the inverse of the slope of the almost-linear  $i-v$  curve at point  $Q$ . Resistance  $r_z$  is the **incremental resistance** of the zener diode at operating point  $Q$ . It is also known as the **dynamic resistance** of the zener, and its value is specified on the device data sheet. Typically,  $r_z$  is in the range of a few ohms to a few tens of ohms. Obviously, the lower the value of  $r_z$  is, the more constant the zener voltage remains as its current varies, and thus the more ideal its performance becomes in the design of voltage regulators. In this regard, we observe from Fig. 4.19 that while  $r_z$  remains low and almost constant over a wide range of current, its value increases considerably in the vicinity of the knee. Therefore, as a general design guideline, one should avoid operating the zener in this low-current region.

Zener diodes are fabricated with voltages  $V_Z$  in the range of a few volts to a few hundred volts. In addition to specifying  $V_Z$  (at a particular current  $I_{ZT}$ ),  $r_z$ , and  $I_{ZK}$ , the manufacturer



**Figure 4.19** The diode  $i-v$  characteristic with the breakdown region shown in some detail.

**Figure 4.20** Model for the zener diode.

also specifies the maximum power that the device can safely dissipate. Thus a 0.5-W, 6.8-V zener diode can operate safely at currents up to a maximum of about 70 mA.

The almost-linear  $i-v$  characteristic of the zener diode suggests that the device can be modeled as indicated in Fig. 4.20. Here  $V_{Z0}$  denotes the point at which the straight line of slope  $1/r_z$  intersects the voltage axis (refer to Fig. 4.19). Although  $V_{Z0}$  is shown in Fig. 4.19 to be slightly different from the knee voltage  $V_{ZK}$ , in practice their values are almost equal. The equivalent circuit model of Fig. 4.20 can be analytically described by

$$V_Z = V_{Z0} + r_z I_Z \quad (4.20)$$

and it applies for  $I_Z > I_{ZK}$  and, obviously,  $V_Z > V_{Z0}$ .

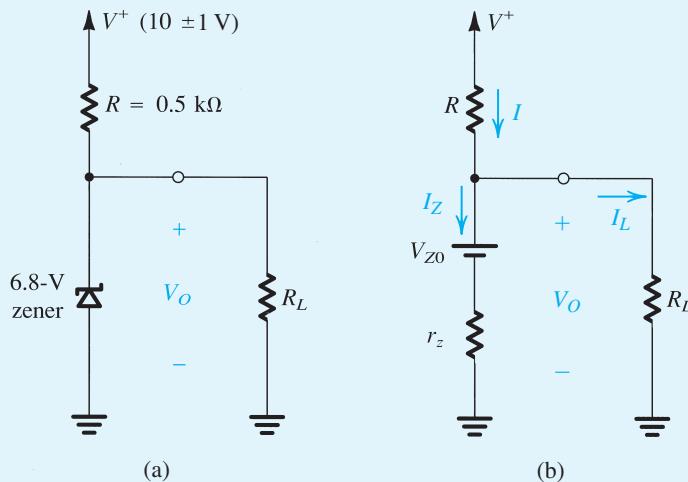
#### 4.4.2 Use of the Zener as a Shunt Regulator

We now illustrate, by way of an example, the use of zener diodes in the design of shunt regulators, so named because the regulator circuit appears in parallel (shunt) with the load.

#### Example 4.7

The 6.8-V zener diode in the circuit of Fig. 4.21(a) is specified to have  $V_Z = 6.8$  V at  $I_Z = 5$  mA,  $r_z = 20 \Omega$ , and  $I_{ZK} = 0.2$  mA. The supply voltage  $V^+$  is nominally 10 V but can vary by  $\pm 1$  V.

- Find  $V_o$  with no load and with  $V^+$  at its nominal value.
- Find the change in  $V_o$  resulting from the  $\pm 1$ -V change in  $V^+$ . Note that  $(\Delta V_o / \Delta V^+)$ , usually expressed in mV/V, is known as **line regulation**.
- Find the change in  $V_o$  resulting from connecting a load resistance  $R_L$  that draws a current  $I_L = 1$  mA, and hence find the **load regulation**  $(\Delta V_o / \Delta I_L)$  in mV/mA.
- Find the change in  $V_o$  when  $R_L = 2$  k $\Omega$ .
- Find the value of  $V_o$  when  $R_L = 0.5$  k $\Omega$ .
- What is the minimum value of  $R_L$  for which the diode still operates in the breakdown region?



**Figure 4.21** (a) Circuit for Example 4.7. (b) The circuit with the zener diode replaced with its equivalent circuit model.

### Solution

First we must determine the value of the parameter  $V_{Z0}$  of the zener diode model. Substituting  $V_Z = 6.8 \text{ V}$ ,  $I_Z = 5 \text{ mA}$ , and  $r_z = 20 \Omega$  in Eq. (4.20) yields  $V_{Z0} = 6.7 \text{ V}$ . Figure 4.21(b) shows the circuit with the zener diode replaced with its model.

(a) With no load connected, the current through the zener is given by

$$\begin{aligned} I_Z &= I = \frac{V^+ - V_{Z0}}{R + r_z} \\ &= \frac{10 - 6.7}{0.5 + 0.02} = 6.35 \text{ mA} \end{aligned}$$

Thus,

$$\begin{aligned} V_O &= V_{Z0} + I_Z r_z \\ &= 6.7 + 6.35 \times 0.02 = 6.83 \text{ V} \end{aligned}$$

(b) For a  $\pm 1\text{-V}$  change in  $V^+$ , the change in output voltage can be found from

$$\begin{aligned} \Delta V_O &= \Delta V^+ \frac{r_z}{R + r_z} \\ &= \pm 1 \times \frac{20}{500 + 20} = \pm 38.5 \text{ mV} \end{aligned}$$

Thus,

$$\text{Line regulation} = 38.5 \text{ mV/V}$$

**Example 4.7** *continued*

(c) When a load resistance  $R_L$  that draws a load current  $I_L = 1 \text{ mA}$  is connected, the zener current will decrease by 1 mA. The corresponding change in zener voltage can be found from

$$\begin{aligned}\Delta V_o &= r_z \Delta I_z \\ &= 20 \times -1 = -20 \text{ mV}\end{aligned}$$

Thus the load regulation is

$$\text{Load regulation} \equiv \frac{\Delta V_o}{\Delta I_L} = -20 \text{ mV/mA}$$

(d) When a load resistance of  $2 \text{ k}\Omega$  is connected, the load current will be approximately  $6.8 \text{ V}/2 \text{ k}\Omega = 3.4 \text{ mA}$ . Thus the change in zener current will be  $\Delta I_z = -3.4 \text{ mA}$ , and the corresponding change in zener voltage (output voltage) will thus be

$$\begin{aligned}\Delta V_o &= r_z \Delta I_z \\ &= 20 \times -3.4 = -68 \text{ mV}\end{aligned}$$

This value could have been obtained by multiplying the load regulation by the value of  $I_L$  (3.4 mA).

(e) An  $R_L$  of  $0.5 \text{ k}\Omega$  would draw a load current of  $6.8/0.5 = 13.6 \text{ mA}$ . This is not possible, because the current  $I$  supplied through  $R$  is only 6.4 mA (for  $V^+ = 10 \text{ V}$ ). Therefore, the zener must be cut off. If this is indeed the case, then  $V_o$  is determined by the voltage divider formed by  $R_L$  and  $R$  (Fig. 4.21a),

$$\begin{aligned}V_o &= V^+ \frac{R_L}{R + R_L} \\ &= 10 \frac{0.5}{0.5 + 0.5} = 5 \text{ V}\end{aligned}$$

Since this voltage is lower than the breakdown voltage of the zener, the diode is indeed no longer operating in the breakdown region.

(f) For the zener to be at the edge of the breakdown region,  $I_z = I_{zK} = 0.2 \text{ mA}$  and  $V_z \simeq V_{zK} \simeq 6.7 \text{ V}$ . At this point the lowest (worst-case) current supplied through  $R$  is  $(9 - 6.7)/0.5 = 4.6 \text{ mA}$ , and thus the load current is  $4.6 - 0.2 = 4.4 \text{ mA}$ . The corresponding value of  $R_L$  is

$$R_L = \frac{6.7}{4.4} \simeq 1.5 \text{ k}\Omega$$

### 4.4.3 Temperature Effects

The dependence of the zener voltage  $V_z$  on temperature is specified in terms of its **temperature coefficient TC**, or **temco** as it is commonly known, which is usually expressed in  $\text{mV}^\circ\text{C}$ . The value of TC depends on the zener voltage, and for a given diode the TC varies with the operating current. Zener diodes whose  $V_z$  are lower than about 5 V exhibit a negative TC. On the other hand, zeners with higher voltages exhibit a positive TC. The TC of a zener diode with a  $V_z$  of about 5 V can be made zero by operating the diode at a specified current. Another commonly used technique for obtaining a reference voltage with low temperature coefficient

is to connect a zener diode with a positive temperature coefficient of about  $2 \text{ mV}/^\circ\text{C}$  in series with a forward-conducting diode. Since the forward-conducting diode has a voltage drop of  $\approx 0.7 \text{ V}$  and a TC of about  $-2 \text{ mV}/^\circ\text{C}$ , the series combination will provide a voltage of  $(V_z + 0.7)$  with a TC of about zero.

## EXERCISES

- 4.16** A zener diode whose nominal voltage is 10 V at 10 mA has an incremental resistance of  $50 \Omega$ . What voltage do you expect if the diode current is halved? Doubled? What is the value of  $V_{zo}$  in the zener model?  
**Ans.** 9.75 V; 10.5 V; 9.5 V
- 4.17** A zener diode exhibits a constant voltage of 5.6 V for currents greater than five times the knee current.  $I_{ZK}$  is specified to be 1 mA. The zener is to be used in the design of a shunt regulator fed from a 15-V supply. The load current varies over the range of 0 mA to 15 mA. Find a suitable value for the resistor  $R$ . What is the maximum power dissipation of the zener diode?  
**Ans.**  $470 \Omega$ ; 112 mW
- 4.18** A shunt regulator utilizes a zener diode whose voltage is 5.1 V at a current of 50 mA and whose incremental resistance is  $7 \Omega$ . The diode is fed from a supply of 15-V nominal voltage through a  $200-\Omega$  resistor. What is the output voltage at no load? Find the line regulation and the load regulation.  
**Ans.** 5.1 V; 33.8 mV/V;  $-7 \text{ mV}/\text{mA}$

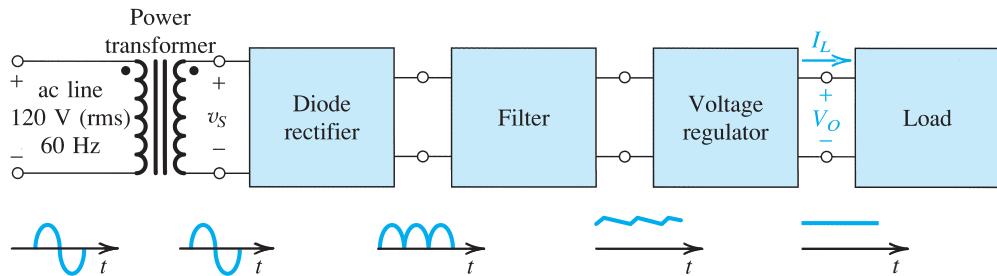
### 4.4.4 A Final Remark

Though simple and useful, zener diodes have lost a great deal of their popularity in recent years. They have been virtually replaced in voltage-regulator design by specially designed integrated circuits (ICs) that perform the voltage-regulation function much more effectively and with greater flexibility than zener diodes.

## 4.5 Rectifier Circuits

One of the most important applications of diodes is in the design of rectifier circuits. A diode rectifier forms an essential building block of the dc power supplies required to power electronic equipment. A block diagram of such a power supply is shown in Fig. 4.22. As indicated, the power supply is fed from the 120-V (rms) 60-Hz ac line, and it delivers a dc voltage  $V_o$  (usually in the range of 4 V to 20 V) to an electronic circuit represented by the *load* block. The dc voltage  $V_o$  is required to be as constant as possible in spite of variations in the ac line voltage and in the current drawn by the load.

The first block in a dc power supply is the **power transformer**. It consists of two separate coils wound around an iron core that magnetically couples the two windings. The **primary winding**, having  $N_1$  turns, is connected to the 120-V ac supply, and the **secondary winding**, having  $N_2$  turns, is connected to the circuit of the dc power supply. Thus an ac voltage  $v_s$  of  $120(N_2/N_1) \text{ V}$  (rms) develops between the two terminals of the secondary winding. By



**Figure 4.22** Block diagram of a dc power supply.

selecting an appropriate turns ratio ( $N_1/N_2$ ) for the transformer, the designer can step the line voltage down to the value required to yield the particular dc voltage output of the supply. For instance, a secondary voltage of 8-V rms may be appropriate for a dc output of 5 V. This can be achieved with a 15:1 turns ratio.

In addition to providing the appropriate sinusoidal amplitude for the dc power supply, the power transformer provides electrical isolation between the electronic equipment and the power-line circuit. This isolation minimizes the risk of electric shock to the equipment user.

The diode rectifier converts the input sinusoid  $v_s$  to a unipolar output, which can have the pulsating waveform indicated in Fig. 4.22. Although this waveform has a nonzero average or a dc component, its pulsating nature makes it unsuitable as a dc source for electronic circuits, hence the need for a filter. The variations in the magnitude of the rectifier output are considerably reduced by the filter block in Fig. 4.22. In this section we shall study a number of rectifier circuits and a simple implementation of the output filter.

The output of the rectifier filter, though much more constant than without the filter, still contains a time-dependent component, known as **ripple**. To reduce the ripple and to stabilize the magnitude of the dc output voltage against variations caused by changes in load current, a voltage regulator is employed. Such a regulator can be implemented using the zener shunt regulator configuration studied in Section 4.4. Alternatively, and much more commonly at present, an integrated-circuit regulator can be used.

### 4.5.1 The Half-Wave Rectifier

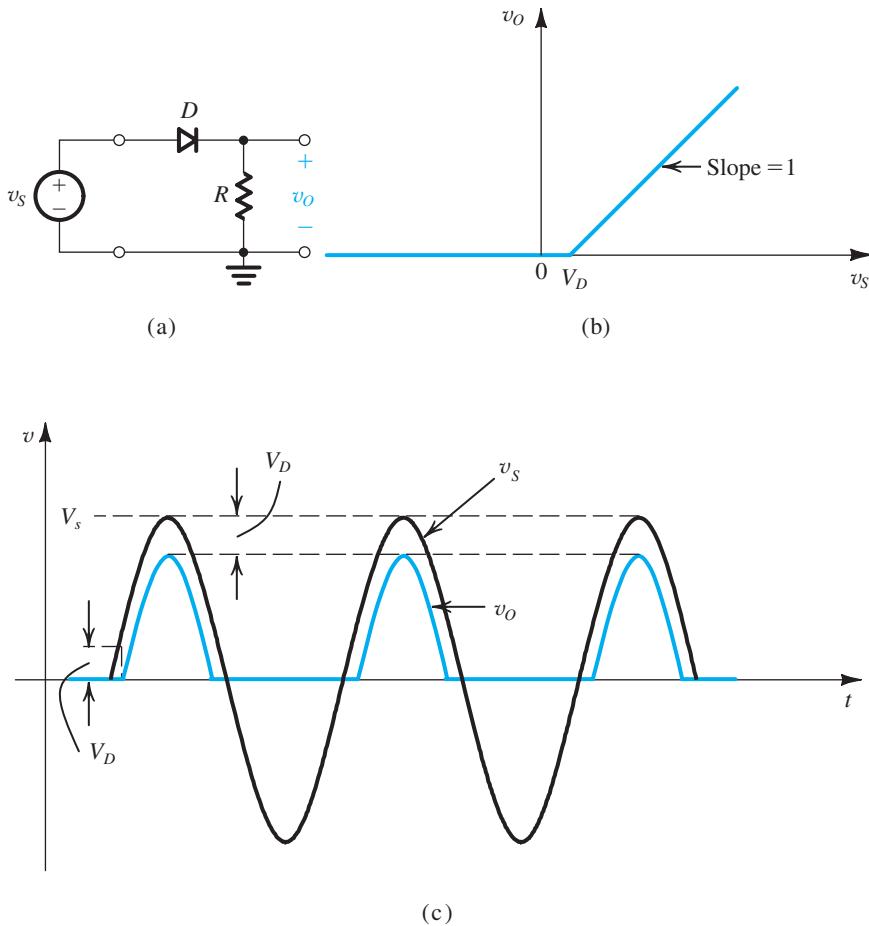
The half-wave rectifier utilizes alternate half-cycles of the input sinusoid. Figure 4.23(a) shows the circuit of a half-wave rectifier. This circuit was analyzed in Section 4.1 (see Fig. 4.3) assuming an ideal diode. Using the more realistic constant-voltage-drop diode model, we obtain

$$v_o = 0, \quad v_s < V_D \quad (4.21a)$$

$$v_o = v_s - V_D, \quad v_s \geq V_D \quad (4.21b)$$

The transfer characteristic represented by these equations is sketched in Fig. 4.23(b), where  $V_D = 0.7$  V or 0.8 V. Figure 4.23(c) shows the output voltage obtained when the input  $v_s$  is a sinusoid.

In selecting diodes for rectifier design, two important parameters must be specified: the current-handling capability required of the diode, determined by the largest current the diode is expected to conduct, and the **peak inverse voltage** (PIV) that the diode must be able to



**Figure 4.23** (a) Half-wave rectifier. (b) Transfer characteristic of the rectifier circuit. (c) Input and output waveforms.

withstand without breakdown, determined by the largest reverse voltage that is expected to appear across the diode. In the rectifier circuit of Fig. 4.23(a), we observe that when  $v_s$  is negative the diode will be cut off and  $v_o$  will be zero. It follows that the PIV is equal to the peak of  $v_s$ ,

$$\text{PIV} = V_s \quad (4.22)$$

It is usually prudent, however, to select a diode that has a reverse breakdown voltage at least 50% greater than the expected PIV.

Before leaving the half-wave rectifier, the reader should note two points. First, it is possible to use the diode exponential characteristic to determine the exact transfer characteristic of the rectifier (see Problem 4.68). However, the amount of work involved is usually too great to be justified in practice. Of course, such an analysis can be easily done using a computer circuit-analysis program such as SPICE.

Second, whether we analyze the circuit accurately or not, it should be obvious that this circuit does not function properly when the input signal is small. For instance, this circuit cannot be used to rectify an input sinusoid of 100-mV amplitude. For such an application one

resorts to a so-called precision rectifier, a circuit utilizing diodes in conjunction with op amps. One such circuit is presented in Section 4.5.5.

### EXERCISE

- 4.19** For the half-wave rectifier circuit in Fig. 4.23(a), show the following: (a) For the half-cycles during which the diode conducts, conduction begins at an angle  $\theta = \sin^{-1}(V_D/V_s)$  and terminates at  $(\pi - \theta)$ , for a total conduction angle of  $(\pi - 2\theta)$ . (b) The average value (dc component) of  $v_o$  is  $V_o \simeq (1/\pi)V_s - V_D/2$ . (c) The peak diode current is  $(V_s - V_D)/R$ .

Find numerical values for these quantities for the case of 12-V (rms) sinusoidal input,  $V_D \simeq 0.7$  V, and  $R = 100 \Omega$ . Also, give the value for PIV.

**Ans.** (a)  $\theta = 2.4^\circ$ , conduction angle =  $175^\circ$ ; (b) 5.05 V; (c) 163 mA; 17 V

### 4.5.2 The Full-Wave Rectifier

The full-wave rectifier utilizes both halves of the input sinusoid. To provide a unipolar output, it inverts the negative halves of the sine wave. One possible implementation is shown in Fig. 4.24(a). Here the transformer secondary winding is **center-tapped** to provide two equal voltages  $v_s$  across the two halves of the secondary winding with the polarities indicated. Note that when the input line voltage (feeding the primary) is positive, both of the signals labeled  $v_s$  will be positive. In this case  $D_1$  will conduct and  $D_2$  will be reverse biased. The current through  $D_1$  will flow through  $R$  and back to the center tap of the secondary. The circuit then behaves like a half-wave rectifier, and the output during the positive half-cycles when  $D_1$  conducts will be identical to that produced by the half-wave rectifier.

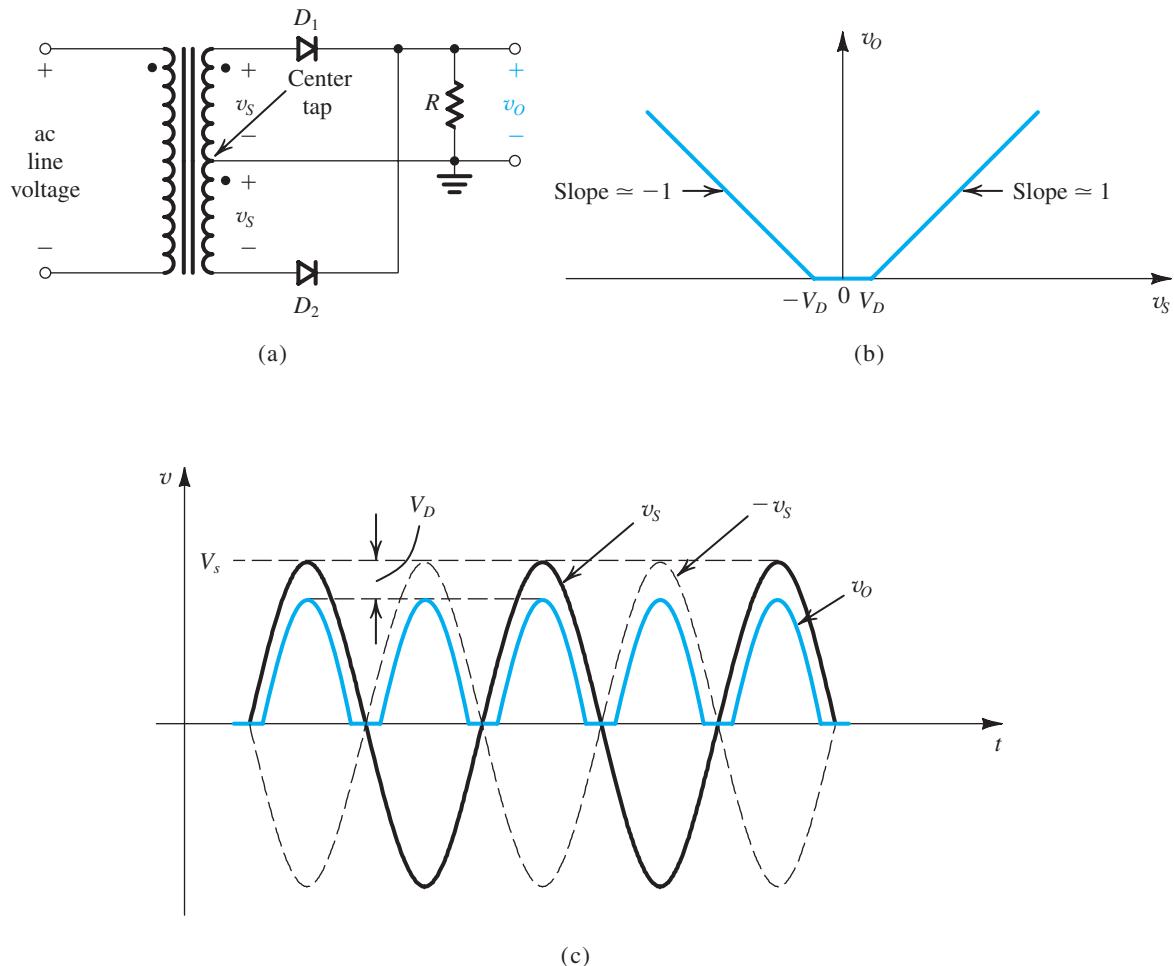
Now, during the negative half-cycle of the ac line voltage, both of the voltages labeled  $v_s$  will be negative. Thus  $D_1$  will be cut off while  $D_2$  will conduct. The current conducted by  $D_2$  will flow through  $R$  and back to the center tap. It follows that during the negative half-cycles while  $D_2$  conducts, the circuit behaves again as a half-wave rectifier. The important point, however, is that the current through  $R$  always flows in the same direction, and thus  $v_o$  will be unipolar, as indicated in Fig. 4.24(c). The output waveform shown is obtained by assuming that a conducting diode has a constant voltage drop  $V_D$ . Thus the transfer characteristic of the full-wave rectifier takes the shape shown in Fig. 4.24(b).

The full-wave rectifier obviously produces a more “energetic” waveform than that provided by the half-wave rectifier. In almost all rectifier applications, one opts for a full-wave type of some kind.

To find the PIV of the diodes in the full-wave rectifier circuit, consider the situation during the positive half-cycles. Diode  $D_1$  is conducting, and  $D_2$  is cut off. The voltage at the cathode of  $D_2$  is  $v_o$ , and that at its anode is  $-v_s$ . Thus the reverse voltage across  $D_2$  will be  $(v_o + v_s)$ , which will reach its maximum when  $v_o$  is at its peak value of  $(V_s - V_D)$ , and  $v_s$  is at its peak value of  $V_s$ ; thus,

$$\text{PIV} = 2V_s - V_D$$

which is approximately twice that for the case of the half-wave rectifier.



**Figure 4.24** Full-wave rectifier utilizing a transformer with a center-tapped secondary winding: (a) circuit; (b) transfer characteristic assuming a constant-voltage-drop model for the diodes; (c) input and output waveforms.

### EXERCISE

- 4.20** For the full-wave rectifier circuit in Fig. 4.24(a), show the following: (a) The output is zero for an angle of  $2 \sin^{-1}(V_D/V_s)$  centered around the zero-crossing points of the sine-wave input. (b) The average value (dc component) of  $v_o$  is  $V_o \approx (2/\pi)V_s - V_D$ . (c) The peak current through each diode is  $(V_s - V_D)/R$ . Find the fraction (percentage) of each cycle during which  $v_o > 0$ , the value of  $V_o$ , the peak diode current, and the value of PIV, all for the case in which  $v_s$  is a 12-V (rms) sinusoid,  $V_D \approx 0.7$  V, and  $R = 100 \Omega$ .

**Ans.** 97.4%; 10.1 V; 163 mA; 33.2 V

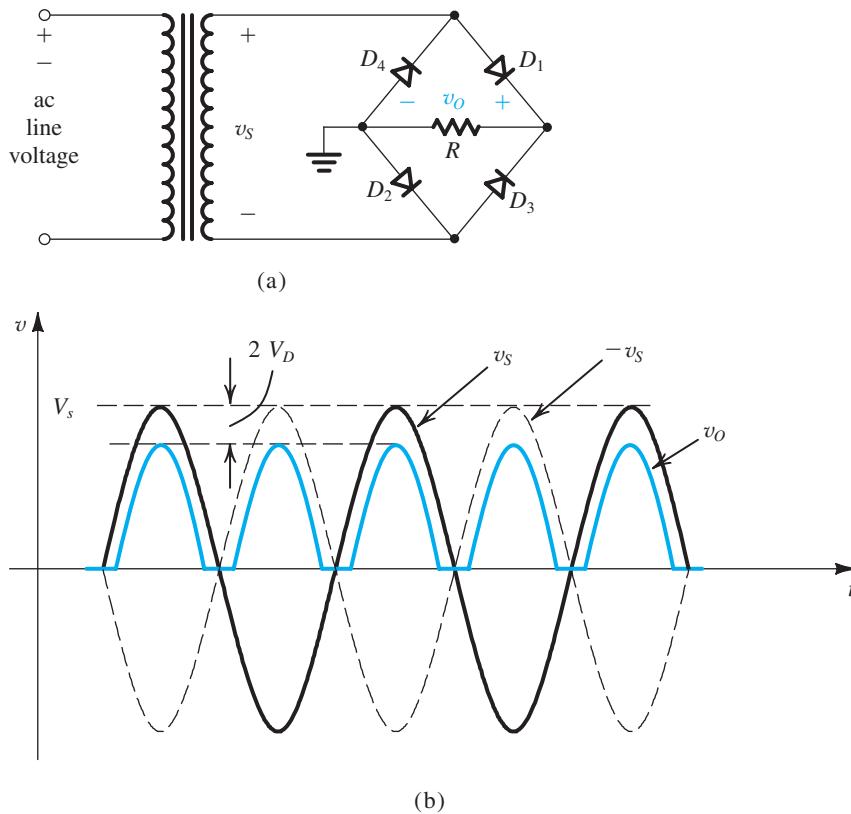
### 4.5.3 The Bridge Rectifier

An alternative implementation of the full-wave rectifier is shown in Fig. 4.25(a). This circuit, known as the bridge rectifier because of the similarity of its configuration to that of the Wheatstone bridge, does not require a center-tapped transformer, a distinct advantage over the full-wave rectifier circuit of Fig. 4.24. The bridge rectifier, however, requires four diodes as compared to two in the previous circuit. This is not much of a disadvantage, because diodes are inexpensive and one can buy a diode bridge in one package.

The bridge-rectifier circuit operates as follows: During the positive half-cycles of the input voltage,  $v_s$  is positive, and thus current is conducted through diode  $D_1$ , resistor  $R$ , and diode  $D_2$ . Meanwhile, diodes  $D_3$  and  $D_4$  will be reverse biased. Observe that there are two diodes in series in the conduction path, and thus  $v_o$  will be lower than  $v_s$  by two diode drops (compared to one drop in the circuit previously discussed). This is somewhat of a disadvantage of the bridge rectifier.

Next, consider the situation during the negative half-cycles of the input voltage. The secondary voltage  $v_s$  will be negative, and thus  $-v_s$  will be positive, forcing current through  $D_3$ ,  $R$ , and  $D_4$ . Meanwhile, diodes  $D_1$  and  $D_2$  will be reverse biased. The important point to note, though, is that during both half-cycles, current flows through  $R$  in the same direction (from right to left), and thus  $v_o$  will always be positive, as indicated in Fig. 4.25(b).

To determine the peak inverse voltage (PIV) of each diode, consider the circuit during the positive half-cycles. The reverse voltage across  $D_3$  can be determined from the loop formed



**Figure 4.25** The bridge rectifier: (a) circuit; (b) input and output waveforms.

by  $D_3$ ,  $R$ , and  $D_2$  as

$$v_{D3}(\text{reverse}) = v_o + v_{D2}(\text{forward})$$

Thus the maximum value of  $v_{D3}$  occurs at the peak of  $v_o$  and is given by

$$\text{PIV} = V_s - 2V_D + V_D = V_s - V_D$$

Observe that here the PIV is about half the value for the full-wave rectifier with a center-tapped transformer. This is another advantage of the bridge rectifier.

Yet one more advantage of the bridge-rectifier circuit over that utilizing a center-tapped transformer is that only about half as many turns are required for the secondary winding of the transformer. Another way of looking at this point can be obtained by observing that each half of the secondary winding of the center-tapped transformer is utilized for only half the time. These advantages have made the bridge rectifier the most popular rectifier circuit configuration.

### EXERCISE

- 4.21** For the bridge-rectifier circuit of Fig. 4.25(a), use the constant-voltage-drop diode model to show that  
 (a) the average (or dc component) of the output voltage is  $V_o \simeq (2/\pi)V_s - 2V_D$  and (b) the peak diode current is  $(V_s - 2V_D)/R$ . Find numerical values for the quantities in (a) and (b) and the PIV for the case in which  $v_s$  is a 12-V (rms) sinusoid,  $V_D \simeq 0.7$  V, and  $R = 100$   $\Omega$ .

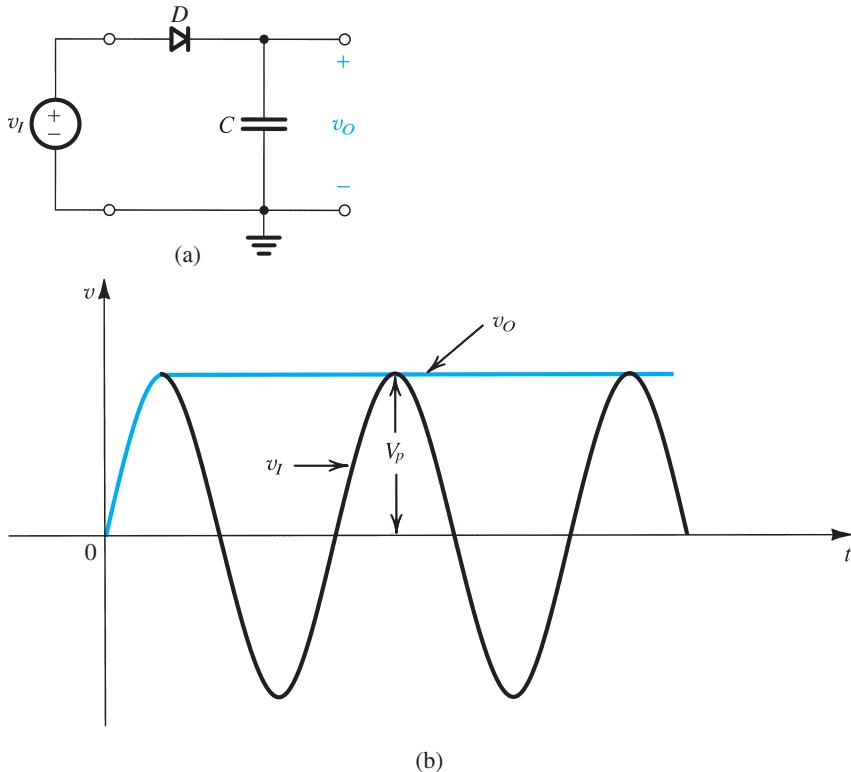
**Ans.** 9.4 V; 156 mA; 16.3 V

#### 4.5.4 The Rectifier with a Filter Capacitor—The Peak Rectifier

The pulsating nature of the output voltage produced by the rectifier circuits discussed above makes it unsuitable as a dc supply for electronic circuits. A simple way to reduce the variation of the output voltage is to place a capacitor across the load resistor. It will be shown that this **filter capacitor** serves to reduce substantially the variations in the rectifier output voltage.

To see how the rectifier circuit with a filter capacitor works, consider first the simple circuit shown in Fig. 4.26. Let the input  $v_i$  be a sinusoid with a peak value  $V_p$ , and assume the diode to be ideal. As  $v_i$  goes positive, the diode conducts and the capacitor is charged so that  $v_o = v_i$ . This situation continues until  $v_i$  reaches its peak value  $V_p$ . Beyond the peak, as  $v_i$  decreases, the diode becomes reverse biased and the output voltage remains constant at the value  $V_p$ . In fact, theoretically speaking, the capacitor will retain its charge and hence its voltage indefinitely, because there is no way for the capacitor to discharge. Thus the circuit provides a dc voltage output equal to the peak of the input sine wave. This is a very encouraging result in view of our desire to produce a dc output.

Next, we consider the more practical situation where a load resistance  $R$  is connected across the capacitor  $C$ , as depicted in Fig. 4.27(a). However, we will continue to assume the diode to be ideal. As before, for a sinusoidal input, the capacitor charges to the peak of the input  $V_p$ . Then the diode cuts off, and the capacitor discharges through the load resistance  $R$ . The capacitor discharge will continue for almost the entire cycle, until the time at which  $v_i$



**Figure 4.26** (a) A simple circuit used to illustrate the effect of a filter capacitor. (b) Input and output waveforms assuming an ideal diode. Note that the circuit provides a dc voltage equal to the peak of the input sine wave. The circuit is therefore known as a *peak rectifier* or a *peak detector*.

exceeds the capacitor voltage. Then the diode turns on again and charges the capacitor up to the peak of  $v_I$ , and the process repeats itself. Observe that to keep the output voltage from decreasing too much during capacitor discharge, one selects a value for  $C$  so that the time constant  $CR$  is much greater than the discharge interval.

We are now ready to analyze the circuit in detail. Figure 4.27(b) shows the steady-state input and output voltage waveforms under the assumption that  $CR \gg T$ , where  $T$  is the period of the input sinusoid. The waveforms of the load current

$$i_L = v_O/R \quad (4.23)$$

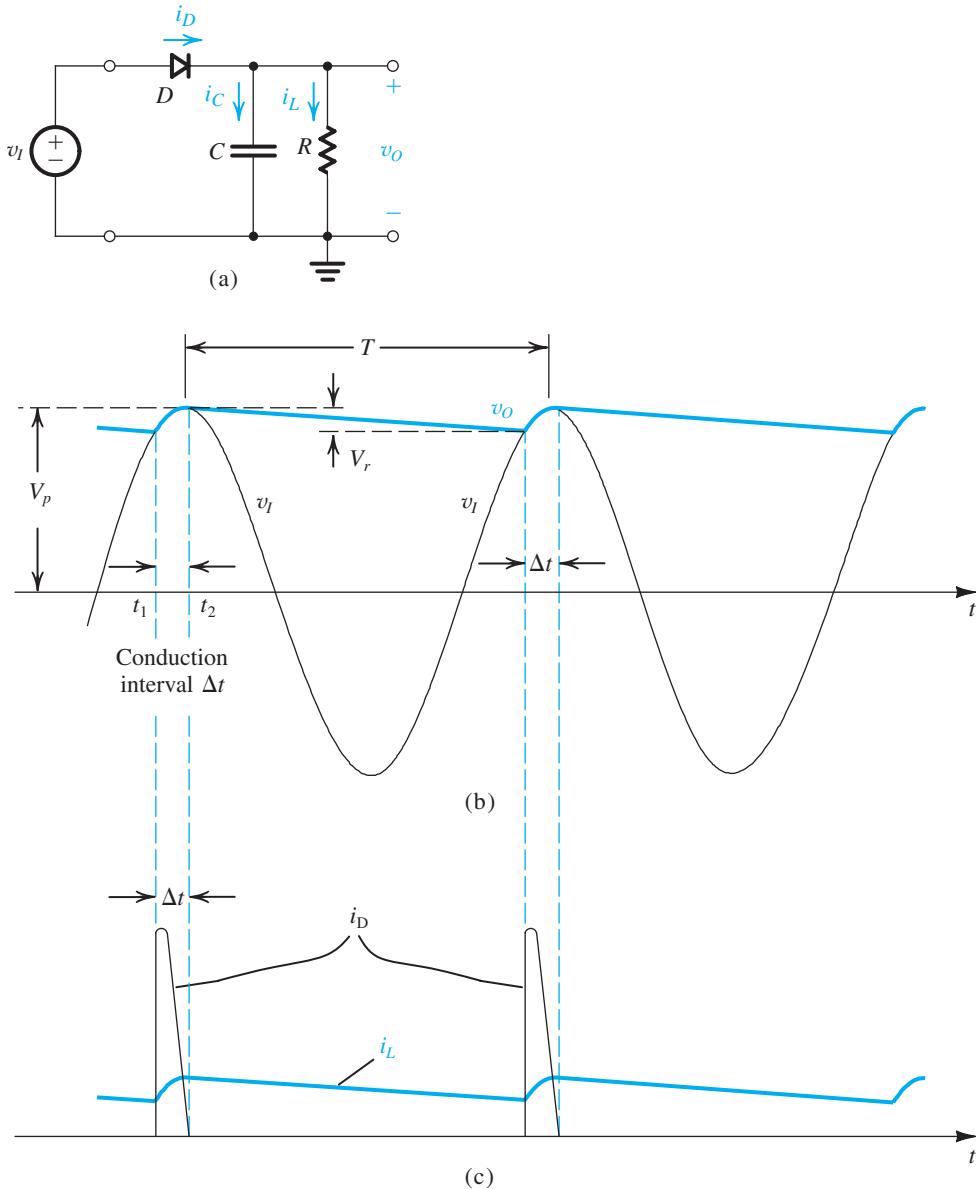
and of the diode current (when it is conducting)

$$i_D = i_C + i_L \quad (4.24)$$

$$= C \frac{dv_I}{dt} + i_L \quad (4.25)$$

are shown in Fig. 4.27(c). The following observations are in order:

1. The diode conducts for a brief interval,  $\Delta t$ , near the peak of the input sinusoid and supplies the capacitor with charge equal to that lost during the much longer discharge interval. The latter is approximately equal to the period  $T$ .



**Figure 4.27** Voltage and current waveforms in the peak-rectifier circuit with  $CR \gg T$ . The diode is assumed ideal.

2. Assuming an ideal diode, the diode conduction begins at time  $t_1$ , at which the input  $v_I$  equals the exponentially decaying output  $v_O$ . Conduction stops at  $t_2$  shortly after the peak of  $v_I$ ; the exact value of  $t_2$  can be determined by setting  $i_D = 0$  in Eq. (4.25).
3. During the diode-off interval, the capacitor  $C$  discharges through  $R$ , and thus  $v_O$  decays exponentially with a time constant  $CR$ . The discharge interval begins just past the peak of  $v_I$ . At the end of the discharge interval, which lasts for almost the entire period  $T$ ,  $v_O = V_p - V_r$ , where  $V_r$  is the peak-to-peak ripple voltage. When  $CR \gg T$ , the value of  $V_r$  is small.

4. When  $V_r$  is small,  $v_o$  is almost constant and equal to the peak value of  $v_I$ . Thus the dc output voltage is approximately equal to  $V_p$ . Similarly, the current  $i_L$  is almost constant, and its dc component  $I_L$  is given by

➤

$$I_L = \frac{V_p}{R} \quad (4.26)$$

If desired, a more accurate expression for the output dc voltage can be obtained by taking the average of the extreme values of  $v_o$ ,

➤

$$V_o = V_p - \frac{1}{2}V_r \quad (4.27)$$

With these observations in hand, we now derive expressions for  $V_r$  and for the average and peak values of the diode current. During the diode-off interval,  $v_o$  can be expressed as

$$v_o = V_p e^{-t/CR}$$

At the end of the discharge interval we have

$$V_p - V_r \simeq V_p e^{-T/CR}$$

Now, since  $CR \gg T$ , we can use the approximation  $e^{-T/CR} \simeq 1 - T/CR$  to obtain

$$V_r \simeq V_p \frac{T}{CR} \quad (4.28)$$

We observe that to keep  $V_r$  small we must select a capacitance  $C$  so that  $CR \gg T$ . The **ripple voltage**  $V_r$  in Eq. (4.28) can be expressed in terms of the frequency  $f = 1/T$  as

➤

$$V_r = \frac{V_p}{fCR} \quad (4.29a)$$

Using Eq. (4.26) we can express  $V_r$  by the alternate expression

$$V_r = \frac{I_L}{fC} \quad (4.29b)$$

Note that an alternative interpretation of the approximation made above is that the capacitor discharges by means of a constant current  $I_L = V_p/R$ . This approximation is valid as long as  $V_r \ll V_p$ .

Assuming that diode conduction ceases almost at the peak of  $v_I$ , we can determine the **conduction interval**  $\Delta t$  from

$$V_p \cos(\omega\Delta t) = V_p - V_r$$

where  $\omega = 2\pi f = 2\pi/T$  is the angular frequency of  $v_I$ . Since  $(\omega\Delta t)$  is a small angle, we can employ the approximation  $\cos(\omega\Delta t) \simeq 1 - \frac{1}{2}(\omega\Delta t)^2$  to obtain

➤

$$\omega\Delta t \simeq \sqrt{2V_r/V_p} \quad (4.30)$$

We note that when  $V_r \ll V_p$ , the conduction angle  $\omega\Delta t$  will be small, as assumed.

To determine the average diode current during conduction,  $i_{Dav}$ , we equate the charge that the diode supplies to the capacitor,

$$Q_{\text{supplied}} = i_{Cav} \Delta t$$

where from Eq. (4.24),

$$i_{Cav} = i_{Dav} - I_L$$

to the charge that the capacitor loses during the discharge interval,

$$Q_{lost} = CV_r$$

to obtain, using Eqs. (4.30) and (4.29a),

$$i_{Dav} = I_L \left( 1 + \pi \sqrt{2V_p/V_r} \right) \quad (4.31)$$

Observe that when  $V_r \ll V_p$ , the average diode current during conduction is much greater than the dc load current. This is not surprising, since the diode conducts for a very short interval and must replenish the charge lost by the capacitor during the much longer interval in which it is discharged by  $I_L$ .

The peak value of the diode current,  $i_{Dmax}$ , can be determined by evaluating the expression in Eq. (4.25) at the onset of diode conduction—that is, at  $t = t_1 = -\Delta t$  (where  $t = 0$  is at the peak). Assuming that  $i_L$  is almost constant at the value given by Eq. (4.26), we obtain

$$i_{Dmax} = I_L \left( 1 + 2\pi \sqrt{2V_p/V_r} \right) \quad (4.32)$$

From Eqs. (4.31) and (4.32), we see that for  $V_r \ll V_p$ ,  $i_{Dmax} \approx 2i_{Dav}$ , which correlates with the fact that the waveform of  $i_D$  is almost a right-angle triangle (see Fig. 4.27c).

### Example 4.8

Consider a peak rectifier fed by a 60-Hz sinusoid having a peak value  $V_p = 100$  V. Let the load resistance  $R = 10$  k $\Omega$ . Find the value of the capacitance  $C$  that will result in a peak-to-peak ripple of 2 V. Also, calculate the fraction of the cycle during which the diode is conducting and the average and peak values of the diode current.

#### Solution

From Eq. (4.29a) we obtain the value of  $C$  as

$$C = \frac{V_p}{V_r f R} = \frac{100}{2 \times 60 \times 10 \times 10^3} = 83.3 \mu\text{F}$$

The conduction angle  $\omega\Delta t$  is found from Eq. (4.30) as

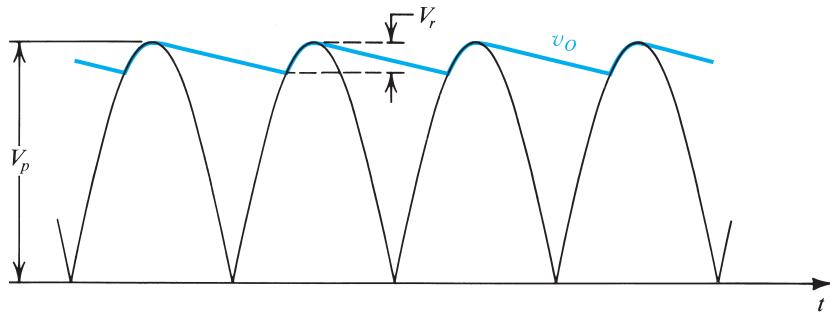
$$\omega\Delta t = \sqrt{2 \times 2/100} = 0.2 \text{ rad}$$

Thus the diode conducts for  $(0.2/2\pi) \times 100 = 3.18\%$  of the cycle. The average diode current is obtained from Eq. (4.31), where  $I_L = 100/10 = 10$  mA, as

$$i_{Dav} = 10 \left( 1 + \pi \sqrt{2 \times 100/2} \right) = 324 \text{ mA}$$

The peak diode current is found using Eq. (4.32),

$$i_{Dmax} = 10 \left( 1 + 2\pi \sqrt{2 \times 100/2} \right) = 638 \text{ mA}$$



**Figure 4.28** Waveforms in the full-wave peak rectifier.

The circuit of Fig. 4.27(a) is known as a half-wave **peak rectifier**. The full-wave rectifier circuits of Figs. 4.24(a) and 4.25(a) can be converted to peak rectifiers by including a capacitor across the load resistor. As in the half-wave case, the output dc voltage will be almost equal to the peak value of the input sine wave (Fig. 4.28). The ripple frequency, however, will be twice that of the input. The peak-to-peak ripple voltage, for this case, can be derived using a procedure identical to that above but with the discharge period  $T$  replaced by  $T/2$ , resulting in

$$\text{➤ } V_r = \frac{V_p}{2fCR} \quad (4.33)$$

While the diode conduction interval,  $\Delta t$ , will still be given by Eq. (4.30), the average and peak currents in each of the diodes will be given by

$$\text{➤ } i_{Dav} = I_L \left( 1 + \pi \sqrt{V_p/2V_r} \right) \quad (4.34)$$

$$\text{➤ } i_{Dmax} = I_L \left( 1 + 2\pi \sqrt{V_p/2V_r} \right) \quad (4.35)$$

Comparing these expressions with the corresponding ones for the half-wave case, we note that for the same values of  $V_p$ ,  $f$ ,  $R$ , and  $V_r$  (and thus the same  $I_L$ ), we need a capacitor half the size of that required in the half-wave rectifier. Also, the current in each diode in the full-wave rectifier is approximately half that which flows in the diode of the half-wave circuit.

The analysis above assumed ideal diodes. The accuracy of the results can be improved by taking the diode voltage drop into account. This can be easily done by replacing the peak voltage  $V_p$  to which the capacitor charges with  $(V_p - V_D)$  for the half-wave circuit and the full-wave circuit using a center-tapped transformer and with  $(V_p - 2V_D)$  for the bridge-rectifier case.

We conclude this section by noting that peak-rectifier circuits find application in signal-processing systems where it is required to detect the peak of an input signal. In such a case, the circuit is referred to as a **peak detector**. A particularly popular application of the peak detector is in the design of a demodulator for amplitude-modulated (AM) signals. We shall not discuss this application further here.

## EXERCISES

- 4.22** Derive the expressions in Eqs. (4.33), (4.34), and (4.35).
- 4.23** Consider a bridge-rectifier circuit with a filter capacitor  $C$  placed across the load resistor  $R$  for the case in which the transformer secondary delivers a sinusoid of 12 V (rms) having a 60-Hz frequency and assuming  $V_D = 0.8$  V and a load resistance  $R = 100 \Omega$ . Find the value of  $C$  that results in a ripple voltage no larger than 1 V peak-to-peak. What is the dc voltage at the output? Find the load current. Find the diodes' conduction angle. Provide the average and peak diode currents. What is the peak reverse voltage across each diode? Specify the diode in terms of its peak current and its PIV.
- Ans.**  $1281 \mu\text{F}$ ; 15.4 V or (a better estimate) 14.9 V; 0.15 A; 0.36 rad ( $20.7^\circ$ ); 1.45 A; 2.74 A; 16.2 V.  
Thus select a diode with 3.5-A to 4-A peak current and a 20-V PIV rating.

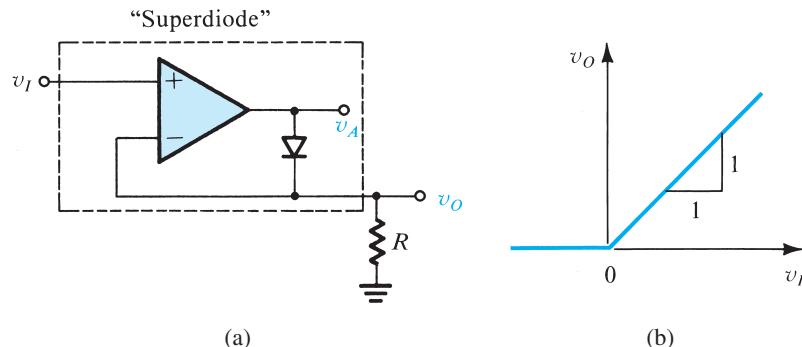
### THE EARLIEST SEMICONDUCTOR DIODE:

The cat's whisker or crystal detector was the first electronic diode to be commercialized as an envelope detector for the radio-frequency signals used in radio telephony. The earliest diode, invented in Germany by Karl Ferdinand Braun, consisted of a small slab of galena (lead sulfide) to which contact was made by sharpened spring wire, which could be adjusted. For this and other contributions to early radios, Braun received the Nobel Prize in Physics in 1909. The silicon-based point-contact diode, later refined and packaged, was an important solid-state component of radar equipment during World War II.

### 4.5.5 Precision Half-Wave Rectifier—The Superdiode<sup>4</sup>

The rectifier circuits studied thus far suffer from having one or two diode drops in the signal paths. Thus these circuits work well only when the signal to be rectified is much larger than the voltage drop of a conducting diode (0.7 V or so). In such a case, the details of the diode forward characteristics or the exact value of the diode voltage do not play a prominent role in determining circuit performance. This is indeed the case in the application of rectifier circuits in power-supply design. There are other applications, however, where the signal to be rectified is small (e.g., on the order of 100 mV or so) and thus clearly insufficient to turn on a diode. Also, in instrumentation applications, the need arises for rectifier circuits with very precise and predictable transfer characteristics. For these applications, a class of circuits has been developed utilizing op amps (Chapter 2) together with diodes to provide precision rectification. In the following discussion, we study one such circuit. A comprehensive study of op amp-diode circuits is available on the website.

<sup>4</sup>This section requires knowledge of operational amplifiers (Chapter 2).



**Figure 4.29** (a) The “superdiode” precision half-wave rectifier and (b) its almost-ideal transfer characteristic. Note that when  $v_I > 0$  and the diode conducts, the op amp supplies the load current, and the source is conveniently buffered, an added advantage. Not shown are the op-amp power supplies.

Figure 4.29(a) shows a precision half-wave rectifier circuit consisting of a diode placed in the negative-feedback path of an op amp, with  $R$  being the rectifier load resistance. The op amp, of course, needs power supplies for its operation. For simplicity, these are not shown in the circuit diagram. The circuit works as follows: If  $v_I$  goes positive, the output voltage  $v_A$  of the op amp will go positive and the diode will conduct, thus establishing a closed feedback path between the op amp’s output terminal and the negative input terminal. This negative-feedback path will cause a virtual short circuit to appear between the two input terminals of the op amp. Thus the voltage at the negative input terminal, which is also the output voltage  $v_O$ , will equal (to within a few millivolts) that at the positive input terminal, which is the input voltage  $v_I$ ,

$$v_O = v_I \quad v_I \geq 0$$

Note that the offset voltage ( $\simeq 0.7$  V) exhibited in the simple half-wave rectifier circuit of Fig. 4.23 is no longer present. For the op-amp circuit to start operation,  $v_I$  has to exceed only a negligibly small voltage equal to the diode drop divided by the op amp’s open-loop gain. In other words, the straight-line transfer characteristic  $v_O - v_I$  almost passes through the origin. This makes this circuit suitable for applications involving very small signals.

Consider now the case when  $v_I$  goes negative. The op amp’s output voltage  $v_A$  will tend to follow and go negative. This will reverse-bias the diode, and no current will flow through resistance  $R$ , causing  $v_O$  to remain equal to 0 V. Thus, for  $v_I < 0$ ,  $v_O = 0$ . Since in this case the diode is off, the op amp will be operating in an open-loop fashion, and its output will be at its negative saturation level.

The transfer characteristic of this circuit will be that shown in Fig. 4.29(b), which is almost identical to the ideal characteristic of a half-wave rectifier. The nonideal diode characteristics have been almost completely masked by placing the diode in the negative-feedback path of an op amp. This is another dramatic application of negative feedback, a subject we will study formally in Chapter 11. The combination of diode and op amp, shown in the dashed box in Fig. 4.29(a), is appropriately referred to as a “superdiode.”

## EXERCISES

- 4.24** Consider the **operational rectifier** or superdiode circuit of Fig. 4.29(a), with  $R = 1 \text{ k}\Omega$ . For  $v_i = 10 \text{ mV}$ ,  $1 \text{ V}$ , and  $-1 \text{ V}$ , what are the voltages that result at the rectifier output and at the output of the op amp? Assume that the op amp is ideal and that its output saturates at  $\pm 12 \text{ V}$ . The diode has a  $0.7\text{-V}$  drop at  $1\text{-mA}$  current.

**Ans.**  $10 \text{ mV}$ ,  $0.59 \text{ V}$ ;  $1 \text{ V}$ ,  $1.7 \text{ V}$ ;  $0 \text{ V}$ ,  $-12 \text{ V}$

- 4.25** If the diode in the circuit of Fig. 4.29(a) is reversed, find the transfer characteristic  $v_o$  as a function of  $v_i$ .

**Ans.**  $v_o = 0$  for  $v_i \geq 0$ ;  $v_o = v_i$  for  $v_i \leq 0$

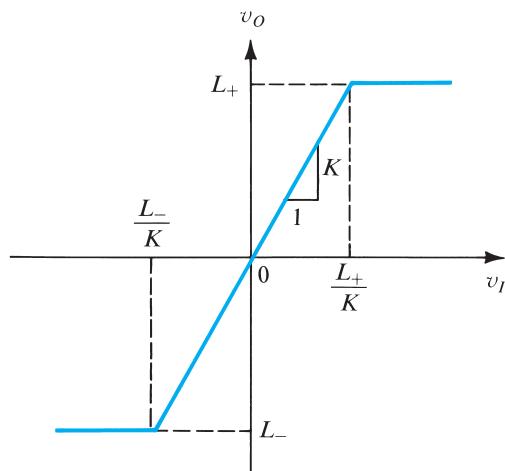
## 4.6 Limiting and Clamping Circuits

A

In this section, we shall present additional nonlinear circuit applications of diodes.

### 4.6.1 Limiter Circuits

Figure 4.30 shows the general transfer characteristic of a limiter circuit. As indicated, for inputs in a certain range,  $L_-/K \leq v_i \leq L_+/K$ , the limiter acts as a linear circuit, providing an output proportional to the input,  $v_o = Kv_i$ . Although in general  $K$  can be greater than 1, the



**Figure 4.30** General transfer characteristic for a limiter circuit.

circuits discussed in this section have  $K \leq 1$  and are known as **passive limiters**. (Examples of active limiters will be presented in Chapter 18.) If  $v_I$  exceeds the upper threshold ( $L_+/K$ ), the output voltage is *limited* or clamped to the upper limiting level  $L_+$ . On the other hand, if  $v_I$  is reduced below the lower limiting threshold ( $L_-/K$ ), the output voltage  $v_O$  is limited to the lower limiting level  $L_-$ .

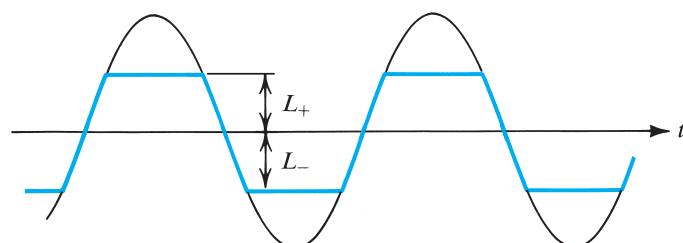
The general transfer characteristic of Fig. 4.30 describes a **double limiter**—that is, a limiter that works on both the positive and negative peaks of an input waveform. **Single limiters**, of course, exist. Finally, note that if an input waveform such as that shown in Fig. 4.31 is fed to a double limiter, its two peaks will be *clipped off*. Limiters therefore are sometimes referred to as **clippers**.

The limiter whose characteristics are depicted in Fig. 4.30 is described as a **hard limiter**. **Soft limiting** is characterized by smoother transitions between the linear region and the saturation regions and a slope greater than zero in the saturation regions, as illustrated in Fig. 4.32. Depending on the application, either hard or soft limiting may be preferred.

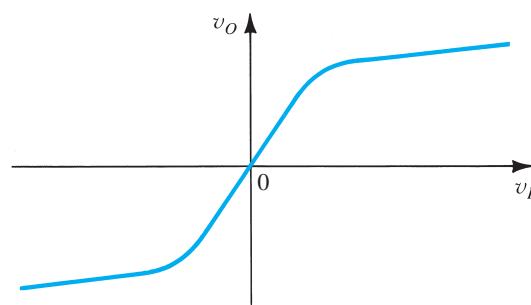
Limiters find application in a variety of signal-processing systems. One of their simplest applications is in limiting the voltage between the two input terminals of an op amp to a value lower than the breakdown voltage of the transistors that make up the input stage of the op-amp circuit. We will have more to say on this and other limiter applications at later points in this book.

Diodes can be combined with resistors to provide simple realizations of the limiter function. A number of examples are depicted in Fig. 4.33. In each part of the figure both the circuit and its transfer characteristic are given. The transfer characteristics are obtained using the constant-voltage-drop ( $V_D = 0.7$  V) diode model but assuming a smooth transition between the linear and saturation regions of the transfer characteristic.

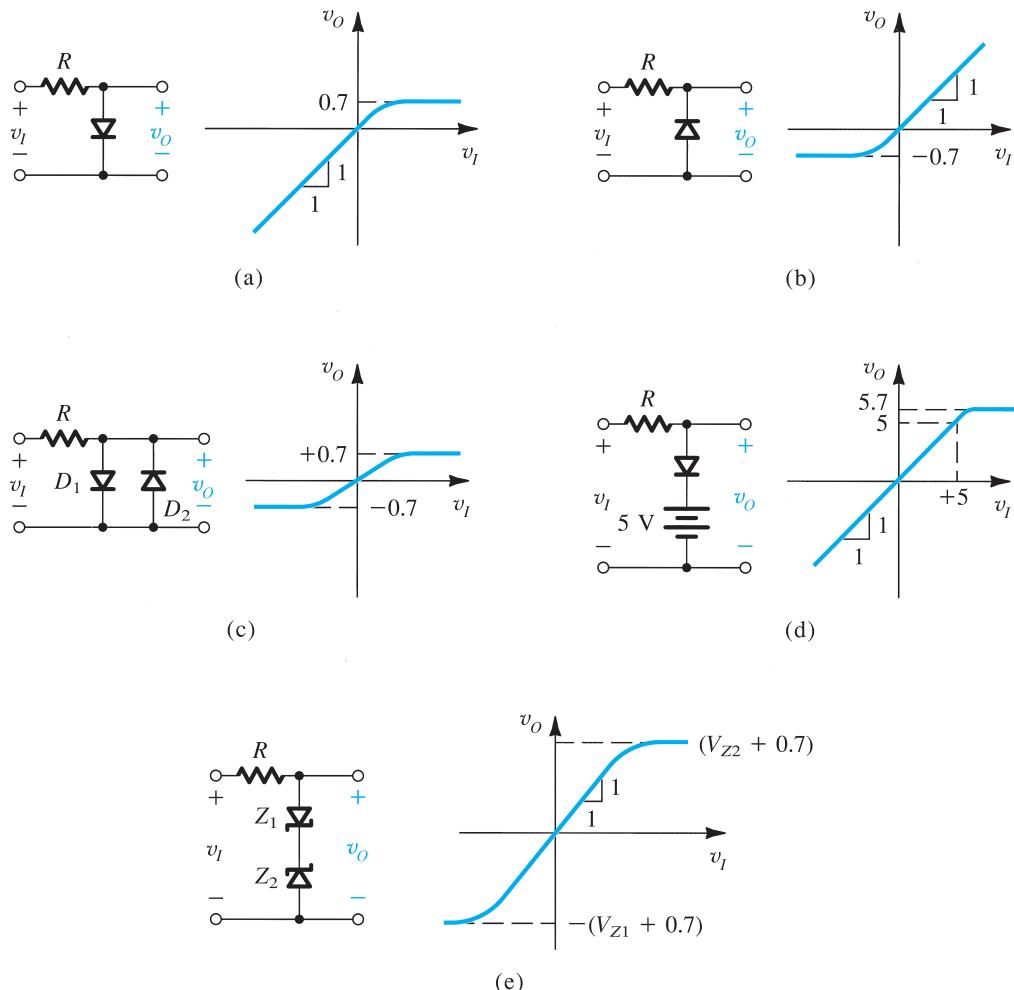
The circuit in Fig. 4.33(a) is that of the half-wave rectifier except that here the output is taken across the diode. For  $v_I < 0.5$  V, the diode is cut off, no current flows, and the voltage drop across  $R$  is zero; thus  $v_O = v_I$ . As  $v_I$  exceeds 0.5 V, the diode turns on, eventually limiting



**Figure 4.31** Applying a sine wave to a limiter can result in clipping off its two peaks.



**Figure 4.32** Soft limiting.



**Figure 4.33** A variety of basic limiting circuits.

$v_O$  to one diode drop (0.7 V). The circuit of Fig. 4.33(b) is similar to that in Fig. 4.33(a) except that the diode is reversed.

Double limiting can be implemented by placing two diodes of opposite polarity in parallel, as shown in Fig. 4.33(c). Here the linear region of the characteristic is obtained for  $-0.5V \leq v_I \leq 0.5V$ . For this range of  $v_I$ , both diodes are off and  $v_O = v_I$ . As  $v_I$  exceeds 0.5 V,  $D_1$  turns on and eventually limits  $v_O$  to +0.7 V. Similarly, as  $v_I$  goes more negative than -0.5 V,  $D_2$  turns on and eventually limits  $v_O$  to -0.7 V.

The thresholds and saturation levels of diode limiters can be controlled by using strings of diodes and/or by connecting a dc voltage in series with the diode(s). The latter idea is illustrated in Fig. 4.33(d). Finally, rather than strings of diodes, we may use two zener diodes in series, as shown in Fig. 4.33(e). In this circuit, limiting occurs in the positive direction at a voltage of  $V_{Z2} + 0.7$ , where 0.7 V represents the voltage drop across zener diode  $Z_1$  when conducting in the forward direction. For negative inputs,  $Z_1$  acts as a zener, while  $Z_2$  conducts

in the forward direction. It should be mentioned that pairs of zener diodes connected in series are available commercially for applications of this type under the name **double-anode zener**.

More flexible limiter circuits are possible if op amps are combined with diodes and resistors. Examples of such circuits are discussed in Chapter 18.

### EXERCISE

- 4.26** Assuming the diodes to be ideal, describe the transfer characteristic of the circuit shown in Fig. E4.26.

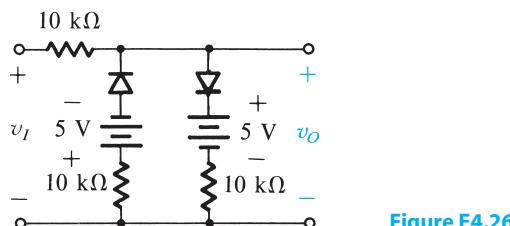


Figure E4.26

**Ans.**  $v_O = v_I$  for  $-5 \leq v_I \leq +5$   
 $v_O = \frac{1}{2}v_I - 2.5$  for  $v_I \leq -5$   
 $v_O = \frac{1}{2}v_I + 2.5$  for  $v_I \geq +5$

### 4.6.2 The Clamped Capacitor or DC Restorer

If in the basic peak-rectifier circuit, the output is taken across the diode rather than across the capacitor, an interesting circuit with important applications results. The circuit, called a dc restorer, is shown in Fig. 4.34 fed with a square wave. Because of the polarity in which the diode is connected, the capacitor will charge to a voltage  $v_C$  with the polarity indicated in Fig. 4.34 and equal to the magnitude of the most negative peak of the input signal. Subsequently, the diode turns off and the capacitor retains its voltage indefinitely. If,

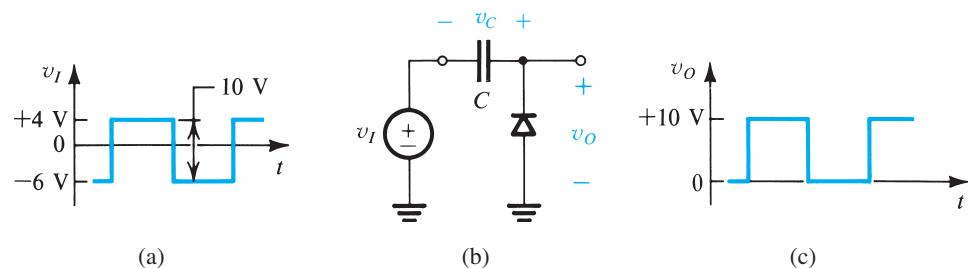


Figure 4.34 The clamped capacitor or dc restorer with a square-wave input and no load.

for instance, the input square wave has the arbitrary levels  $-6\text{ V}$  and  $+4\text{ V}$ , then  $v_C$  will be equal to  $6\text{ V}$ . Now, since the output voltage  $v_O$  is given by

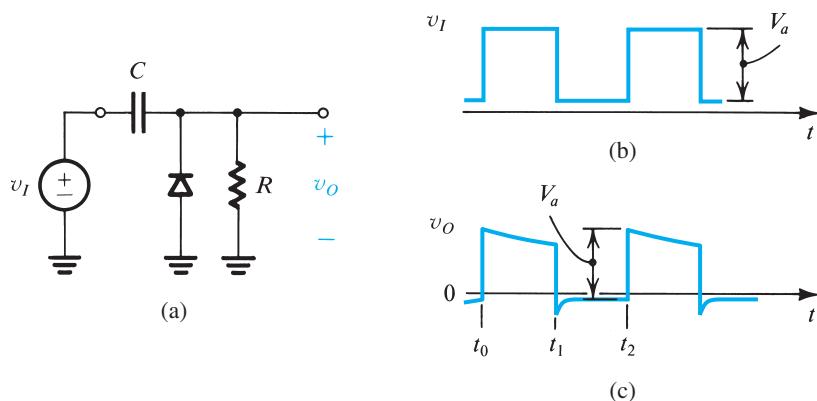
$$v_O = v_I + v_C$$

it follows that the output waveform will be identical to that of the input, except that it is shifted upward by  $v_C$  volts. In our example the output will thus be a square wave with levels of  $0\text{ V}$  and  $+10\text{ V}$ .

Another way of visualizing the operation of the circuit in Fig. 4.34 is to note that because the diode is connected across the output with the polarity shown, it prevents the output voltage from going below  $0\text{ V}$  (by conducting and charging up the capacitor, thus causing the output to rise to  $0\text{ V}$ ), but this connection will not constrain the positive excursion of  $v_O$ . The output waveform will therefore have its lowest peak *clamped* to  $0\text{ V}$ , which is why the circuit is called a **clamped capacitor**. It should be obvious that reversing the diode polarity will provide an output waveform whose highest peak is clamped to  $0\text{ V}$ . In either case, the output waveform will have a finite average value or dc component. This dc component is entirely unrelated to the average value of the input waveform. As an application, consider a pulse signal being transmitted through a capacitively coupled or ac-coupled system. The capacitive coupling will cause the pulse train to lose whatever dc component it originally had. Feeding the resulting pulse waveform to a clamping circuit provides it with a well-determined dc component, a process known as **dc restoration**. This is why the circuit is also called a **dc restorer**.

Restoring dc is useful because the dc component or average value of a pulse waveform is an effective measure of its **duty cycle**.<sup>5</sup> The duty cycle of a pulse waveform can be modulated (in a process called **pulsewidth modulation**) and made to carry information. In such a system, detection or demodulation could be achieved simply by feeding the received pulse waveform to a dc restorer and then using a simple  $RC$  low-pass filter to separate the average of the output waveform from the superimposed pulses.

When a load resistance  $R$  is connected across the diode in a clamping circuit, as shown in Fig. 4.35, the situation changes significantly. While the output is above ground, a current must flow in  $R$ . Since at this time the diode is off, this current obviously comes from the capacitor,



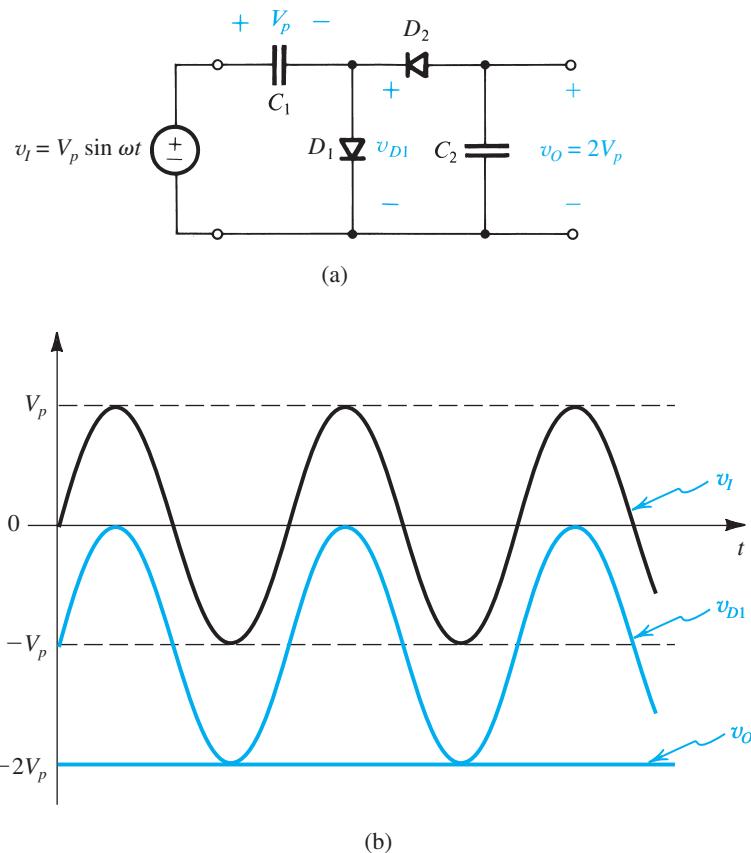
**Figure 4.35** The clamped capacitor with a load resistance  $R$ .

<sup>5</sup>The duty cycle of a pulse waveform is the proportion of each cycle occupied by the pulse. In other words, it is the pulse width expressed as a fraction of the pulse period.

thus causing the capacitor to discharge and the output voltage to fall. This is shown in Fig. 4.35 for a square-wave input. During the interval  $t_0$  to  $t_1$ , the output voltage falls exponentially with time constant  $CR$ . At  $t_1$  the input decreases by  $V_a$  volts, and the output attempts to follow. This causes the diode to conduct heavily and to quickly charge the capacitor. At the end of the interval  $t_1$  to  $t_2$ , the output voltage would normally be a few tenths of a volt negative (e.g.,  $-0.5$  V). Then, as the input rises by  $V_a$  volts (at  $t_2$ ), the output follows, and the cycle repeats itself. In the steady state the charge lost by the capacitor during the interval  $t_0$  to  $t_1$  is recovered during the interval  $t_1$  to  $t_2$ . This charge equilibrium enables us to calculate the average diode current as well as the details of the output waveform.

### 4.6.3 The Voltage Doubler

Figure 4.36(a) shows a circuit composed of two sections in cascade: a clamped capacitor formed by  $C_1$  and  $D_1$ , and a peak rectifier formed by  $D_2$  and  $C_2$ . When excited by a sinusoid of amplitude  $V_p$  the clamping section provides the voltage waveform  $v_{D1}$  shown, assuming ideal diodes, in Fig. 4.36(b). Note that while the positive peaks are clamped to 0 V, the negative peak reaches  $-2V_p$ . In response to this waveform, the peak-detector section provides across capacitor  $C_2$  a dc voltage equal to the negative peak of  $v_{D1}$ , that is,  $-2V_p$ . Because the output voltage is double the input peak, the circuit is known as a voltage doubler. The technique can be extended to provide output dc voltages that are higher multiples of  $V_p$ .



**Figure 4.36** Voltage doubler: (a) circuit; (b) waveforms of the input voltage, the voltage across  $D_1$ , and the output voltage  $v_o = -2V_p$ .

**EXERCISE**

**4.27** If the diode in the circuit of Fig. 4.34 is reversed, what will the dc component of  $v_o$  become?

**Ans.**  $-5\text{ V}$

## 4.7 Special Diode Types

A

In this section, we discuss briefly some important special types of diodes.

### 4.7.1 The Schottky-Barrier Diode (SBD)

The Schottky-barrier diode (SBD) is formed by bringing metal into contact with a moderately doped *n*-type semiconductor material. The resulting metal–semiconductor junction behaves like a diode, conducting current in one direction (from the metal anode to the semiconductor cathode) and acting as an open circuit in the other, and is known as the Schottky-barrier diode or simply the Schottky diode. In fact, the current–voltage characteristic of the SBD is remarkably similar to that of a *pn*-junction diode, with two important exceptions:

1. In the SBD, current is conducted by majority carriers (electrons). Thus the SBD does not exhibit the minority-carrier charge-storage effects found in forward-biased *pn* junctions. As a result, Schottky diodes can be switched from on to off, and vice versa, much faster than is possible with *pn*-junction diodes.
2. The forward voltage drop of a conducting SBD is lower than that of a *pn*-junction diode. For example, an SBD made of silicon exhibits a forward voltage drop of 0.3 V to 0.5 V, compared to the 0.6 V to 0.8 V found in silicon *pn*-junction diodes. SBDs can also be made of gallium arsenide (GaAs) and, in fact, play an important role in the design of GaAs circuits.<sup>6</sup> Gallium-arsenide SBDs exhibit forward voltage drops of about 0.7 V.

Apart from GaAs circuits, Schottky diodes find application in the design of a special form of bipolar-transistor logic circuits, known as Schottky-TTL, where TTL stands for transistor–transistor logic.

Before leaving the subject of Schottky-barrier diodes, it is important to note that not every metal–semiconductor contact is a diode. In fact, metal is commonly deposited on the semiconductor surface in order to make terminals for the semiconductor devices and to connect different devices in an integrated-circuit chip. Such metal–semiconductor contacts are known as **ohmic contacts** to distinguish them from the rectifying contacts that result in SBDs. Ohmic contacts are usually made by depositing metal on very heavily doped (and thus low-resistivity) semiconductor regions. (Recall that SBDs use moderately doped material.)

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<sup>6</sup>The website accompanying this text contains material on GaAs circuits.

### 4.7.2 Varactors

In Chapter 3 we learned that reverse-biased *pn* junctions exhibit a charge-storage effect that is modeled with the depletion-layer or junction capacitance  $C_j$ . As Eq. (3.49) indicates,  $C_j$  is a function of the reverse-bias voltage  $V_R$ . This dependence turns out to be useful in a number of applications, such as the automatic tuning of radio receivers. Special diodes are therefore fabricated to be used as voltage-variable capacitors known as **varactors**. These devices are optimized to make the capacitance a strong function of voltage by arranging that the grading coefficient  $m$  is 3 or 4.

### 4.7.3 Photodiodes

If a reverse-biased *pn* junction is illuminated—that is, exposed to incident light—the photons impacting the junction cause covalent bonds to break, and thus electron-hole pairs are generated in the depletion layer. The electric field in the depletion region then sweeps the liberated electrons to the *n* side and the holes to the *p* side, giving rise to a reverse current across the junction. This current, known as photocurrent, is proportional to the intensity of the incident light. Such a diode, called a photodiode, can be used to convert light signals into electrical signals.

Photodiodes are usually fabricated using a compound semiconductor<sup>7</sup> such as gallium arsenide. The photodiode is an important component of a growing family of circuits known as **optoelectronics** or **photonics**. As the name implies, such circuits utilize an optimum combination of electronics and optics for signal processing, storage, and transmission. Usually, electronics is the preferred means for signal processing, whereas optics is most suited for transmission and storage. Examples include fiber-optic transmission of telephone and television signals and the use of optical storage in CD-ROM computer discs. Optical transmission provides very wide bandwidths and low signal attenuation. Optical storage allows vast amounts of data to be stored reliably in a small space.

Finally, we should note that without reverse bias, the illuminated photodiode functions as a **solar cell**. Usually fabricated from low-cost silicon, a solar cell converts light to electrical energy.

### 4.7.4 Light-Emitting Diodes (LEDs)

The light-emitting diode (LED) performs the inverse of the function of the photodiode; it converts a forward current into light. The reader will recall from Chapter 3 that in a forward-biased *pn* junction, minority carriers are injected across the junction and diffuse into the *p* and *n* regions. The diffusing minority carriers then recombine with the majority carriers. Such recombination can be made to give rise to light emission. This can be done by fabricating the *pn* junction using a semiconductor of the type known as direct-bandgap materials. Gallium arsenide belongs to this group and can thus be used to fabricate light-emitting diodes.

The light emitted by an LED is proportional to the number of recombinations that take place, which in turn is proportional to the forward current in the diode.

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<sup>7</sup>Whereas an elemental semiconductor, such as silicon, uses an element from column IV of the periodic table, a compound semiconductor uses a combination of elements from columns III and V or II and VI. For example, GaAs is formed of gallium (column III) and arsenic (column V) and is thus known as a III-V compound.

LEDs are very popular devices. They find application in the design of numerous types of displays, including the displays of laboratory instruments such as digital voltmeters. They can be made to produce light in a variety of colors. Furthermore, LEDs can be designed so as to produce coherent light with a very narrow bandwidth. The resulting device is a **laser diode**. Laser diodes find application in optical communication systems and in DVD players, among other things.

Combining an LED with a photodiode in the same package results in a device known as an **optoisolator**. The LED converts an electrical signal applied to the optoisolator into light, which the photodiode detects and converts back to an electrical signal at the output of the optoisolator. Use of the optoisolator provides complete electrical isolation between the electrical circuit that is connected to the isolator's input and the circuit that is connected to its output. Such isolation can be useful in reducing the effect of electrical interference on signal transmission within a system, and thus optoisolators are frequently employed in the design of digital systems. They can also be used in the design of medical instruments to reduce the risk of electrical shock to patients.

Note that the optical coupling between an LED and a photodiode need not be accomplished inside a small package. Indeed, it can be implemented over a long distance using an optical fiber, as is done in fiber-optic communication links.

### FROM INDICATION TO ILLUMINATION:

Light-emitting diodes (LEDs), which once served only as low-powered status indicators, are now lighting our way! Increasingly, automotive lighting uses LEDs; increasingly, too, LED bulbs of higher and higher power are replacing both incandescent and fluorescent lighting in homes and offices. Incandescent bulbs are only 5% efficient in the conversion of electricity into light—the other 95% is dissipated as heat. The light conversion efficiency of LEDs, however, is 60%. Moreover, LEDs last 25 times longer (25,000 hours) than incandescent bulbs and 3 times longer than fluorescents.

## Summary

- In the forward direction, the ideal diode conducts any current forced by the external circuit while displaying a zero voltage drop. The ideal diode does not conduct in the reverse direction; any applied voltage appears as reverse bias across the diode.
- The unidirectional-current-flow property makes the diode useful in the design of rectifier circuits.
- The forward conduction of practical silicon-junction diodes is accurately characterized by the relationship  $i = I_s e^{v/V_T}$ .
- A silicon diode conducts a negligible current until the forward voltage is at least 0.5 V. Then the current increases rapidly, with the voltage drop increasing by 60 mV for every decade of current change.
- In the reverse direction, a silicon diode conducts a current on the order of  $10^{-9}$  A. This current is much greater than  $I_s$  because of leakage effects and increases with the magnitude of reverse voltage.
- Beyond a certain value of reverse voltage (that depends on the diode), breakdown occurs, and current increases rapidly with a small corresponding increase in voltage.
- Diodes designed to operate in the breakdown region are called zener diodes. They are employed in the design of voltage regulators whose function is to provide a constant dc voltage that varies little with variations in power-supply voltage and/or load current.

- In many applications, a conducting diode is modeled as having a constant voltage drop, usually approximately 0.7 V.
- A diode biased to operate at a dc current  $I_D$  has a small-signal resistance  $r_d = V_T/I_D$ .
- Rectifiers convert ac voltages into unipolar voltages. Half-wave rectifiers do this by passing the voltage in half of each cycle and blocking the opposite-polarity voltage in the other half of the cycle. Full-wave rectifiers accomplish the task by passing the voltage in half of each cycle and inverting the voltage in the other half-cycle.
- The bridge-rectifier circuit is the preferred full-wave rectifier configuration.
- The variation of the output waveform of the rectifier is reduced considerably by connecting a capacitor  $C$  across the output load resistance  $R$ . The resulting circuit is the peak rectifier. The output waveform then consists of a dc voltage almost equal to the peak of the input sine wave,  $V_p$ , on which is superimposed a ripple component of frequency  $2f$  (in the full-wave case) and of peak-to-peak amplitude  $V_r = V_p/2fCR$ . To reduce this ripple voltage further, a voltage regulator is employed.
- Combination of diodes, resistors, and possibly reference voltages can be used to design voltage limiters that prevent one or both extremities of the output waveform from going beyond predetermined values, the limiting level(s).
- Applying a time-varying waveform to a circuit consisting of a capacitor in series with a diode and taking the output across the diode provides a clamping function. Specifically, depending on the polarity of the diode, either the positive or negative peaks of the signal will be clamped to the voltage at the other terminal of the diode (usually ground). In this way the output waveform has a nonzero average or dc component, and the circuit is known as a dc restorer.
- By cascading a clamping circuit with a peak-rectifier circuit, a voltage doubler is realized.

## PROBLEMS

### Computer Simulation Problems

**SIM** Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

### Section 4.1: The Ideal Diode

**4.1** An AA flashlight cell, whose Thévenin equivalent is a voltage source of 1.5 V and a resistance of  $1\ \Omega$ , is connected

to the terminals of an ideal diode. Describe two possible situations that result. What are the diode current and terminal voltage when (a) the connection is between the diode cathode and the positive terminal of the battery and (b) the anode and the positive terminal are connected?

**4.2** For the circuits shown in Fig. P4.2 using ideal diodes, find the values of the voltages and currents indicated.

**4.3** For the circuits shown in Fig. P4.3 using ideal diodes, find the values of the labeled voltages and currents.

**4.4** In each of the ideal-diode circuits shown in Fig. P4.4,  $v_i$  is a 1-kHz, 5-V peak sine wave. Sketch the waveform resulting at  $v_o$ . What are its positive and negative peak values?

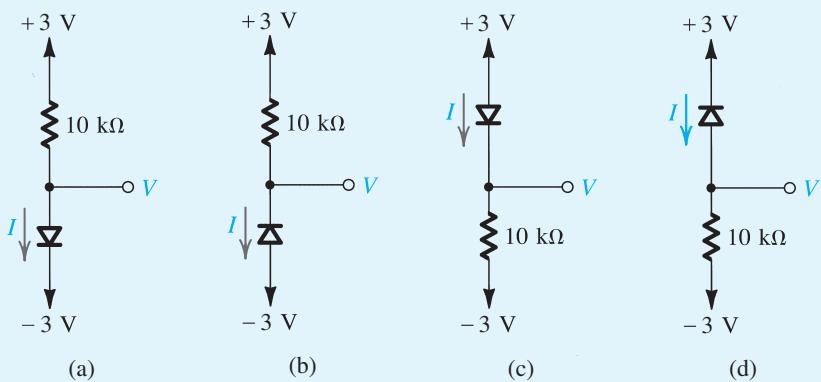


Figure P4.2

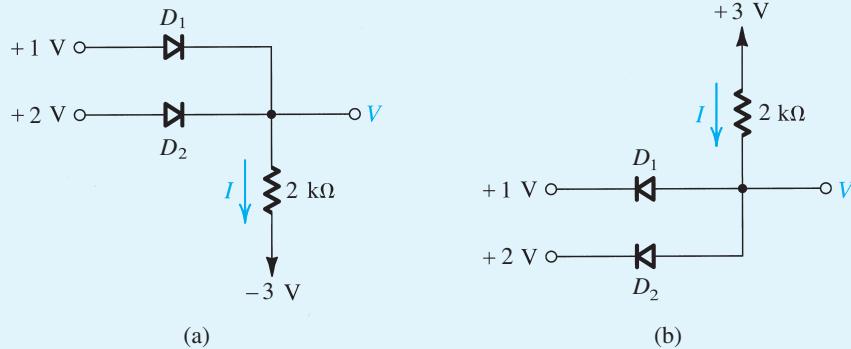


Figure P4.3

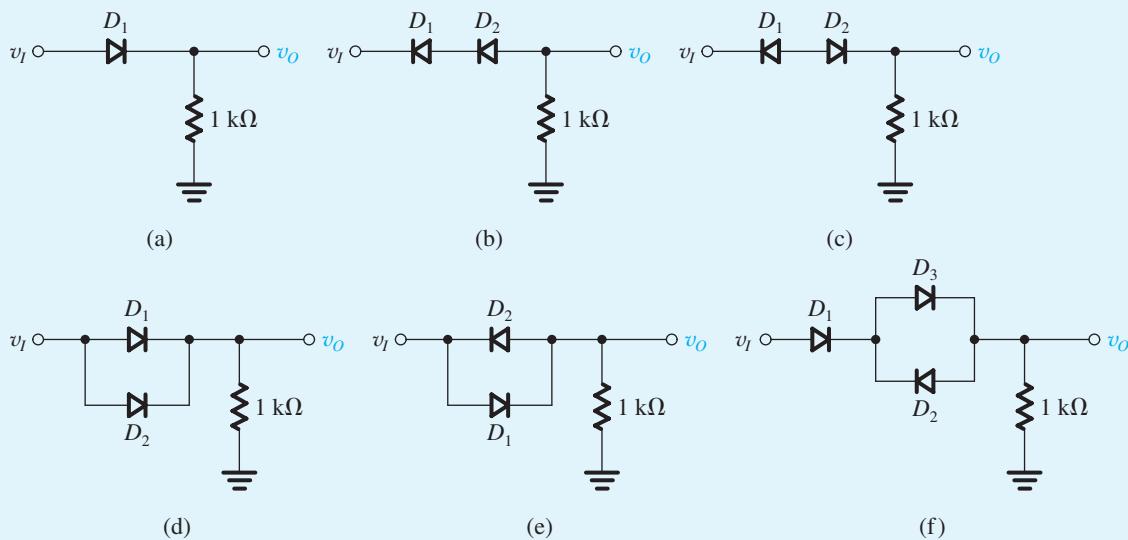
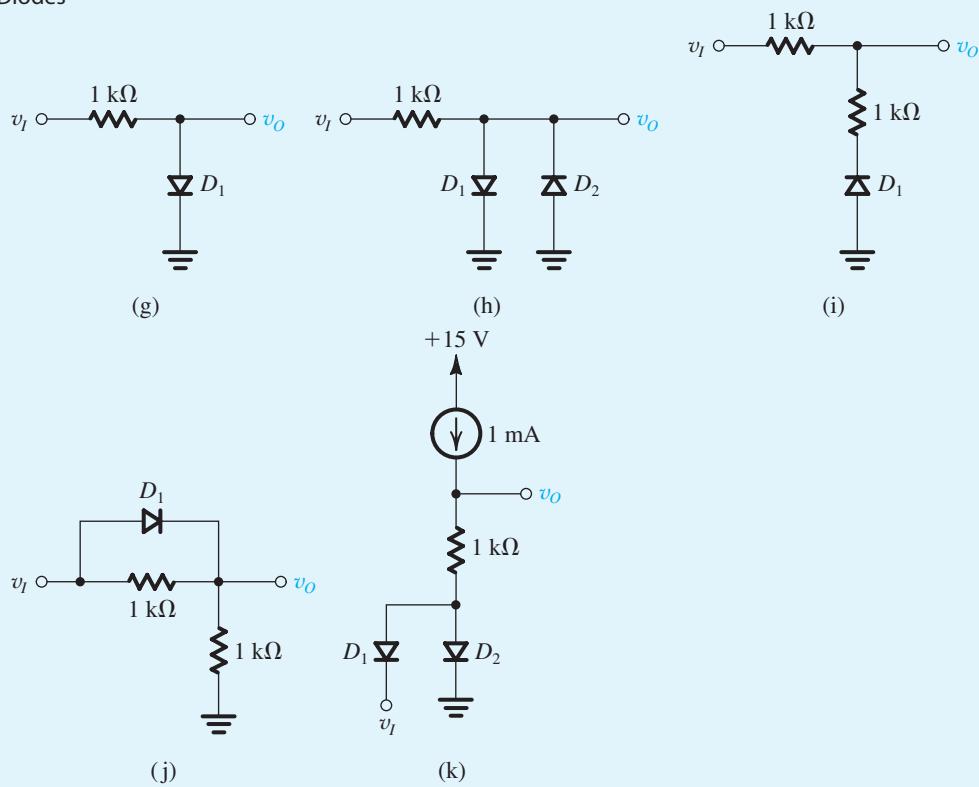


Figure P4.4

Figure P4.4 *continued*

**4.5** The circuit shown in Fig. P4.5 is a model for a battery charger. Here  $v_I$  is a 6-V peak sine wave,  $D_1$  and  $D_2$  are ideal diodes,  $I$  is a 60-mA current source, and  $B$  is a 3-V battery. Sketch and label the waveform of the battery current  $i_B$ . What is its peak value? What is its average value? If the peak value of  $v_I$  is reduced by 10%, what do the peak and average values of  $i_B$  become?

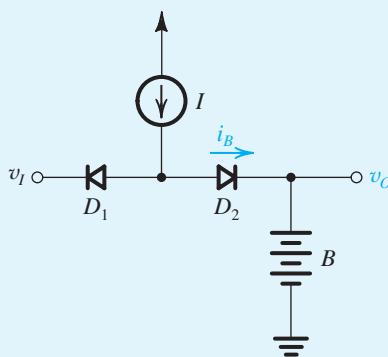


Figure P4.5

**4.6** The circuits shown in Fig. P4.6 can function as logic gates for input voltages that are either high or low. Using “1” to denote the high value and “0” to denote the low value, prepare a table with four columns including all possible input combinations and the resulting values of  $X$  and  $Y$ . What logic function is  $X$  of  $A$  and  $B$ ? What logic function is  $Y$  of  $A$  and  $B$ ? For what values of  $A$  and  $B$  do  $X$  and  $Y$  have the same value? For what values of  $A$  and  $B$  do  $X$  and  $Y$  have opposite values?

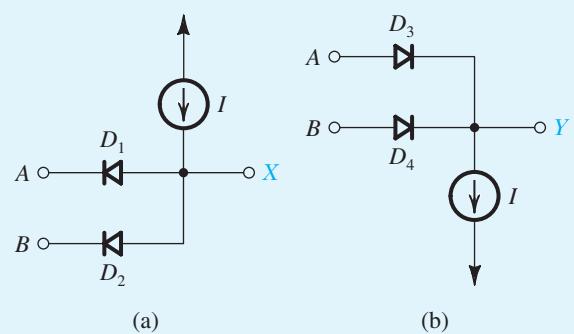


Figure P4.6

**D 4.7** For the logic gate of Fig. 4.5(a), assume ideal diodes and input voltage levels of 0 V and +5 V. Find a suitable value for  $R$  so that the current required from each of the input signal sources does not exceed 0.2 mA.

**D 4.8** Repeat Problem 4.7 for the logic gate of Fig. 4.5(b).

**4.9** Assuming that the diodes in the circuits of Fig. P4.9 are ideal, find the values of the labeled voltages and currents.

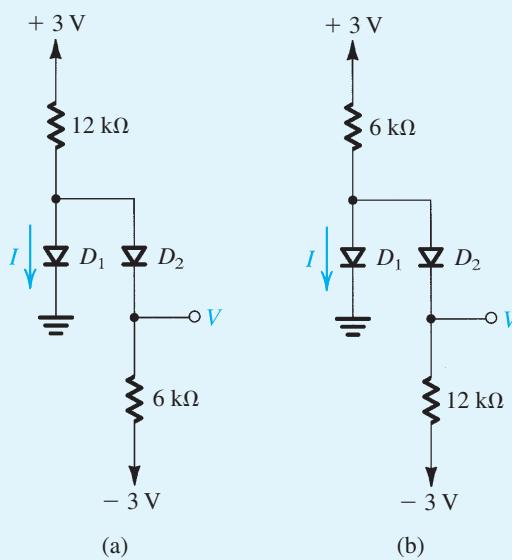


Figure P4.9

**4.10** Assuming that the diodes in the circuits of Fig. P4.10 are ideal, utilize Thévenin's theorem to simplify the circuits and thus find the values of the labeled currents and voltages.

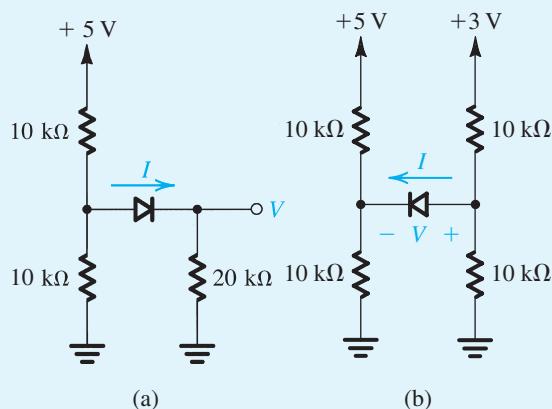


Figure P4.10

**D 4.11** For the rectifier circuit of Fig. 4.3(a), let the input sine wave have 120-V rms value and assume the diode to

be ideal. Select a suitable value for  $R$  so that the peak diode current does not exceed 40 mA. What is the greatest reverse voltage that will appear across the diode?

**4.12** Consider the rectifier circuit of Fig. 4.3(a) in the event that the input source  $v_I$  has a source resistance  $R_s$ . For the case  $R_s = R$  and assuming the diode to be ideal, sketch and clearly label the transfer characteristic  $v_o$  versus  $v_I$ .

**4.13** A symmetrical square wave of 5-V peak-to-peak amplitude and zero average is applied to a circuit resembling that in Fig. 4.3(a) and employing a 100- $\Omega$  resistor. What is the peak output voltage that results? What is the average output voltage that results? What is the peak diode current? What is the average diode current? What is the maximum reverse voltage across the diode?

**4.14** Repeat Problem 4.13 for the situation in which the average voltage of the square wave is 1 V, while its peak-to-peak value remains at 5 V.

**D \*4.15** Design a battery-charging circuit, resembling that in Fig. 4.4(a) and using an ideal diode, in which current flows to the 12-V battery 25% of the time with an average value of 100 mA. What peak-to-peak sine-wave voltage is required? What resistance is required? What peak diode current flows? What peak reverse voltage does the diode endure? If resistors can be specified to only one significant digit, and the peak-to-peak voltage only to the nearest volt, what design would you choose to guarantee the required charging current? What fraction of the cycle does diode current flow? What is the average diode current? What is the peak diode current? What peak reverse voltage does the diode endure?

**4.16** The circuit of Fig. P4.16 can be used in a signaling system using one wire plus a common ground return. At any moment, the input has one of three values: +3 V, 0 V, -3 V.

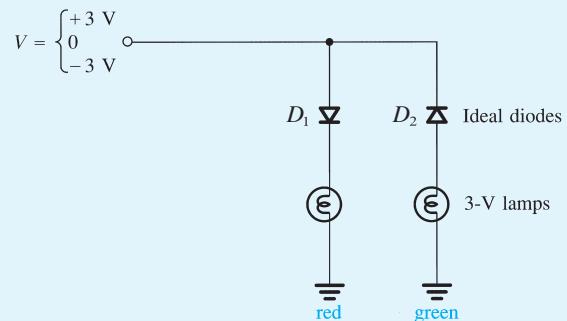


Figure P4.16

What is the status of the lamps for each input value? (Note that the lamps can be located apart from each other and that there may be several of each type of connection, all on one wire!)

### Section 4.2: Terminal Characteristics of Junction Diodes

**4.17** Calculate the value of the thermal voltage,  $V_T$ , at  $-55^\circ\text{C}$ ,  $0^\circ\text{C}$ ,  $+40^\circ\text{C}$ , and  $+125^\circ\text{C}$ . At what temperature is  $V_T$  exactly 25 mV?

**4.18** At what forward voltage does a diode conduct a current equal to  $10,000I_s$ ? In terms of  $I_s$ , what current flows in the same diode when its forward voltage is 0.7 V?

**4.19** A diode for which the forward voltage drop is 0.7 V at 1.0 mA is operated at 0.5 V. What is the value of the current?

**4.20** A particular diode is found to conduct 1 mA with a junction voltage of 0.7 V. What current will flow in this diode if the junction voltage is raised to 0.71 V? To 0.8 V? If the junction voltage is lowered to 0.69 V? To 0.6 V? What change in junction voltage will increase the diode current by a factor of 10?

**4.21** The following measurements are taken on particular junction diodes for which  $V$  is the terminal voltage and  $I$  is the diode current. For each diode, estimate values of  $I_s$  and the terminal voltage at 10% of the measured current.

- (a)  $V = 0.700 \text{ V}$  at  $I = 1.00 \text{ A}$
- (b)  $V = 0.650 \text{ V}$  at  $I = 1.00 \text{ mA}$
- (c)  $V = 0.650 \text{ V}$  at  $I = 10 \mu\text{A}$
- (d)  $V = 0.700 \text{ V}$  at  $I = 100 \text{ mA}$

**4.22** Listed below are the results of measurements taken on several different junction diodes. For each diode, the data provided are the diode current  $I$  and the corresponding diode voltage  $V$ . In each case, estimate  $I_s$ , and the diode voltage at  $10I$  and  $I/10$ .

- (a) 10.0 mA, 700 mV
- (b) 1.0 mA, 700 mV
- (c) 10 A, 800 mV
- (d) 1 mA, 700 mV
- (e) 10  $\mu\text{A}$ , 600 mV

**4.23** The circuit in Fig. P4.23 utilizes three identical diodes having  $I_s = 10^{-14} \text{ A}$ . Find the value of the current  $I$  required to obtain an output voltage  $V_o = 2.0 \text{ V}$ . If a current of 1 mA is drawn away from the output terminal by a load, what is the change in output voltage?

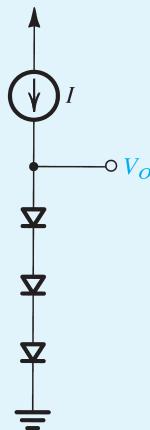


Figure P4.23

**4.24** A junction diode is operated in a circuit in which it is supplied with a constant current  $I$ . What is the effect on the forward voltage of the diode if an identical diode is connected in parallel?

**4.25** Two diodes with saturation currents  $I_{s1}$  and  $I_{s2}$  are connected in parallel with their cathodes joined together and connected to grounds. The two anodes are joined together and fed with a constant current  $I$ . Find the currents  $I_{D1}$  and  $I_{D2}$  that flow through the two diodes, and the voltage  $V_D$  that appears across their parallel combination.

**4.26** Four diodes are connected in parallel: anodes joined together and fed with a constant current  $I$ , and cathodes joined together and connected to ground. What relative junction areas should these diodes have if their currents must have binary-weighted ratios, with the smallest being 0.1 mA? What value of  $I$  is needed?

**4.27** In the circuit shown in Fig. P4.27,  $D_1$  has 10 times the junction area of  $D_2$ . What value of  $V$  results? To obtain a value for  $V$  of 60 mV, what current  $I_2$  is needed?

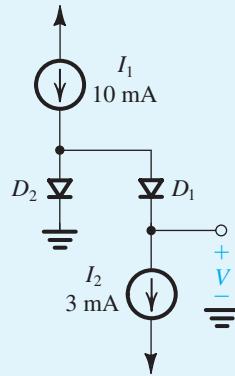


Figure P4.27

- 4.28** For the circuit shown in Fig. P4.28, both diodes are identical. Find the value of  $R$  for which  $V = 50$  mV.

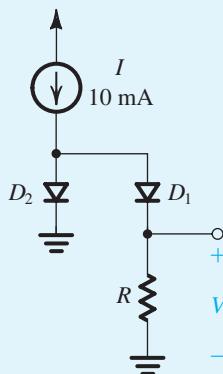


Figure P4.28

- 4.29** A diode fed with a constant current  $I = 1$  mA has a voltage  $V = 690$  mV at  $20^\circ\text{C}$ . Find the diode voltage at  $-20^\circ\text{C}$  and at  $+85^\circ\text{C}$ .

- 4.30** In the circuit shown in Fig. P4.30,  $D_1$  is a large-area, high-current diode whose reverse leakage is high and independent of applied voltage, while  $D_2$  is a much smaller, low-current diode. At an ambient temperature of  $20^\circ\text{C}$ , resistor  $R_1$  is adjusted to make  $V_{R1} = V_2 = 520$  mV. Subsequent measurement indicates that  $R_1$  is  $520$  k $\Omega$ . What do you expect the voltages  $V_{R1}$  and  $V_2$  to become at  $0^\circ\text{C}$  and at  $40^\circ\text{C}$ ?

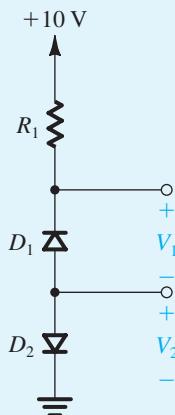


Figure P4.30

- 4.31** When a 10-A current is applied to a particular diode, it is found that the junction voltage immediately becomes 700 mV. However, as the power being dissipated in the diode raises its temperature, it is found that the voltage decreases and eventually reaches 600 mV. What is the apparent rise in

junction temperature? What is the power dissipated in the diode in its final state? What is the temperature rise per watt of power dissipation? (This is called the thermal resistance.)

- \*4.32** A designer of an instrument that must operate over a wide supply-voltage range, noting that a diode's junction-voltage drop is relatively independent of junction current, considers the use of a large diode to establish a small relatively constant voltage. A power diode, for which the nominal current at 0.8 V is 10 A, is available. If the current source feeding the diode changes in the range 1 mA to 3 mA and if, in addition, the temperature changes by  $\pm 20^\circ\text{C}$ , what is the expected range of diode voltage?

- \*4.33** As an alternative to the idea suggested in Problem 4.32, the designer considers a second approach to producing a relatively constant small voltage from a variable current supply: It relies on the ability to make quite accurate copies of any small current that is available (using a process called current mirroring). The designer proposes to use this idea to supply two diodes of different junction areas with equal currents and to measure their junction-voltage difference. Two types of diodes are available: for a forward voltage of 700 mV, one conducts 0.1 mA, while the other conducts 1 A. Now, for identical currents in the range of 1 mA to 3 mA supplied to each, what range of difference voltages result? What is the effect of a temperature change of  $\pm 20^\circ\text{C}$  on this arrangement?

### Section 4.3: Modeling the Diode Forward Characteristic

- \*4.34** Consider the graphical analysis of the diode circuit of Fig. 4.10 with  $V_{DD} = 1$  V,  $R = 1$  k $\Omega$ , and a diode having  $I_s = 10^{-15}$  A. Calculate a small number of points on the diode characteristic in the vicinity of where you expect the load line to intersect it, and use a graphical process to refine your estimate of diode current. What value of diode current and voltage do you find? Analytically, find the voltage corresponding to your estimate of current. By how much does it differ from the graphically estimated value?

- 4.35** Use the iterative-analysis procedure to determine the diode current and voltage in the circuit of Fig. 4.10 for  $V_{DD} = 1$  V,  $R = 1$  k $\Omega$ , and a diode having  $I_s = 10^{-15}$  A.

- 4.36** A "1-mA diode" (i.e., one that has  $v_D = 0.7$  V at  $i_D = 1$  mA) is connected in series with a 500- $\Omega$  resistor to a 1.0 V supply.

- (a) Provide a rough estimate of the diode current you would expect.  
 (b) Estimate the diode current more closely using iterative analysis.

**D 4.37** Assuming the availability of diodes for which  $v_D = 0.75$  V at  $i_D = 1$  mA, design a circuit that utilizes four diodes connected in series, in series with a resistor  $R$  connected to a 15-V power supply. The voltage across the string of diodes is to be 3.3 V.

**4.38** A diode operates in a series circuit with a resistance  $R$  and a dc source  $V$ . A designer, considering using a constant-voltage model, is uncertain whether to use 0.7 V or 0.6 V for  $V_D$ . For what value of  $V$  is the difference in the calculated values of current only 1%? For  $V = 3$  V and  $R = 1$  k $\Omega$ , what two current estimates would result from the use of the two values of  $V_D$ ? What is their percentage difference?

**4.39** A designer has a supply of diodes for which a current of 2 mA flows at 0.7 V. Using a 1-mA current source, the designer wishes to create a reference voltage of 1.3 V. Suggest a combination of series and parallel diodes that will do the job as well as possible. How many diodes are needed? What voltage is actually achieved?

**4.40** Solve the problems in Example 4.2 using the constant-voltage-drop ( $V_D = 0.7$  V) diode model.

**4.41** For the circuits shown in Fig. P4.2, using the constant-voltage-drop ( $V_D = 0.7$  V) diode model, find the voltages and currents indicated.

**4.42** For the circuits shown in Fig. P4.3, using the constant-voltage-drop ( $V_D = 0.7$  V) diode model, find the voltages and currents indicated.

**4.43** For the circuits in Fig. P4.9, using the constant-voltage-drop ( $V_D = 0.7$  V) diode model, find the values of the labeled currents and voltages.

**4.44** For the circuits in Fig. P4.10, utilize Thévenin's theorem to simplify the circuits and find the values of the labeled currents and voltages. Assume that conducting diodes can be represented by the constant-voltage-drop model ( $V_D = 0.7$  V).

**D 4.45** Repeat Problem 4.11, representing the diode by the constant-voltage-drop ( $V_D = 0.7$  V) model. How different is the resulting design?

**4.46** The small-signal model is said to be valid for voltage variations of about 5 mV. To what percentage current change does this correspond? (Consider both positive and negative signals.) What is the maximum allowable voltage signal (positive or negative) if the current change is to be limited to 10%?

**4.47** In a particular circuit application, ten “20-mA diodes” (a 20-mA diode is a diode that provides a 0.7-V drop when the current through it is 20 mA) connected in parallel operate at a total current of 0.1 A. For the diodes closely matched, what current flows in each? What is the corresponding small-signal resistance of each diode and of the combination? Compare this with the incremental resistance of a single diode conducting 0.1 A. If each of the 20-mA diodes has a series resistance of 0.2  $\Omega$  associated with the wire bonds to the junction, what is the equivalent resistance of the 10 parallel-connected diodes? What connection resistance would a single diode need in order to be totally equivalent? (Note: This is why the parallel connection of real diodes can often be used to advantage.)

**4.48** In the circuit shown in Fig. P4.48,  $I$  is a dc current and  $v_s$  is a sinusoidal signal. Capacitors  $C_1$  and  $C_2$  are very large; their function is to couple the signal to and from the diode but block the dc current from flowing into the signal source or the load (not shown). Use the diode small-signal model to show that the signal component of the output voltage is

$$v_o = v_s \frac{V_T}{V_T + IR_s}$$

If  $v_s = 10$  mV, find  $v_o$  for  $I = 1$  mA, 0.1 mA, and 1  $\mu$ A. Let  $R_s = 1$  k $\Omega$ . At what value of  $I$  does  $v_o$  become one-half of  $v_s$ ? Note that this circuit functions as a signal attenuator with the attenuation factor controlled by the value of the dc current  $I$ .

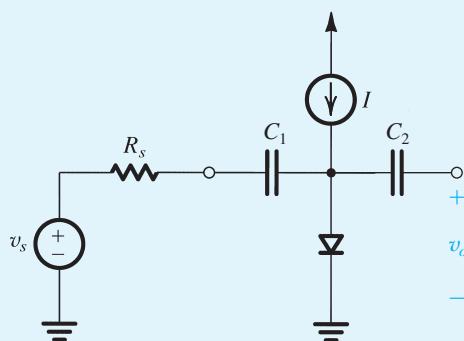


Figure P4.48

**4.49** In the attenuator circuit of Fig. P4.48, let  $R_s = 10 \text{ k}\Omega$ . The diode is a 1-mA device; that is, it exhibits a voltage drop of 0.7 V at a dc current of 1 mA. For small input signals, what value of current  $I$  is needed for  $v_o/v_s = 0.50?$  0.10? 0.01? 0.001? In each case, what is the largest input signal that can be used while ensuring that the signal component of the diode current is limited to  $\pm 10\%$  of its dc current? What output signals correspond?

**4.50** In the capacitor-coupled attenuator circuit shown in Fig. P4.50,  $I$  is a dc current that varies from 0 mA to 1 mA, and  $C_1$  and  $C_2$  are large coupling capacitors. For very small input signals, so that the diodes can be represented by their small-signal resistances  $r_{d1}$  and  $r_{d2}$ , give the small-signal equivalent circuit and thus show that  $\frac{v_o}{v_i} = \frac{r_{d2}}{r_{d1} + r_{d2}}$  and hence that  $\frac{v_o}{v_i} = I$ , where  $I$  is in mA. Find  $v_o/v_i$  for  $I = 0 \mu\text{A}, 1 \mu\text{A}, 10 \mu\text{A}, 100 \mu\text{A}, 500 \mu\text{A}, 600 \mu\text{A}, 900 \mu\text{A}, 990 \mu\text{A}$ , and 1 mA. Note that this is a signal attenuator whose transmission is linearly controlled by the dc current  $I$ .

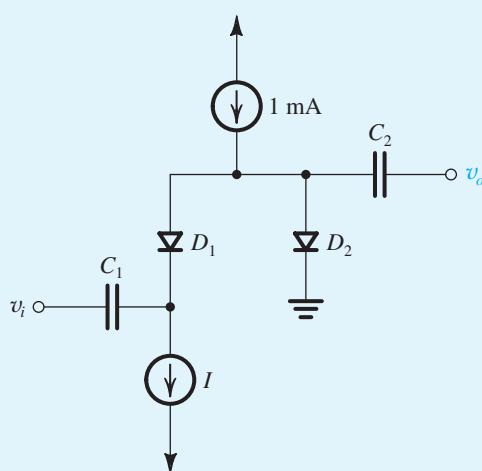


Figure P4.50

**\*4.51** In the circuit shown in Fig. P4.51, diodes  $D_1$  through  $D_4$  are identical, and each exhibits a voltage drop of 0.7 V at a 1-mA current.

(a) For small input signals (e.g., 10-mV peak), find the small-signal equivalent circuit and use it to determine values of the small-signal transmission  $v_o/v_i$  for various values of  $I$ : 0  $\mu\text{A}, 1 \mu\text{A}, 10 \mu\text{A}, 100 \mu\text{A}, 1 \text{ mA},$  and 10 mA.

- (b) For a forward-conducting diode, what is the largest signal-voltage magnitude that it can support while the corresponding signal current is limited to 10% of the dc bias current? Now, for the circuit in Fig. P4.51, for 10-mV peak input, what is the smallest value of  $I$  for which the diode currents remain within  $\pm 10\%$  of their dc values?
- (c) For  $I = 1 \text{ mA}$ , what is the largest possible output signal for which the diode currents deviate by at most 10% of their dc values? What is the corresponding peak input? What is the total current in each diode?

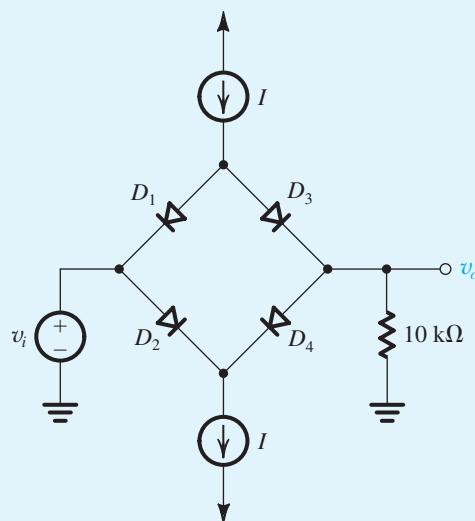


Figure P4.51

**\*\*4.52** In Problem 4.51 we investigated the operation of the circuit in Fig. P4.51 for small input signals. In this problem we wish to find the voltage-transfer characteristic (VTC)  $v_o$  versus  $v_i$  for  $-12 \text{ V} \leq v_i \leq 12 \text{ V}$  for the case  $I = 1 \text{ mA}$  and each of the diodes exhibits a voltage drop of 0.7 V at a current of 1 mA. Toward this end, use the diode exponential characteristic to construct a table that gives the values of: the current  $i_o$  in the 10-kΩ resistor, the current in each of the four diodes, the voltage drop across each of the four diodes, and the input voltage  $v_i$ , for  $v_o = 0, +1 \text{ V}, +2 \text{ V}, +5 \text{ V}, +9 \text{ V}, +9.9 \text{ V}, +9.99 \text{ V}, +10.5 \text{ V}, +11 \text{ V},$  and  $+12 \text{ V}$ . Use these data, with extrapolation to negative values of  $v_i$  and  $v_o$ , to sketch the required VTC. Also sketch the VTC that results if  $I$  is reduced to 0.5 mA. (Hint: From symmetry, observe that as  $v_o$  increases and  $i_o$  correspondingly increases,  $i_{D_3}$  and  $i_{D_2}$  increase by equal amounts and  $i_{D_4}$  and  $i_{D_1}$  decrease by (the same) equal amounts.)

**SIM** \*4.53 In the circuit shown in Fig. P4.53,  $I$  is a dc current and  $v_i$  is a sinusoidal signal with small amplitude (less than 10 mV) and a frequency of 100 kHz. Representing the diode by its small-signal resistance  $r_d$ , which is a function of  $I$ , sketch the small-signal equivalent circuit and use it to determine the sinusoidal output voltage  $V_o$ , and thus find the phase shift between  $V_i$  and  $V_o$ . Find the value of  $I$  that will provide a phase shift of  $-45^\circ$ , and find the range of phase shift achieved as  $I$  is varied over the range of 0.1 times to 10 times this value.

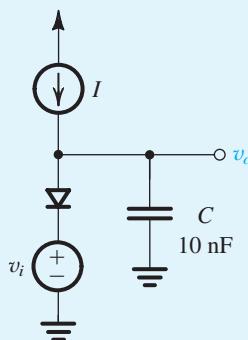


Figure P4.53

\*4.54 Consider the voltage-regulator circuit shown in Fig. P4.54. The value of  $R$  is selected to obtain an output voltage  $V_o$  (across the diode) of 0.7 V.

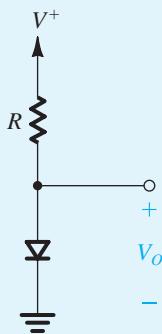


Figure P4.54

(a) Use the diode small-signal model to show that the change in output voltage corresponding to a change of 1 V in  $V^+$  is

$$\frac{\Delta V_o}{\Delta V^+} = \frac{V_T}{V^+ + V_T - 0.7}$$

This quantity is known as the line regulation and is usually expressed in mV/V.

(b) Generalize the expression above for the case of  $m$  diodes connected in series and the value of  $R$  adjusted so that the voltage across each diode is 0.7 V (and  $V_o = 0.7m$  V).

(c) Calculate the value of line regulation for the case  $V^+ = 15$  V (nominally) and (i)  $m = 1$  and (ii)  $m = 4$ .

\*4.55 Consider the voltage-regulator circuit shown in Fig P4.54 under the condition that a load current  $I_L$  is drawn from the output terminal.

(a) If the value of  $I_L$  is sufficiently small that the corresponding change in regulator output voltage  $\Delta V_o$  is small enough to justify using the diode small-signal model, show that

$$\frac{\Delta V_o}{I_L} = -(r_d \parallel R)$$

This quantity is known as the load regulation and is usually expressed in mV/mA.

(b) If the value of  $R$  is selected such that at no load the voltage across the diode is 0.7 V and the diode current is  $I_D$ , show that the expression derived in (a) becomes

$$\frac{\Delta V_o}{I_L} = -\frac{V_T}{I_D} \frac{V^+ - 0.7}{V^+ - 0.7 + V_T}$$

Select the lowest possible value for  $I_D$  that results in a load regulation whose magnitude is  $\leq 5$  mV/mA. If  $V^+$  is nominally 15 V, what value of  $R$  is required? Also, specify the diode required in terms of its  $I_S$ .

(c) Generalize the expression derived in (b) for the case of  $m$  diodes connected in series and  $R$  adjusted to obtain  $V_o = 0.7m$  V at no load.

**D** \*4.56 Design a diode voltage regulator to supply 1.5 V to a 1.5-kΩ load. Use two diodes specified to have a 0.7-V drop at a current of 1 mA. The diodes are to be connected to a +5-V supply through a resistor  $R$ . Specify the value for  $R$ . What is the diode current with the load connected? What is the increase resulting in the output voltage when the load is disconnected? What change results if the load resistance is reduced to 1 kΩ? To 750 Ω? To 500 Ω? (Hint: Use the small-signal diode model to calculate all changes in output voltage.)

**D** \*4.57 A voltage regulator consisting of two diodes in series fed with a constant-current source is used as a replacement for a single carbon-zinc cell (battery) of nominal voltage 1.5 V. The regulator load current varies from 2 mA to

7 mA. Constant-current supplies of 5 mA, 10 mA, and 15 mA are available. Which would you choose, and why? What change in output voltage would result when the load current varies over its full range?

**\*\*4.58** A particular design of a voltage regulator is shown in Fig. P4.58. Diodes  $D_1$  and  $D_2$  are 10-mA units; that is, each has a voltage drop of 0.7 V at a current of 10 mA. Use the diode exponential model and iterative analysis to answer the following questions:

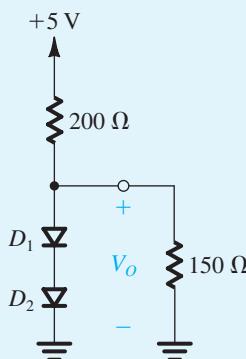


Figure P4.58

- What is the regulator output voltage  $V_o$  with the 150- $\Omega$  load connected?
- Find  $V_o$  with no load.
- With the load connected, to what value can the 5-V supply be lowered while maintaining the loaded output voltage within 0.1 V of its nominal value?
- What does the loaded output voltage become when the 5-V supply is raised by the same amount as the drop found in (c)?
- For the range of changes explored in (c) and (d), by what percentage does the output voltage change for each percentage change of supply voltage in the worst case?

### Section 4.4: Operation in the Reverse Breakdown Region—Zener Diodes

**4.59** Partial specifications of a collection of zener diodes are provided below. For each, identify the missing parameter and estimate its value. Note from Fig. 4.19 that  $V_{ZK} \approx V_{Z0}$  and  $I_{ZK}$  is very small.

- $V_z = 10.0\text{ V}$ ,  $V_{ZK} = 9.6\text{ V}$ , and  $I_{ZT} = 50\text{ mA}$
- $I_{ZT} = 10\text{ mA}$ ,  $V_z = 9.1\text{ V}$ , and  $r_z = 30\text{ }\Omega$

- $r_z = 2\text{ }\Omega$ ,  $V_z = 6.8\text{ V}$ , and  $V_{ZK} = 6.6\text{ V}$
- $V_z = 18\text{ V}$ ,  $I_{ZT} = 5\text{ mA}$ , and  $V_{ZK} = 17.6\text{ V}$
- $I_{ZT} = 200\text{ mA}$ ,  $V_z = 7.5\text{ V}$ , and  $r_z = 1.5\text{ }\Omega$

Assuming that the power rating of a breakdown diode is established at about twice the specified zener current ( $I_{ZT}$ ), what is the power rating of each of the diodes described above?

**D 4.60** A designer requires a shunt regulator of approximately 20 V. Two kinds of zener diodes are available: 6.8-V devices with  $r_z$  of 10  $\Omega$  and 5.1-V devices with  $r_z$  of 25  $\Omega$ . For the two major choices possible, find the load regulation. In this calculation neglect the effect of the regulator resistance  $R$ .

**4.61** A shunt regulator utilizing a zener diode with an incremental resistance of 8  $\Omega$  is fed through an 82- $\Omega$  resistor. If the raw supply changes by 1.0 V, what is the corresponding change in the regulated output voltage?

**4.62** A 9.1-V zener diode exhibits its nominal voltage at a test current of 20 mA. At this current the incremental resistance is specified as 10  $\Omega$ . Find  $V_{Z0}$  of the zener model. Find the zener voltage at a current of 10 mA and at 50 mA.

**D 4.63** Design a 7.5-V zener regulator circuit using a 7.5-V zener specified at 10 mA. The zener has an incremental resistance  $r_z = 30\text{ }\Omega$  and a knee current of 0.5 mA. The regulator operates from a 10-V supply and has a 1.5-k $\Omega$  load. What is the value of  $R$  you have chosen? What is the regulator output voltage when the supply is 10% high? Is 10% low? What is the output voltage when both the supply is 10% high and the load is removed? What is the smallest possible load resistor that can be used while the zener operates at a current no lower than the knee current while the supply is 10% low? What is the load voltage in this case?

**D 4.64** Provide two designs of shunt regulators utilizing the 1N5235 zener diode, which is specified as follows:  $V_z = 6.8\text{ V}$  and  $r_z = 5\text{ }\Omega$  for  $I_z = 20\text{ mA}$ ; at  $I_z = 0.25\text{ mA}$  (nearer the knee),  $r_z = 750\text{ }\Omega$ . For both designs, the supply voltage is nominally 9 V and varies by  $\pm 1\text{ V}$ . For the first design, assume that the availability of supply current is not a problem, and thus operate the diode at 20 mA. For the second design, assume that the current from the raw supply is limited, and therefore you are forced to operate the diode at 0.25 mA. For the purpose of these initial designs, assume no load. For each design find the value of  $R$  and the line regulation.

**D \*4.65** A zener shunt regulator employs a 9.1-V zener diode for which  $V_z = 9.1\text{ V}$  at  $I_z = 9\text{ mA}$ , with  $r_z = 40\text{ }\Omega$  and

$I_{ZK} = 0.5$  mA. The available supply voltage of 15 V can vary as much as  $\pm 10\%$ . For this diode, what is the value of  $V_{z0}$ ? For a nominal load resistance  $R_L$  of 1 k $\Omega$  and a nominal zener current of 10 mA, what current must flow in the supply resistor  $R$ ? For the nominal value of supply voltage, select a value for resistor  $R$ , specified to one significant digit, to provide at least that current. What nominal output voltage results? For a  $\pm 10\%$  change in the supply voltage, what variation in output voltage results? If the load current is reduced by 50%, what increase in  $V_o$  results? What is the smallest value of load resistance that can be tolerated while maintaining regulation when the supply voltage is low? What is the lowest possible output voltage that results? Calculate values for the line regulation and for the load regulation for this circuit using the numerical results obtained in this problem.

**D \*4.66** It is required to design a zener shunt regulator to provide a regulated voltage of about 10 V. The available 10-V, 1-W zener of type 1N4740 is specified to have a 10-V drop at a test current of 25 mA. At this current, its  $r_z$  is 7  $\Omega$ . The raw supply,  $V_s$ , available has a nominal value of 20 V but can vary by as much as  $\pm 25\%$ . The regulator is required to supply a load current of 0 mA to 20 mA. Design for a minimum zener current of 5 mA.

- (a) Find  $V_{z0}$ .
- (b) Calculate the required value of  $R$ .
- (c) Find the line regulation. What is the change in  $V_o$  expressed as a percentage, corresponding to the  $\pm 25\%$  change in  $V_s$ ?
- (d) Find the load regulation. By what percentage does  $V_o$  change from the no-load to the full-load condition?
- (e) What is the maximum current that the zener in your design is required to conduct? What is the zener power dissipation under this condition?

### Section 4.5: Rectifier Circuits

**4.67** Consider the half-wave rectifier circuit of Fig. 4.23(a) with the diode reversed. Let  $v_s$  be a sinusoid with 10-V peak amplitude, and let  $R = 1$  k $\Omega$ . Use the constant-voltage-drop diode model with  $V_D = 0.7$  V.

- (a) Sketch the transfer characteristic.
- (b) Sketch the waveform of  $v_o$ .
- (c) Find the average value of  $v_o$ .
- (d) Find the peak current in the diode.
- (e) Find the PIV of the diode.

**4.68** Using the exponential diode characteristic, show that for  $v_s$  and  $v_o$  both greater than zero, the circuit of Fig. 4.23(a) has the transfer characteristic

$$v_o = v_s - v_D \text{ (at } i_D = 1 \text{ mA)} - V_T \ln(v_o/R)$$

where  $v_s$  and  $v_o$  are in volts and  $R$  is in kilohms. Note that this relationship can be used to obtain the voltage transfer characteristic  $v_o$  vs.  $v_s$  by finding  $v_s$  corresponding to various values of  $v_o$ .

**SIM 4.69** Consider a half-wave rectifier circuit with a triangular-wave input of 5-V peak-to-peak amplitude and zero average, and with  $R = 1$  k $\Omega$ . Assume that the diode can be represented by the constant-voltage-drop model with  $V_D = 0.7$  V. Find the average value of  $v_o$ .

**4.70** A half-wave rectifier circuit with a 1-k $\Omega$  load operates from a 120-V (rms) 60-Hz household supply through a 12-to-1 step-down transformer. It uses a silicon diode that can be modeled to have a 0.7-V drop for any current. What is the peak voltage of the rectified output? For what fraction of the cycle does the diode conduct? What is the average output voltage? What is the average current in the load?

**4.71** A full-wave rectifier circuit with a 1-k $\Omega$  load operates from a 120-V (rms) 60-Hz household supply through a 6-to-1 transformer having a center-tapped secondary winding. It uses two silicon diodes that can be modeled to have a 0.7-V drop for all currents. What is the peak voltage of the rectified output? For what fraction of a cycle does each diode conduct? What is the average output voltage? What is the average current in the load?

**4.72** A full-wave bridge-rectifier circuit with a 1-k $\Omega$  load operates from a 120-V (rms) 60-Hz household supply through a 12-to-1 step-down transformer having a single secondary winding. It uses four diodes, each of which can be modeled to have a 0.7-V drop for any current. What is the peak value of the rectified voltage across the load? For what fraction of a cycle does each diode conduct? What is the average voltage across the load? What is the average current through the load?

**D 4.73** It is required to design a full-wave rectifier circuit using the circuit of Fig. 4.24 to provide an average output voltage of:

- (a) 10 V
- (b) 100 V

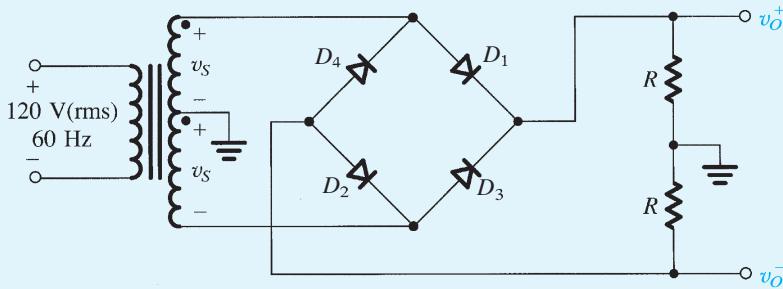


Figure P4.76

In each case find the required turns ratio of the transformer. Assume that a conducting diode has a voltage drop of 0.7 V. The ac line voltage is 120 V rms.

**D 4.74** Repeat Problem 4.73 for the bridge-rectifier circuit of Fig. 4.25.

**D 4.75** Consider the full-wave rectifier in Fig. 4.24 when the transformer turns ratio is such that the voltage across the entire secondary winding is 20 V rms. If the input ac line voltage (120 V rms) fluctuates by as much as  $\pm 10\%$ , find the required PIV of the diodes. (Remember to use a factor of safety in your design.)

**4.76** The circuit in Fig. P4.76 implements a complementary-output rectifier. Sketch and clearly label the waveforms of  $v_o^+$  and  $v_o^-$ . Assume a 0.7-V drop across each conducting diode. If the magnitude of the average of each output is to be 12 V, find the required amplitude of the sine wave across the entire secondary winding. What is the PIV of each diode?

**4.77** Augment the rectifier circuit of Problem 4.70 with a capacitor chosen to provide a peak-to-peak ripple voltage of (i) 10% of the peak output and (ii) 1% of the peak output. In each case:

- What average output voltage results?
- What fraction of the cycle does the diode conduct?
- What is the average diode current?
- What is the peak diode current?

**4.78** Repeat Problem 4.77 for the rectifier in Problem 4.71.

**4.79** Repeat Problem 4.77 for the rectifier in Problem 4.72.

**D \*4.80** It is required to use a peak rectifier to design a dc power supply that provides an average dc output voltage of 12 V on which a maximum of  $\pm 1$ -V ripple is allowed. The rectifier feeds a load of  $200 \Omega$ . The rectifier is fed from the line voltage (120 V rms, 60 Hz) through a transformer. The diodes available have 0.7-V drop when conducting. If the designer opts for the half-wave circuit:

- Specify the rms voltage that must appear across the transformer secondary.
- Find the required value of the filter capacitor.
- Find the maximum reverse voltage that will appear across the diode, and specify the PIV rating of the diode.
- Calculate the average current through the diode during conduction.
- Calculate the peak diode current.

**D \*4.81** Repeat Problem 4.80 for the case in which the designer opts for a full-wave circuit utilizing a center-tapped transformer.

**D \*4.82** Repeat Problem 4.80 for the case in which the designer opts for a full-wave bridge-rectifier circuit.

**D \*4.83** Consider a half-wave peak rectifier fed with a voltage  $v_s$  having a triangular waveform with 24-V peak-to-peak amplitude, zero average, and 1-kHz frequency. Assume that the diode has a 0.7-V drop when conducting. Let the load resistance  $R = 100 \Omega$  and the filter capacitor  $C = 100 \mu F$ . Find the average dc output voltage, the time interval during which the diode conducts, the average diode current during conduction, and the maximum diode current.

**D \*4.84** Consider the circuit in Fig. P4.76 with two equal filter capacitors placed across the load resistor  $R$ . Assume that the diodes available exhibit a 0.7-V drop when conducting. Design the circuit to provide  $\pm 12$ -V dc output voltages with a peak-to-peak ripple no greater than 1 V. Each supply should be capable of providing 100-mA dc current to its load resistor  $R$ . Completely specify the capacitors, diodes, and the transformer.

**4.85** The op amp in the precision rectifier circuit of Fig. P4.85 is ideal with output saturation levels of  $\pm 13$  V. Assume that when conducting the diode exhibits a constant voltage drop of 0.7 V. Find  $v_-$ ,  $v_o$ , and  $v_A$  for:

- (a)  $v_I = +1$  V
- (b)  $v_I = +3$  V
- (c)  $v_I = -1$  V
- (d)  $v_I = -3$  V

Also, find the average output voltage obtained when  $v_I$  is a symmetrical square wave of 1-kHz frequency, 5-V amplitude, and zero average.

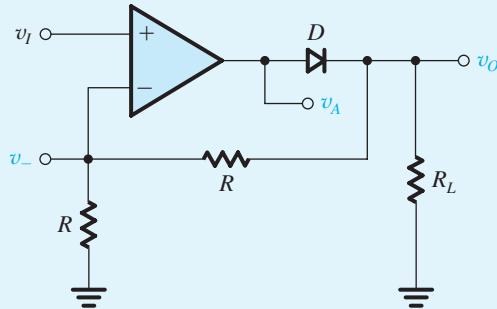


Figure P4.85

**4.86** The op amp in the circuit of Fig. P4.86 is ideal with output saturation levels of  $\pm 12$  V. The diodes exhibit a constant 0.7-V drop when conducting. Find  $v_-$ ,  $v_A$ , and  $v_o$  for:

- (a)  $v_I = +1$  V
- (b)  $v_I = +3$  V

- (c)  $v_I = -1$  V
- (d)  $v_I = -3$  V

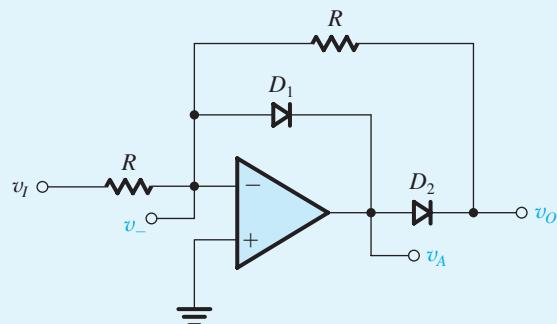
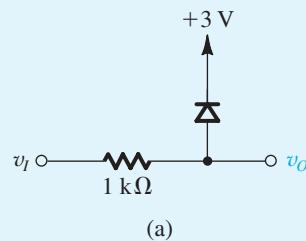


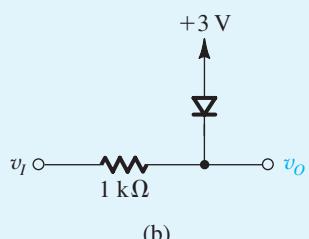
Figure P4.86

### Section 4.6: Limiting and Clamping Circuits

**4.87** Sketch the transfer characteristic  $v_o$  versus  $v_I$  for the limiter circuits shown in Fig. P4.87. All diodes begin conducting at a forward voltage drop of 0.5 V and have voltage drops of 0.7 V when conducting a current  $i_D \geq 1$  mA.

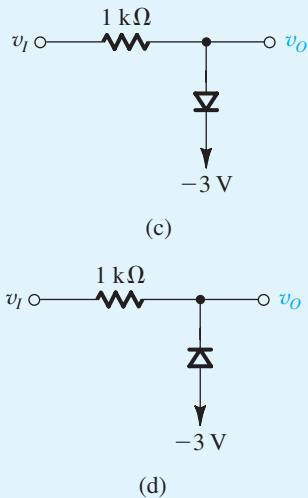


(a)



(b)

Figure P4.87

Figure P4.87 *continued*

**4.88** The circuits in Fig. P4.87(a) and (d) are connected as follows: The two input terminals are tied together, and the two output terminals are tied together. Sketch the transfer characteristic of the circuit resulting, assuming that the cut-in voltage of the diodes is 0.5 V and their voltage drop when conducting a current  $i_D \geq 1$  mA is 0.7 V.

**4.89** Repeat Problem 4.88 for the two circuits in Fig. P4.87(a) and (b) connected together as follows: The two input terminals are tied together, and the two output terminals are tied together.

**4.90** Sketch and clearly label the transfer characteristic of the circuit in Fig. P4.90 for  $-15 \text{ V} \leq v_I \leq +15 \text{ V}$ . Assume that

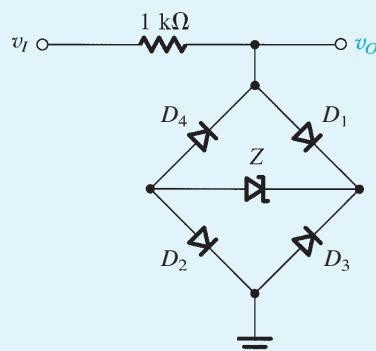


Figure P4.90

the diodes can be represented by the constant-voltage-drop model with  $V_D = 0.7 \text{ V}$ . Also assume that the zener voltage is  $6.8 \text{ V}$  and that  $r_z$  is negligibly small.

**\*4.91** Plot the transfer characteristic of the circuit in Fig. P4.91 by evaluating  $v_I$  corresponding to  $v_O = 0.5 \text{ V}, 0.6 \text{ V}, 0.7 \text{ V}, 0.8 \text{ V}, 0 \text{ V}, -0.5 \text{ V}, -0.6 \text{ V}, -0.7 \text{ V}$ , and  $-0.8 \text{ V}$ . Use the exponential model for the diodes, and assume that they have 0.7-V drops at 1-mA currents. Characterize the circuit as a hard or soft limiter. What is the value of  $K$ ? Estimate  $L_+$  and  $L_-$ .

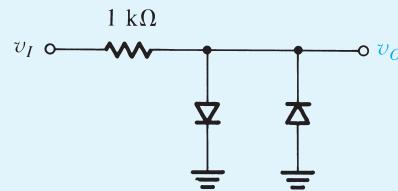


Figure P4.91

**4.92** Design limiter circuits using only diodes and  $10\text{-k}\Omega$  resistors to provide an output signal limited to the range:

- 0.7 V and above
- +2.1 V and below
- $\pm 1.4 \text{ V}$

Assume that each diode has a 0.7-V drop when conducting.

**4.93** Design a two-sided limiting circuit using a resistor, two diodes, and two power supplies to feed a  $1\text{-k}\Omega$  load with nominal limiting levels of  $\pm 2.2 \text{ V}$ . Use diodes modeled by a constant 0.7 V. In the nonlimiting region, the voltage gain should be at least 0.94 V/V.

**\*\*4.94** In the circuit shown in Fig. P4.94, the diodes exhibit a 0.7-V drop at 0.1 mA. For inputs over the range of  $\pm 5 \text{ V}$ , use the diode exponential model to provide a calibrated sketch of the voltages at outputs B and C versus  $v_A$ . For a 5-V peak,

100-Hz sinusoid applied at A, sketch the signals at nodes B and C.

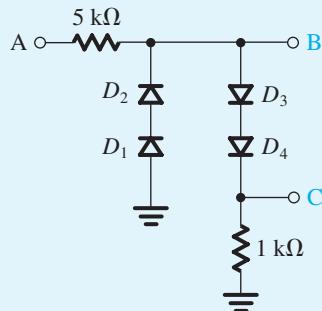


Figure P4.94

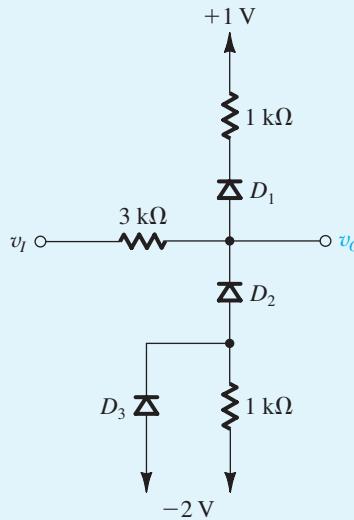


Figure P4.95

**\*\*4.95** Sketch and label the voltage-transfer characteristic  $v_o$  versus  $v_i$  of the circuit shown in Fig. P4.95 over a  $\pm 10$ -V range of input signals. Use the diode exponential model and assume that all diodes are 1-mA units (i.e., each exhibits a 0.7-V drop at a current of 1 mA). What are the slopes of the characteristics at the extreme  $\pm 10$ -V levels?

**4.96** A clamped capacitor using an ideal diode with cathode grounded is supplied with a sine wave of 5-V rms. What is the average (dc) value of the resulting output?

**\*4.97** For the circuits in Fig. P4.97, each utilizing an ideal diode (or diodes), sketch the output for the input shown. Label the most positive and most negative output levels. Assume  $CR \gg T$ .

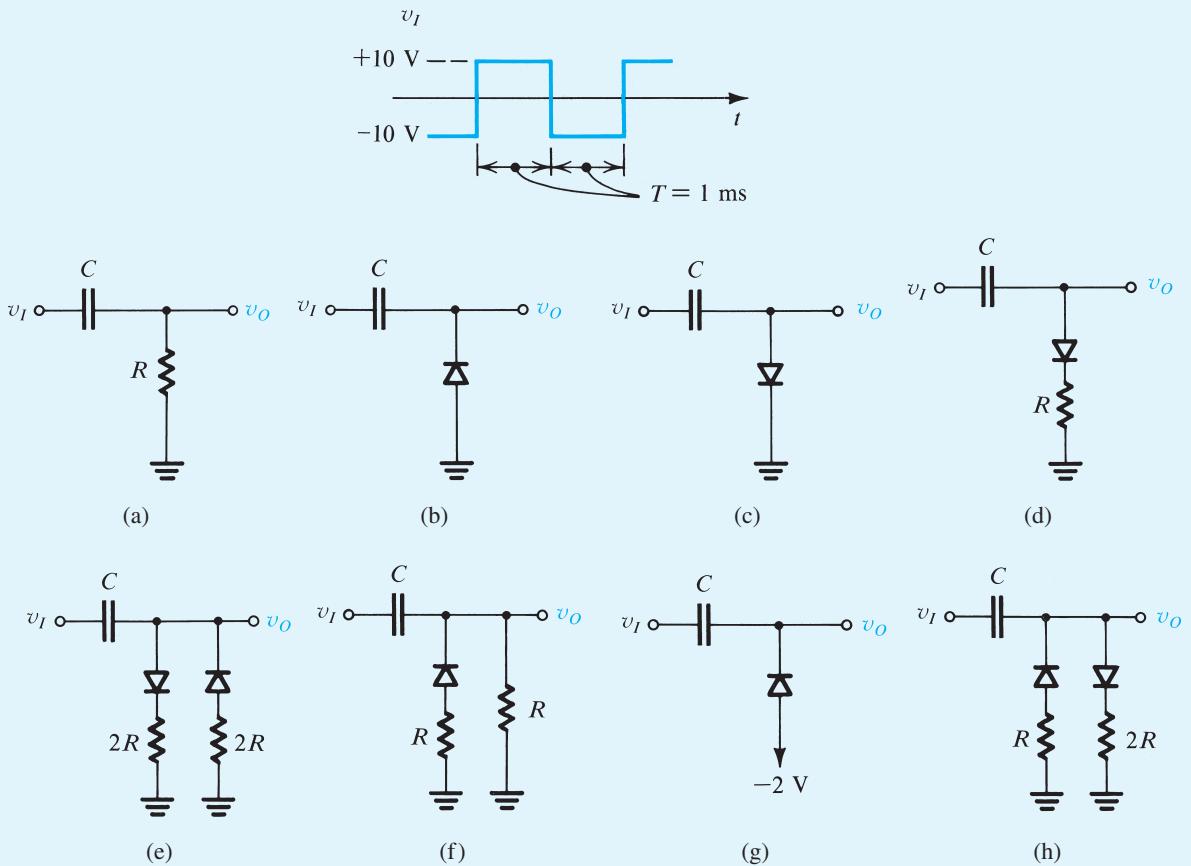


Figure P4.97

## CHAPTER 5

# MOS Field-Effect Transistors (MOSFETs)

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**5.2 Current–Voltage Characteristics** 264

**5.3 MOSFET Circuits at DC** 276

**5.4 The Body Effect and Other Topics** 288

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## IN THIS CHAPTER YOU WILL LEARN

1. The physical structure of the MOS transistor and how it works.
  2. How the voltage between two terminals of the transistor controls the current that flows through the third terminal, and the equations that describe these current–voltage characteristics.
  3. How to analyze and design circuits that contain MOS transistors, resistors, and dc sources.
- 

## Introduction

Having studied the junction diode, which is the most basic two-terminal semiconductor device, we now turn our attention to three-terminal semiconductor devices. Three-terminal devices are far more useful than two-terminal ones because they can be used in a multitude of applications, ranging from signal amplification to digital logic and memory. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way a three-terminal device can be used to realize a controlled source, which as we have learned in Chapter 1 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. As we shall see in Chapter 14, the switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

There are two major types of three-terminal semiconductor devices: the metal-oxide-semiconductor field-effect transistor (MOSFET), which is studied in this chapter, and the bipolar junction transistor (BJT), which we shall study in Chapter 6. Although each of the two transistor types offers unique features and areas of application, the MOSFET has become by far the most widely used electronic device, especially in the design of integrated circuits (ICs), which are entire circuits fabricated on a single silicon chip.

Compared to BJTs, MOSFETs can be made quite small (i.e., requiring a small area on the silicon IC chip), and their manufacturing process is relatively simple (see Appendix A). Also, their operation requires comparatively little power. Furthermore, circuit designers have found ingenious ways to implement digital and analog functions utilizing MOSFETs almost exclusively (i.e., with very few or no resistors). All of these properties have made it possible to pack large numbers of MOSFETs (as many as 4 billion!) on a single IC chip to implement very sophisticated, very-large-scale-integrated (VLSI) digital circuits such as those for memory and microprocessors. Analog circuits such as amplifiers and filters can also be implemented in MOS technology, albeit in smaller, less-dense chips. Also, both analog and digital functions are increasingly being implemented on the same IC chip, in what is known as mixed-signal design.

The objective of this chapter is to develop in the reader a high degree of familiarity with the MOSFET: its physical structure and operation, terminal characteristics, and dc circuit applications. This will provide a solid foundation for the application of the MOSFET in amplifier design (Chapter 7) and in digital circuit design (Chapter 14). Although discrete MOS transistors exist, and the material studied in this chapter will enable the reader to design discrete MOS circuits, our study of the MOSFET is strongly influenced by the fact that most of its applications are in integrated-circuit design. The design of IC analog and digital MOS circuits occupies a large proportion of the remainder of this book.

### THE FIRST FIELD-EFFECT DEVICES:

In 1925 a patent for solid-state electric-field-controlled conductor was filed in Canada by Julius E. Lilienfeld, a physicist at the University of Leipzig, Germany. Other patent refinements followed in the United States in 1926 and 1928. Regrettably, no research papers were published. Consequently, in 1934 Oskar Heil, a German physicist working at the University of Cambridge, U.K., filed a patent on a similar idea. But all these early concepts of electric-field control of a semiconducting path languished because suitable technology was not available.

The invention of the bipolar transistor in 1947 at Bell Telephone Laboratories resulted in the speedy development of bipolar devices, a circumstance that further delayed the development of field-effect transistors. Although the field-effect device was described in a paper by William Shockley in 1952, it was not until 1960 that a patent on an insulated-gate field-effect device, the MOSFET, was filed by Dawon Kahng and Martin Atalla, also at Bell Labs. Clearly, the idea of field-effect control for amplification and switching has changed the world. With integrated-circuit chips today containing billions of MOS devices, MOS dominates the electronics world!

## 5.1 Device Structure and Physical Operation

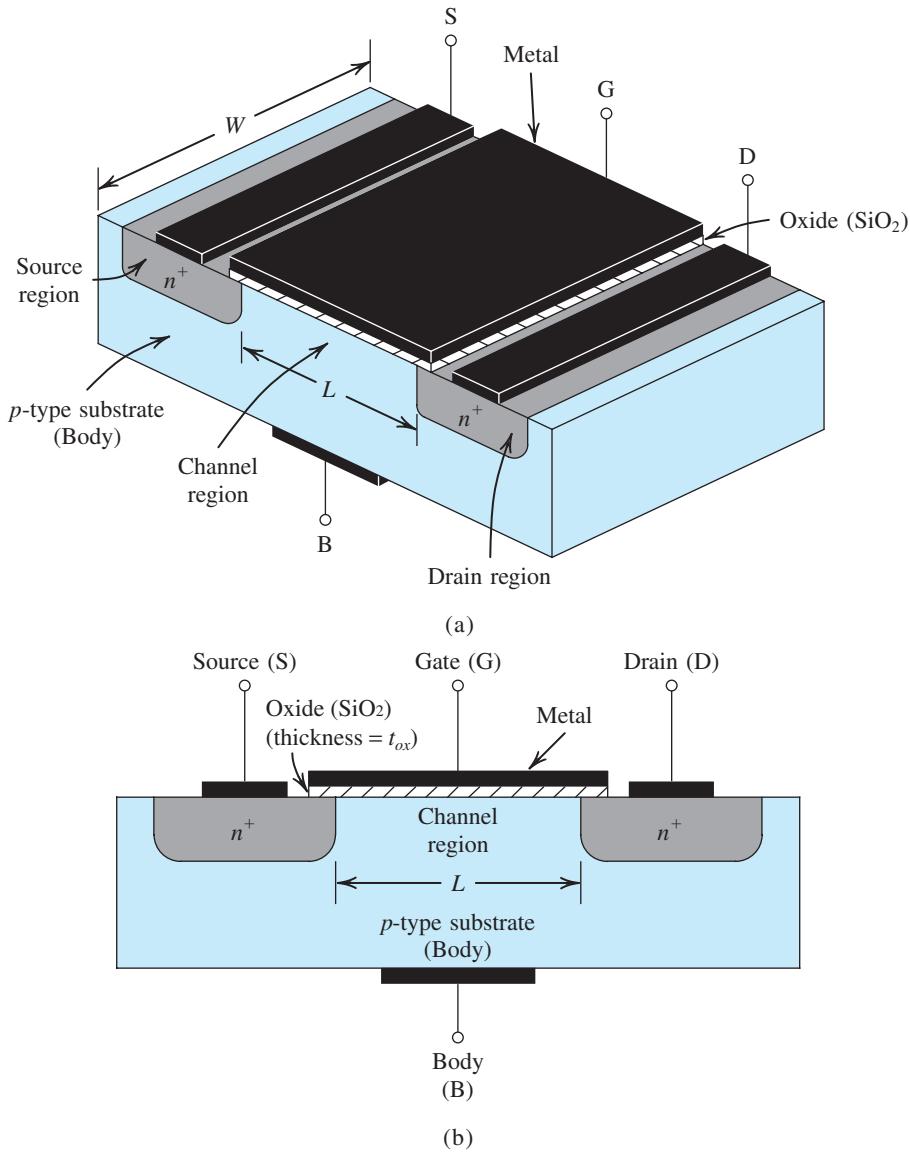
The enhancement-type MOSFET is the most widely used field-effect transistor. Except for the last section, this chapter is devoted to the study of the enhancement-type MOSFET. We begin in this section by learning about its structure and physical operation. This will lead to the current–voltage characteristics of the device, studied in the next section.

### 5.1.1 Device Structure

Figure 5.1 shows the physical structure of the *n*-channel enhancement-type MOSFET. The meaning of the names “enhancement” and “*n*-channel” will become apparent shortly. The transistor is fabricated on a *p*-type substrate, which is a single-crystal silicon wafer that provides physical support for the device (and for the entire circuit in the case of an integrated circuit). Two heavily doped *n*-type regions, indicated in the figure as the *n*<sup>+</sup> **source**<sup>1</sup> and the *n*<sup>+</sup> **drain** regions, are created in the substrate. A thin layer of silicon dioxide ( $\text{SiO}_2$ ) of thickness  $t_{ox}$  (typically 1 nm to 10 nm),<sup>2</sup> which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the **gate electrode** of the device. Metal contacts are

<sup>1</sup>The notation *n*<sup>+</sup> indicates heavily doped *n*-type silicon. Conversely, *n*<sup>−</sup> is used to denote lightly doped *n*-type silicon. Similar notation applies for *p*-type silicon.

<sup>2</sup>A nanometer (nm) is  $10^{-9}$  m or 0.001  $\mu\text{m}$ . A micrometer ( $\mu\text{m}$ ), or micron, is  $10^{-6}$  m. Sometimes the oxide thickness is expressed in angstroms. An angstrom ( $\text{\AA}$ ) is  $10^{-1}$  nm, or  $10^{-10}$  m.



**Figure 5.1** Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross section. Typically  $L = 0.03 \mu\text{m}$  to  $1 \mu\text{m}$ ,  $W = 0.05 \mu\text{m}$  to  $100 \mu\text{m}$ , and the thickness of the oxide layer ( $t_{\text{ox}}$ ) is in the range of 1 to 10 nm.

also made to the source region, the drain region, and the substrate, also known as the **body**.<sup>3</sup> Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

<sup>3</sup>In Fig. 5.1, the contact to the body is shown on the bottom of the device. This will prove helpful in Section 5.4 in explaining a phenomenon known as the “body effect.” It is important to note, however, that in actual ICs, contact to the body is made at a location on the top of the device.

At this point it should be clear that the name of the device (metal-oxide-semiconductor FET) is derived from its physical structure. The name, however, has become a general one and is used also for FETs that do not use metal for the gate electrode. In fact, most modern MOSFETs are fabricated using a process known as silicon-gate technology, in which a certain type of silicon, called polysilicon, is used to form the gate electrode (see Appendix A). Our description of MOSFET operation and characteristics applies irrespective of the type of gate electrode.

Another name for the MOSFET is the **insulated-gate FET** or **IGFET**. This name also arises from the physical structure of the device, emphasizing the fact that the gate electrode is electrically insulated from the device body (by the oxide layer). It is this insulation that causes the current in the gate terminal to be extremely small (of the order of  $10^{-15}$  A).

Observe that the substrate forms *pn* junctions with the source and drain regions. In normal operation these *pn* junctions are kept reverse biased at all times. Since, as we shall see shortly, the drain will always be at a positive voltage relative to the source, the two *pn* junctions can be effectively cut off by simply connecting the substrate terminal to the source terminal. We shall assume this to be the case in the following description of MOSFET operation. Thus, here, the substrate will be considered as having no effect on device operation, and the MOSFET will be treated as a three-terminal device, with the terminals being the gate (G), the source (S), and the drain (D). It will be shown that a voltage applied to the gate controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labeled “channel region.” Note that this region has a length  $L$  and a width  $W$ , two important parameters of the MOSFET. Typically,  $L$  is in the range of 0.03  $\mu\text{m}$  to 1  $\mu\text{m}$ , and  $W$  is in the range of 0.05  $\mu\text{m}$  to 100  $\mu\text{m}$ . Finally, note that the MOSFET is a symmetrical device; thus its source and drain can be interchanged with no change in device characteristics.

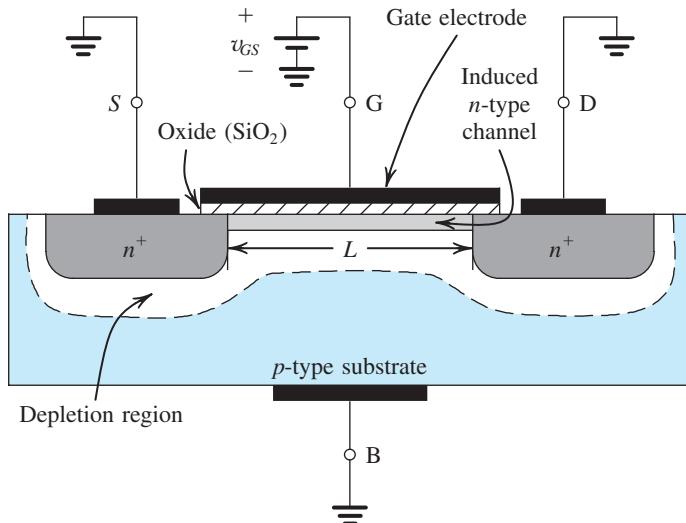
### 5.1.2 Operation with Zero Gate Voltage

With zero voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the *pn* junction between the  $n^+$  drain region and the *p*-type substrate, and the other diode is formed by the *pn* junction between the *p*-type substrate and the  $n^+$  source region. These back-to-back diodes prevent current conduction from drain to source when a voltage  $v_{DS}$  is applied. In fact, the path between drain and source has a very high resistance (of the order of  $10^{12} \Omega$ ).

### 5.1.3 Creating a Channel for Current Flow

Consider next the situation depicted in Fig. 5.2. Here we have grounded the source and the drain and applied a positive voltage to the gate. Since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted  $v_{GS}$ . The positive voltage on the gate causes, in the first instance, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are “uncovered” because the neutralizing holes have been pushed downward into the substrate.

As well, the positive gate voltage attracts electrons from the  $n^+$  source and drain regions (where they are in abundance) into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an *n* region is in effect created, connecting the source and drain regions, as indicated in Fig. 5.2. Now if a voltage is applied between drain and source, current flows through this induced *n* region, carried by the mobile



**Figure 5.2** The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

electrons. The *induced n* region thus forms a **channel** for current flow from drain to source and is aptly called so. Correspondingly, the MOSFET of Fig. 5.2 is called an ***n*-channel MOSFET** or, alternatively, an **NMOS transistor**. Note that an *n*-channel MOSFET is formed in a *p*-type substrate: The channel is created by *inverting* the substrate surface from *p* type to *n* type. Hence the induced channel is also called an **inversion layer**.

The value of  $v_{GS}$  at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted  $V_t$ .<sup>4</sup> Obviously,  $V_t$  for an *n*-channel FET is positive. The value of  $V_t$  is controlled during device fabrication and typically lies in the range of 0.3 V to 1.0 V.

The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode). The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage  $v_{DS}$  is applied. This is the origin of the name “field-effect transistor” (FET).

The voltage across this parallel-plate capacitor, that is, the voltage across the oxide, must exceed  $V_t$  for a channel to form. When  $v_{DS} = 0$ , as in Fig. 5.2, the voltage at every point along the channel is zero, and the voltage across the oxide (i.e., between the gate and the points along the channel) is uniform and equal to  $v_{GS}$ . The excess of  $v_{GS}$  over  $V_t$  is termed the **effective voltage** or the **overdrive voltage** and is the quantity that determines the charge in the channel. In this book, we shall denote  $(v_{GS} - V_t)$  by  $v_{OV}$ ,

$$v_{GS} - V_t \equiv v_{OV} \quad (5.1)$$

<sup>4</sup>Some texts use  $V_T$  to denote the threshold voltage. We use  $V_t$  to avoid confusion with the thermal voltage  $V_T$ .

We can express the magnitude of the electron charge in the channel by

➤  $|Q| = C_{ox}(WL)v_{ov}$  (5.2)

where  $C_{ox}$ , called the **oxide capacitance**, is the capacitance of the parallel-plate capacitor per unit gate area (in units of  $\text{F/m}^2$ ),  $W$  is the width of the channel, and  $L$  is the length of the channel. The oxide capacitance  $C_{ox}$  is given by

➤ 
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$
 (5.3)

where  $\epsilon_{ox}$  is the permittivity of the silicon dioxide,

$$\epsilon_{ox} = 3.9\epsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

The oxide thickness  $t_{ox}$  is determined by the process technology used to fabricate the MOSFET. As an example, for a process with  $t_{ox} = 4 \text{ nm}$ ,

$$C_{ox} = \frac{3.45 \times 10^{-11}}{4 \times 10^{-9}} = 8.6 \times 10^{-3} \text{ F/m}^2$$

It is much more convenient to express  $C_{ox}$  per micron squared. For our example, this yields  $8.6 \text{ fF}/\mu\text{m}^2$ , where fF denotes femtofarad ( $10^{-15} \text{ F}$ ). For a MOSFET fabricated in this technology with a channel length  $L = 0.18 \mu\text{m}$  and a channel width  $W = 0.72 \mu\text{m}$ , the total capacitance between gate and channel is

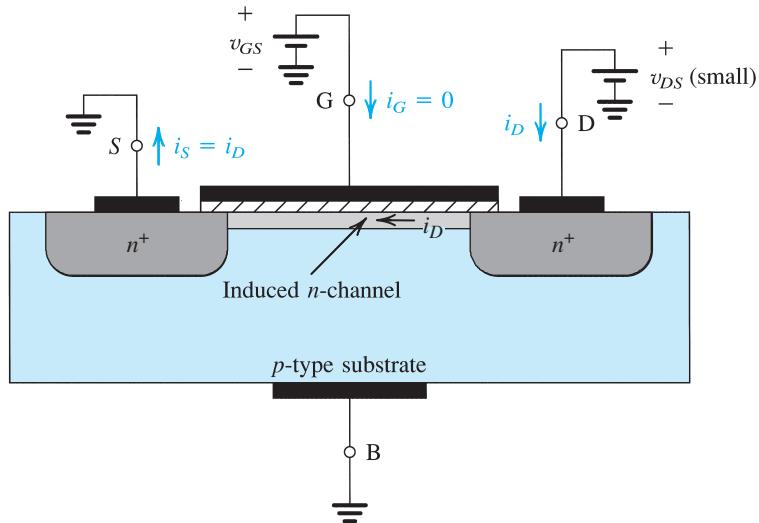
$$C = C_{ox}WL = 8.6 \times 0.18 \times 0.72 = 1.1 \text{ fF}$$

Finally, note from Eq. (5.2) that as  $v_{ov}$  is increased, the magnitude of the channel charge increases proportionately. Sometimes this is depicted as an increase in the depth of the channel; that is, the larger the overdrive voltage, the deeper the channel.

### 5.1.4 Applying a Small $v_{DS}$

Having induced a channel, we now apply a positive voltage  $v_{DS}$  between drain and source, as shown in Fig. 5.3. We first consider the case where  $v_{DS}$  is small (i.e., 50 mV or so). The voltage  $v_{DS}$  causes a current  $i_D$  to flow through the induced  $n$  channel. Current is carried by free electrons traveling from source to drain (hence the names source and drain). By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel,  $i_D$ , will be from drain to source, as indicated in Fig. 5.3.

We now wish to calculate the value of  $i_D$ . Toward that end, we first note that because  $v_{DS}$  is small, we can continue to assume that the voltage between the gate and various points along the channel remains approximately constant and equal to the value at the source end,  $v_{GS}$ . Thus, the effective voltage between the gate and the various points along the channel remains equal to  $v_{ov}$ , and the channel charge  $Q$  is still given by Eq. (5.2). Of particular interest



**Figure 5.3** An NMOS transistor with  $v_{GS} > V_t$  and with a small  $v_{DS}$  applied. The device acts as a resistance whose value is determined by  $v_{GS}$ . Specifically, the channel conductance is proportional to  $v_{GS} - V_t$ , and thus  $i_D$  is proportional to  $(v_{GS} - V_t)v_{DS}$ . Note that the depletion region is not shown (for simplicity).

in calculating the current  $i_D$  is the charge per unit channel length, which can be found from Eq. (5.2) as

$$\frac{|Q|}{\text{unit channel length}} = C_{ox}Wv_{ov} \quad (5.4)$$

The voltage  $v_{DS}$  establishes an electric field  $E$  across the length of the channel,

$$|E| = \frac{v_{DS}}{L} \quad (5.5)$$

This electric field in turn causes the channel electrons to drift toward the drain with a velocity given by

$$\text{Electron drift velocity} = \mu_n|E| = \mu_n \frac{v_{DS}}{L} \quad (5.6)$$

where  $\mu_n$  is the mobility of the electrons at the surface of the channel. It is a physical parameter whose value depends on the fabrication process technology. The value of  $i_D$  can now be found by multiplying the charge per unit channel length (Eq. 5.4) by the electron drift velocity (Eq. 5.6),

$$i_D = \left[ (\mu_n C_{ox}) \left( \frac{W}{L} \right) v_{ov} \right] v_{DS} \quad (5.7)$$

Thus, for small  $v_{DS}$ , the channel behaves as a linear resistance whose value is controlled by the overdrive voltage  $v_{OV}$ , which in turn is determined by  $v_{GS}$ :

$$\rightarrow i_D = \left[ (\mu_n C_{ox}) \left( \frac{W}{L} \right) (v_{GS} - V_t) \right] v_{DS} \quad (5.8)$$

The conductance  $g_{DS}$  of the channel can be found from Eq. (5.7) or (5.8) as

$$g_{DS} = (\mu_n C_{ox}) \left( \frac{W}{L} \right) v_{OV} \quad (5.9)$$

or

$$g_{DS} = (\mu_n C_{ox}) \left( \frac{W}{L} \right) (v_{GS} - V_t) \quad (5.10)$$

Observe that the conductance is determined by the product of three factors:  $(\mu_n C_{ox})$ ,  $(W/L)$ , and  $v_{OV}$  (or equivalently,  $v_{GS} - V_t$ ). To gain insight into MOSFET operation, we consider each of the three factors in turn.

The first factor,  $(\mu_n C_{ox})$ , is determined by the process technology used to fabricate the MOSFET. It is the product of the electron mobility,  $\mu_n$ , and the oxide capacitance,  $C_{ox}$ . It makes physical sense for the channel conductance to be proportional to each of  $\mu_n$  and  $C_{ox}$ <sup>5</sup> (why?) and hence to their product, which is termed the **process transconductance** parameter and given the symbol  $k'_n$ , where the subscript  $n$  denotes  $n$  channel,

$$k'_n = \mu_n C_{ox} \quad (5.11)$$

It can be shown that with  $\mu_n$  having the dimensions of meters squared per volt-second ( $\text{m}^2/\text{V}\cdot\text{s}$ ) and  $C_{ox}$  having the dimensions of farads per meter squared ( $\text{F}/\text{m}^2$ ), the dimensions of  $k'_n$  are amperes per volt squared ( $\text{A}/\text{V}^2$ ).

The second factor in the expression for the conductance  $g_{DS}$  in Eqs. (5.9) and (5.10) is the transistor **aspect ratio** ( $W/L$ ). That the channel conductance is proportional to the channel width  $W$  and inversely proportional to the channel length  $L$  should make perfect physical sense. The  $(W/L)$  ratio is obviously a dimensionless quantity that is determined by the device designer. Indeed, the values of  $W$  and  $L$  can be selected by the device designer to give the device the  $i-v$  characteristics desired. For a given fabrication process, however, there is a minimum channel length,  $L_{min}$ . In fact, the minimum channel length that is possible with a given fabrication process is used to characterize the process and is being continually reduced as technology advances. For instance, in 2014 the state-of-the-art in commercially available MOS technology was a 32-nm process, meaning that for this process the minimum channel length possible was 32 nm. Finally, we should note that the oxide thickness  $t_{ox}$  scales down with  $L_{min}$ . Thus, for a 0.13-μm technology,  $t_{ox}$  is 2.7 nm, but for the currently popular 65-nm technology,  $t_{ox}$  is about 2.2 nm.

---

<sup>5</sup>This name arises from the fact that  $(\mu_n C_{ox})$  determines the transconductance of the MOSFET, as will be seen shortly.

The product of the process transconductance parameter  $k'_n$  and the transistor aspect ratio ( $W/L$ ) is the **MOSFET transconductance parameter**  $k_n$ ,

$$k_n = k'_n(W/L) \quad (5.12a)$$

or

$$k_n = (\mu_n C_{ox})(W/L) \quad (5.12b)$$

The MOSFET parameter  $k_n$  has the dimensions of  $\text{A}/\text{V}^2$ .

The third term in the expression of the channel conductance  $g_{DS}$  is the overdrive voltage  $v_{OV}$ . This is hardly surprising, since  $v_{OV}$  directly determines the magnitude of electron charge in the channel. As will be seen,  $v_{OV}$  is a very important circuit-design parameter. In this book, we will use  $v_{OV}$  and  $v_{GS} - V_t$  interchangeably.

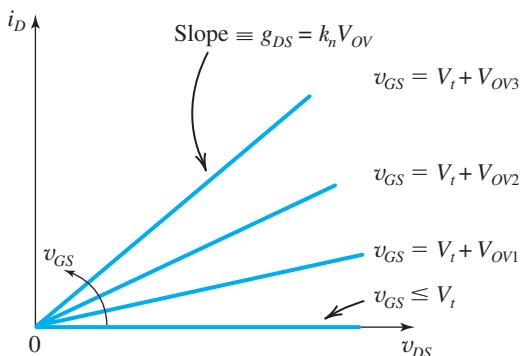
We conclude this subsection by noting that with  $v_{DS}$  kept small, the MOSFET behaves as a linear resistance  $r_{DS}$  whose value is controlled by the gate voltage  $v_{GS}$ ,

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}} \quad (5.13a)$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - V_t)} \quad (5.13b)$$

The operation of the MOSFET as a voltage-controlled resistance is further illustrated in Fig. 5.4, which is a sketch of  $i_D$  versus  $v_{DS}$  for various values of  $v_{GS}$ . Observe that the resistance is infinite for  $v_{GS} \leq V_t$  and decreases as  $v_{GS}$  is increased above  $V_t$ . It is interesting to note that although  $v_{GS}$  is used as the parameter for the set of graphs in Fig. 5.4, the graphs in fact depend only on  $v_{OV}$  (and, of course,  $k_n$ ).

The description above indicates that for the MOSFET to conduct, a channel has to be induced. Then, increasing  $v_{GS}$  above the threshold voltage  $V_t$  enhances the channel, hence the names **enhancement-mode operation** and **enhancement-type MOSFET**. Finally, we note that the current that leaves the source terminal ( $i_S$ ) is equal to the current that enters the drain terminal ( $i_D$ ), and the gate current  $i_G = 0$ .



**Figure 5.4** The  $i_D - v_{DS}$  characteristics of the MOSFET in Fig. 5.3 when the voltage applied between drain and source,  $v_{DS}$ , is kept small. The device operates as a linear resistance whose value is controlled by  $v_{GS}$ .

## EXERCISE

- 5.1** A 0.18- $\mu\text{m}$  fabrication process is specified to have  $t_{ox} = 4 \text{ nm}$ ,  $\mu_n = 450 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $V_t = 0.5 \text{ V}$ . Find the value of the process transconductance parameter  $k'_n$ . For a MOSFET with minimum length fabricated in this process, find the required value of  $W$  so that the device exhibits a channel resistance  $r_{DS}$  of 1 k $\Omega$  at  $v_{GS} = 1 \text{ V}$ .

**Ans.** 388  $\mu\text{A/V}^2$ ; 0.93  $\mu\text{m}$

### 5.1.5 Operation as $v_{DS}$ Is Increased

We next consider the situation as  $v_{DS}$  is increased. For this purpose, let  $v_{GS}$  be held constant at a value greater than  $V_t$ ; that is, let the MOSFET be operated at a constant overdrive voltage  $V_{OV}$ . Refer to Fig. 5.5, and note that  $v_{DS}$  appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source to drain, the voltage (measured relative to the source) increases from zero to  $v_{DS}$ . Thus the voltage between the gate and points along the channel decreases from  $v_{GS} = V_t + V_{OV}$  at the source end to  $v_{GD} = v_{GS} - v_{DS} = V_t + V_{OV} - v_{DS}$  at the drain end. Since the channel depth depends on this voltage, and specifically on the amount by which this voltage exceeds  $V_t$ , we find that the channel is no longer of uniform depth; rather, the channel will take the tapered shape shown in Fig. 5.5, being deepest at the source end (where the depth is proportional to  $V_{OV}$ ) and shallowest at the drain end<sup>6</sup> (where the depth is proportional to  $V_{OV} - v_{DS}$ ). This point is further illustrated in Fig. 5.6.

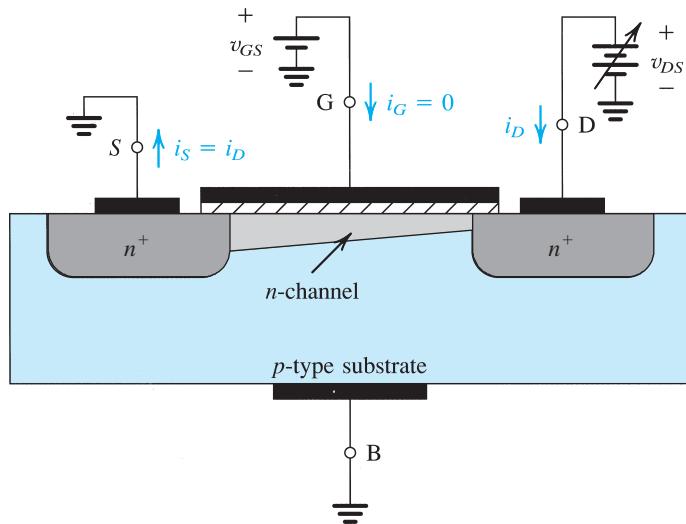
As  $v_{DS}$  is increased, the channel becomes more tapered and its resistance increases correspondingly. Thus, the  $i_D - v_{DS}$  curve does not continue as a straight line but bends as shown in Fig. 5.7. The equation describing this portion of the  $i_D - v_{DS}$  curve can be easily derived by utilizing the information in Fig. 5.6. Specifically, note that the charge in the tapered channel is proportional to the channel cross-sectional area shown in Fig. 5.6(b). This area in turn can be easily seen as proportional to  $\frac{1}{2}[V_{OV} + (V_{OV} - v_{DS})]$  or  $(V_{OV} - \frac{1}{2}v_{DS})$ . Thus, the relationship between  $i_D$  and  $v_{DS}$  can be found by replacing  $V_{OV}$  in Eq. (5.7) by  $(V_{OV} - \frac{1}{2}v_{DS})$ ,

$$i_D = k'_n \left( \frac{W}{L} \right) \left( V_{OV} - \frac{1}{2}v_{DS} \right) v_{DS} \quad (5.14)$$

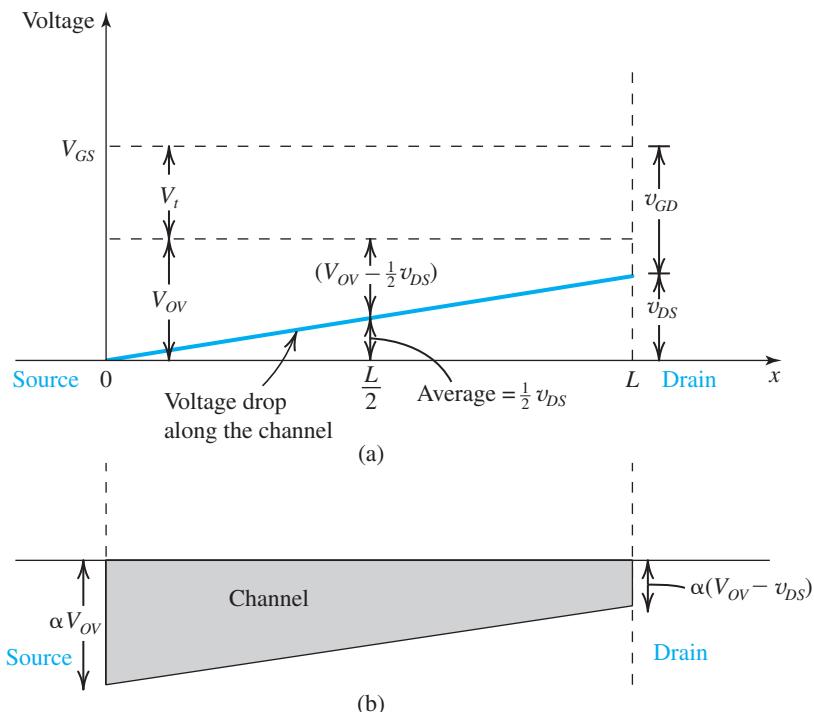
This relationship describes the semiparabolic portion of the  $i_D - v_{DS}$  curve in Fig. 5.7. It applies to the entire segment down to  $v_{DS} = 0$ . Specifically, note that as  $v_{DS}$  is reduced, we can neglect  $\frac{1}{2}v_{DS}$  relative to  $V_{OV}$  in the factor in parentheses, and the expression reduces to that in Eq. (5.7). The latter of course is an approximation and applies only for small  $v_{DS}$  (i.e., near the origin).

There is another useful interpretation of the expression in Eq. (5.14). From Fig. 5.6(a) we see that the average voltage along the channel is  $\frac{1}{2}v_{DS}$ . Thus, the average voltage that gives rise to channel charge and hence to  $i_D$  is no longer  $V_{OV}$  but  $(V_{OV} - \frac{1}{2}v_{DS})$ , which is indeed the factor that appears in Eq. (5.14). Finally, we note that Eq. (5.14) is frequently written in the

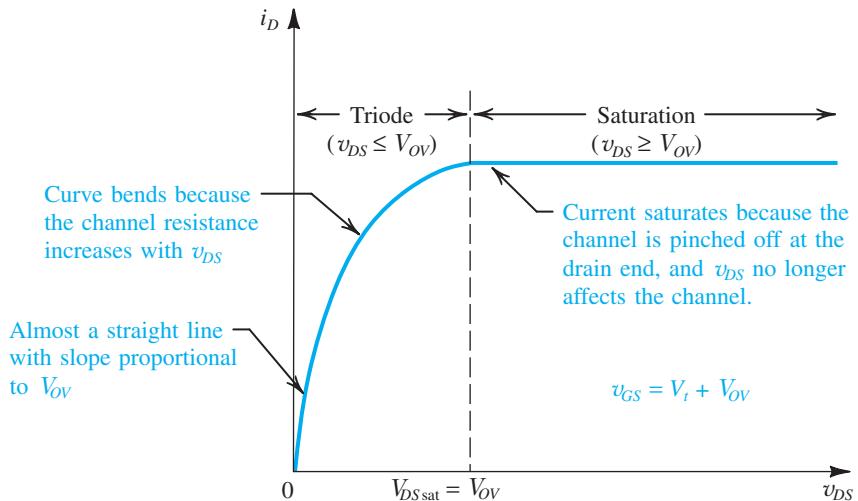
<sup>6</sup>For simplicity, we do not show in Fig. 5.5 the depletion region. Physically speaking, it is the widening of the depletion region as a result of the increased  $v_{DS}$  that makes the channel shallower near the drain.



**Figure 5.5** Operation of the enhancement NMOS transistor as  $v_{DS}$  is increased. The induced channel acquires a tapered shape, and its resistance increases as  $v_{DS}$  is increased. Here,  $v_{GS}$  is kept constant at a value  $> V_t$ ;  $v_{GS} = V_t + V_{ov}$ .



**Figure 5.6** (a) For a MOSFET with  $v_{GS} = V_t + V_{ov}$ , application of  $v_{DS}$  causes the voltage drop along the channel to vary linearly, with an average value of  $\frac{1}{2}v_{DS}$  at the midpoint. Since  $v_{GD} > V_t$ , the channel still exists at the drain end. (b) The channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to  $V_{ov}$ , that at the drain end is proportional to  $(V_{ov} - v_{DS})$ .



**Figure 5.7** The drain current  $i_D$  versus the drain-to-source voltage  $v_{DS}$  for an enhancement-type NMOS transistor operated with  $v_{GS} = V_t + V_{OV}$ .

alternate form

$$i_D = k'_n \left( \frac{W}{L} \right) \left( V_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right) \quad (5.15)$$

Furthermore, for an arbitrary value of  $V_{OV}$ , we can replace  $V_{OV}$  by  $(v_{GS} - V_t)$  and rewrite Eq. (5.15) as

➤

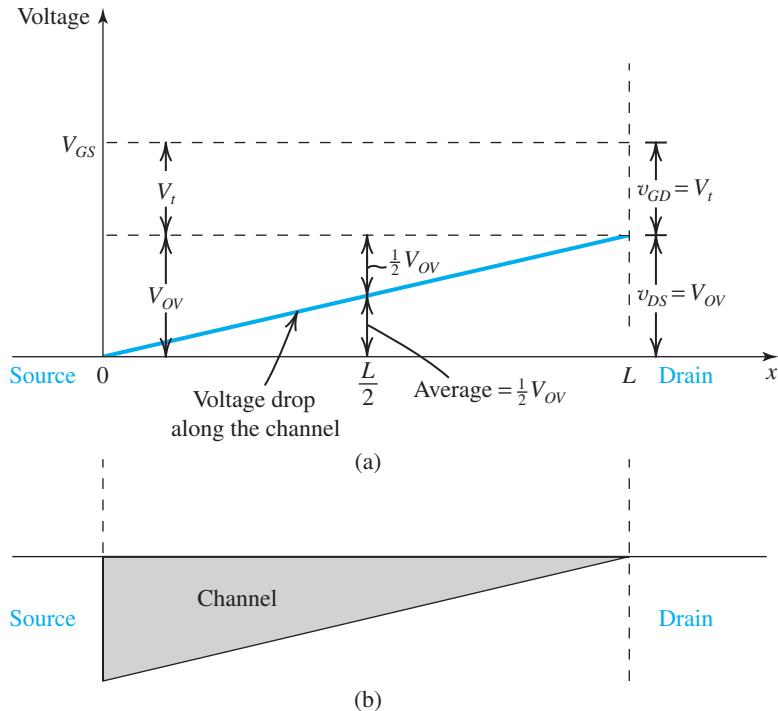
$$i_D = k'_n \left( \frac{W}{L} \right) \left[ (v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right] \quad (5.16)$$

### 5.1.6 Operation for $v_{DS} \geq V_{OV}$ : Channel Pinch-Off and Current Saturation

The above description of operation assumed that even though the channel became tapered, it still had a finite (nonzero) depth at the drain end. This in turn is achieved by keeping  $v_{DS}$  sufficiently small that the voltage between the gate and the drain,  $v_{GD}$ , exceeds  $V_t$ . This is indeed the situation shown in Fig. 5.6(a). Note that for this situation to obtain,  $v_{DS}$  must not exceed  $V_{OV}$ , for as  $v_{DS} = V_{OV}$ ,  $v_{GD} = V_t$ , and the channel depth at the drain end reduces to zero.

Figure 5.8 shows  $v_{DS}$  reaching  $V_{OV}$  and  $v_{GD}$  correspondingly reaching  $V_t$ . The zero depth of the channel at the drain end gives rise to the term **channel pinch-off**. Increasing  $v_{DS}$  beyond this value (i.e.,  $v_{DS} > V_{OV}$ ) has no effect on the channel shape and charge, and the current through the channel remains constant at the value reached for  $v_{DS} = V_{OV}$ . The drain current thus **saturates** at the value found by substituting  $v_{DS} = V_{OV}$  in Eq. (5.14),

$$i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) V_{OV}^2 \quad (5.17)$$



**Figure 5.8** Operation of MOSFET with  $v_{GS} = V_t + V_{OV}$ , as  $v_{DS}$  is increased to  $V_{OV}$ . At the drain end,  $v_{GD}$  decreases to  $V_t$  and the channel depth at the drain end reduces to zero (pinch-off). At this point, the MOSFET enters the saturation mode of operation. Further increasing  $v_{DS}$  (beyond  $V_{DS\text{sat}} = V_{OV}$ ) has no effect on the channel shape and  $i_D$  remains constant.

The MOSFET is then said to have entered the **saturation region** (or, equivalently, the saturation mode of operation). The voltage  $v_{DS}$  at which saturation occurs is denoted  $V_{DS\text{sat}}$ ,

$$V_{DS\text{sat}} = V_{OV} = V_{GS} - V_t \quad (5.18)$$

It should be noted that channel pinch-off does *not* mean channel blockage: Current continues to flow through the pinched-off channel, and the electrons that reach the drain end of the channel are accelerated through the depletion region that exists there (not shown in Fig. 5.5) and into the drain terminal. Any increase in  $v_{DS}$  above  $V_{DS\text{sat}}$  appears as a voltage drop across the depletion region. Thus, both the current through the channel and the voltage drop across it remain constant in saturation.

The saturation portion of the  $i_D - v_{DS}$  curve is, as expected, a horizontal straight line, as indicated in Fig. 5.7. Also indicated in Fig. 5.7 is the name of the region of operation obtained with a continuous (non-pinched-off) channel, the **triode region**. This name is a carryover from the days of vacuum-tube devices, whose operation a FET resembles.

Finally, we note that the expression for  $i_D$  in saturation can be generalized by replacing the constant overdrive voltage  $V_{OV}$  by a variable one,  $v_{OV}$ :

$$i_D = \frac{1}{2}k'_n \left( \frac{W}{L} \right) v_{OV}^2 \quad (5.19)$$

Also,  $v_{ov}$  can be replaced by  $(v_{gs} - V_t)$  to obtain the alternate expression for saturation-mode  $i_D$ ,

$$\rightarrow i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (v_{gs} - V_t)^2 \quad (5.20)$$

### Example 5.1

Consider a process technology for which  $L_{\min} = 0.4 \mu\text{m}$ ,  $t_{ox} = 8 \text{ nm}$ ,  $\mu_n = 450 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $V_t = 0.7 \text{ V}$ .

- Find  $C_{ox}$  and  $k'_n$ .
- For a MOSFET with  $W/L = 8 \mu\text{m}/0.8 \mu\text{m}$ , calculate the values of  $V_{ov}$ ,  $V_{gs}$ , and  $V_{ds\min}$  needed to operate the transistor in the saturation region with a dc current  $I_D = 100 \mu\text{A}$ .
- For the device in (b), find the values of  $V_{ov}$  and  $V_{gs}$  required to cause the device to operate as a  $1000\text{-}\Omega$  resistor for very small  $v_{ds}$ .

#### Solution

(a)

$$\begin{aligned} C_{ox} &= \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.32 \times 10^{-3} \text{ F/m}^2 \\ &= 4.32 \text{ fF}/\mu\text{m}^2 \\ k'_n &= \mu_n C_{ox} = 450 (\text{cm}^2/\text{V}\cdot\text{s}) \times 4.32 (\text{fF}/\mu\text{m}^2) \\ &= 450 \times 10^8 (\mu\text{m}^2/\text{V}\cdot\text{s}) \times 4.32 \times 10^{-15} (\text{F}/\mu\text{m}^2) \\ &= 194 \times 10^{-6} (\text{F}/\text{V}\cdot\text{s}) \\ &= 194 \mu\text{A/V}^2 \end{aligned}$$

(b) For operation in the saturation region,

$$i_D = \frac{1}{2} k'_n \frac{W}{L} V_{ov}^2$$

Thus,

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8} V_{ov}^2$$

which results in

$$V_{ov} = 0.32 \text{ V}$$

Thus,

$$V_{gs} = V_t + V_{ov} = 1.02 \text{ V}$$

and

$$V_{ds\min} = V_{ov} = 0.32 \text{ V}$$

(c) For the MOSFET in the triode region with  $v_{DS}$  very small,

$$r_{DS} = \frac{1}{k'_n \frac{W}{L} V_{ov}}$$

Thus

$$1000 = \frac{1}{194 \times 10^{-6} \times 10 \times V_{ov}}$$

which yields

$$V_{ov} = 0.52 \text{ V}$$

Thus,

$$V_{GS} = 1.22 \text{ V}$$

## EXERCISES

- 5.2** For a 0.18- $\mu\text{m}$  process technology for which  $t_{ox}=4 \text{ nm}$  and  $\mu_n=450 \text{ cm}^2/\text{V}\cdot\text{s}$ , find  $C_{ox}$ ,  $k'_n$ , and the overdrive voltage  $V_{ov}$  required to operate a transistor having  $W/L=20$  in saturation with  $I_D=0.3 \text{ mA}$ . What is the minimum value of  $V_{DS}$  needed?

**Ans.** 8.6 fF/ $\mu\text{m}^2$ ; 387  $\mu\text{A}/\text{V}^2$ ; 0.28 V; 0.28 V

- D5.3** A circuit designer intending to operate a MOSFET in saturation is considering the effect of changing the device dimensions and operating voltages on the drain current  $I_D$ . Specifically, by what factor does  $I_D$  change in each of the following cases?

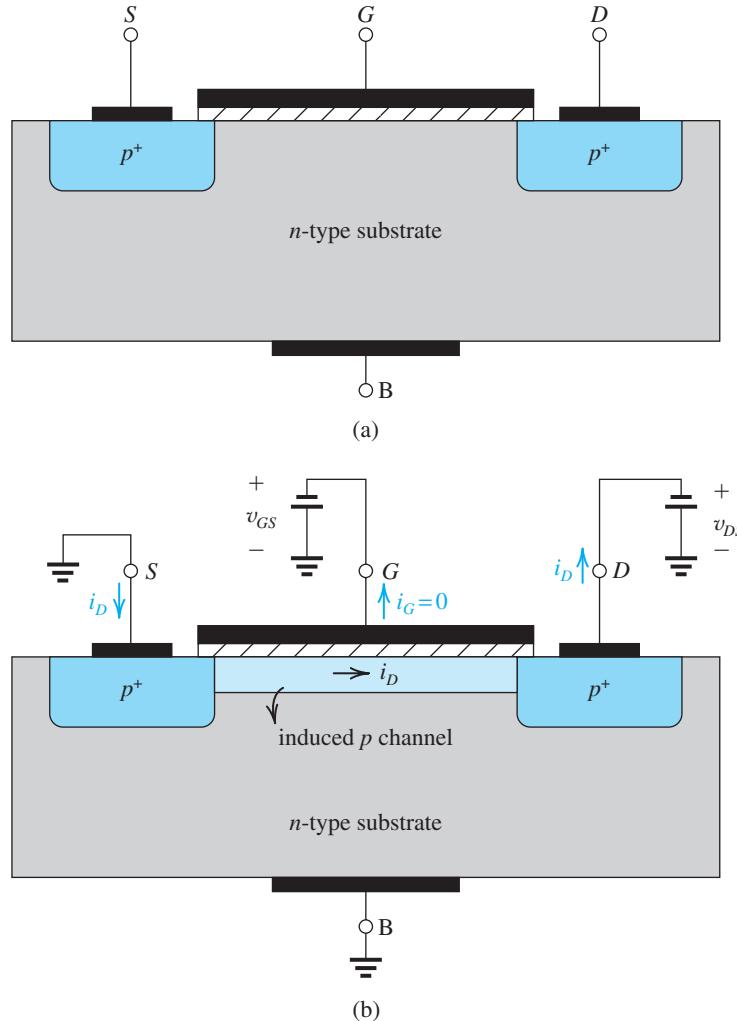
- (a) The channel length is doubled.
- (b) The channel width is doubled.
- (c) The overdrive voltage is doubled.
- (d) The drain-to-source voltage is doubled.
- (e) Changes (a), (b), (c), and (d) are made simultaneously.

Which of these cases might cause the MOSFET to leave the saturation region?

**Ans.** 0.5; 2; 4; no change; 4; case (c) if  $v_{DS}$  is smaller than  $2V_{ov}$

### 5.1.7 The p-Channel MOSFET

Figure 5.9(a) shows a cross-sectional view of a *p*-channel enhancement-type MOSFET. The structure is similar to that of the NMOS device except that here the substrate is *n* type and the source and the drain regions are *p*<sup>+</sup> type; that is, all semiconductor regions are reversed in polarity relative to their counterparts in the NMOS case. The PMOS and NMOS transistors are said to be *complementary* devices.



**Figure 5.9** (a) Physical structure of the PMOS transistor. Note that it is similar to the NMOS transistor shown in Fig. 5.1(b) except that all semiconductor regions are reversed in polarity. (b) A negative voltage  $v_{GS}$  of magnitude greater than  $|V_{tp}|$  induces a *p* channel, and a negative  $v_{DS}$  causes a current  $i_D$  to flow from source to drain.

To induce a channel for current flow between source and drain, a negative voltage is applied to the gate, that is, between gate and source, as indicated in Fig. 5.9(b). By increasing the magnitude of the negative  $v_{GS}$  beyond the magnitude of the threshold voltage  $V_{tp}$ , which by convention is negative, a *p* channel is established as shown in Fig. 5.9(b). This condition can be described as

$$v_{GS} \leq V_{tp}$$

or, to avoid dealing with negative signs,

$$|v_{GS}| \geq |V_{tp}|$$

Now, to cause a current  $i_D$  to flow in the  $p$  channel, a negative voltage  $v_{DS}$  is applied to the drain.<sup>7</sup> The current  $i_D$  is carried by holes and flows through the channel from source to drain. As we have done for the NMOS transistor, we define the process transconductance parameter for the PMOS device as

$$k'_p = \mu_p C_{ox}$$

where  $\mu_p$  is the mobility of the holes in the induced  $p$  channel. Typically,  $\mu_p = 0.25 \mu_n$  to  $0.5 \mu_n$  and is process-technology dependent. The transistor transconductance parameter  $k_p$  is obtained by multiplying  $k'_p$  by the aspect ratio  $W/L$ ,

$$k_p = k'_p (W/L)$$

The remainder of the description of the physical operation of the  $p$ -channel MOSFET follows that for the NMOS device, except of course for the sign reversals of all voltages. We will present the complete current–voltage characteristics of both NMOS and PMOS transistors in the next section.

PMOS technology originally dominated MOS integrated-circuit manufacturing, and the original microprocessors utilized PMOS transistors. As the technological difficulties of fabricating NMOS transistors were solved, NMOS completely supplanted PMOS. The main reason for this change is that electron mobility  $\mu_n$  is higher by a factor of 2 to 4 than the hole mobility  $\mu_p$ , resulting in NMOS transistors having greater gains and speeds of operation than PMOS devices. Subsequently, a technology was developed that permits the fabrication of both NMOS and PMOS transistors on the same chip. Appropriately called **complementary MOS**, or **CMOS**, this technology is currently the dominant electronics technology.

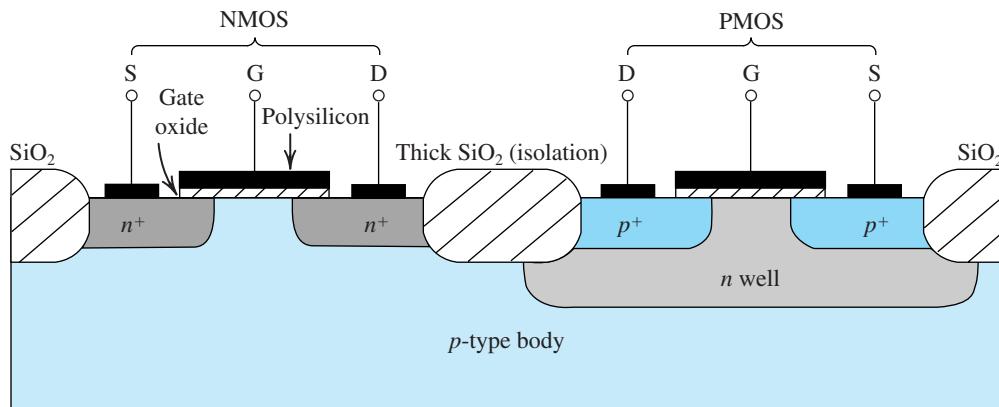
### 5.1.8 Complementary MOS or CMOS

As the name implies, complementary MOS technology employs MOS transistors of both polarities. Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit configurations. Indeed, at the present time CMOS is the most widely used of all the IC technologies. This statement applies to both analog and digital circuits. CMOS technology has virtually replaced designs based on NMOS transistors alone. Furthermore, by 2014 CMOS technology had taken over many applications that just a few years earlier were possible only with bipolar devices. Throughout this book, we will study many CMOS circuit techniques.

Figure 5.10 shows a cross section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Observe that while the NMOS transistor is implemented directly in the  $p$ -type substrate, the PMOS transistor is fabricated in a specially created  $n$  region, known as an  **$n$  well**. The two devices are isolated from each other by a thick region of oxide that functions as an insulator. Not shown on the diagram are the connections made to the  $p$ -type body and to the  $n$  well. The latter connection serves as the body terminal for the PMOS transistor.

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<sup>7</sup>If a positive voltage is applied to the drain, the  $pn$  junction between the drain region and the substrate will become forward biased, and the device will no longer operate as a MOSFET. Proper MOSFET operation is predicated on the  $pn$  junctions between the source and drain regions and the substrate being always reverse biased.



**Figure 5.10** Cross section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate  $n$ -type region, known as an  $n$  well. Another arrangement is also possible in which an  $n$ -type substrate (body) is used and the  $n$  device is formed in a  $p$  well. Not shown are the connections made to the  $p$ -type body and to the  $n$  well; the latter functions as the body terminal for the  $p$ -channel device.

### 5.1.9 Operating the MOS Transistor in the Subthreshold Region

The above description of the  $n$ -channel MOSFET operation implies that for  $v_{GS} < V_t$ , no current flows and the device is cut off. This is not entirely true, for it has been found that for values of  $v_{GS}$  smaller than but close to  $V_t$ , a small drain current flows. In this **subthreshold region** of operation, the drain current is exponentially related to  $v_{GS}$ , much like the  $i_C - v_{BE}$  relationship of a BJT, as will be shown in the next chapter.

Although in most applications the MOS transistor is operated with  $v_{GS} > V_t$ , there are special, but a growing number of, applications that make use of subthreshold operation. In Chapter 14, we will briefly consider subthreshold operation.

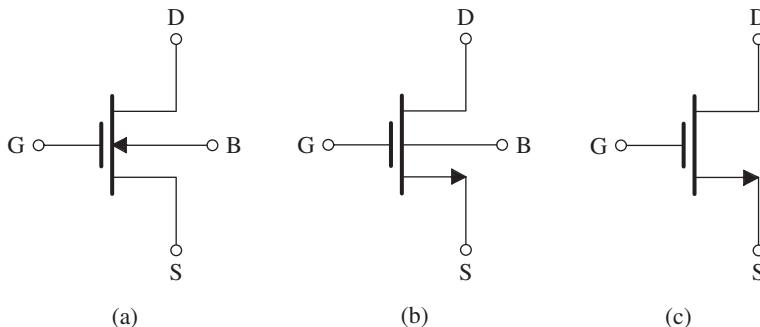
## 5.2 Current–Voltage Characteristics

Building on the physical foundation established in the previous section for the operation of the enhancement MOS transistor, in this section we present its complete current–voltage characteristics. These characteristics can be measured at dc or at low frequencies and thus are called static characteristics. The dynamic effects that limit the operation of the MOSFET at high frequencies and high switching speeds will be discussed in Chapter 10.

### 5.2.1 Circuit Symbol

Figure 5.11(a) shows the circuit symbol for the  $n$ -channel enhancement-type MOSFET. Observe that the spacing between the two vertical lines that represent the gate and the channel indicates the fact that the gate electrode is insulated from the body of the device. The polarity of the  $p$ -type substrate (body) and the  $n$  channel is indicated by the arrowhead on the line representing the body (B). This arrowhead also indicates the polarity of the transistor, namely, that it is an  $n$ -channel device.

Although the MOSFET is a symmetrical device, it is often useful in circuit design to designate one terminal as the source and the other as the drain (without having to write S and



**Figure 5.11** (a) Circuit symbol for the *n*-channel enhancement-type MOSFET. (b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). (c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

D beside the terminals). This objective is achieved in the modified circuit symbol shown in Fig. 5.11(b). Here an arrowhead is placed on the source terminal, thus distinguishing it from the drain terminal. The arrowhead points in the normal direction of current flow and thus indicates the polarity of the device (i.e., *n* channel). Observe that in the modified symbol, there is no need to show the arrowhead on the body line. Although the circuit symbol of Fig. 5.11(b) clearly distinguishes the source from the drain, in practice it is the polarity of the voltage impressed across the device that determines source and drain; *the drain is always positive relative to the source in an n-channel FET*.

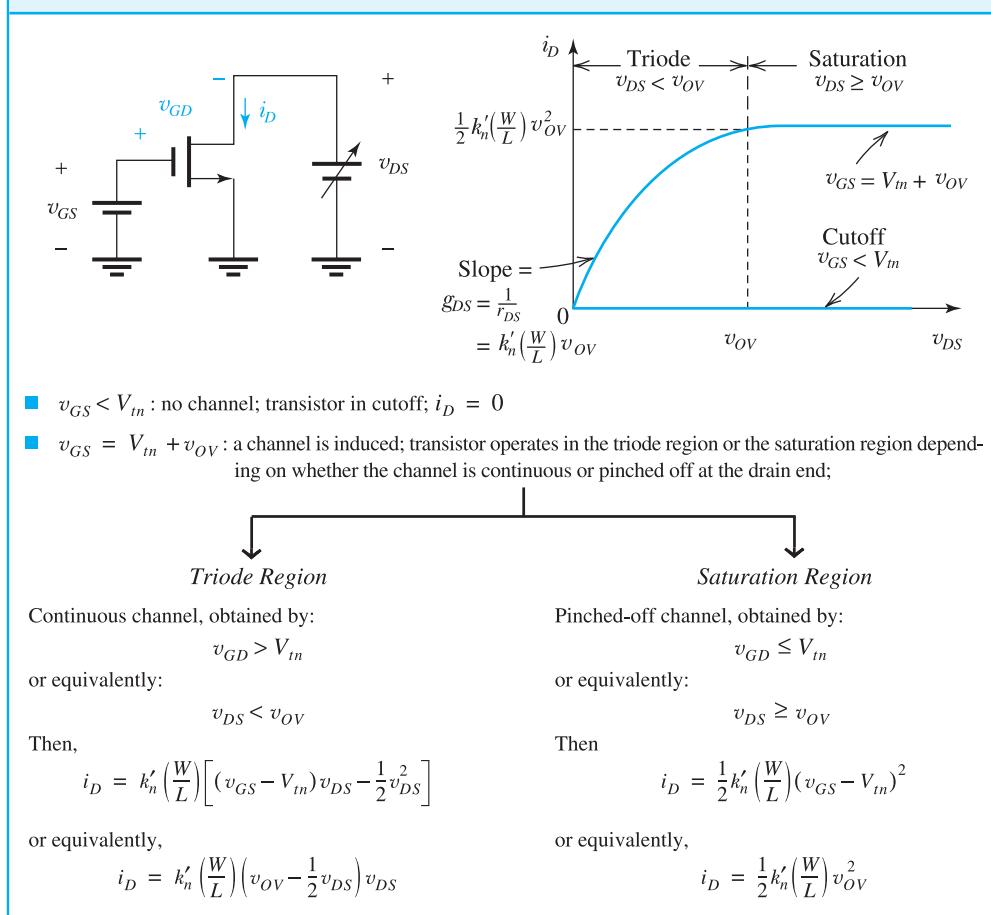
In applications where the source is connected to the body of the device, a further simplification of the circuit symbol is possible, as indicated in Fig. 5.11(c). This symbol is also used in applications when the effect of the body on circuit operation is not important, as will be seen later.

## 5.2.2 The $i_D-v_{DS}$ Characteristics

Table 5.1 provides a compilation of the conditions and the formulas for the operation of the NMOS transistor in each of the three possible regions: the cutoff region, the triode region, and the saturation region. The first two are useful if the MOSFET is to be utilized as a switch. On the other hand, if the MOSFET is to be used to design an amplifier, it must be operated in the saturation region. The rationale for these choices will be addressed in Chapter 7.

At the top of Table 5.1 we show a circuit consisting of an NMOS transistor and two dc supplies providing  $v_{GS}$  and  $v_{DS}$ . This conceptual circuit can be used to measure the  $i_D-v_{DS}$  characteristic curves of the NMOS transistor. Each curve is measured by setting  $v_{GS}$  to a desired constant value, varying  $v_{DS}$ , and measuring the corresponding  $i_D$ . Two of these characteristic curves are shown in the accompanying diagram: one for  $v_{GS} < V_m$  and the other for  $v_{GS} = V_m + v_{OV}$ . (Note that we now use  $V_m$  to denote the threshold voltage of the NMOS transistor, to distinguish it from that of the PMOS transistor, denoted  $V_{tp}$ .)

As Table 5.1 shows, the boundary between the triode region and the saturation region is determined by whether  $v_{DS}$  is less or greater than the overdrive voltage  $v_{OV}$  at which the transistor is operating. An equivalent way to check for the region of operation is to examine the relative values of the drain and gate voltages. To operate in the triode region, the gate voltage must exceed the drain voltage by at least  $V_m$  volts, which ensures that the channel remains continuous (not pinched off). On the other hand, to operate in saturation, the channel must be

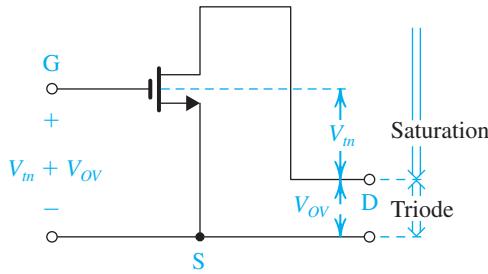
**Table 5.1** Regions of Operation of the Enhancement NMOS Transistor

pinched off at the drain end; pinch-off is achieved here by keeping  $v_D$  higher than  $v_G - V_m$ , that is, not allowing  $v_D$  to fall below  $v_G$  by more than  $V_m$  volts. The graphical construction of Fig. 5.12 should serve to remind the reader of these conditions.

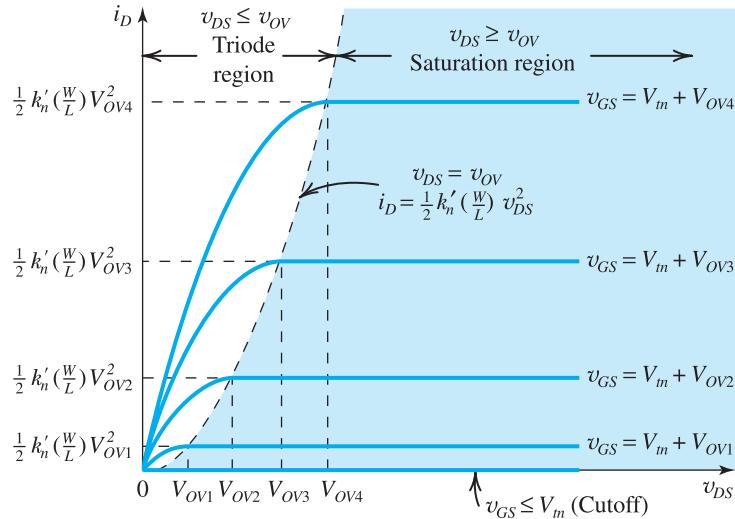
A set of  $i_D - v_{DS}$  characteristics for the NMOS transistor is shown in Fig. 5.13. Observe that each graph is obtained by setting  $v_{GS}$  above  $V_m$  by a specific value of overdrive voltage, denoted  $V_{OV1}$ ,  $V_{OV2}$ ,  $V_{OV3}$ , and  $V_{OV4}$ . This in turn is the value of  $v_{DS}$  at which the corresponding graph saturates, and the value of the resulting saturation current is directly determined by the value of  $v_{OV}$ , namely,  $\frac{1}{2} k_n V_{OV1}^2$ ,  $\frac{1}{2} k_n V_{OV2}^2$ , ... The reader is advised to commit to memory both the structure of these graphs and the coordinates of the saturation points.

Finally, observe that the boundary between the triode and the saturation regions, that is, the locus of the saturation points, is a parabolic curve described by

$$i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) v_{DS}^2$$



**Figure 5.12** The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.



**Figure 5.13** The  $i_D - v_{DS}$  characteristics for an enhancement-type NMOS transistor.

### 5.2.3 The $i_D - v_{GS}$ Characteristic

When the MOSFET is used to design an amplifier, it is operated in the saturation region. As Fig. 5.13 indicates, in saturation the drain current is constant determined by  $v_{GS}$  (or  $v_{OV}$ ) and is independent of  $v_{DS}$ . That is, the MOSFET operates as a constant-current source where the value of the current is determined by  $v_{GS}$ . In effect, then, the MOSFET operates as a voltage-controlled current source with the control relationship described by

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) (v_{GS} - V_m)^2 \quad (5.21)$$

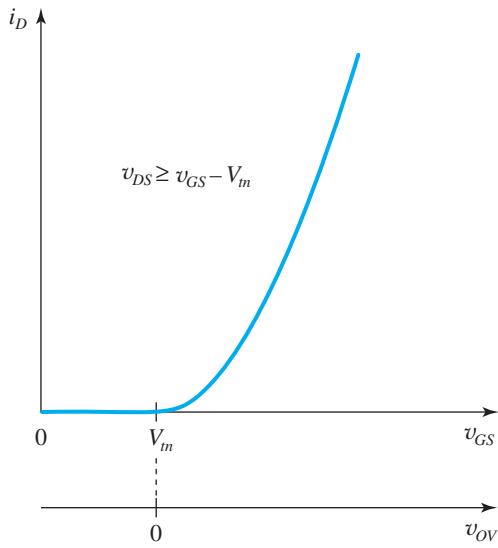
or in terms of  $v_{OV}$ ,

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) v_{OV}^2 \quad (5.22)$$

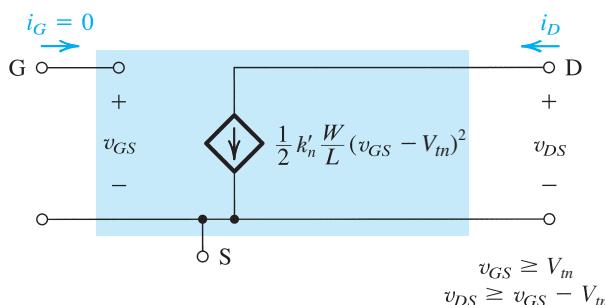
This is the relationship that underlies the application of the MOSFET as an amplifier. That it is nonlinear should be of concern to those interested in designing linear amplifiers. Nevertheless, in Chapter 7, we will see how one can obtain linear amplification from this nonlinear control or transfer characteristic.

Figure 5.14 shows the  $i_D - v_{GS}$  characteristic of an NMOS transistor operating in saturation. Note that if we are interested in a plot of  $i_D$  versus  $v_{OV}$ , we simply shift the origin to the point  $v_{GS} = V_m$ .

The view of the MOSFET in the saturation region as a voltage-controlled current source is illustrated by the equivalent-circuit representation shown in Fig. 5.15. For reasons that will become apparent shortly, the circuit in Fig. 5.15 is known as a **large-signal equivalent circuit**. Note that the current source is ideal, with an infinite output resistance representing the independence, in saturation, of  $i_D$  from  $v_{DS}$ . This, of course, has been assumed in the idealized model of device operation utilized thus far. We are about to rectify an important shortcoming of this model. First, however, we present an example.



**Figure 5.14** The  $i_D - v_{GS}$  characteristic of an NMOS transistor operating in the saturation region. The  $i_D - v_{OV}$  characteristic can be obtained by simply relabeling the horizontal axis, that is, shifting the origin to the point  $v_{GS} = V_m$ .



**Figure 5.15** Large-signal, equivalent-circuit model of an *n*-channel MOSFET operating in the saturation region.

### Example 5.2

Consider an NMOS transistor fabricated in a 0.18- $\mu\text{m}$  process with  $L = 0.18 \mu\text{m}$  and  $W = 2 \mu\text{m}$ . The process technology is specified to have  $C_{ox} = 8.6 \text{ fF}/\mu\text{m}^2$ ,  $\mu_n = 450 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $V_m = 0.5 \text{ V}$ .

- (a) Find  $V_{GS}$  and  $V_{DS}$  that result in the MOSFET operating at the edge of saturation with  $I_D = 100 \mu\text{A}$ .
- (b) If  $V_{GS}$  is kept constant, find  $V_{DS}$  that results in  $I_D = 50 \mu\text{A}$ .
- (c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with  $V_{DS} = 0.3 \text{ V}$ . Find the change in  $i_D$  resulting from  $v_{GS}$  changing from 0.7 V by +0.01 V and by -0.01 V.

#### Solution

First we determine the process transconductance parameter  $k'_n$ ,

$$\begin{aligned} k'_n &= \mu_n C_{ox} \\ &= 450 \times 10^{-4} \times 8.6 \times 10^{-15} \times 10^{12} \text{ A/V}^2 \\ &= 387 \mu\text{A/V}^2 \end{aligned}$$

and the transistor transconductance parameter  $k_n$ ,

$$\begin{aligned} k_n &= k'_n \left( \frac{W}{L} \right) \\ &= 387 \left( \frac{2}{0.18} \right) = 4.3 \text{ mA/V}^2 \end{aligned}$$

(a) With the transistor operating in saturation,

$$I_D = \frac{1}{2} k_n V_{ov}^2$$

Thus,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{ov}^2$$

which results in

$$V_{ov} = 0.22 \text{ V}$$

Thus,

$$V_{GS} = V_m + V_{ov} = 0.5 + 0.22 = 0.72 \text{ V}$$

and since operation is at the edge of saturation,

$$V_{DS} = V_{ov} = 0.22 \text{ V}$$

**Example 5.2** *continued*

(b) With  $V_{GS}$  kept constant at 0.72 V and  $I_D$  reduced from the value obtained at the edge of saturation, the MOSFET will now be operating in the triode region, thus

$$\begin{aligned} I_D &= k_n \left[ V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ 50 &= 4.3 \times 10^3 \left[ 0.22 V_{DS} - \frac{1}{2} V_{DS}^2 \right] \end{aligned}$$

which can be rearranged to the form

$$V_{DS}^2 - 0.44 V_{DS} + 0.023 = 0$$

This quadratic equation has two solutions

$$V_{DS} = 0.06 \text{ V} \quad \text{and} \quad V_{DS} = 0.39 \text{ V}$$

The second answer is greater than  $V_{OV}$  and thus is physically meaningless, since we know that the transistor is operating in the triode region. Thus we have

$$V_{DS} = 0.06 \text{ V}$$

(c) For  $v_{GS} = 0.7 \text{ V}$ ,  $V_{OV} = 0.2 \text{ V}$ , and since  $V_{DS} = 0.3 \text{ V}$ , the transistor is operating in saturation and

$$\begin{aligned} I_D &= \frac{1}{2} k_n V_{OV}^2 \\ &= \frac{1}{2} \times 4300 \times 0.04 \\ &= 86 \mu\text{A} \end{aligned}$$

Now for  $v_{GS} = 0.710 \text{ V}$ ,  $v_{OV} = 0.21 \text{ V}$  and

$$i_D = \frac{1}{2} \times 4300 \times 0.21^2 = 94.8 \mu\text{A}$$

and for  $v_{GS} = 0.690 \text{ V}$ ,  $v_{OV} = 0.19 \text{ V}$ , and

$$i_D = \frac{1}{2} \times 4300 \times 0.19^2 = 77.6 \mu\text{A}$$

Thus, with  $\Delta v_{GS} = +0.01 \text{ V}$ ,  $\Delta i_D = 8.8 \mu\text{A}$ ; and for  $\Delta v_{GS} = -0.01 \text{ V}$ ,  $\Delta i_D = -8.4 \mu\text{A}$ .

We conclude that the two changes are almost equal, an indication of almost-linear operation when the changes in  $v_{GS}$  are kept small. This is just a preview of the “small-signal operation” of the MOSFET studied in Chapter 7.

## EXERCISES

- 5.4** An NMOS transistor is operating at the edge of saturation with an overdrive voltage  $V_{OV}$  and a drain current  $I_D$ . If  $V_{OV}$  is doubled, and we must maintain operation at the edge of saturation, what should  $V_{DS}$  be changed to? What value of drain current results?

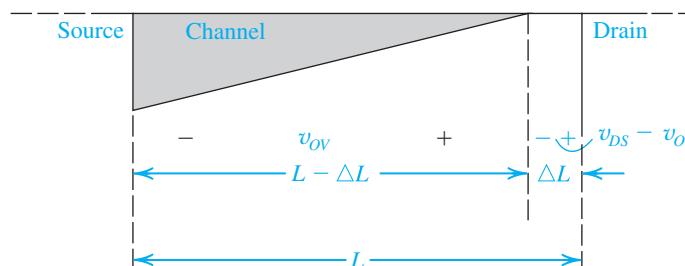
**Ans.**  $2V_{OV}; 4I_D$

- 5.5** An *n*-channel MOSFET operating with  $V_{OV} = 0.5$  V exhibits a linear resistance  $r_{DS} = 1$  k $\Omega$  when  $v_{DS}$  is very small. What is the value of the device transconductance parameter  $k_n$ ? What is the value of the current  $I_D$  obtained when  $v_{DS}$  is increased to 0.5 V? and to 1 V?

**Ans.**  $2 \text{ mA/V}^2; 0.25 \text{ mA}; 0.25 \text{ mA}$

### 5.2.4 Finite Output Resistance in Saturation

Equation (5.21) and the corresponding large-signal equivalent circuit in Fig. 5.15, as well as the graphs in Fig. 5.13, indicate that in saturation,  $i_D$  is independent of  $v_{DS}$ . Thus, a change  $\Delta v_{DS}$  in the drain-to-source voltage causes a zero change in  $i_D$ , which implies that the incremental resistance looking into the drain of a saturated MOSFET is infinite. This, however, is an idealization based on the premise that once the channel is pinched off at the drain end, further increases in  $v_{DS}$  have no effect on the channel's shape. But, in practice, increasing  $v_{DS}$  beyond  $v_{OV}$  does affect the channel somewhat. Specifically, as  $v_{DS}$  is increased, the channel pinch-off point is moved slightly away from the drain, toward the source. This is illustrated in Fig. 5.16, from which we note that the voltage across the channel remains constant at  $v_{OV}$ , and the additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain. Note, however, that (with depletion-layer widening) the channel length is in effect reduced, from  $L$  to  $L - \Delta L$ , a phenomenon known as **channel-length modulation**. Now, since  $i_D$  is inversely proportional to the channel length (Eq. 5.21),  $i_D$  increases with  $v_{DS}$ .



**Figure 5.16** Increasing  $v_{DS}$  beyond  $v_{DSsat}$  causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by  $\Delta L$ ).

This effect can be accounted for in the expression for  $i_D$  by including a factor  $1 + \lambda(v_{DS} - v_{OV})$  or, for simplicity,  $(1 + \lambda v_{DS})$ ,

$$\rightarrow i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (v_{GS} - V_m)^2 (1 + \lambda v_{DS}) \quad (5.23)$$

Here  $\lambda$  is a device parameter having the units of reciprocal volts ( $V^{-1}$ ). The value of  $\lambda$  depends both on the process technology used to fabricate the device and on the channel length  $L$  that the circuit designer selects. Specifically, the value of  $\lambda$  is much larger for newer submicron technologies than for older technologies. This makes intuitive sense: Newer technologies have very short channels, and are thus much more greatly impacted by the channel-length modulation effect. Also, for a given process technology,  $\lambda$  is inversely proportional to  $L$ .

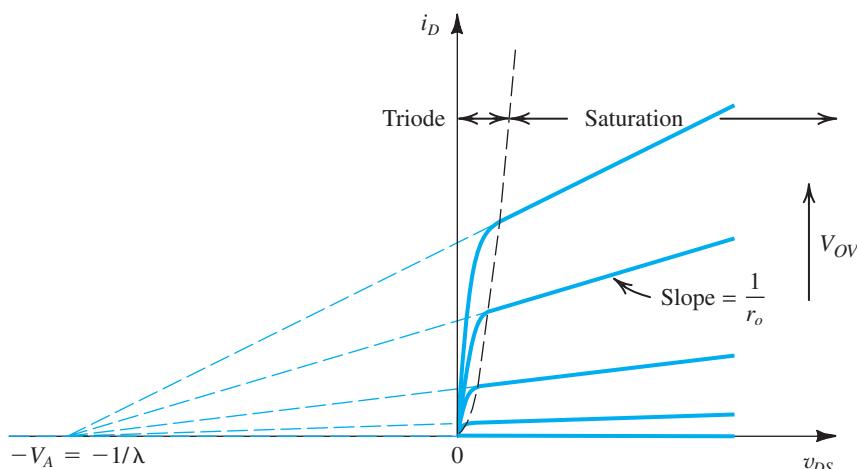
A typical set of  $i_D-v_{DS}$  characteristics showing the effect of channel-length modulation is displayed in Fig. 5.17. The observed linear dependence of  $i_D$  on  $v_{DS}$  in the saturation region is represented in Eq. (5.23) by the factor  $(1 + \lambda v_{DS})$ . From Fig. 5.17 we observe that when the straight-line  $i_D-v_{DS}$  characteristics are extrapolated, they intercept the  $v_{DS}$  axis at the point,  $v_{DS} = -V_A$ , where  $V_A$  is a positive voltage. Equation (5.23), however, indicates that  $i_D = 0$  at  $v_{DS} = -1/\lambda$ . It follows that

$$\rightarrow V_A = \frac{1}{\lambda}$$

and thus  $V_A$  is a device parameter with the dimensions of V. For a given process,  $V_A$  is proportional to the channel length  $L$  that the designer selects for a MOSFET. We can isolate the dependence of  $V_A$  on  $L$  by expressing it as

$$\rightarrow V_A = V'_A L$$

where  $V'_A$  is entirely process-technology dependent, with the dimensions of volts per micron. Typically,  $V'_A$  falls in the range of 5 V/ $\mu$ m to 50 V/ $\mu$ m. The voltage  $V_A$  is usually referred to as the Early voltage, after J. M. Early, who discovered a similar phenomenon for the BJT (Chapter 6).



**Figure 5.17** Effect of  $v_{DS}$  on  $i_D$  in the saturation region. The MOSFET parameter  $V_A$  depends on the process technology and, for a given process, is proportional to the channel length  $L$ .

Equation (5.23) indicates that when channel-length modulation is taken into account, the saturation values of  $i_D$  depend on  $v_{DS}$ . Thus, for a given  $v_{GS}$ , a change  $\Delta v_{DS}$  yields a corresponding change  $\Delta i_D$  in the drain current  $i_D$ . It follows that the output resistance of the current source representing  $i_D$  in saturation is no longer infinite. Defining the output resistance  $r_o$  as<sup>8</sup>

$$r_o \equiv \left[ \frac{\partial i_D}{\partial v_{DS}} \right]_{v_{GS} \text{ constant}}^{-1} \quad (5.24)$$

and using Eq. (5.23) results in

$$r_o = \left[ \lambda \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_m)^2 \right]^{-1} \quad (5.25)$$

which can be written as

$$r_o = \frac{1}{\lambda I_D} \quad (5.26)$$

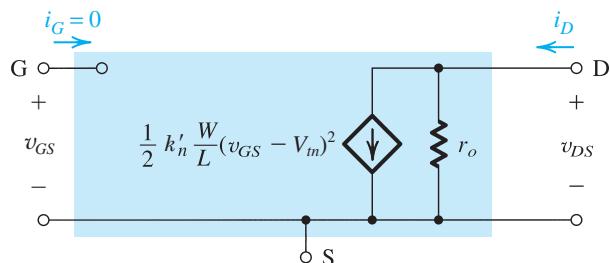
or, equivalently,

$$r_o = \frac{V_A}{I'_D} \quad (5.27) \quad \leftarrow$$

where  $I'_D$  is the drain current *without* channel-length modulation taken into account; that is,

$$I'_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_m)^2 \quad (5.27')$$

Thus the output resistance is inversely proportional to the drain current.<sup>9</sup> Finally, we show in Fig. 5.18 the large-signal, equivalent-circuit model incorporating  $r_o$ .



**Figure 5.18** Large-signal, equivalent-circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance  $r_o$ . The output resistance models the linear dependence of  $i_D$  on  $v_{DS}$  and is given by Eq. (5.27).

<sup>8</sup>In this book we use  $r_o$  to denote the output resistance in saturation, and  $r_{DS}$  to denote the drain-to-source resistance in the triode region, for small  $v_{DS}$ .

<sup>9</sup>In applying Eq. (5.27) we will usually drop the prime on  $I_D$  and simply use  $r_o = V_A/I_D$  where  $I_D$  is the drain current without channel-length modulation.

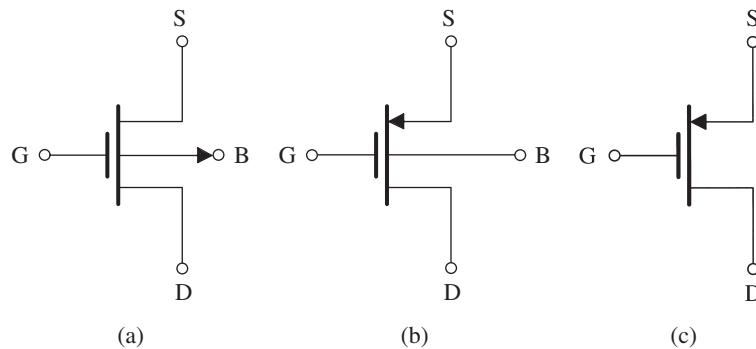
## EXERCISE

- 5.6** An NMOS transistor is fabricated in a  $0.4\text{-}\mu\text{m}$  process having  $\mu_n C_{ox} = 200 \mu\text{A/V}^2$  and  $V'_A = 50 \text{ V}/\mu\text{m}$  of channel length. If  $L = 0.8 \mu\text{m}$  and  $W = 16 \mu\text{m}$ , find  $V_A$  and  $\lambda$ . Find the value of  $I_D$  that results when the device is operated with an overdrive voltage  $V_{ov} = 0.5 \text{ V}$  and  $V_{DS} = 1 \text{ V}$ . Also, find the value of  $r_o$  at this operating point. If  $V_{DS}$  is increased by 2 V, what is the corresponding change in  $I_D$ ?

**Ans.** 40 V;  $0.025 \text{ V}^{-1}$ ; 0.51 mA;  $80 \text{ k}\Omega$ ; 0.025 mA

### 5.2.5 Characteristics of the *p*-Channel MOSFET

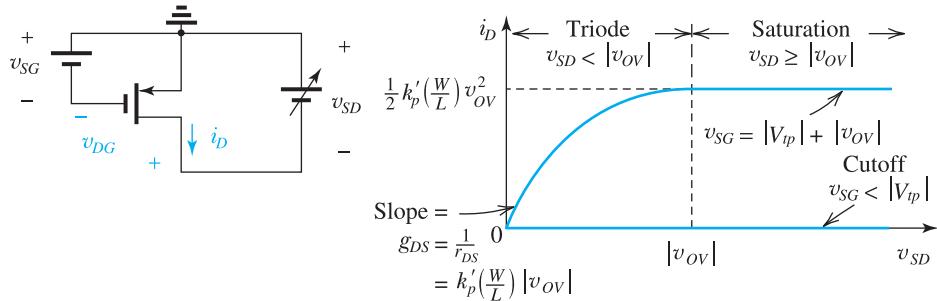
The circuit symbol for the *p*-channel enhancement-type MOSFET is shown in Fig. 5.19(a). Figure 5.19(b) shows a modified circuit symbol in which an arrowhead pointing in the normal direction of current flow is included on the source terminal. For the case where the source is connected to the substrate, the simplified symbol of Fig. 5.19(c) is usually used.



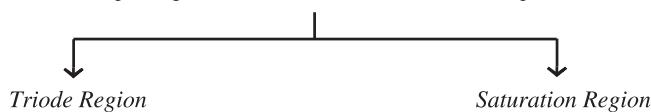
**Figure 5.19** (a) Circuit symbol for the *p*-channel enhancement-type MOSFET. (b) Modified symbol with an arrowhead on the source lead. (c) Simplified circuit symbol for the case where the source is connected to the body.

The regions of operation of the PMOS transistor and the corresponding conditions and expression for  $i_D$  are shown in Table 5.2. Observe that the equations are written in a way that emphasizes physical intuition and avoids the confusion of negative signs. Thus while  $V_{tp}$  is by convention negative, we use  $|V_{tp}|$ , and the voltages  $v_{SG}$  and  $v_{SD}$  are positive. Also, in all of our circuit diagrams we will always draw *p*-channel devices with their sources on top so that current flows from top to bottom. Finally, we note that PMOS devices also suffer from the channel-length modulation effect. This can be taken into account by including a factor  $(1 + |\lambda|v_{SD})$  in the saturation-region expression for  $i_D$  as follows

$$i_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) (v_{SG} - |V_{tp}|)^2 (1 + |\lambda|v_{SD}) \quad (5.28)$$

**Table 5.2** Regions of Operation of the Enhancement PMOS Transistor

- \$v\_{SG} < |V\_{tp}|\$: no channel; transistor in cutoff; \$i\_D = 0\$
- \$v\_{SG} = |V\_{tp}| + |v\_{OV}|\$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;



Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently

$$v_{SD} < |v_{OV}|$$

Then

$$i_D = k'_p \left( \frac{W}{L} \right) \left[ (v_{SG} - |V_{tp}|) v_{SD} - \frac{1}{2} v_{SD}^2 \right]$$

or equivalently

$$i_D = k'_p \left( \frac{W}{L} \right) \left( |v_{OV}| - \frac{1}{2} v_{SD} \right) v_{SD}$$

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

Then

$$i_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) (v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) v_{OV}^2$$

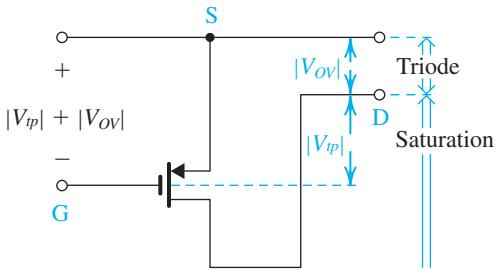
or equivalently

$$i_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) (v_{SG} - |V_{tp}|)^2 \left( 1 + \frac{v_{SD}}{|V_A|} \right) \quad (5.29)$$

where \$\lambda\$ and \$V\_A\$ (the Early voltage for the PMOS transistor) are by convention negative quantities, hence we use \$|\lambda|\$ and \$|V\_A|\$.

Finally, we should note that for a given CMOS fabrication process \$\lambda\_n\$ and \$|\lambda\_p|\$ are generally not equal, and similarly for \$V\_{An}\$ and \$|V\_{Ap}|\$.

To recap, to turn a PMOS transistor on, the gate voltage has to be made lower than that of the source by at least \$|V\_{tp}|\$. To operate in the triode region, the drain voltage has to exceed that of the gate by at least \$|V\_{tp}|\$; otherwise, the PMOS operates in saturation. Finally, Fig. 5.20 provides a pictorial representation of these operating conditions.

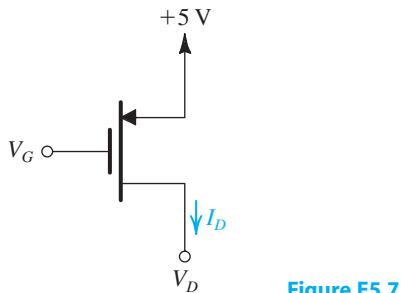


**Figure 5.20** The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

### EXERCISE

- 5.7 The PMOS transistor shown in Fig. E5.7 has  $V_{tp} = -1$  V,  $k'_p = 60 \mu\text{A/V}^2$ , and  $W/L = 10$ .

- Find the range of  $V_G$  for which the transistor conducts.
- In terms of  $V_G$ , find the range of  $V_D$  for which the transistor operates in the triode region.
- In terms of  $V_G$ , find the range of  $V_D$  for which the transistor operates in saturation.
- Neglecting channel-length modulation (i.e., assuming  $\lambda = 0$ ), find the values of  $|V_{ov}|$  and  $V_G$  and the corresponding range of  $V_D$  to operate the transistor in the saturation mode with  $I_D = 75 \mu\text{A}$ .
- If  $\lambda = -0.02 \text{ V}^{-1}$ , find the value of  $r_o$  corresponding to the overdrive voltage determined in (d).
- For  $\lambda = -0.02 \text{ V}^{-1}$  and for the value of  $V_{ov}$  determined in (d), find  $I_D$  at  $V_D = +3$  V and at  $V_D = 0$  V; hence, calculate the value of the apparent output resistance in saturation. Compare to the value found in (e).



**Figure E5.7**

**Ans.** (a)  $V_G \leq +4$  V; (b)  $V_D \geq V_G + 1$ ; (c)  $V_D \leq V_G + 1$ ; (d) 0.5 V, 3.5 V,  $\leq 4.5$  V; (e)  $0.67 \text{ M}\Omega$ ; (f) 78  $\mu\text{A}$ , 82.5  $\mu\text{A}$ , 0.67  $\text{M}\Omega$  (same)

## 5.3 MOSFET Circuits at DC

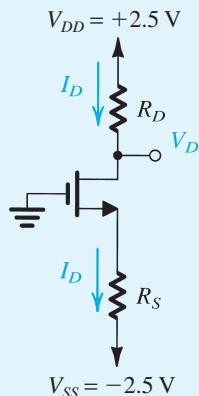
Having studied the current-voltage characteristics of MOSFETs, we now consider circuits in which only dc voltages and currents are of concern. Specifically, we shall present a series of design and analysis examples of MOSFET circuits at dc. The objective is to instill in the

reader a familiarity with the device and the ability to perform MOSFET circuit analysis both rapidly and effectively.

In the following examples, to keep matters simple and thus focus attention on the essence of MOSFET circuit operation, we will generally neglect channel-length modulation; that is, we will assume  $\lambda = 0$ . We will find it convenient to work in terms of the overdrive voltage;  $V_{ov} = V_{GS} - V_m$  for NMOS and  $|V_{ov}| = V_{SG} - |V_{tp}|$  for PMOS.

### Example 5.3

Design the circuit of Fig. 5.21: that is, determine the values of  $R_D$  and  $R_S$  so that the transistor operates at  $I_D = 0.4$  mA and  $V_D = +0.5$  V. The NMOS transistor has  $V_t = 0.7$  V,  $\mu_n C_{ox} = 100 \mu\text{A/V}^2$ ,  $L = 1 \mu\text{m}$ , and  $W = 32 \mu\text{m}$ . Neglect the channel-length modulation effect (i.e., assume that  $\lambda = 0$ ).



**Figure 5.21** Circuit for Example 5.3.

### Solution

To establish a dc voltage of +0.5 V at the drain, we must select  $R_D$  as follows:

$$\begin{aligned} R_D &= \frac{V_{DD} - V_D}{I_D} \\ &= \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega \end{aligned}$$

To determine the value required for  $R_S$ , we need to know the voltage at the source, which can be easily found if we know  $V_{GS}$ . This in turn can be determined from  $V_{ov}$ . Toward that end, we note that since  $V_D = 0.5$  V is greater than  $V_G$ , the NMOS transistor is operating in the saturation region, and we can use the saturation-region expression of  $i_D$  to determine the required value of  $V_{ov}$ ,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2$$

Then substituting  $I_D = 0.4$  mA = 400  $\mu\text{A}$ ,  $\mu_n C_{ox} = 100 \mu\text{A/V}^2$ , and  $W/L = 32/1$  gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{ov}^2$$

**Example 5.3** *continued*

which results in

$$V_{ov} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{ov} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 5.21, we note that the gate is at ground potential. Thus, the source must be at  $-1.2 \text{ V}$ , and the required value of  $R_s$  can be determined from

$$\begin{aligned} R_s &= \frac{V_s - V_{ss}}{I_D} \\ &= \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega \end{aligned}$$

**EXERCISE**

- D5.8** Redesign the circuit of Fig. 5.21 for the following case:  $V_{DD} = -V_{SS} = 2.5 \text{ V}$ ,  $V_t = 1 \text{ V}$ ,  $\mu_n C_{ox} = 60 \mu\text{A/V}^2$ ,  $W/L = 120 \mu\text{m}/3 \mu\text{m}$ ,  $I_D = 0.3 \text{ mA}$ , and  $V_D = +0.4 \text{ V}$ .

**Ans.**  $R_D = 7 \text{ k}\Omega$ ;  $R_s = 3.3 \text{ k}\Omega$

**Example 5.4**

Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the  $i-v$  relationship of the resulting two-terminal device in terms of the MOSFET parameters  $k_n = k'_n(W/L)$  and  $V_m$ . Neglect channel-length modulation (i.e.,  $\lambda = 0$ ). Note that this two-terminal device is known as a **diode-connected transistor**.

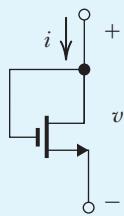


Figure 5.22

**Solution**

Since  $v_D = v_G$  implies operation in the saturation mode,

$$i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (v_{GS} - V_m)^2$$

Now,  $i = i_D$  and  $v = v_{GS}$ , thus

$$i = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (v - V_m)^2$$

Replacing  $k'_n \left( \frac{W}{L} \right)$  by  $k_n$  results in

$$i = \frac{1}{2} k_n (v - V_m)^2$$

**EXERCISES**

- D5.9** For the circuit in Fig. E5.9, find the value of  $R$  that results in  $V_D = 0.7$  V. The MOSFET has  $V_m = 0.5$  V,  $\mu_n C_{ox} = 0.4$  mA/V<sup>2</sup>,  $W/L = \frac{0.72 \mu\text{m}}{0.18 \mu\text{m}}$ , and  $\lambda = 0$ .

**Ans.** 34.4 kΩ

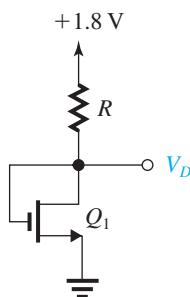


Figure E5.9

- D5.10** Figure E5.10 shows a circuit obtained by augmenting the circuit of Fig. E5.9 considered in Exercise 5.9 with a transistor  $Q_2$  identical to  $Q_1$  and a resistance  $R_2$ . Find the value of  $R_2$  that results in  $Q_2$  operating at the edge of the saturation region. Use your solution to Exercise 5.9.

**Ans.** 50 kΩ

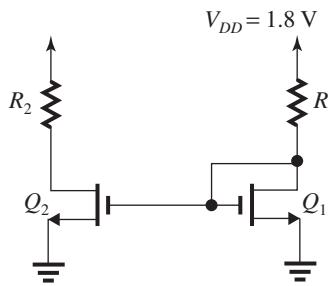


Figure E5.10

**Example 5.5**

Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let  $V_m = 1$  V and  $k'_n(W/L) = 1 \text{ mA/V}^2$ .

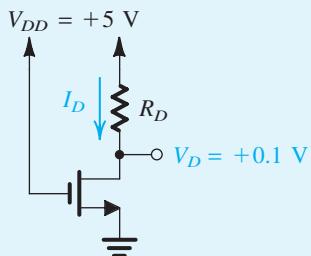


Figure 5.23 Circuit for Example 5.5.

**Solution**

Since the drain voltage is lower than the gate voltage by 4.9 V and  $V_m = 1$  V, the MOSFET is operating in the triode region. Thus the current  $I_D$  is given by

$$\begin{aligned} I_D &= k'_n \frac{W}{L} \left[ (V_{GS} - V_m)V_{DS} - \frac{1}{2}V_{DS}^2 \right] \\ I_D &= 1 \times \left[ (5 - 1) \times 0.1 - \frac{1}{2} \times 0.01 \right] \\ &= 0.395 \text{ mA} \end{aligned}$$

The required value for  $R_D$  can be found as follows:

$$\begin{aligned} R_D &= \frac{V_{DD} - V_D}{I_D} \\ &= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega \end{aligned}$$

In a practical discrete-circuit design problem, one selects the closest standard value available for, say, 5% resistors—in this case, 12 kΩ; see Appendix J. Since the transistor is operating in the triode region with a small  $V_{DS}$ , the effective drain-to-source resistance can be determined as follows:

$$\begin{aligned} r_{DS} &= \frac{V_{DS}}{I_D} \\ &= \frac{0.1}{0.395} = 253 \Omega \end{aligned}$$

Alternatively, we can determine  $r_{DS}$  by using the formula

$$r_{DS} = \frac{1}{k_n V_{OV}}$$

to obtain

$$r_{DS} = \frac{1}{1 \times (5 - 1)} = 0.25 \text{ k}\Omega = 250 \Omega$$

which is close to the value found above.

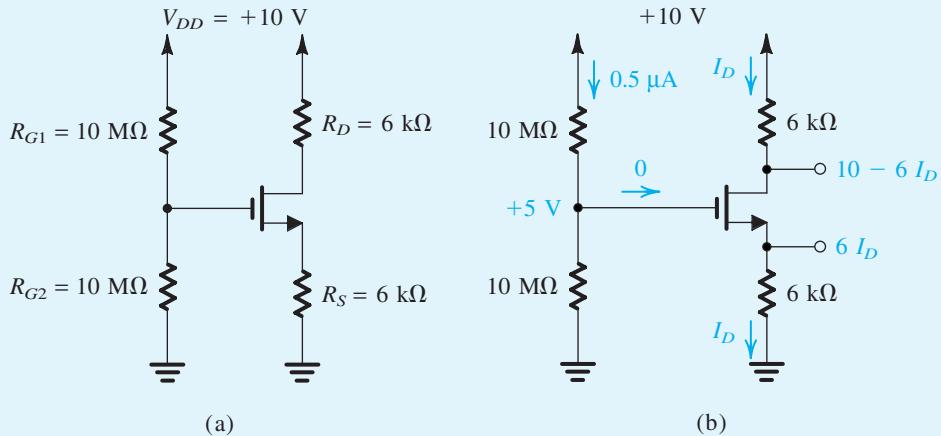
### EXERCISE

**5.11** If in the circuit of Example 5.5 the value of  $R_D$  is doubled, find approximate values for  $I_D$  and  $V_D$ .

**Ans.** 0.2 mA; 0.05 V

### Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let  $V_m = 1 \text{ V}$  and  $k'_n(W/L) = 1 \text{ mA/V}^2$ . Neglect the channel-length modulation effect (i.e., assume  $\lambda = 0$ ).

**Example 5.6** *continued***Figure 5.24** (a) Circuit for Example 5.6. (b) The circuit with some of the analysis details shown.**Solution**

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two  $10\text{-M}\Omega$  resistors,

$$V_G = V_{DD} \frac{R_{G2}}{R_{G2} + R_{G1}} = 10 \times \frac{10}{10 + 10} = +5 \text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 5.24(b). Since the voltage at the gate is 5 V and the voltage at the source is  $I_D$  (mA)  $\times$   $6\text{ (k}\Omega\text{)} = 6I_D$  (V), we have

$$V_{GS} = 5 - 6I_D$$

Thus  $I_D$  is given by

$$\begin{aligned} I_D &= \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_m)^2 \\ &= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2 \end{aligned}$$

which results in the following quadratic equation in  $I_D$ :

$$18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for  $I_D$ : 0.89 mA and 0.5 mA. The first value results in a source voltage of  $6 \times 0.89 = 5.34$  V, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5 \text{ mA}$$

$$V_S = 0.5 \times 6 = +3 \text{ V}$$

$$V_{GS} = 5 - 3 = 2 \text{ V}$$

$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Since  $V_D > V_G - V_m$ , the transistor is operating in saturation, as initially assumed.

## EXERCISES

- 5.12** For the circuit of Fig. 5.24, what is the largest value that  $R_D$  can have while the transistor remains in the saturation mode?

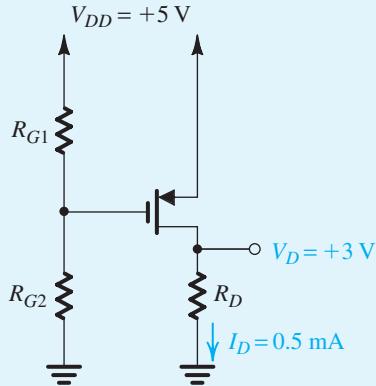
**Ans.**  $12 \text{ k}\Omega$

- D5.13** Redesign the circuit of Fig. 5.24 for the following requirements:  $V_{DD} = +5 \text{ V}$ ,  $I_D = 0.32 \text{ mA}$ ,  $V_S = 1.6 \text{ V}$ ,  $V_D = 3.4 \text{ V}$ , with a  $1-\mu\text{A}$  current through the voltage divider  $R_{G1}$ ,  $R_{G2}$ . Assume the same MOSFET as in Example 5.6.

**Ans.**  $R_{G1} = 1.6 \text{ M}\Omega$ ;  $R_{G2} = 3.4 \text{ M}\Omega$ ,  $R_S = R_D = 5 \text{ k}\Omega$

## Example 5.7

Design the circuit of Fig. 5.25 so that the transistor operates in saturation with  $I_D = 0.5 \text{ mA}$  and  $V_D = +3 \text{ V}$ . Let the PMOS transistor have  $V_{tp} = -1 \text{ V}$  and  $k'_p(W/L) = 1 \text{ mA/V}^2$ . Assume  $\lambda = 0$ . What is the largest value that  $R_D$  can have while maintaining saturation-region operation?

**Example 5.7** *continued***Figure 5.25** Circuit for Example 5.7.**Solution**

Since the MOSFET is to be in saturation, we can write

$$I_D = \frac{1}{2} k'_p \frac{W}{L} |V_{ov}|^2$$

Substituting  $I_D = 0.5\text{ mA}$  and  $k'_p W/L = 1\text{ mA/V}^2$ , we obtain

$$|V_{ov}| = 1\text{ V}$$

and

$$V_{SG} = |V_{tp}| + |V_{ov}| = 1 + 1 = 2\text{ V}$$

Since the source is at  $+5\text{ V}$ , the gate voltage must be set to  $+3\text{ V}$ . This can be achieved by the appropriate selection of the values of  $R_{G1}$  and  $R_{G2}$ . A possible selection is  $R_{G1} = 2\text{ M}\Omega$  and  $R_{G2} = 3\text{ M}\Omega$ .

The value of  $R_D$  can be found from

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6\text{ k}\Omega$$

Saturation-mode operation will be maintained up to the point that  $V_D$  exceeds  $V_G$  by  $|V_{tp}|$ ; that is, until

$$V_{D_{max}} = 3 + 1 = 4\text{ V}$$

This value of drain voltage is obtained with  $R_D$  given by

$$R_D = \frac{4}{0.5} = 8\text{ k}\Omega$$

**EXERCISE**

- D5.14** For the circuit in Fig. E5.14, find the value of  $R$  that results in the PMOS transistor operating with an overdrive voltage  $|V_{ov}| = 0.6$  V. The threshold voltage is  $V_{tp} = -0.4$  V, the process transconductance parameter  $k'_p = 0.1 \text{ mA/V}^2$ , and  $W/L = 10 \mu\text{m}/0.18 \mu\text{m}$ .

**Ans.**  $800 \Omega$

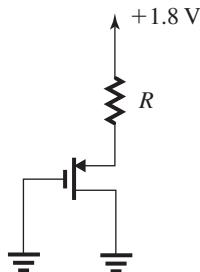


Figure E5.14

**Example 5.8**

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with  $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$  and  $V_m = -V_{tp} = 1 \text{ V}$ . Assuming  $\lambda = 0$  for both devices, find the drain currents  $i_{DN}$  and  $i_{DP}$ , as well as the voltage  $v_o$ , for  $v_i = 0 \text{ V}$ ,  $+2.5 \text{ V}$ , and  $-2.5 \text{ V}$ .

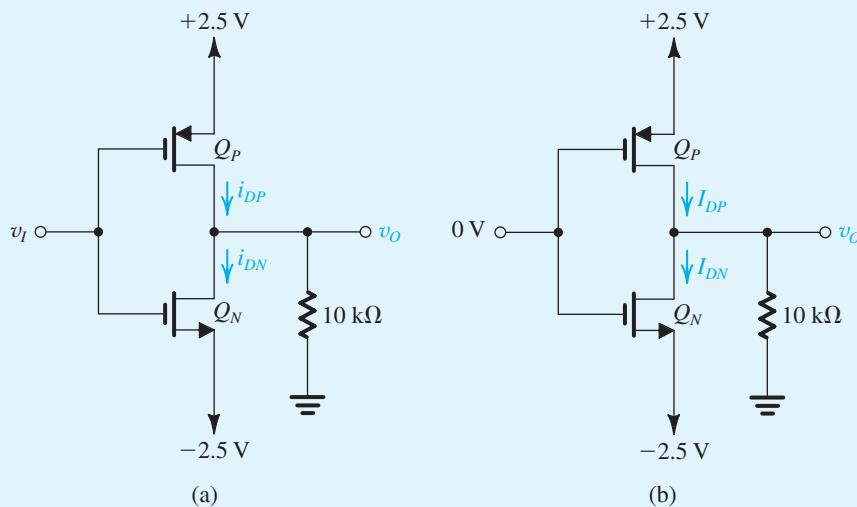


Figure 5.26 Circuits for Example 5.8.

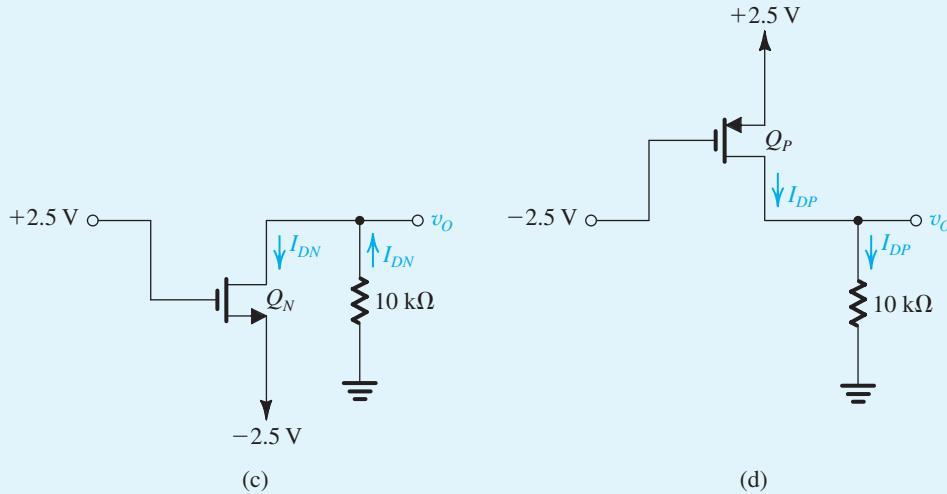
**Example 5.8** *continued***Figure 5.26** *continued***Solution**

Figure 5.26(b) shows the circuit for the case  $v_I = 0$  V. We note that since  $Q_N$  and  $Q_P$  are perfectly matched and are operating at equal values of  $|V_{GS}| = 2.5$  V, the circuit is symmetrical, which dictates that  $v_o = 0$  V. Thus both  $Q_N$  and  $Q_P$  are operating with  $|V_{DG}| = 0$  and, hence, in saturation. The drain currents can now be found from

$$I_{DP} = I_{DN} = \frac{1}{2} \times 1 \times (2.5 - 1)^2 = 1.125 \text{ mA}$$

Next, we consider the circuit with  $v_I = +2.5$  V. Transistor  $Q_P$  will have a  $V_{SG}$  of zero and thus will be cut off, reducing the circuit to that shown in Fig. 5.26(c). We note that  $v_o$  will be negative, and thus  $v_{GD}$  will be greater than  $V_m$ , causing  $Q_N$  to operate in the triode region. For simplicity we shall assume that  $v_{DS}$  is small and thus use

$$\begin{aligned} I_{DN} &\simeq k'_n (W_n/L_n) (V_{GS} - V_m) V_{DS} \\ &= 1[2.5 - (-2.5) - 1][v_o - (-2.5)] \end{aligned}$$

From the circuit diagram shown in Fig. 5.26(c), we can also write

$$I_{DN}(\text{mA}) = \frac{0 - v_o}{10(\text{k}\Omega)}$$

These two equations can be solved simultaneously to yield

$$I_{DN} = 0.244 \text{ mA} \quad v_o = -2.44 \text{ V}$$

Note that  $V_{DS} = -2.44 - (-2.5) = 0.06 \text{ V}$ , which is small as assumed.

Finally, the situation for the case  $v_I = -2.5 \text{ V}$  [Fig. 5.26(d)] will be the exact complement of the case  $v_I = +2.5 \text{ V}$ : Transistor  $Q_N$  will be off. Thus  $I_{DN} = 0$ ,  $Q_P$  will be operating in the triode region with  $I_{DP} = 0.244 \text{ mA}$  and  $v_o = +2.44 \text{ V}$ .

### EXERCISE

- 5.15** The NMOS and PMOS transistors in the circuit of Fig. E5.15 are matched with  $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$  and  $V_m = -V_{tp} = 1 \text{ V}$ . Assuming  $\lambda = 0$  for both devices, find the drain currents  $i_{DN}$  and  $i_{DP}$  and the voltage  $v_o$  for  $v_I = 0 \text{ V}$ ,  $+2.5 \text{ V}$ , and  $-2.5 \text{ V}$ .

**Ans.**  $v_I = 0 \text{ V}$ : 0 mA, 0 mA, 0 V;  $v_I = +2.5 \text{ V}$ : 0.104 mA, 0 mA, 1.04 V;  $v_I = -2.5 \text{ V}$ : 0 mA, 0.104 mA, -1.04 V

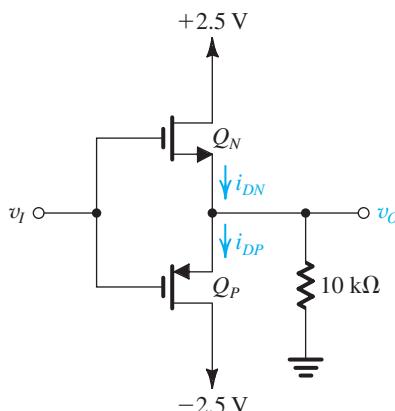


Figure E5.15

**Concluding Remark** If a MOSFET is conducting but its mode of operation (saturation or triode) is not known, we assume operation in the saturation region, solve the problem, and check whether the conditions for saturation-mode operation are satisfied. If not, then the MOSFET is operating in the triode region and the analysis is done accordingly.

## GORDON MOORE— HIS LAW:

A half-century ago, Gordon Moore, who would go on to become a cofounder first of Fairchild Semiconductor and then of Intel, presented a startling idea in the issue of *Electronics Magazine* dated April 19, 1965. Moore, who had a doctorate in chemistry, had projected the potential growth of the integrated-circuit industry based on five points spanning a seven-year period from 1958 to 1965. The conclusion he reached—that the number of transistors per chip had been increasing and would continue to increase by a factor of 2 every two years or so—was destined to propel progress in integrated circuits over the succeeding decades into the twenty-first century. Doubling of the number of transistors was predicted on the basis of another prediction: the continuing shrinkage of transistor dimensions. In early recognition of the importance of this prediction, Carver Mead, a pioneer in very large scale integration (VLSI), soon began to refer to this prediction as “Moore’s law.” (See Chapter 15, Section 15.1, for the implications of Moore’s law).



## 5.4 The Body Effect and Other Topics

In this section we briefly consider a number of important though secondary issues.

### 5.4.1 The Role of the Substrate—The Body Effect

In many applications the source terminal is connected to the substrate (or body) terminal B, which results in the *pn* junction between the substrate and the induced channel (review Fig. 5.5) having a constant zero (cutoff) bias. In such a case the substrate does not play any role in circuit operation and its existence can be ignored altogether.

In integrated circuits, however, the substrate is usually common to many MOS transistors. In order to maintain the cutoff condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (the most positive in a PMOS circuit). The resulting reverse-bias voltage between source and body ( $V_{SB}$  in an *n*-channel device) will have an effect on device operation. To appreciate this fact, consider an NMOS transistor and let its substrate be made negative relative to the source. The reverse-bias voltage will widen the depletion region (refer to Fig. 5.2). This in turn reduces the channel depth. To return the channel to its former state,  $v_{GS}$  has to be increased.

The effect of  $V_{SB}$  on the channel can be most conveniently represented as a change in the threshold voltage  $V_t$ . Specifically, it has been shown that increasing the reverse substrate bias voltage  $V_{SB}$  results in an increase in  $V_t$  according to the relationship

➤ 
$$V_t = V_{t0} + \gamma \left[ \sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right] \quad (5.30)$$

where  $V_{t0}$  is the threshold voltage for  $V_{SB} = 0$ ;  $\phi_f$  is a physical parameter with  $(2\phi_f)$  typically 0.6 V;  $\gamma$  is a fabrication-process parameter given by

➤ 
$$\gamma = \frac{\sqrt{2qN_A\epsilon_s}}{C_{ox}} \quad (5.31)$$

where  $q$  is the magnitude of the electron charge ( $1.6 \times 10^{-19}$  C),  $N_A$  is the doping concentration of the *p*-type substrate, and  $\epsilon_s$  is the permittivity of silicon ( $11.7\epsilon_0 = 11.7 \times 8.854 \times 10^{-14} = 1.04 \times 10^{-12}$  F/cm). The parameter  $\gamma$  has the dimension of  $\sqrt{V}$  and is typically  $0.4 \text{ V}^{1/2}$ . Finally, note that Eq. (5.30) applies equally well for *p*-channel devices with  $V_{SB}$  replaced by

the reverse bias of the substrate,  $V_{BS}$  (or, alternatively, replace  $V_{SB}$  by  $|V_{SB}|$ ) and note that  $\gamma$  is negative. Also, in evaluating  $\gamma$ ,  $N_A$  must be replaced with  $N_D$ , the doping concentration of the  $n$  well in which the PMOS is formed. For  $p$ -channel devices,  $2\phi_f$  is typically 0.75 V, and  $\gamma$  is typically  $-0.5 \text{ V}^{1/2}$ .

### EXERCISE

- 5.16** An NMOS transistor has  $V_{t0} = 0.8 \text{ V}$ ,  $2\phi_f = 0.7 \text{ V}$ , and  $\gamma = 0.4 \text{ V}^{1/2}$ . Find  $V_t$  when  $V_{SB} = 3 \text{ V}$ .

**Ans.** 1.23 V

Equation (5.30) indicates that an incremental change in  $V_{SB}$  gives rise to an incremental change in  $V_t$ , which in turn results in an incremental change in  $i_D$  even though  $v_{GS}$  might have been kept constant. It follows that the body voltage controls  $i_D$ ; thus the body acts as another gate for the MOSFET, a phenomenon known as the **body effect**. Here we note that the parameter  $\gamma$  is known as the **body-effect parameter**.

### 5.4.2 Temperature Effects

Both  $V_t$  and  $k'$  are temperature sensitive. The magnitude of  $V_t$  decreases by about 2 mV for every 1°C rise in temperature. This decrease in  $|V_t|$  gives rise to a corresponding increase in drain current as temperature is increased. However, because  $k'$  decreases with temperature and its effect is a dominant one, the overall observed effect of a temperature increase is a *decrease* in drain current. This very interesting result is put to use in applying the MOSFET in power circuits (Chapter 12).

### 5.4.3 Breakdown and Input Protection

As the voltage on the drain is increased, a value is reached at which the *pn* junction between the drain region and substrate suffers avalanche breakdown (see Section 3.5.3). This breakdown usually occurs at voltages of 20 V to 150 V and results in a somewhat rapid increase in current (known as a **weak avalanche**).

Another breakdown effect that occurs at lower voltages (about 20 V) in modern devices is called **punch-through**. It occurs in devices with relatively short channels when the drain voltage is increased to the point that the depletion region surrounding the drain region extends through the channel to the source. The drain current then increases rapidly. Normally, punch-through does not result in permanent damage to the device.

Yet another kind of breakdown occurs when the gate-to-source voltage exceeds about 30 V. This is the breakdown of the gate oxide and results in permanent damage to the device. Although 30 V may seem high, it must be remembered that the MOSFET has a very high input resistance and a very small input capacitance, and thus small amounts of static charge accumulating on the gate capacitor can cause its breakdown voltage to be exceeded.

To prevent the accumulation of static charge on the gate capacitor of a MOSFET, gate-protection devices are usually included at the input terminals of MOS integrated circuits. The protection mechanism invariably makes use of clamping diodes.

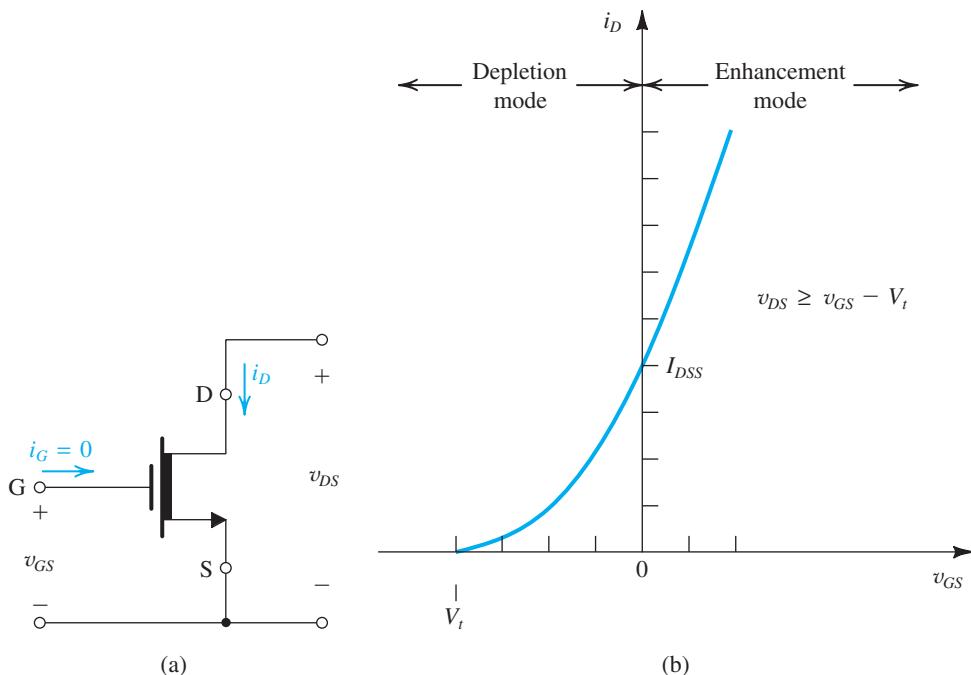
### 5.4.4 Velocity Saturation

At high longitudinal electric fields, the drift velocity of charge carriers in the channel reaches an upper limit (approximately  $10^7$  cm/s for electrons and holes in silicon). This effect, which in modern very-short-channel devices can occur for  $v_{DS}$  lower than 1 V, is called velocity saturation. It can be shown that when velocity saturation occurs, the current  $i_D$  will no longer be related to  $v_{GS}$  by the square-law relationship. Rather,  $i_D$  becomes linearly dependent on  $v_{GS}$  and the transconductance  $g_m$  becomes constant and independent of  $v_{GS}$ . In Chapter 15, we shall consider velocity saturation in our study of deep-submicron (i.e.,  $L < 0.25 \mu\text{m}$ ) CMOS digital circuits.

### 5.4.5 The Depletion-Type MOSFET

We conclude this section with a brief discussion of another type of MOSFET, the depletion-type MOSFET. Its structure is similar to that of the enhancement-type MOSFET with one important difference: The depletion MOSFET has a physically implanted channel. Thus an  $n$ -channel depletion-type MOSFET has an  $n$ -type silicon region connecting the  $n^+$  source and the  $n^+$  drain regions at the top of the  $p$ -type substrate. Thus if a voltage  $v_{DS}$  is applied between drain and source, a current  $i_D$  flows for  $v_{GS} = 0$ . In other words, there is no need to induce a channel, unlike the case of the enhancement MOSFET.

The channel depth and hence its conductivity can be controlled by  $v_{GS}$  in exactly the same manner as in the enhancement-type device. Applying a positive  $v_{GS}$  enhances the channel by attracting more electrons into it. Here, however, we also can apply a negative  $v_{GS}$ , which causes electrons to be repelled from the channel, and thus the channel becomes shallower and its conductivity decreases. The negative  $v_{GS}$  is said to **deplete** the channel of its charge carriers,



**Figure 5.27** The circuit symbol (a) and the  $i_D-v_{GS}$  characteristic in saturation (b) for an  $n$ -channel depletion-type MOSFET.

and this mode of operation (negative  $v_{GS}$ ) is called **depletion mode**. As the magnitude of  $v_{GS}$  is increased in the negative direction, a value is reached at which the channel is completely depleted of charge carriers and  $i_D$  is reduced to zero even though  $v_{DS}$  may be still applied. This negative value of  $v_{GS}$  is the threshold voltage of the *n*-channel depletion-type MOSFET.

The description above suggests (correctly) that a depletion-type MOSFET can be operated in the enhancement mode by applying a positive  $v_{GS}$  and in the depletion mode by applying a negative  $v_{GS}$ . This is illustrated in Fig. 5.27, which shows both the circuit symbol for the depletion NMOS transistor (Fig. 5.27a) and its  $i_D-v_{GS}$  characteristic. Observe that here the threshold voltage  $V_m$  is negative. The  $i_D-v_{DS}$  characteristics (not shown) are similar to those for the enhancement-type MOSFET except for the negative  $V_m$ . Finally, note that the device symbol denotes the existing channel via the shaded area next to the vertical line.

Depletion-type MOSFETs can be fabricated on the same IC chip as enhancement-type devices, resulting in circuits with improved characteristics, as will be shown in a later chapter. The depletion-type MOSFET, however, is a specialty device and is not commonly used.

## EXERCISE

- 5.17** For a depletion-type NMOS transistor with  $V_t = -2$  V and  $k'_n(W/L) = 2$  mA/V<sup>2</sup>, find the minimum  $v_{DS}$  required to operate in the saturation region when  $v_{GS} = +1$  V. What is the corresponding value of  $i_D$ ?

**Ans.** 3 V; 9 mA

## Summary

- The enhancement-type MOSFET is currently the most widely used semiconductor device. It is the basis of CMOS technology, which is the most popular IC fabrication technology at this time. CMOS provides both *n*-channel (NMOS) and *p*-channel (PMOS) transistors, which increases design flexibility. The minimum MOSFET channel length achievable with a given CMOS process is used to characterize the process. This figure has been continually reduced and is currently 32 nm.
- The overdrive voltage,  $|v_{ov}| \equiv |v_{GS}| - |V_t|$ , is the key quantity that governs the operation of the MOSFET. For the MOSFET to operate in the saturation region, which is the region for amplifier application,  $|v_{DS}| \geq |v_{ov}|$ , and the resulting  $i_D = \frac{1}{2}\mu_n C_{ox}(W/L)v_{ov}^2$  (for NMOS; replace  $\mu_n$  with  $\mu_p$  for PMOS). If  $|v_{DS}| < |v_{ov}|$ , the MOSFET operates in the triode region, which together with cutoff is used for operating the MOSFET as a switch.
- Tables 5.1 and 5.2 provide summaries of the conditions and relationships that describe the operation of NMOS and PMOS transistors, respectively.
- In saturation,  $i_D$  shows some linear dependence on  $v_{DS}$  as a result of the change in channel length. This channel-length modulation phenomenon becomes more pronounced as  $L$  decreases. It is modeled by ascribing an output resistance  $r_o = |V_A|/I_D$  to the MOSFET model. Here, the Early voltage  $|V_A| = |V'_A|L$ , where  $|V'_A|$  is a process-dependent parameter.
- In the analysis of dc MOSFET circuits, if a MOSFET is conducting, but its region of operation (saturation or triode) is not known, one assumes saturation-mode operation. Then, one solves the problem and checks to determine whether the assumption was justified. If not, then the transistor is operating in the triode region, and the analysis is done accordingly.
- The depletion-type MOSFET has an implanted channel and thus can be operated in either the depletion or enhancement mode. It is characterized by the same equations used for the enhancement device except for having a negative  $V_m$  (positive  $V_{tp}$  for depletion PMOS transistors).

# PROBLEMS

## Computer Simulations Problems

**SIM** Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

## Section 5.1: Device Structure and Physical Operation

**5.1** MOS technology is used to fabricate a capacitor, utilizing the gate metallization and the substrate as the capacitor electrodes. Find the area required per 1-pF capacitance for oxide thickness ranging from 2 nm to 10 nm. For a square plate capacitor of 10 pF, what dimensions are needed?

**5.2** Calculate the total charge stored in the channel of an NMOS transistor having  $C_{ox} = 9 \text{ fF}/\mu\text{m}^2$ ,  $L = 0.36 \mu\text{m}$ , and  $W = 3.6 \mu\text{m}$ , and operated at  $V_{ov} = 0.2 \text{ V}$  and  $V_{DS} = 0 \text{ V}$ .

**5.3** Use dimensional analysis to show that the units of the process transconductance parameter  $k'_n$  are  $\text{A}/\text{V}^2$ . What are the dimensions of the MOSFET transconductance parameter  $k_n$ ?

**5.4** An NMOS transistor that is operated with a small  $v_{DS}$  is found to exhibit a resistance  $r_{DS}$ . By what factor will  $r_{DS}$  change in each of the following situations?

- $V_{ov}$  is doubled.
- The device is replaced with another fabricated in the same technology but with double the width.

(c) The device is replaced with another fabricated in the same technology but with both the width and length doubled.

(d) The device is replaced with another fabricated in a more advanced technology for which the oxide thickness is halved and similarly for  $W$  and  $L$  (assume  $\mu_n$  remains unchanged).

**D 5.5** An NMOS transistor fabricated in a technology for which  $k'_n = 400 \mu\text{A}/\text{V}^2$  and  $V_t = 0.5 \text{ V}$  is required to operate with a small  $v_{DS}$  as a variable resistor ranging in value from  $250 \Omega$  to  $1 \text{k}\Omega$ . Specify the range required for the control voltage  $V_{GS}$  and the required transistor width  $W$ . It is required to use the smallest possible device, as limited by the minimum channel length of this technology ( $L_{min} = 0.18 \mu\text{m}$ ) and the maximum allowed voltage of  $1.8 \text{ V}$ .

**5.6** Sketch a set of  $i_D - v_{DS}$  characteristic curves for an NMOS transistor operating with a small  $v_{DS}$  (in the manner shown in Fig. 5.4). Let the MOSFET have  $k_n = 5 \text{ mA}/\text{V}^2$  and  $V_m = 0.5 \text{ V}$ . Sketch and clearly label the graphs for  $V_{GS} = 0.5, 1.0, 1.5, 2.0, \text{ and } 2.5 \text{ V}$ . Let  $V_{DS}$  be in the range 0 to 50 mV. Give the value of  $r_{DS}$  obtained for each of the five values of  $V_{GS}$ . Although only a sketch, your diagram should be drawn to scale as much as possible.

**D 5.7** An  $n$ -channel MOS device in a technology for which oxide thickness is 4 nm, minimum channel length is  $0.18 \mu\text{m}$ ,  $k'_n = 400 \mu\text{A}/\text{V}^2$ , and  $V_t = 0.5 \text{ V}$  operates in the triode region, with small  $v_{DS}$  and with the gate-source voltage in the range  $0 \text{ V}$  to  $+1.8 \text{ V}$ . What device width is needed to ensure that the minimum available resistance is  $1 \text{k}\Omega$ ?

**5.8** Consider an NMOS transistor operating in the triode region with an overdrive voltage  $V_{ov}$ . Find an expression for the incremental resistance

$$r_{ds} \equiv 1 / \left. \frac{\partial i_D}{\partial v_{DS}} \right|_{v_{DS}=V_{DS}}$$

Give the values of  $r_{ds}$  in terms of  $k_n$  and  $V_{OV}$  for  $V_{DS} = 0$ ,  $0.2V_{OV}$ ,  $0.5V_{OV}$ ,  $0.8V_{OV}$ , and  $V_{OV}$ .

**5.9** An NMOS transistor with  $k_n = 4 \text{ mA/V}^2$  and  $V_t = 0.5 \text{ V}$  is operated with  $V_{GS} = 1.0 \text{ V}$ . At what value of  $V_{DS}$  does the transistor enter the saturation region? What value of  $I_D$  is obtained in saturation?

**5.10** Consider a CMOS process for which  $L_{\min} = 0.25 \mu\text{m}$ ,  $t_{ox} = 6 \text{ nm}$ ,  $\mu_n = 460 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $V_t = 0.5 \text{ V}$ .

- (a) Find  $C_{ox}$  and  $k'_n$ .
- (b) For an NMOS transistor with  $W/L = 20 \mu\text{m}/0.25 \mu\text{m}$ , calculate the values of  $V_{OV}$ ,  $V_{GS}$ , and  $V_{DS\min}$  needed to operate the transistor in the saturation region with a dc current  $I_D = 0.5 \text{ mA}$ .
- (c) For the device in (b), find the values of  $V_{OV}$  and  $V_{GS}$  required to cause the device to operate as a  $100\text{-}\Omega$  resistor for very small  $v_{DS}$ .

**5.11** A *p*-channel MOSFET with a threshold voltage  $V_{tp} = -0.7 \text{ V}$  has its source connected to ground.

- (a) What should the gate voltage be for the device to operate with an overdrive voltage of  $|V_{OV}| = 0.4 \text{ V}$ ?
- (b) With the gate voltage as in (a), what is the highest voltage allowed at the drain while the device operates in the saturation region?
- (c) If the drain current obtained in (b) is  $0.5 \text{ mA}$ , what would the current be for  $V_D = -20 \text{ mV}$  and for  $V_D = -2 \text{ V}$ ?

**5.12** With the knowledge that  $\mu_p = 0.4 \mu_n$ , what must be the relative width of *n*-channel and *p*-channel devices having equal channel lengths if they are to have equal drain currents when operated in the saturation mode with overdrive voltages of the same magnitude?

**5.13** An *n*-channel device has  $k'_n = 100 \mu\text{A/V}^2$ ,  $V_t = 0.7 \text{ V}$ , and  $W/L = 20$ . The device is to operate as a switch for small  $v_{DS}$ , utilizing a control voltage  $v_{GS}$  in the range  $0 \text{ V}$  to  $5 \text{ V}$ . Find the switch closure resistance,  $r_{DS}$ , and closure

voltage,  $V_{DS}$ , obtained when  $v_{GS} = 5 \text{ V}$  and  $i_D = 1 \text{ mA}$ . If  $\mu_p \simeq 0.4 \mu_n$ , what must  $W/L$  be for a *p*-channel device that provides the same performance as the *n*-channel device in this application?

**5.14** Consider an *n*-channel MOSFET with  $t_{ox} = 6 \text{ nm}$ ,  $\mu_n = 460 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $V_t = 0.5 \text{ V}$ , and  $W/L = 10$ . Find the drain current in the following cases:

- (a)  $v_{GS} = 2.5 \text{ V}$  and  $v_{DS} = 1 \text{ V}$
- (b)  $v_{GS} = 2 \text{ V}$  and  $v_{DS} = 1.5 \text{ V}$
- (c)  $v_{GS} = 2.5 \text{ V}$  and  $v_{DS} = 0.2 \text{ V}$
- (d)  $v_{GS} = v_{DS} = 2.5 \text{ V}$

**\*5.15** This problem illustrates the central point in the electronics revolution that has been in effect for the past four decades: By continually reducing the MOSFET size, we are able to pack more devices on an IC chip. Gordon Moore, co-founder of Intel Corporation, predicted this exponential growth of chip-packing density very early in the history of the development of the integrated circuit in the formulation that has become known as **Moore's law**.

The table on the next page shows four technology generations, each characterized by the minimum possible MOSFET channel length (row 1). In going from one generation to another, both  $L$  and  $t_{ox}$  are scaled by the same factor. The power supply utilized  $V_{DD}$  is also scaled by the same factor, to keep the magnitudes of all electrical fields within the device unchanged. Unfortunately, but for good reasons,  $V_t$  cannot be scaled similarly.

Complete the table entries, noting that row 5 asks for the transconductance parameter of an NMOS transistor with  $W/L = 10$ ; row 9 asks for the value of  $I_D$  obtained with  $V_{GS} = V_{DS} = V_{DD}$ ; row 10 asks for the power  $P = V_{DD}I_D$  dissipated in the circuit. An important quantity is the power density,  $P/A$ , asked for in row 11. Finally, you are asked to find the number of transistors that can be placed on an IC chip fabricated in each of the technologies in terms of the number obtained with the  $0.5\text{-}\mu\text{m}$  technology ( $n$ ).

1	$L$ ( $\mu\text{m}$ )	0.5	0.25	0.18	0.13
2	$t_{ox}$ (nm)	10			
3	$C_{ox}$ (fF/ $\mu\text{m}^2$ )				
4	$k'_n$ ( $\mu\text{A}/\text{V}^2$ ) ( $\mu_n = 500 \text{ cm}^2/\text{V}\cdot\text{s}$ )				
5	$k_n$ (mA/V <sup>2</sup> ) For $W/L = 10$				
6	Device area, $A$ ( $\mu\text{m}^2$ )				
7	$V_{DD}$ (V)	5			
8	$V_t$ (V)	0.7	0.5	0.4	0.4
9	$I_D$ (mA) For $V_{GS} = V_{DS} = V_{DD}$				
10	$P$ (mW)				
11	$P/A$ (mW/ $\mu\text{m}^2$ )				
12	Devices per chip	$n$			

### Section 5.2: Current–Voltage Characteristics

In the following problems, when  $\lambda$  is not specified, assume it is zero.

**5.16** Show that when channel-length modulation is neglected (i.e.,  $\lambda = 0$ ), plotting  $i_D/k_n$  versus  $v_{DS}$  for various values of  $v_{OV}$ , and plotting  $i_D/k_n$  versus  $v_{OV}$  for  $v_{DS} \geq v_{OV}$ , results in universal representation of the  $i_D - v_{DS}$  and  $i_D - v_{GS}$  characteristics of the NMOS transistor. That is, the resulting graphs are both technology and device independent. Furthermore, these graphs apply equally well to the PMOS transistor by a simple relabeling of variables. (How?) What is the slope at  $v_{DS} = 0$  of each of the  $i_D/k_n$  versus  $v_{DS}$  graphs? For the  $i_D/k_n$  versus  $v_{OV}$  graph, find the slope at a point  $v_{OV} = V_{OV}$ .

**5.17** An NMOS transistor having  $V_t = 0.8$  V is operated in the triode region with  $v_{DS}$  small. With  $V_{GS} = 1.2$  V, it is found to have a resistance  $r_{DS}$  of  $1 \text{ k}\Omega$ . What value of  $V_{GS}$  is required to obtain  $r_{DS} = 200 \Omega$ ? Find the corresponding resistance values obtained with a device having twice the value of  $W$ .

**5.18** A particular MOSFET for which  $V_m = 0.5$  V and  $k'_n(W/L) = 1.6 \text{ mA/V}^2$  is to be operated in the saturation region. If  $i_D$  is to be  $50 \mu\text{A}$ , find the required  $v_{GS}$  and the minimum required  $v_{DS}$ . Repeat for  $i_D = 200 \mu\text{A}$ .

**5.19** A particular *n*-channel MOSFET is measured to have a drain current of 0.4 mA at  $V_{GS} = V_{DS} = 1$  V and of 0.1 mA at  $V_{GS} = V_{DS} = 0.8$  V. What are the values of  $k_n$  and  $V_t$  for this device?

**D 5.20** For a particular IC-fabrication process, the transconductance parameter  $k'_n = 400 \mu\text{A/V}^2$ , and  $V_t = 0.5$  V. In an application in which  $v_{GS} = v_{DS} = V_{\text{supply}} = 1.8$  V, a drain current of 2 mA is required of a device of minimum length of 0.18  $\mu\text{m}$ . What value of channel width must the design use?

**5.21** An NMOS transistor, operating in the linear-resistance region with  $v_{DS} = 50$  mV, is found to conduct 25  $\mu\text{A}$  for  $v_{GS} = 1$  V and 50  $\mu\text{A}$  for  $v_{GS} = 1.5$  V. What is the apparent value of threshold voltage  $V_t$ ? If  $k'_n = 50 \mu\text{A/V}^2$ , what is the device  $W/L$  ratio? What current would you expect to flow with  $v_{GS} = 2$  V and  $v_{DS} = 0.1$  V? If the device is operated at  $v_{GS} = 2$  V, at what value of  $v_{DS}$  will the drain end of the MOSFET channel just reach pinch-off, and what is the corresponding drain current?

**5.22** For an NMOS transistor, for which  $V_t = 0.4$  V, operating with  $v_{GS}$  in the range of 1.0 V to 1.8 V, what is the largest value of  $v_{DS}$  for which the channel remains continuous?

**5.23** An NMOS transistor, fabricated with  $W = 20 \mu\text{m}$  and  $L = 1 \mu\text{m}$  in a technology for which  $k'_n = 100 \mu\text{A/V}^2$  and  $V_t = 0.8$  V, is to be operated at very low values of  $v_{DS}$  as a linear resistor. For  $v_{GS}$  varying from 1.0 V to 4.8 V, what range of resistor values can be obtained? What is the available range if

- (a) the device width is halved?
- (b) the device length is halved?
- (c) both the width and length are halved?

**5.24** When the drain and gate of a MOSFET are connected together, a two-terminal device known as a “diode-connected transistor” results. Figure P5.24 shows such devices obtained from MOS transistors of both polarities. Show that

- (a) the  $i-v$  relationship is given by

$$i = \frac{1}{2} k' \frac{W}{L} (v - |V_t|)^2$$

- (b) the incremental resistance  $r$  for a device biased to operate at  $v = |V_t| + V_{ov}$  is given by

$$r \equiv 1 / \left[ \frac{\partial i}{\partial v} \right] = 1 / \left( k' \frac{W}{L} V_{ov} \right)$$

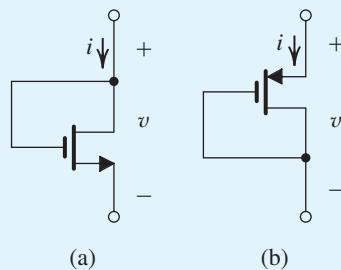


Figure P5.24

**5.25** For the circuit in Fig. P5.25, sketch  $i_D$  versus  $v_S$  for  $v_S$  varying from 0 to  $V_{DD}$ . Clearly label your sketch.

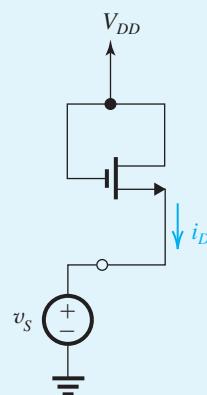


Figure P5.25

**5.26** For the circuit in Fig. P5.26, find an expression for  $v_{DS}$  in terms of  $i_D$ . Sketch and clearly label a graph for  $v_{DS}$  versus  $i_D$ .

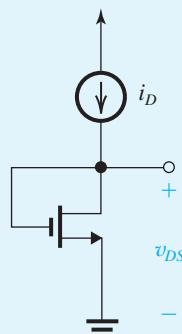


Figure P5.26

Case	Voltage (V)						Region of operation
	$V_s$	$V_g$	$V_d$	$V_{gs}$	$V_{ov}$	$V_{ds}$	
a	+1.0	+1.0	+2.0				
b	+1.0	+2.5	+2.0				
c	+1.0	+2.5	+1.5				
d	+1.0	+1.5	0				
e	0	+2.5	+1.0				
f	+1.0	+1.0	+1.0				
g	-1.0	0	0				
h	-1.5	0	0				
i	-1.0	0	+1.0				
j	+0.5	+2.0	+0.5				

\*5.27 The table above lists 10 different cases labeled (a) to (j) for operating an NMOS transistor with  $V_t = 1$  V. In each case the voltages at the source, gate, and drain (relative to the circuit ground) are specified. You are required to complete the table entries. Note that if you encounter a case for which  $v_{ds}$  is negative, you should exchange the drain and source before solving the problem. You can do this because the MOSFET is a symmetric device.

5.28 The NMOS transistor in Fig. P5.28 has  $V_t = 0.4$  V and  $k_n'(W/L) = 1$  mA/V<sup>2</sup>. Sketch and clearly label  $i_D$  versus  $v_G$  with  $v_G$  varying in the range 0 to +1.8 V. Give equations for the various portions of the resulting graph.

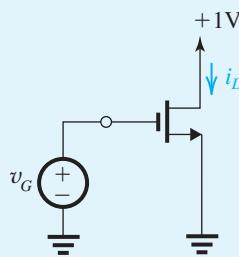


Figure P5.28

5.29 Figure P5.29 shows two NMOS transistors operating in saturation at equal  $V_{gs}$  and  $V_{ds}$ .

- If the two devices are matched except for a maximum possible mismatch in their  $W/L$  ratios of 3%, what is the maximum resulting mismatch in the drain currents?
- If the two devices are matched except for a maximum possible mismatch in their  $V_t$  values of 10 mV, what is the maximum resulting mismatch in the drain currents? Assume that the nominal value of  $V_t$  is 0.6 V.

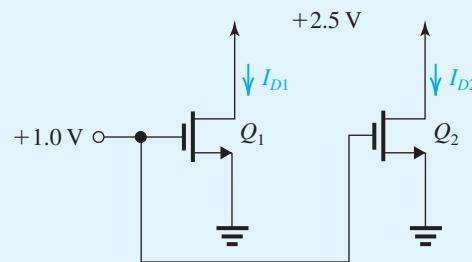


Figure P5.29

**5.30** For a particular MOSFET operating in the saturation region at a constant  $v_{GS}$ ,  $i_D$  is found to be 0.5 mA for  $v_{DS} = 1$  V and 0.52 mA for  $v_{DS} = 2$  V. What values of  $r_o$ ,  $V_A$ , and  $\lambda$  correspond?

**5.31** A particular MOSFET has  $V_A = 20$  V. For operation at 0.1 mA and 1 mA, what are the expected output resistances? In each case, for a change in  $v_{DS}$  of 1 V, what percentage change in drain current would you expect?

**D 5.32** In a particular IC design in which the standard channel length is 1  $\mu\text{m}$ , an NMOS device with  $W/L$  of 10 operating at 200  $\mu\text{A}$  is found to have an output resistance of 100  $\text{k}\Omega$ , about  $\frac{1}{5}$  of that needed. What dimensional change can be made to solve the problem? What is the new device length? The new device width? The new  $W/L$  ratio? What is  $V_A$  for the standard device in this IC? The new device?

**D 5.33** For a particular  $n$ -channel MOS technology, in which the minimum channel length is 0.5  $\mu\text{m}$ , the associated value of  $\lambda$  is  $0.03 \text{ V}^{-1}$ . If a particular device for which  $L$  is 1.5  $\mu\text{m}$  operates in saturation at  $v_{DS} = 1$  V with a drain current of 100  $\mu\text{A}$ , what does the drain current become if  $v_{DS}$  is raised to 5 V? What percentage change does this represent? What can be done to reduce the percentage by a factor of 2?

**5.34** An NMOS transistor is fabricated in a 0.5- $\mu\text{m}$  process having  $k'_n = 200 \mu\text{A/V}^2$  and  $V'_A = 20 \text{ V}/\mu\text{m}$  of channel length. If  $L = 1.5 \mu\text{m}$  and  $W = 15 \mu\text{m}$ , find  $V_A$  and  $\lambda$ . Find the value of  $I_D$  that results when the device is operated with an overdrive voltage of 0.5 V and  $V_{DS} = 2$  V. Also, find the value of  $r_o$  at this operating point. If  $V_{DS}$  is increased by 1 V, what is the corresponding change in  $I_D$ ?

**5.35** If in an NMOS transistor, both  $W$  and  $L$  are quadrupled and  $V_{ov}$  is halved, by what factor does  $r_o$  change?

**D 5.36** Consider the circuit in Fig. P5.29 with both transistors perfectly matched but with the dc voltage at the drain of  $Q_1$  lowered to +2 V. If the two drain currents are to be matched within 1% (i.e., the maximum difference allowed between the two currents is 1%), what is the minimum required value of  $V_A'$ ? If the technology is specified to have  $V'_A = 100 \text{ V}/\mu\text{m}$ , what is the minimum channel length the designer must use?

**5.37** Complete the missing entries in the following table, which describes characteristics of suitably biased NMOS transistors:

MOS	1	2	3	4
$\lambda (\text{V}^{-1})$		0.02		
$V_A (\text{V})$	20			100
$I_D (\text{mA})$	0.5		0.1	
$r_o (\text{k}\Omega)$		25	100	500

**5.38** A PMOS transistor has  $k'_p(W/L) = 100 \mu\text{A/V}^2$ ,  $V_t = -1.0 \text{ V}$ , and  $\lambda = -0.02 \text{ V}^{-1}$ . The gate is connected to ground and the source to +5 V. Find the drain current for  $v_D = +4 \text{ V}$ , +2 V, +1 V, 0 V, and -5 V.

**5.39** A  $p$ -channel transistor for which  $|V_t| = 0.8 \text{ V}$  and  $|V_A| = 40 \text{ V}$  operates in saturation with  $|v_{GS}| = 3 \text{ V}$ ,  $|v_{DS}| = 4 \text{ V}$ , and  $i_D = 3 \text{ mA}$ . Find corresponding signed values for  $v_{GS}$ ,  $v_{SG}$ ,  $v_{DS}$ ,  $v_{SD}$ ,  $V_t$ ,  $V_A$ ,  $\lambda$ , and  $k'_p(W/L)$ .

**5.40** The table below lists the terminal voltages of a PMOS transistor in six cases, labeled a, b, c, d, e, and f. The transistor has  $V_{tp} = -1 \text{ V}$ . Complete the table entries.

	$V_S$	$V_G$	$V_D$	$V_{SG}$	$ V_{ov} $	$V_{SD}$	Region of operation
a	+2	+2	0				
b	+2	+1	0				
c	+2	0	0				
d	+2	0	+1				
e	+2	0	+1.5				
f	+2	0	+2				

**5.41** The PMOS transistor in Fig. P5.41 has  $V_{tp} = -0.5$  V. As the gate voltage  $v_G$  is varied from +3 V to 0 V, the transistor moves through all of its three possible modes of operation. Specify the values of  $v_G$  at which the device changes modes of operation.

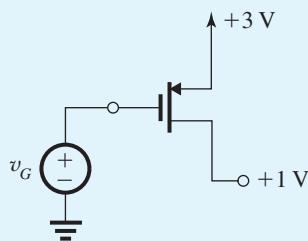


Figure P5.41

**\*5.42** Various NMOS and PMOS transistors, numbered 1 to 4, are measured in operation, as shown in the table at the bottom of the page. For each transistor, find the values of  $\mu C_{ox} W/L$  and  $V_t$  that apply and complete the table, with  $V$  in volts,  $I$  in  $\mu\text{A}$ , and  $\mu C_{ox} W/L$  in  $\mu\text{A}/\text{V}^2$ . Assume  $\lambda = 0$ .

**\*5.43** All the transistors in the circuits shown in Fig. P5.43 have the same values of  $|V_t|$ ,  $k'$ ,  $W/L$ , and  $\lambda$ . Moreover,  $\lambda$  is negligibly small. All operate in saturation at  $I_D = I$  and  $|V_{GS}| = |V_{DS}| = 1$  V. Find the voltages  $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$ . If  $|V_t| = 0.5$  V and  $I = 0.1$  mA, how large a resistor can be inserted in series with each drain while maintaining saturation? If the current source  $I$  requires at least 0.5 V between its terminals to operate properly, what is the largest resistor that can be placed in series with each MOSFET source while ensuring

saturated-mode operation of each transistor at  $I_D = I$ ? In the latter limiting situation, what do  $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$  become?

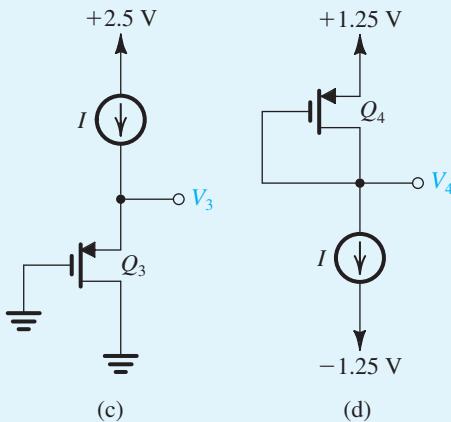
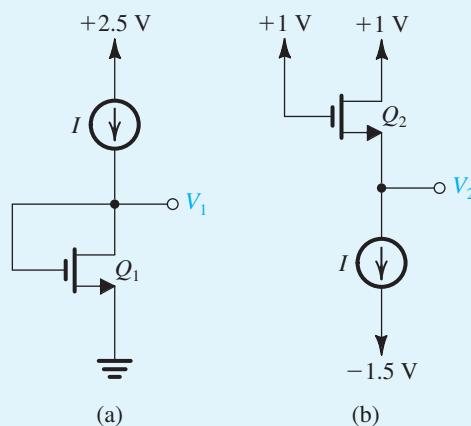


Figure P5.43

Case	Transistor	$V_s$	$V_g$	$V_d$	$I_d$	Type	Mode	$\mu C_{ox} W/L$	$V_t$
a	1	0	1	2.5	100				
	1	0	1.5	2.5	400				
b	2	5	3	-4.5	50				
	2	5	2	-0.5	450				
c	3	5	3	4	200				
	3	5	2	0	800				
d	4	-2	0	0	72				
	4	-4	0	-3	270				

### Section 5.3: MOSFET Circuits at DC

Note: If  $\lambda$  is not specified, assume it is zero.

- D 5.44** Design the circuit of Fig. P5.44 to establish a drain current of 0.1 mA and a drain voltage of +0.3 V. The MOSFET has  $V_t = 0.5$  V,  $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ ,  $L = 0.4 \mu\text{m}$ , and  $W = 5 \mu\text{m}$ . Specify the required values for  $R_s$  and  $R_d$ .

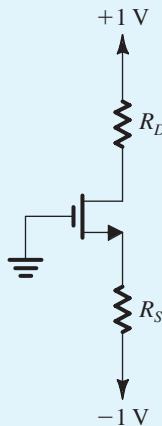


Figure P5.44

- 5.45** The NMOS transistor in the circuit of Fig. P5.44 has  $V_t = 0.4$  V and  $k_n = 4 \text{ mA/V}^2$ . The voltages at the source and the drain are measured and found to be  $-0.6$  V and  $+0.2$  V, respectively. What current  $I_D$  is flowing, and what must the values of  $R_d$  and  $R_s$  be? What is the largest value for  $R_d$  for which  $I_D$  remains unchanged from the value found?

- D 5.46** For the circuit in Fig. E5.10, assume that  $Q_1$  and  $Q_2$  are matched except for having different widths,  $W_1$  and  $W_2$ . Let  $V_t = 0.5$  V,  $k'_n = 0.4 \text{ mA/V}^2$ ,  $L_1 = L_2 = 0.36 \mu\text{m}$ ,  $W_1 = 1.44 \mu\text{m}$ , and  $\lambda = 0$ .

- Find the value of  $R$  required to establish a current of  $50 \mu\text{A}$  in  $Q_1$ .
- Find  $W_2$  and  $R_2$  so that  $Q_2$  operates at the edge of saturation with a current of  $0.5$  mA.

- 5.47** The transistor in the circuit of Fig. P5.47 has  $k'_n = 0.4 \text{ mA/V}^2$ ,  $V_t = 0.4$  V, and  $\lambda = 0$ . Show that operation at the

edge of saturation is obtained when the following condition is satisfied:

$$\left(\frac{W}{L}\right)R_D \simeq 2.5 \text{ k}\Omega$$

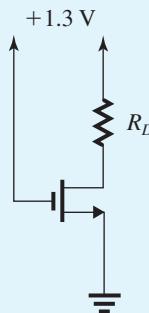


Figure P5.47

- D 5.48** It is required to operate the transistor in the circuit of Fig. P5.47 at the edge of saturation with  $I_D = 0.1$  mA. If  $V_t = 0.4$  V, find the required value of  $R_D$ .

- D 5.49** The PMOS transistor in the circuit of Fig. P5.49 has  $V_t = -0.5$  V,  $\mu_p C_{ox} = 100 \mu\text{A/V}^2$ ,  $L = 0.18 \mu\text{m}$ , and  $\lambda = 0$ . Find the values required for  $W$  and  $R$  in order to establish a drain current of  $180 \mu\text{A}$  and a voltage  $V_D$  of  $1$  V.

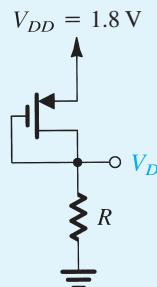


Figure P5.49

- D 5.50** The NMOS transistors in the circuit of Fig. P5.50 have  $V_t = 0.5$  V,  $\mu_n C_{ox} = 250 \mu\text{A/V}^2$ ,  $\lambda = 0$ , and  $L_1 = L_2 = 0.25 \mu\text{m}$ . Find the required values of gate width for each of  $Q_1$

and  $Q_2$ , and the value of  $R$ , to obtain the voltage and current values indicated.

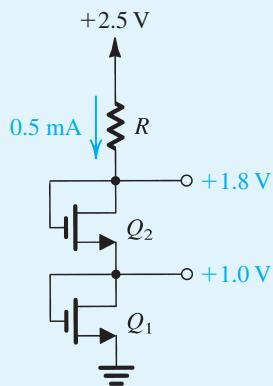


Figure P5.50

**D 5.51** The NMOS transistors in the circuit of Fig. P5.51 have  $V_t = 0.5$  V,  $\mu_n C_{ox} = 90 \mu\text{A/V}^2$ ,  $\lambda = 0$ , and  $L_1 = L_2 = L_3 = 0.5 \mu\text{m}$ . Find the required values of gate width for each of  $Q_1$ ,  $Q_2$ , and  $Q_3$  to obtain the voltage and current values indicated.

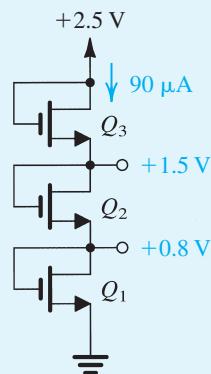


Figure P5.51

**5.52** Consider the circuit of Fig. 5.24(a). In Example 5.5 it was found that when  $V_t = 1$  V and  $k'_n(W/L) = 1 \text{ mA/V}^2$ ,

the drain current is 0.5 mA and the drain voltage is +7 V. If the transistor is replaced with another having  $V_t = 1.5$  V with  $k'_n(W/L) = 1.5 \text{ mA/V}^2$ , find the new values of  $I_D$  and  $V_D$ . Comment on how tolerant (or intolerant) the circuit is to changes in device parameters.

**D 5.53** Using a PMOS transistor with  $V_t = -1.5$  V,  $k'_p(W/L) = 4 \text{ mA/V}^2$ , and  $\lambda = 0$ , design a circuit that resembles that in Fig. 5.24(a). Using a 10-V supply, design for a gate voltage of +6 V, a drain current of 0.5 mA, and a drain voltage of +5 V. Find the values of  $R_s$  and  $R_d$ . Also, find the values of the resistances in the voltage divider feeding the gate, assuming a 1- $\mu\text{A}$  current in the divider.

**5.54** The MOSFET in Fig. P5.54 has  $V_t = 0.4$  V,  $k'_n = 500 \mu\text{A/V}^2$ , and  $\lambda = 0$ . Find the required values of  $W/L$  and of  $R$  so that when  $v_i = V_{DD} = +1.3$  V,  $r_{DS} = 50 \Omega$  and  $v_o = 50 \text{ mV}$ .

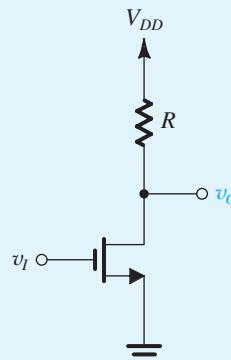


Figure P5.54

**5.55** In the circuits shown in Fig. P5.55, transistors are characterized by  $|V_t| = 1$  V,  $k'W/L = 4 \text{ mA/V}^2$ , and  $\lambda = 0$ .

- Find the labeled voltages  $V_1$  through  $V_7$ .
- In each of the circuits, replace the current source with a resistor. Select the resistor value to yield a current as close to that of the current source as possible, while using resistors specified in the 1% table provided in Appendix J.

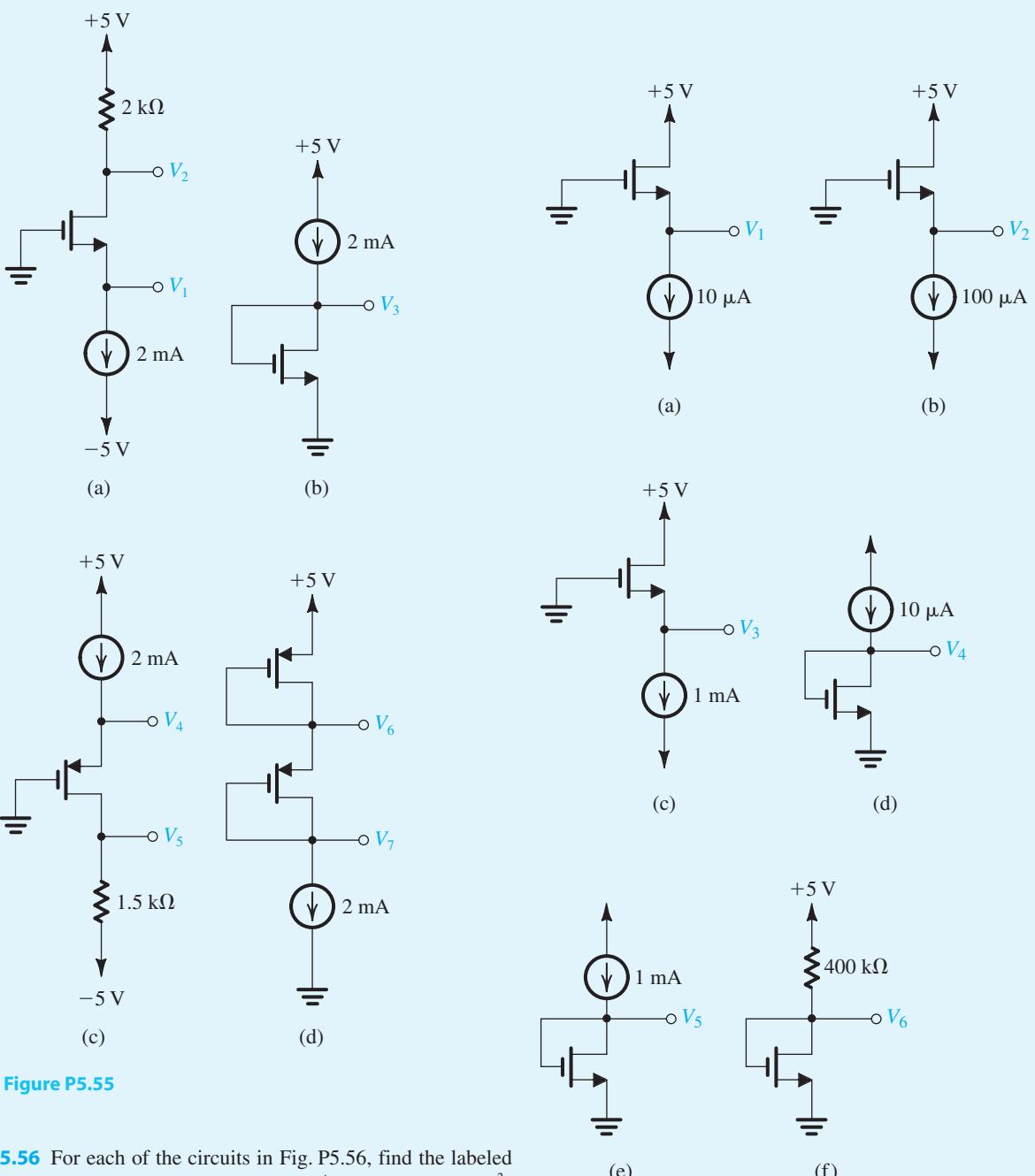


Figure P5.55

**5.56** For each of the circuits in Fig. P5.56, find the labeled node voltages. For all transistors,  $k'_n(W/L) = 0.5 \text{ mA/V}^2$ ,  $V_t = 0.8 \text{ V}$ , and  $\lambda = 0$ .

Figure P5.56 continued

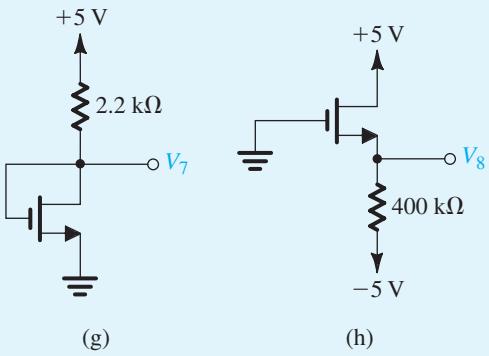


Figure P5.56 continued

**5.57** For each of the circuits shown in Fig. P5.57, find the labeled node voltages. The NMOS transistors have  $V_t = 0.9\text{ V}$  and  $k'_n(W/L) = 1.5\text{ mA/V}^2$ .

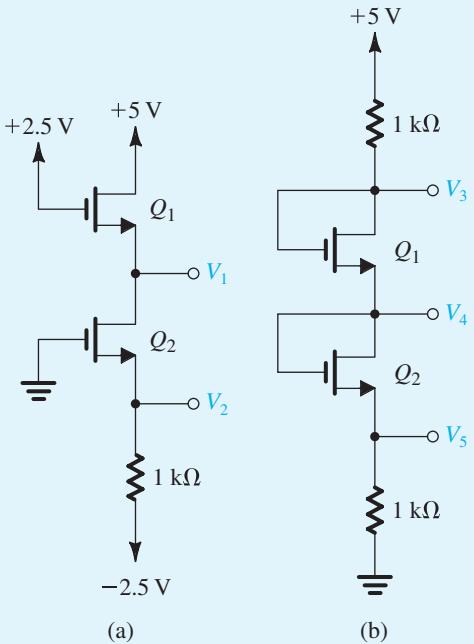


Figure P5.57

**\*5.58** For the circuit in Fig. P5.58:

- (a) Show that for the PMOS transistor to operate in saturation, the following condition must be satisfied:

$$IR \leq |V_{tp}|$$

- (b) If the transistor is specified to have  $|V_{tp}| = 1\text{ V}$  and  $k_p = 0.2\text{ mA/V}^2$ , and for  $I = 0.1\text{ mA}$ , find the voltages  $V_{SD}$  and  $V_{SG}$  for  $R = 0, 10\text{ k}\Omega, 30\text{ k}\Omega$ , and  $100\text{ k}\Omega$ .

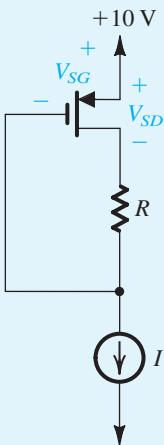


Figure P5.58

**5.59** For the circuits in Fig. P5.59,  $\mu_n C_{ox} = 3\mu_p C_{ox} = 270\text{ }\mu\text{A/V}^2$ ,  $|V_t| = 0.5\text{ V}$ ,  $\lambda = 0$ ,  $L = 1\text{ }\mu\text{m}$ , and  $W = 3\text{ }\mu\text{m}$ , unless otherwise specified. Find the labeled currents and voltages.

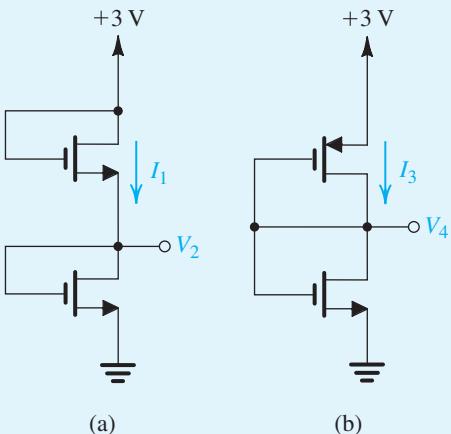


Figure P5.59

**SIM \*5.60** For the devices in the circuit of Fig. P5.60,  $|V_t| = 1$  V,  $\lambda = 0$ ,  $\mu_n C_{ox} = 50 \mu\text{A/V}^2$ ,  $L = 1 \mu\text{m}$ , and  $W = 10 \mu\text{m}$ . Find  $V_2$  and  $I_2$ . How do these values change if  $Q_3$  and  $Q_4$  are made to have  $W = 100 \mu\text{m}$ ?

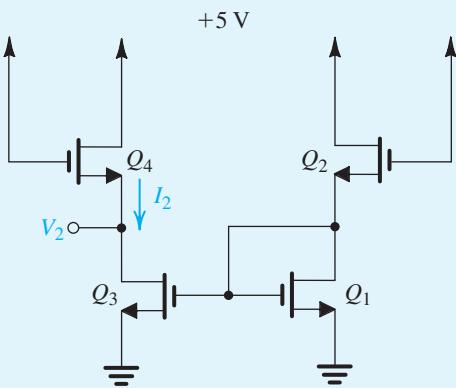


Figure P5.60

**5.61** In the circuit of Fig. P5.61, transistors  $Q_1$  and  $Q_2$  have  $V_t = 0.7$  V, and the process transconductance parameter  $k'_n = 125 \mu\text{A/V}^2$ . Find  $V_1$ ,  $V_2$ , and  $V_3$  for each of the following cases:

- (a)  $(W/L)_1 = (W/L)_2 = 20$
- (b)  $(W/L)_1 = 1.5(W/L)_2 = 20$

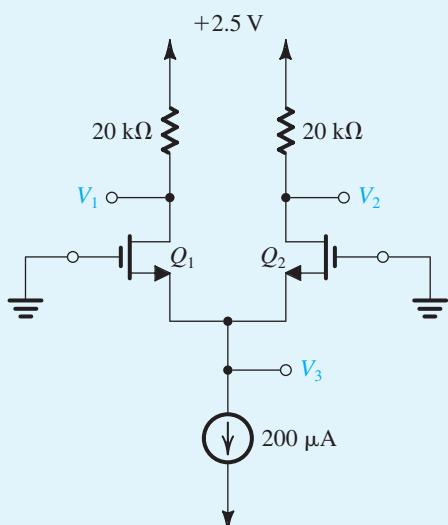


Figure P5.61

## Section 5.4: The Body Effect and Other Topics

**5.62** In a particular application, an *n*-channel MOSFET operates with  $V_{SB}$  in the range 0 V to 4 V. If  $V_{t0}$  is nominally 1.0 V, find the range of  $V_t$  that results if  $\gamma = 0.5 \text{ V}^{1/2}$  and  $2\phi_f = 0.6$  V. If the gate oxide thickness is increased by a factor of 4, what does the threshold voltage become?

**5.63** A *p*-channel transistor operates in saturation with its source voltage 3 V lower than its substrate. For  $\gamma = 0.5 \text{ V}^{1/2}$ ,  $2\phi_f = 0.75$  V, and  $V_{t0} = -0.7$  V, find  $V_t$ .

**\*5.64** (a) Using the expression for  $i_D$  in saturation and neglecting the channel-length modulation effect (i.e., let  $\lambda = 0$ ), derive an expression for the per unit change in  $i_D$  per  $^\circ\text{C}$   $[(\partial i_D/i_D)/\partial T]$  in terms of the per unit change in  $k'_n$  per  $^\circ\text{C}$   $[(\partial k'_n/k'_n)/\partial T]$ , the temperature coefficient of  $V_t$  in  $\text{V}/^\circ\text{C}$   $(\partial V_t/\partial T)$ , and  $V_{GS}$  and  $V_t$ .

(b) If  $V_t$  decreases by 2 mV for every  $^\circ\text{C}$  rise in temperature, find the temperature coefficient of  $k'_n$  that results in  $i_D$  decreasing by 0.2%/ $^\circ\text{C}$  when the NMOS transistor with  $V_t = 1$  V is operated at  $V_{GS} = 5$  V.

**5.65** A depletion-type *n*-channel MOSFET with  $k'_n W/L = 2 \text{ mA/V}^2$  and  $V_t = -3$  V has its source and gate grounded. Find the region of operation and the drain current for  $v_D = 0.1$  V, 1 V, 3 V, and 5 V. Neglect the channel-length-modulation effect.

**5.66** For a particular depletion-mode NMOS device,  $V_t = -2$  V,  $k'_n W/L = 200 \mu\text{A/V}^2$ , and  $\lambda = 0.02 \text{ V}^{-1}$ . When operated at  $v_{GS} = 0$ , what is the drain current that flows for  $v_{DS} = 1$  V, 2 V, 3 V, and 10 V? What does each of these currents become if the device width is doubled with  $L$  the same? With  $L$  also doubled?

**\*5.67** Neglecting the channel-length-modulation effect, show that for the depletion-type NMOS transistor of Fig. P5.67, the  $i-v$  relationship is given by

$$\begin{aligned} i &= \frac{1}{2} k'_n (W/L) (v^2 - 2V_t v) && \text{for } v \geq V_t \\ i &= -\frac{1}{2} k'_n (W/L) V_t^2 && \text{for } v \leq V_t \end{aligned}$$

(Recall that  $V_t$  is negative.) Sketch the  $i-v$  relationship for the case:  $V_t = -2$  V and  $k'_n (W/L) = 2 \text{ mA/V}^2$ .

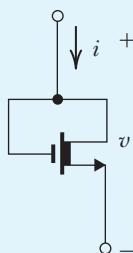


Figure P5.67

## CHAPTER 6

# Bipolar Junction Transistors (BJTs)

**Introduction 305**

**6.1 Device Structure and Physical Operation 306**

**6.2 Current–Voltage Characteristics 320**

**6.3 BJT Circuits at DC 333**

**6.4 Transistor Breakdown and Temperature Effects 351**

**Summary 354**

**Problems 355**

## IN THIS CHAPTER YOU WILL LEARN

1. The physical structure of the bipolar transistor and how it works.
  2. How the voltage between two terminals of the transistor controls the current that flows through the third terminal, and the equations that describe these current–voltage characteristics.
  3. How to analyze and design circuits that contain bipolar transistors, resistors, and dc sources.
- 

## Introduction

In this chapter, we study the other major three-terminal device: the bipolar junction transistor (BJT). The presentation of the material in this chapter parallels but does not rely on that for the MOSFET in Chapter 5; thus, if desired, the BJT can be studied before the MOSFET.

Three-terminal devices are far more useful than two-terminal ones, such as the diodes studied in Chapter 4, because they can be used in a multitude of applications, ranging from signal amplification to the design of digital logic and memory circuits. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way, a three-terminal device can be used to realize a controlled source, which as we learned in Chapter 1 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. The switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

The invention of the BJT in 1948 at the Bell Telephone Laboratories ushered in the era of solid-state circuits. The result was not just the replacement of vacuum tubes by transistors in radios and television sets but the eruption of an electronics revolution that led to major changes in the way we work, play, and indeed, live. The invention of the transistor also eventually led to the dominance of information technology and the emergence of the knowledge-based economy.

The bipolar transistor enjoyed nearly three decades as the device of choice in the design of both discrete and integrated circuits. Although the MOSFET had been known very early on, it was not until the 1970s and 1980s that it became a serious competitor to the BJT. By 2014, the MOSFET was undoubtedly the most widely used electronic device, and CMOS technology the technology of choice in the design of integrated circuits. Nevertheless, the BJT remains a significant device that excels in certain applications.

The BJT remains popular in discrete-circuit design, where it is used together with other discrete components such as resistors and capacitors to implement circuits that are assembled

on printed-circuit boards (PCBs). Here we note the availability of a very wide selection of BJT types that fit nearly every conceivable application. As well, the BJT is still the preferred device in some very demanding analog and digital integrated-circuit applications. This is especially true in very-high-frequency and high-speed circuits. In particular, a very-high-speed digital logic-circuit family based on bipolar transistors, namely, emitter-coupled logic, is still in use (Chapter 15). Finally, bipolar transistors can be combined with MOSFETs to create innovative circuits that take advantage of the high-input-impedance and low-power operation of MOSFETs and the very-high-frequency operation and high-current-driving capability of bipolar transistors. The resulting technology is known as BiCMOS, and it is finding increasingly larger areas of application (see Chapters 8, 9, 13, and 15).

In this chapter, we shall start with a description of the physical operation of the BJT. Though simple, this physical description provides considerable insight regarding the performance of the transistor as a circuit element. We then quickly move from describing current flow in terms of electrons and holes to a study of the transistor terminal characteristics. Circuit models for transistor operation in different modes will be developed and utilized in the analysis and design of transistor circuits. The main objective of this chapter is to develop in the reader a high degree of familiarity with the BJT. Thus, it lays the foundation for the use of the BJT in amplifier design (Chapter 7).

## 6.1 Device Structure and Physical Operation

### 6.1.1 Simplified Structure and Modes of Operation

Figure 6.1 shows a simplified structure for the BJT. A practical transistor structure will be shown later (see also Appendix A, which deals with fabrication technology).

As shown in Fig. 6.1, the BJT consists of three semiconductor regions: the emitter region (*n* type), the base region (*p* type), and the collector region (*n* type). Such a transistor is called an *npn* transistor. Another transistor, a dual of the *npn* as shown in Fig. 6.2, has a *p*-type emitter, an *n*-type base, and a *p*-type collector, and is appropriately called a *pnp* transistor.

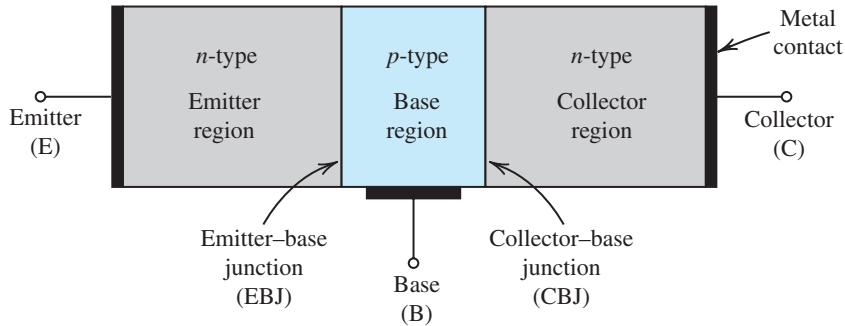
A terminal is connected to each of the three semiconductor regions of the transistor, with the terminals labeled **emitter** (E), **base** (B), and **collector** (C).

The transistor consists of two *pn* junctions, the **emitter-base junction** (EBJ) and the **collector-base junction** (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained, as shown in Table 6.1. The **active mode** is the one used if the transistor is to operate as an amplifier. Switching applications (e.g., logic circuits) utilize both the **cutoff mode** and the **saturation mode**. As the name implies, in the cutoff mode no current flows because both junctions are reverse biased.

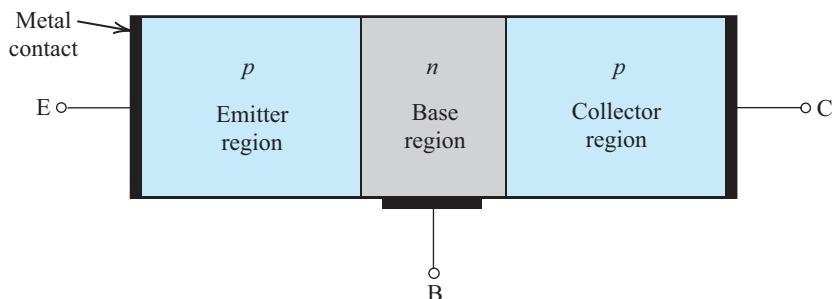
As we will see shortly, charge carriers of both polarities—that is, electrons and holes—participate in the current-conduction process in a bipolar transistor, which is the reason for the name *bipolar*.<sup>1</sup>

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<sup>1</sup>This should be contrasted with the situation in the MOSFET, where current is conducted by charge carriers of one type only: electrons in *n*-channel devices or holes in *p*-channel devices. In earlier days, some referred to FETs as unipolar devices.



**Figure 6.1** A simplified structure of the *npn* transistor.



**Figure 6.2** A simplified structure of the *pnp* transistor.

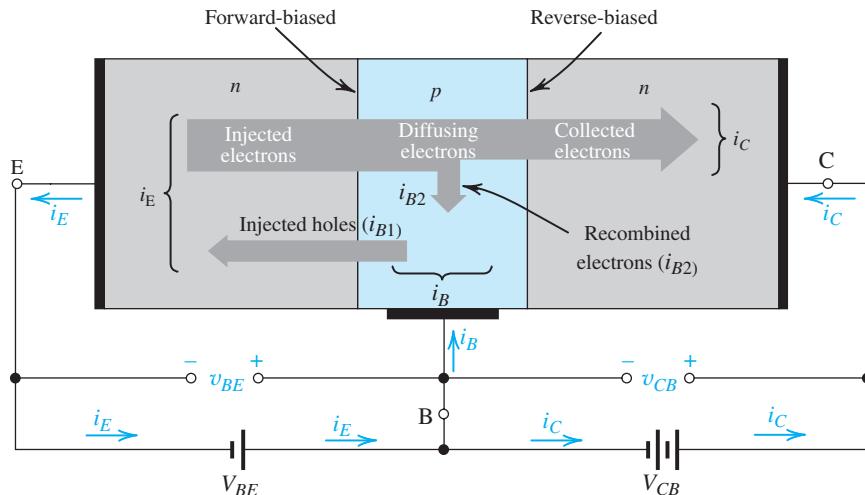
**Table 6.1** BJT Modes of Operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

### 6.1.2 Operation of the *npn* Transistor in the Active Mode

Of the three modes of operation of the BJT, the active mode is the most important. Therefore, we begin our study of the BJT by considering its physical operation in the active mode.<sup>2</sup> This situation is illustrated in Fig. 6.3 for the *npn* transistor. Two external voltage sources (shown as batteries) are used to establish the required bias conditions for active-mode operation. The voltage  $V_{BE}$  causes the *p*-type base to be higher in potential than the *n*-type emitter, thus forward biasing the emitter-base junction. The collector-base voltage  $V_{CB}$  causes the *n*-type collector to be at a higher potential than the *p*-type base, thus reverse biasing the collector-base junction.

<sup>2</sup>The material in this section assumes that the reader is familiar with the operation of the *pn* junction under forward-bias conditions (Section 3.5).



**Figure 6.3** Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

**Current Flow** The forward bias on the emitter–base junction will cause current to flow across this junction. Current will consist of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter. As will become apparent shortly, it is highly desirable to have the first component (electrons from emitter to base) be much larger than the second component (holes from base to emitter). This can be accomplished by fabricating the device with a heavily doped emitter and a lightly doped base; that is, the device is designed to have a high density of electrons in the emitter and a low density of holes in the base.

The current that flows across the emitter–base junction will constitute the emitter current  $i_E$ , as indicated in Fig. 6.3. The direction of  $i_E$  is “out of” the emitter lead, which, following the usual conventions, is in the direction of the positive-charge flow (hole current) and opposite to the direction of the negative-charge flow (electron current), with the emitter current  $i_E$  being equal to the sum of these two components. However, since the electron component is much larger than the hole component, the emitter current will be dominated by the electron component.

From our study in Section 3.5 of the current flow across a forward-biased *pn* junction, we know that the magnitude of both the electron component and the hole component of  $i_E$  will be proportional to  $e^{v_{BE}/V_T}$ , where  $v_{BE}$  is the forward voltage across the base–emitter junction and  $V_T$  is the thermal voltage (approximately 25 mV at room temperature).

Let’s now focus our attention on the first current component, namely, that carried by electrons injected from the emitter into the base. These electrons will be **minority carriers** in the *p*-type base region. Because their concentration will be highest at the emitter side of the base, the injected electrons will diffuse through the base region toward the collector. In their journey across the base, some of the electrons will combine with holes, which are majority carriers in the base. However, since the base is usually very thin and, as mentioned earlier, lightly doped, the proportion of electrons that are “lost” through this **recombination process** will be quite small. Thus, most of the diffusing electrons will reach the boundary of the collector–base depletion region. Because the collector is more positive than the base (by the

reverse-bias voltage  $v_{CB}$ ), these successful electrons will be swept across the CBJ depletion region into the collector. They will thus get collected and constitute the collector current  $i_C$ .

**The Collector Current** From the foregoing statements, we see that the collector current is carried by the electrons that reach the collector region. Its direction will be opposite to that of the flow of electrons, and thus into the collector terminal. Its magnitude will be proportional to  $e^{v_{BE}/V_T}$ , thus

$$i_C = I_S e^{v_{BE}/V_T} \quad (6.1)$$

where the constant of proportionality  $I_S$ , as in the case of the diode, is called the **saturation current** and is a transistor parameter. We will have more to say about  $I_S$  shortly.

An important observation to make here is that  $i_C$  is independent of the value of  $v_{CB}$ . That is, as long as the collector is positive with respect to the base, the electrons that reach the collector side of the base region will be swept into the collector and will register as collector current.

**The Base Current** Reference to Fig. 6.3 shows that the base current  $i_B$  is composed of two components. The first component  $i_{B1}$  is due to the holes injected from the base region into the emitter region. This current component is proportional to  $e^{v_{BE}/V_T}$ . The second component of base current,  $i_{B2}$ , is due to holes that have to be supplied by the external circuit in order to replace the holes lost from the base through the recombination process. Because  $i_{B2}$  is proportional to the number of electrons injected into the base, it also will be proportional to  $e^{v_{BE}/V_T}$ . Thus the total base current,  $i_B = i_{B1} + i_{B2}$ , will be proportional to  $e^{v_{BE}/V_T}$ , and can be expressed as a fraction of the collector current  $i_C$  as follows:

$$i_B = \frac{i_C}{\beta} \quad (6.2)$$

That is,

$$i_B = \left( \frac{I_S}{\beta} \right) e^{v_{BE}/V_T} \quad (6.3)$$

where  $\beta$  is a transistor parameter.

For modern *npn* transistors,  $\beta$  is in the range 50 to 200, but it can be as high as 1000 for special devices. For reasons that will become clear later, the parameter  $\beta$  is called the **common-emitter current gain**.

The above description indicates that the value of  $\beta$  is highly influenced by two factors: the width of the base region,  $W$ , and the relative dopings of the base region and the emitter region,  $N_A/N_D$ . To obtain a high  $\beta$  (which is highly desirable since  $\beta$  represents a gain parameter) the base should be thin ( $W$  small) and lightly doped and the emitter heavily doped (making  $N_A/N_D$  small). For modern integrated circuit fabrication technologies,  $W$  is in the nanometer range.

**The Emitter Current** Since the current that enters a transistor must leave it, it can be seen from Fig. 6.3 that the emitter current  $i_E$  is equal to the sum of the collector current  $i_C$  and the base current  $i_B$ ; that is,

$$i_E = i_C + i_B \quad (6.4)$$

Use of Eqs. (6.2) and (6.4) gives

$$i_E = \frac{\beta + 1}{\beta} i_C \quad (6.5)$$

That is,

$$i_E = \frac{\beta + 1}{\beta} I_S e^{v_{BE}/V_T} \quad (6.6)$$

Alternatively, we can express Eq. (6.5) in the form

➤  $i_C = \alpha i_E \quad (6.7)$

where the constant  $\alpha$  is related to  $\beta$  by

➤  $\alpha = \frac{\beta}{\beta + 1} \quad (6.8)$

Thus the emitter current in Eq. (6.6) can be written

➤  $i_E = (I_S/\alpha) e^{v_{BE}/V_T} \quad (6.9)$

Finally, we can use Eq. (6.8) to express  $\beta$  in terms of  $\alpha$ , that is,

➤  $\beta = \frac{\alpha}{1 - \alpha} \quad (6.10)$

It can be seen from Eq. (6.8) that  $\alpha$  is a constant (for a particular transistor) that is less than but very close to unity. For instance, if  $\beta = 100$ , then  $\alpha \simeq 0.99$ . Equation (6.10) reveals an important fact: Small changes in  $\alpha$  correspond to very large changes in  $\beta$ . This mathematical observation manifests itself physically, with the result that transistors of the same type may have widely different values of  $\beta$ . For reasons that will become apparent later,  $\alpha$  is called the **common-base current gain**.

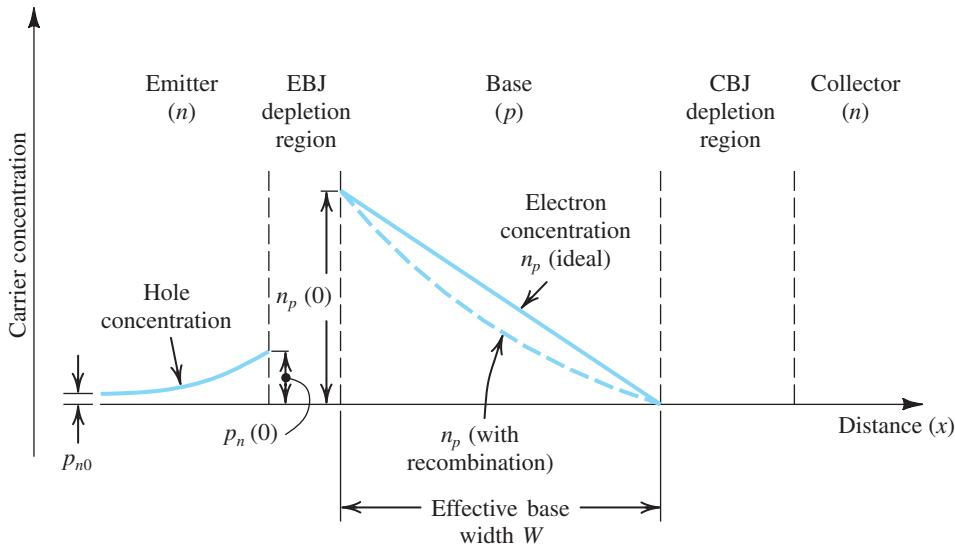
**Minority-Carrier Distribution** Our understanding of the physical operation of the BJT can be enhanced by considering the distribution of minority charge carriers in the base and the emitter. Figure 6.4 shows the profiles of the concentration of electrons in the base and holes in the emitter of an *npn* transistor operating in the active mode. Observe that since the doping concentration in the emitter,  $N_D$ , is much higher than the doping concentration in the base,  $N_A$ , the concentration of electrons injected from emitter to base,  $n_p(0)$ , is much higher than the concentration of holes injected from the base to the emitter,  $p_n(0)$ . Both quantities are proportional to  $e^{v_{BE}/V_T}$ , thus

$$n_p(0) = n_{p0} e^{v_{BE}/V_T} \quad (6.11)$$

where  $n_{p0}$  is the thermal-equilibrium value of the minority-carrier (electron) concentration in the base region.

Next, observe that because the base is very thin, the concentration of excess electrons decays almost linearly (as opposed to the usual exponential decay, as observed for the excess holes in the emitter region). Furthermore, the reverse bias on the collector–base junction causes the concentration of excess electrons at the collector side of the base to be zero. (Recall that electrons that reach that point are swept into the collector.)

The tapered minority-carrier concentration profile (Fig. 6.4) causes the electrons injected into the base to diffuse through the base region toward the collector. This electron diffusion



**Figure 6.4** Profiles of minority-carrier concentrations in the base and in the emitter of an *npn* transistor operating in the active mode:  $v_{BE} > 0$  and  $v_{CB} \geq 0$ .

current  $I_n$  is directly proportional to the slope of the straight-line concentration profile,

$$\begin{aligned} I_n &= A_E q D_n \frac{dn_p(x)}{dx} \\ &= A_E q D_n \left( -\frac{n_p(0)}{W} \right) \end{aligned} \quad (6.12)$$

where  $A_E$  is the cross-sectional area of the base–emitter junction (in the direction perpendicular to the page),  $q$  is the magnitude of the electron charge,  $D_n$  is the electron diffusivity in the base, and  $W$  is the effective width of the base. Observe that the negative slope of the minority-carrier concentration results in a negative current  $I_n$  across the base; that is,  $I_n$  flows from right to left (in the negative direction of  $x$ ), which corresponds to the usual convention, namely, opposite to the direction of electron flow.

The recombination in the base region, though slight, causes the excess minority-carrier concentration profile to deviate from a straight line and take the slightly concave shape indicated by the broken line in Fig. 6.4. The slope of the concentration profile at the EBJ is slightly higher than that at the CBJ, with the difference accounting for the small number of electrons lost in the base region through recombination.

Finally, we have the collector current  $i_C = I_n$ , which will yield a negative value for  $i_C$ , indicating that  $i_C$  flows in the negative direction of the  $x$  axis (i.e., from right to left). Since we will take this to be the positive direction of  $i_C$ , we can drop the negative sign in Eq. (6.12). Doing this and substituting for  $n_p(0)$  from Eq. (6.11), we can thus express the collector current  $i_C$  as

$$i_C = I_S e^{v_{BE}/V_T}$$

where the saturation current  $I_S$  is given by

$$I_S = A_E q D_n n_{p0}/W$$

Substituting  $n_{p0} = n_i^2/N_A$ , where  $n_i$  is the intrinsic carrier density and  $N_A$  is the doping concentration in the base, we can express  $I_S$  as

$$I_S = \frac{A_E q D_n n_i^2}{N_A W} \quad (6.13)$$

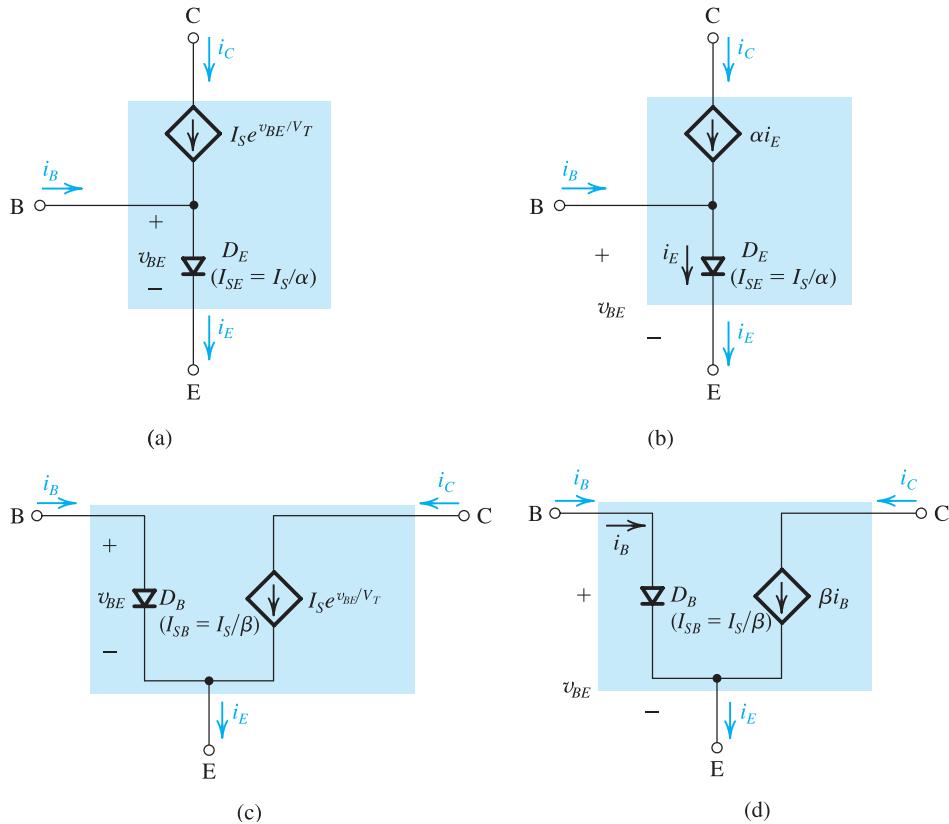
The saturation current  $I_S$  is inversely proportional to the base width  $W$  and is directly proportional to the area of the EBJ. Typically  $I_S$  is in the range of  $10^{-12}$  A to  $10^{-18}$  A (depending on the size of the device). Because  $I_S$  is proportional to  $n_i^2$ , it is a strong function of temperature, approximately doubling for every  $5^\circ\text{C}$  rise in temperature. (For the dependence of  $n_i^2$  on temperature, refer to Eq. 3.2.)

Since  $I_S$  is directly proportional to the junction area (i.e., the device size), it will also be referred to as the **scale current**. Two transistors that are identical except that one has an EBJ area, say, twice that of the other will have saturation currents with that same ratio (i.e., 2). Thus for the same value of  $v_{BE}$  the larger device will have a collector current twice that in the smaller device. This concept is frequently employed in integrated-circuit design.

**Recapitulation and Equivalent-Circuit Models** We have presented a first-order model for the operation of the *npn* transistor in the active mode. Basically, the forward-bias voltage  $v_{BE}$  causes an exponentially related current  $i_C$  to flow in the collector terminal. The collector current  $i_C$  is independent of the value of the collector voltage as long as the collector-base junction remains reverse biased; that is,  $v_{CB} \geq 0$ . Thus in the active mode the collector terminal behaves as an ideal constant-current source where the value of the current is determined by  $v_{BE}$ . The base current  $i_B$  is a factor  $1/\beta$  of the collector current, and the emitter current is equal to the sum of the collector and base currents. Since  $i_B$  is much smaller than  $i_C$  (i.e.,  $\beta \gg 1$ ),  $i_E \simeq i_C$ . More precisely, the collector current is a fraction  $\alpha$  of the emitter current, with  $\alpha$  smaller than, but close to, unity.

This first-order model of transistor operation in the active mode can be represented by the equivalent circuit shown in Fig. 6.5(a). Here, diode  $D_E$  has a scale current  $I_{SE}$  equal to  $(I_S/\alpha)$  and thus provides a current  $i_E$  related to  $v_{BE}$  according to Eq. (6.9). The current of the controlled source, which is equal to the collector current, is controlled by  $v_{BE}$  according to the exponential relationship indicated, a restatement of Eq. (6.1). This model is in essence a nonlinear voltage-controlled current source. It can be converted to the current-controlled current-source model shown in Fig. 6.5(b) by expressing the current of the controlled source as  $\alpha i_E$ . Note that this model is also nonlinear because of the exponential relationship of the current  $i_E$  through diode  $D_E$  and the voltage  $v_{BE}$ . From this model we observe that if the transistor is used as a two-port network with the input port between E and B and the output port between C and B (i.e., with B as a common terminal), then the current gain observed is equal to  $\alpha$ . Thus  $\alpha$  is called the common-base current gain.

Two other equivalent-circuit models, shown in Fig. 6.5(c) and (d), may be used to represent the operation of the BJT. The model of Fig. 6.5(c) is essentially a voltage-controlled current source. However, here diode  $D_B$  conducts the base current and thus its current scale factor is  $I_S/\beta$ , resulting in the  $i_B-v_{BE}$  relationship given in Eq. (6.3). By simply expressing the collector current as  $\beta i_B$  we obtain the current-controlled current-source model shown in Fig. 6.5(d). From this latter model we observe that if the transistor is used as a two-port network with the input port between B and E and the output port between C and E (i.e., with E as the common terminal), then the current gain observed is equal to  $\beta$ . Thus  $\beta$  is called the common-emitter current gain.



**Figure 6.5** Large-signal equivalent-circuit models of the *n*p*n* BJT operating in the forward active mode.

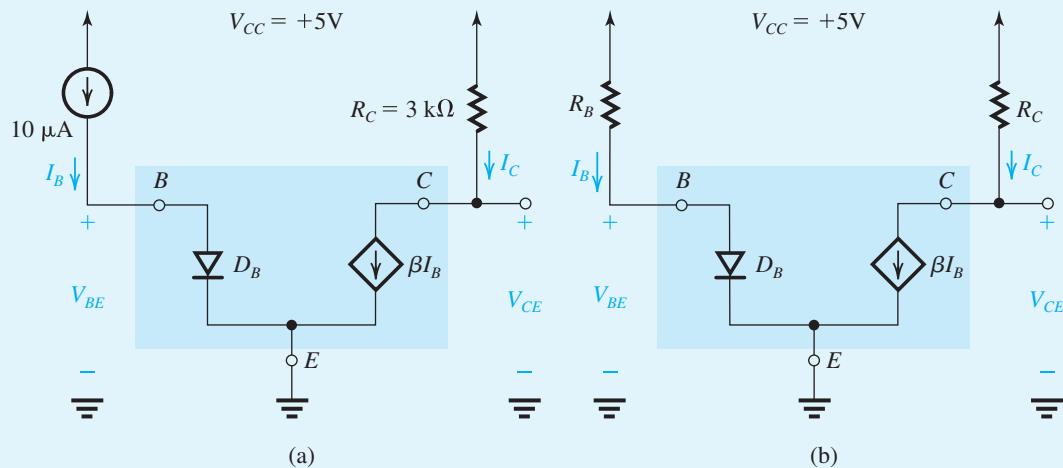
Finally, we note that the models in Fig. 6.5 apply for any positive value of  $v_{BE}$ . That is, unlike the models we will be discussing in Chapter 7, here there is no limitation on the size of  $v_{BE}$ , and thus these models are referred to as **large-signal models**.

### Example 6.1

An *n*p*n* transistor having  $I_S = 10^{-15}$  A and  $\beta = 100$  is connected as follows: The emitter is grounded, the base is fed with a constant-current source supplying a dc current of  $10 \mu\text{A}$ , and the collector is connected to a 5-V dc supply via a resistance  $R_C$  of  $3 \text{ k}\Omega$ . Assuming that the transistor is operating in the active mode, find  $V_{BE}$  and  $V_{CE}$ . Use these values to verify active-mode operation. Replace the current source with a resistance connected from the base to the 5-V dc supply. What resistance value is needed to result in the same operating conditions?

**Example 6.1** *continued***Solution**

If the transistor is operating in the active mode, it can be represented by one of the four possible equivalent-circuit models shown in Fig. 6.5. Because the emitter is grounded, either the model in Fig. 6.5(c) or that in Fig. 6.5(d) would be suitable. Since we know the base current  $I_B$ , the model of Fig. 6.5(d) is the most suitable.



**Figure 6.6** Circuits for Example 6.1.

Figure 6.6(a) shows the circuit as described with the transistor represented by the model of Fig. 6.5(d). We can determine  $V_{BE}$  from the exponential characteristic of  $D_B$  as follows:

$$\begin{aligned} V_{BE} &= V_T \ln \frac{I_B}{I_s/\beta} \\ &= 25 \ln \left( \frac{10 \times 10^{-6}}{10^{-17}} \right) \\ &= 690 \text{ mV} = 0.69 \text{ V} \end{aligned}$$

Next we determine the value of  $V_{CE}$  from

$$V_{CE} = V_{CC} - R_C I_C$$

where

$$I_C = \beta I_B = 100 \times 10 \times 10^{-6} = 10^{-3} \text{ A} = 1 \text{ mA}$$

Thus,

$$V_{CE} = 5 - 3 \times 1 = +2 \text{ V}$$

Since  $V_C$  at +2 V is higher than  $V_B$  at 0.69 V, the transistor is indeed operating in the active mode.

Now, replacing the 10- $\mu\text{A}$  current source with a resistance  $R_B$  connected from the base to the 5-V dc supply  $V_{CC}$ , as in Fig. 6.6(b), the value of  $R_B$  must be

$$\begin{aligned} R_B &= \frac{V_{CC} - V_{BE}}{I_B} \\ &= \frac{5 - 0.69}{10 \mu\text{A}} = 431 \text{ k}\Omega \end{aligned}$$

## EXERCISES

- 6.1** Consider an *npn* transistor with  $v_{BE} = 0.7 \text{ V}$  at  $i_C = 1 \text{ mA}$ . Find  $v_{BE}$  at  $i_C = 0.1 \text{ mA}$  and  $10 \text{ mA}$ .

**Ans.** 0.64 V; 0.76 V

- 6.2** Transistors of a certain type are specified to have  $\beta$  values in the range of 50 to 150. Find the range of their  $\alpha$  values.

**Ans.** 0.980 to 0.993

- 6.3** Measurement of an *npn* BJT in a particular circuit shows the base current to be  $14.46 \mu\text{A}$ , the emitter current to be  $1.460 \text{ mA}$ , and the base-emitter voltage to be  $0.7 \text{ V}$ . For these conditions, calculate  $\alpha$ ,  $\beta$ , and  $I_S$ .

**Ans.** 0.99; 100;  $10^{-15} \text{ A}$

- 6.4** Calculate  $\beta$  for two transistors for which  $\alpha = 0.99$  and 0.98. For collector currents of  $10 \text{ mA}$ , find the base current of each transistor.

**Ans.** 99; 49;  $0.1 \text{ mA}$ ;  $0.2 \text{ mA}$

- 6.5** A transistor for which  $I_S = 10^{-16} \text{ A}$  and  $\beta = 100$  is conducting a collector current of  $1 \text{ mA}$ . Find  $v_{BE}$ . Also, find  $I_{SE}$  and  $I_{SB}$  for this transistor.

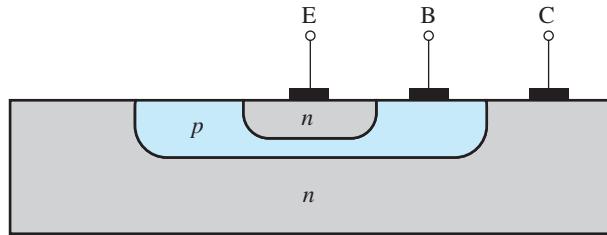
**Ans.** 747.5 mV;  $1.01 \times 10^{-16} \text{ A}$ ;  $10^{-18} \text{ A}$

- 6.6** For the circuit in Fig. 6.6(a) analyzed in Example 6.1, find the maximum value of  $R_C$  that will still result in active-mode operation.

**Ans.**  $4.31 \text{ k}\Omega$

### 6.1.3 Structure of Actual Transistors

Figure 6.7 shows a more realistic (but still simplified) cross section of an *npn* BJT. Note that the collector virtually surrounds the emitter region, thus making it difficult for the electrons injected into the thin base to escape being collected. In this way, the resulting  $\alpha$  is close to



**Figure 6.7** Cross section of an *npn* BJT.

unity and  $\beta$  is large. Also, observe that the device is *not* symmetrical, and thus the emitter and collector cannot be interchanged.<sup>3</sup> For more detail on the physical structure of actual devices, the reader is referred to Appendix A.

The structure in Fig. 6.7 indicates also that the CBJ has a much larger area than the EBJ. Thus the CB diode  $D_C$  has a saturation current  $I_{SC}$  that is much larger than the saturation current of the EB diode  $D_E$ . Typically,  $I_{SC}$  is 10 to 100 times larger than  $I_{SE}$  (recall that  $I_{SE} = I_S/\alpha \simeq I_S$ ).

### EXERCISE

- 6.7** A particular transistor has  $I_s = 10^{-15}$  A and  $\alpha \simeq 1$ . If the CBJ area is 100 times the area of the EBJ, find the collector scale current  $I_{SC}$ .

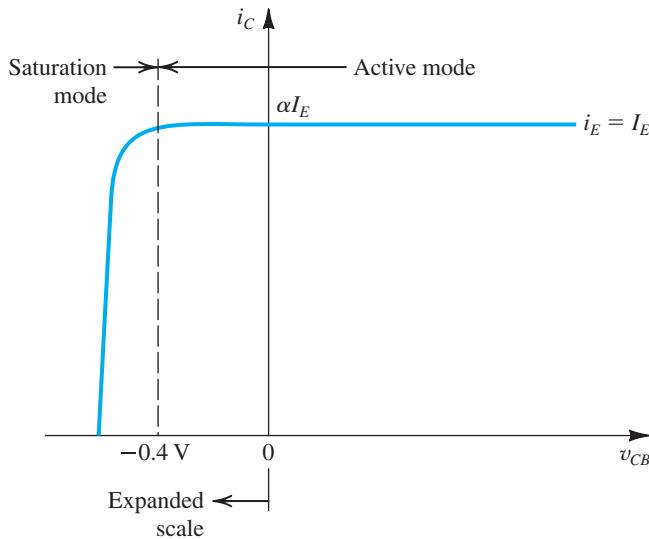
**Ans.**  $10^{-13}$  A

### 6.1.4 Operation in the Saturation Mode<sup>4</sup>

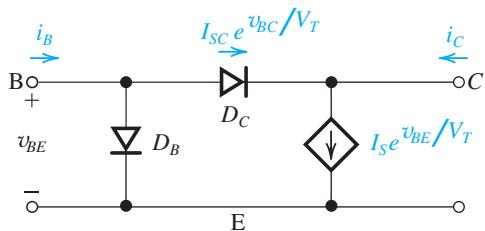
As mentioned above, for the BJT to operate in the active mode, the CBJ must be reverse biased. Thus far, we have stated this condition for the *npn* transistor as  $v_{CB} \geq 0$ . However, we know that a *pn* junction does not effectively become forward biased until the forward voltage across it exceeds approximately 0.4 V. It follows that one can maintain active-mode operation of an *npn* transistor for negative  $v_{CB}$  down to approximately  $-0.4$  V. This is illustrated in Fig. 6.8, which is a sketch of  $i_C$  versus  $v_{CB}$  for an *npn* transistor operated with a constant emitter current  $I_E$ . As expected,  $i_C$  is independent of  $v_{CB}$  in the active mode, a situation that extends

<sup>3</sup>If the emitter and collector are reversed—that is, the CBJ is forward biased and the EBJ is reverse biased—the device operates in a mode called the “reverse-active mode.” The resulting values of  $\alpha$  and  $\beta$ , denoted  $\alpha_R$  and  $\beta_R$  (with  $R$  denoting reverse), are much lower than the values of  $\alpha$  and  $\beta$ , respectively, obtained in the “forward”-active mode discussed above. Hence, the reverse-active mode has no practical application. The MOSFET, on the other hand, being a perfectly symmetrical device, can operate equally well with its drain and source terminals interchanged.

<sup>4</sup>Saturation means something completely different in a BJT and in a MOSFET. The saturation mode of operation of the BJT is analogous to the triode region of operation of the MOSFET. On the other hand, the saturation region of operation of the MOSFET corresponds to the active mode of BJT operation.



**Figure 6.8** The  $i_C$ - $v_{CB}$  characteristic of an *n*p*n* transistor fed with a constant emitter current  $I_E$ . The transistor enters the saturation mode of operation for  $v_{CB} < -0.4$  V, and the collector current diminishes.



**Figure 6.9** Modeling the operation of an *n*p*n* transistor in saturation by augmenting the model of Fig. 6.5(c) with a forward-conducting diode  $D_C$ . Note that the current through  $D_C$  increases  $i_B$  and reduces  $i_C$ .

for  $v_{CB}$  going negative to approximately  $-0.4$  V. Below this value of  $v_{CB}$ , the CBJ begins to conduct sufficiently that the transistor leaves the active mode and enters the saturation mode of operation, where  $i_C$  decreases.

To see why  $i_C$  decreases in saturation, we can construct a model for the saturated *n*p*n* transistor as follows. We augment the model of Fig. 6.5(c) with the forward-conducting CBJ diode  $D_C$ , as shown in Fig. 6.9. Observe that the current  $i_{BC}$  will subtract from the controlled-source current, resulting in the reduced collector current  $i_C$  given by

$$i_C = I_S e^{v_{BE}/V_T} - I_{sc} e^{v_{BC}/V_T} \quad (6.14)$$

where  $I_{sc}$  is the saturation current for  $D_C$  and is related to  $I_S$  by the ratio of the areas of the CBJ and the EBJ. The second term in Eq. (6.14) will play an increasing role as  $v_{BC}$  exceeds  $0.4$  V or so, causing  $i_C$  to decrease and eventually reach zero.

Figure 6.9 also indicates that in saturation the base current will increase to the value

$$i_B = (I_S/\beta) e^{v_{BE}/V_T} + I_{sc} e^{v_{BC}/V_T} \quad (6.15)$$

Equations (6.14) and (6.15) can be combined to obtain the ratio  $i_C/i_B$  for a saturated transistor. We observe that this ratio will be *lower* than the value of  $\beta$ . Furthermore, the ratio will decrease as  $v_{BC}$  is increased and the transistor is driven deeper into saturation. Because  $i_C/i_B$

of a saturated transistor can be set to any desired value lower than  $\beta$  by adjusting  $v_{BC}$ , this ratio is known as **forced**  $\beta$  and denoted  $\beta_{\text{forced}}$ ,

$$\Rightarrow \quad \beta_{\text{forced}} = \left. \frac{i_C}{i_B} \right|_{\text{saturation}} \leq \beta \quad (6.16)$$

As will be shown later, in analyzing a circuit we can determine whether the BJT is in the saturation mode by either of the following two tests:

1. Is the CBJ forward biased by more than 0.4 V?
2. Is the ratio  $i_C/i_B$  lower than  $\beta$ ?

The collector-to-emitter voltage  $v_{CE}$  of a saturated transistor can be found from Fig. 6.9 as the difference between the forward-bias voltages of the EBJ and the CBJ,

$$V_{CE\text{sat}} = V_{BE} - V_{BC} \quad (6.17)$$

Recalling that the CBJ has a much larger area than the EBJ,  $V_{BC}$  will be smaller than  $V_{BE}$  by 0.1 to 0.3 V. Thus,

$$\Rightarrow \quad V_{CE\text{sat}} \simeq 0.1 \text{ to } 0.3 \text{ V}$$

Typically we will assume that a transistor at the edge of saturation has  $V_{CE\text{sat}} = 0.3$  V, while a transistor deep in saturation has  $V_{CE\text{sat}} = 0.2$  V.

## EXERCISES

- 6.8** Use Eq. (6.14) to show that  $i_C$  reaches zero at

$$V_{CE} = V_T \ln(I_{SC}/I_S)$$

Calculate  $V_{CE}$  for a transistor whose CBJ has 100 times the area of the EBJ.

**Ans.** 115 mV

- 6.9** Use Eqs. (6.14), (6.15), and (6.16) to show that a BJT operating in saturation with  $V_{CE} = V_{CE\text{sat}}$  has a forced  $\beta$  given by

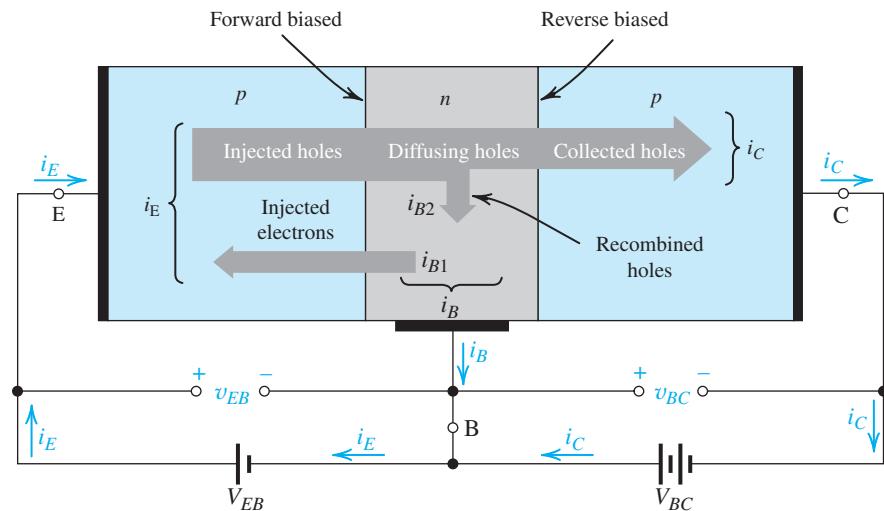
$$\beta_{\text{forced}} = \beta \frac{e^{V_{CE\text{sat}}/V_T} - I_{SC}/I_S}{e^{V_{CE\text{sat}}/V_T} + \beta I_{SC}/I_S}$$

Find  $\beta_{\text{forced}}$  for  $\beta = 100$ ,  $I_{SC}/I_S = 100$ , and  $V_{CE\text{sat}} = 0.2$  V.

**Ans.** 22.2

### 6.1.5 The *pnp* Transistor

The *pnp* transistor operates in a manner similar to that of the *npn* device described above. Figure 6.10 shows a *pnp* transistor biased to operate in the active mode. Here the voltage  $V_{EB}$  causes the *p*-type emitter to be higher in potential than the *n*-type base, thus forward biasing the emitter-base junction. The collector-base junction is reverse biased by the voltage  $V_{BC}$ , which keeps the *p*-type collector lower in potential than the *n*-type base.



**Figure 6.10** Current flow in a *pnp* transistor biased to operate in the active mode.

Unlike the *npn* transistor, current in the *pnp* device is mainly conducted by holes injected from the emitter into the base as a result of the forward-bias voltage  $V_{EB}$ . Since the component of emitter current contributed by electrons injected from base to emitter is kept small by using a lightly doped base, most of the emitter current will be due to holes. The electrons injected from base to emitter give rise to the first component of base current,  $i_{B1}$ . Also, a number of the holes injected into the base will recombine with the majority carriers in the base (electrons) and will thus be lost. The disappearing base electrons will have to be replaced from the external circuit, giving rise to the second component of base current,  $i_{B2}$ . The holes that succeed in reaching the boundary of the depletion region of the collector–base junction will be attracted by the negative voltage on the collector. Thus these holes will be swept across the depletion region into the collector and appear as collector current.

It can easily be seen from the above description that the current–voltage relationship of the *pnp* transistor will be identical to that of the *npn* transistor except that  $v_{BE}$  has to be replaced by  $v_{EB}$ . Also, the large-signal, active-mode operation of the *pnp* transistor can be modeled by any of four equivalent circuits similar to those for the *npn* transistor in Fig. 6.5. Two of these four circuits are shown in Fig. 6.11. Finally, we note that the *pnp* transistor can operate in the saturation mode in a manner analogous to that described for the *npn* device.

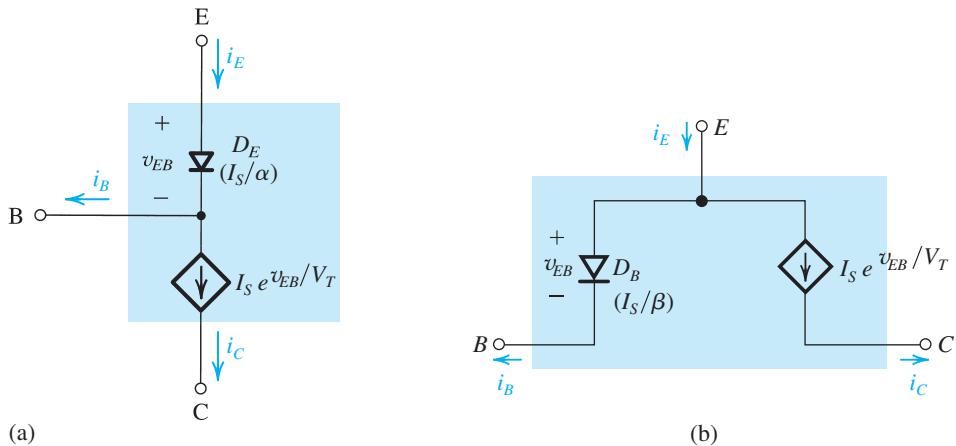
## EXERCISES

- 6.10** Consider the model in Fig. 6.11(a) applied in the case of a *pnp* transistor whose base is grounded, the emitter is fed by a constant-current source that supplies a 2-mA current into the emitter terminal, and the collector is connected to a -10-V dc supply. Find the emitter voltage, the base current, and the collector current if for this transistor  $\beta = 50$  and  $I_s = 10^{-14}$  A.

**Ans.** 0.650 V; 39.2  $\mu$ A; 1.96 mA

- 6.11** For a *pnp* transistor having  $I_s = 10^{-11}$  A and  $\beta = 100$ , calculate  $v_{EB}$  for  $i_C = 1.5$  A.

**Ans.** 0.643 V



**Figure 6.11** Two large-signal models for the *pnp* transistor operating in the active mode.

### THE INVENTION OF THE BJT:

The first working transistor was demonstrated at the Bell Labs in late 1947 by John Bardeen and Walter Brattain, who were part of a team led by William Shockley. Made of germanium, the device became known as a point-contact transistor and operated on the field-effect principle. Within a few weeks, however, Shockley wrote a complete description of the bipolar junction transistor (BJT) and filed for a U.S. patent with the title “Circuit Element Utilizing Semiconductor Material.”

BJTs dominated the electronics world from the early 1950s to the mid-1970s, when MOSFETs took over the leading position. In 1956, Shockley, Bardeen, and Brattain shared the Nobel Prize in Physics for the discovery of the transistor effect.

## 6.2 Current–Voltage Characteristics

### 6.2.1 Circuit Symbols and Conventions

The physical structure used thus far to explain transistor operation is rather cumbersome to employ in drawing the schematic of a multitransistor circuit. Fortunately, a very descriptive and convenient circuit symbol exists for the BJT. Figure 6.12(a) shows the symbol for the *npn* transistor; the *pnp* symbol is given in Fig. 6.12(b). In both symbols the emitter is distinguished by an arrowhead. This distinction is important because, as we have seen in the last section, practical BJTs are not symmetric devices.

The polarity of the device—*npn* or *pnp*—is indicated by the direction of the arrowhead on the emitter. This arrowhead points in the direction of normal current flow in the emitter, which is also the forward direction of the base–emitter junction. Since we have adopted a drawing convention by which currents flow from top to bottom, we will always draw *pnp* transistors in the manner shown in Fig. 6.12(b) (i.e., with their emitters on top).

Figure 6.13 shows *npn* and *pnp* transistors connected to dc sources so as to operate in the active mode. Figure 6.13 also indicates the reference and actual directions of current flow throughout the transistor. Our convention will be to take the reference direction to coincide

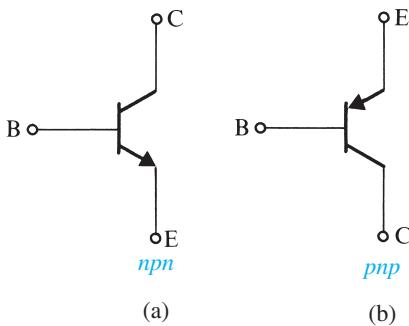


Figure 6.12 Circuit symbols for BJTs.

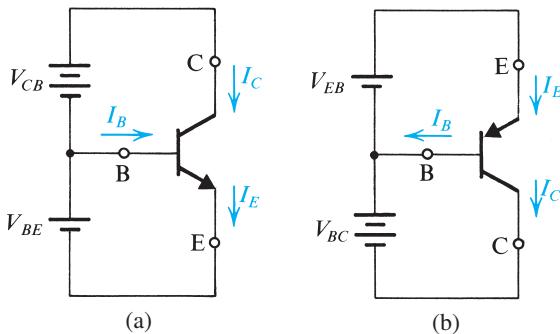


Figure 6.13 Voltage polarities and current flow in transistors operating in the active mode.

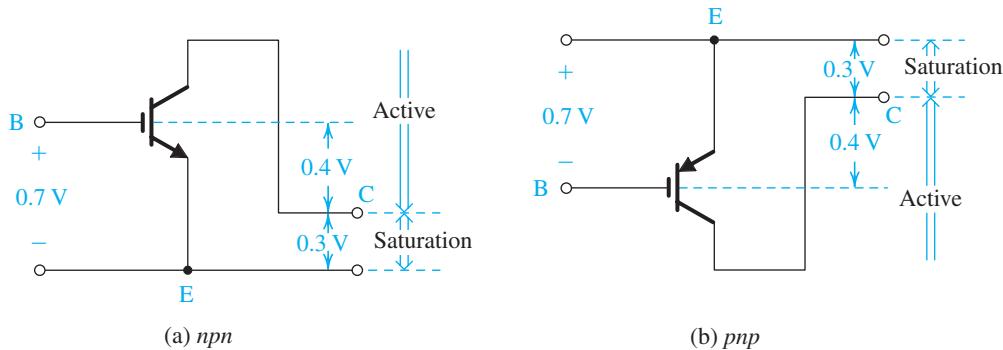
with the normal direction of current flow. Hence, normally, we should not encounter a negative value for  $i_E$ ,  $i_B$ , or  $i_C$ .

The convenience of the circuit-drawing convention that we have adopted should be obvious from Fig. 6.13. Note that currents flow from top to bottom and that voltages are higher at the top and lower at the bottom. The arrowhead on the emitter also implies the polarity of the emitter–base voltage that should be applied in order to forward bias the emitter–base junction. Just a glance at the circuit symbol of the *pnp* transistor, for example, indicates that we should make the emitter higher in voltage than the base (by  $v_{EB}$ ) in order to cause current to flow into the emitter (downward). Note that the symbol  $v_{EB}$  means the voltage by which the emitter (E) is higher than the base (B). Thus for a *pnp* transistor operating in the active mode  $v_{EB}$  is positive, while in an *npn* transistor  $v_{BE}$  is positive.

From the discussion of Section 6.1 it follows that an *npn* transistor whose EBJ is forward biased (usually,  $V_{BE} \simeq 0.7$  V) will operate in the active mode *as long as the collector voltage does not fall below that of the base by more than approximately 0.4 V*. Otherwise, the transistor leaves the active mode and enters the saturation region of operation.<sup>5</sup>

In a parallel manner, the *pnp* transistor will operate in the active mode *if the EBJ is forward biased (usually,  $V_{EB} \simeq 0.7$  V) and the collector voltage is not allowed to rise above that of the base by more than 0.4 V or so*. Otherwise, the CBJ becomes forward biased, and the *pnp* transistor enters the saturation region of operation.

<sup>5</sup>It is interesting to contrast the active-mode operation of the BJT with the corresponding mode of operation of the MOSFET: The BJT needs a minimum  $v_{CE}$  of about 0.3 V, and the MOSFET needs a minimum  $v_{DS}$  equal to  $V_{ov}$ , which for modern technologies is in the range of 0.2 V to 0.3 V. Thus we see a great deal of similarity! Also note that reverse biasing the CBJ of the BJT corresponds to pinching off the channel of the MOSFET. This condition results in the collector current (drain current in the MOSFET) being independent of the collector voltage (the drain voltage in the MOSFET).



**Figure 6.14** Graphical representation of the conditions for operating the BJT in the active mode and in the saturation mode.

**Table 6.2** Summary of the BJT Current–Voltage Relationships in the Active Mode

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace  $v_{BE}$  with  $v_{EB}$ .

$$i_C = \alpha i_E \quad i_B = (1 - \alpha)i_E = \frac{i_E}{\beta + 1}$$

$$i_C = \beta i_B \quad i_E = (\beta + 1)i_B$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$V_T = \text{thermal voltage} = \frac{kT}{q} \simeq 25 \text{ mV at room temperature}$$

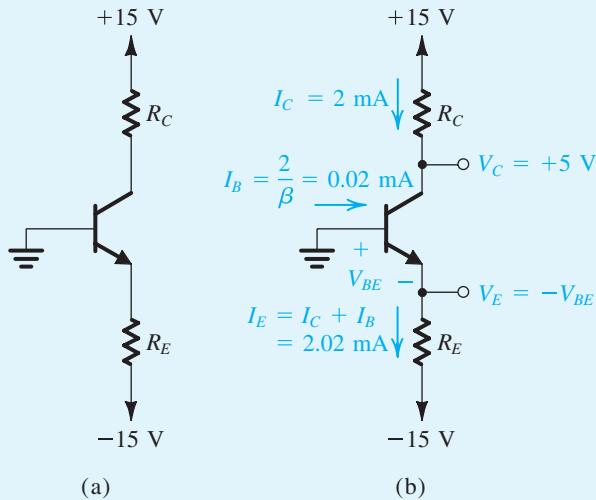
For greater emphasis, we show in Fig. 6.14 a graphical construction that illustrates the conditions for operating the BJT in the active mode and in the saturation mode. Also, for easy reference, we present in Table 6.2 a summary of the BJT current–voltage relationships in the active mode of operation.

**The Collector–Base Reverse Current ( $I_{CBO}$ )** In our discussion of current flow in transistors we ignored the small reverse currents carried by thermally generated minority carriers. Although such currents can be safely neglected in modern transistors, the reverse current across the collector–base junction deserves some mention. This current, denoted  $I_{CBO}$ , is the reverse current flowing from collector to base with the emitter open-circuited (hence the subscript  $O$ ). This current is usually in the nanoampere range, a value that is many times higher than its theoretically predicted value. As with the diode reverse current,  $I_{CBO}$  contains a substantial leakage component, and its value is dependent on  $v_{CB}$ .  $I_{CBO}$  depends strongly on temperature, approximately doubling for every  $10^\circ\text{C}$  rise.<sup>6</sup>

<sup>6</sup>The temperature coefficient of  $I_{CBO}$  is different from that of  $I_S$  because  $I_{CBO}$  contains a substantial leakage component.

### Example 6.2

The transistor in the circuit of Fig. 6.15(a) has  $\beta = 100$  and exhibits a  $v_{BE}$  of 0.7 V at  $i_c = 1$  mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +5 V appears at the collector.



**Figure 6.15** Circuit for Example 6.2.

### Solution

Refer to Fig. 6.15(b). We note at the outset that since we are required to design for  $V_c = +5$  V, the CBJ will be reverse biased and the BJT will be operating in the active mode. To obtain a voltage  $V_c = +5$  V, the voltage drop across  $R_c$  must be  $15 - 5 = 10$  V. Now, since  $I_c = 2$  mA, the value of  $R_c$  should be selected according to

$$R_c = \frac{10 \text{ V}}{2 \text{ mA}} = 5 \text{ k}\Omega$$

Since  $v_{BE} = 0.7$  V at  $i_c = 1$  mA, the value of  $v_{BE}$  at  $i_c = 2$  mA is

$$V_{BE} = 0.7 + V_T \ln\left(\frac{2}{1}\right) = 0.717 \text{ V}$$

Since the base is at 0 V, the emitter voltage should be

$$V_E = -0.717 \text{ V}$$

For  $\beta = 100$ ,  $\alpha = 100/101 = 0.99$ . Thus the emitter current should be

$$I_E = \frac{I_c}{\alpha} = \frac{2}{0.99} = 2.02 \text{ mA}$$

**Example 6.2** *continued*

Now the value required for  $R_E$  can be determined from

$$\begin{aligned} R_E &= \frac{V_E - (-15)}{I_E} \\ &= \frac{-0.717 + 15}{2.02} = 7.07 \text{ k}\Omega \end{aligned}$$

This completes the design. We should note, however, that the calculations above were made with a degree of precision that is usually neither necessary nor justified in practice in view, for instance, of the expected tolerances of component values. Nevertheless, we chose to do the design precisely in order to illustrate the various steps involved.

## EXERCISES

- D6.12** Repeat Example 6.2 for a transistor fabricated in a modern integrated-circuit process. Such a process yields devices that exhibit larger  $v_{BE}$  at the same  $i_C$  because they have much smaller junction areas. The dc power supplies utilized in modern IC technologies fall in the range of 1 V to 3 V. Design a circuit similar to that shown in Fig. 6.15 except that now the power supplies are  $\pm 1.5$  V and the BJT has  $\beta = 100$  and exhibits  $v_{BE}$  of 0.8 V at  $i_C = 1$  mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +0.5 V appears at the collector.

**Ans.**  $R_C = 500 \Omega$ ;  $R_E = 338 \Omega$

- 6.13** In the circuit shown in Fig. E6.13, the voltage at the emitter was measured and found to be -0.7 V. If  $\beta = 50$ , find  $I_E$ ,  $I_B$ ,  $I_C$ , and  $V_C$ .

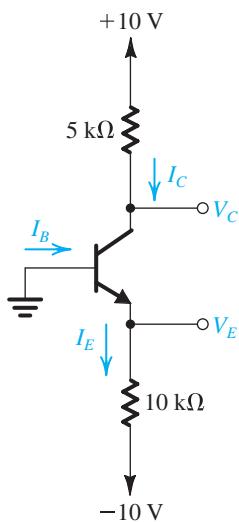


Figure E6.13

**Ans.** 0.93 mA; 18.2 μA; 0.91 mA; +5.45 V

- 6.14** In the circuit shown in Fig. E6.14, measurement indicates  $V_B$  to be +1.0 V and  $V_E$  to be +1.7 V. What are  $\alpha$  and  $\beta$  for this transistor? What voltage  $V_C$  do you expect at the collector?

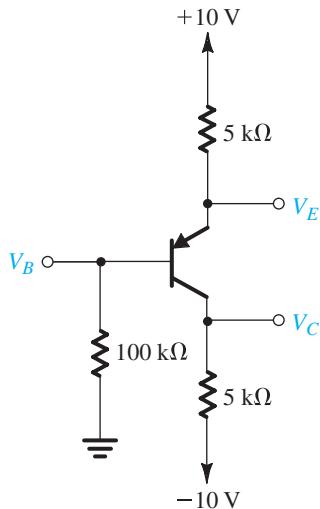


Figure E6.14

**Ans.** 0.994; 165; -1.75 V

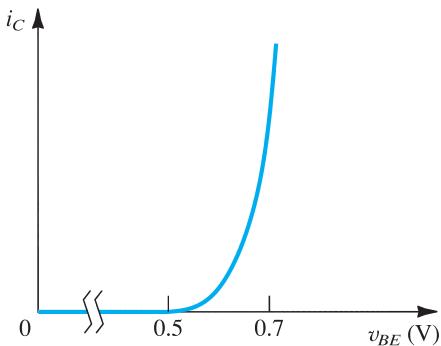
## 6.2.2 Graphical Representation of Transistor Characteristics

It is sometimes useful to describe the transistor  $i$ - $v$  characteristics graphically. Figure 6.16 shows the  $i_C$ - $v_{BE}$  characteristic, which is the exponential relationship

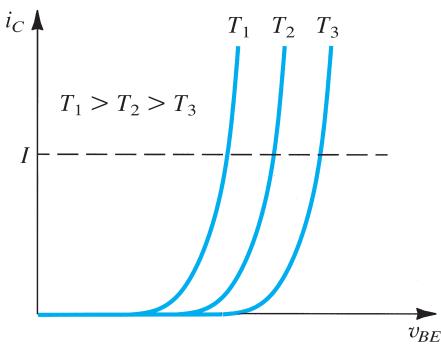
$$i_C = I_S e^{v_{BE}/V_T}$$

which is identical to the diode  $i$ - $v$  relationship. The  $i_E$ - $v_{BE}$  and  $i_B$ - $v_{BE}$  characteristics are also exponential but with different scale currents:  $I_S/\alpha$  for  $i_E$ , and  $I_S/\beta$  for  $i_B$ . Since the constant of the exponential characteristic,  $1/V_T$ , is quite high ( $\approx 40$ ), the curve rises very sharply. For  $v_{BE}$  smaller than about 0.5 V, the current is negligibly small.<sup>7</sup> Also, over most of the normal current range  $v_{BE}$  lies in the range of 0.6 V to 0.8 V. In performing rapid first-order dc calculations, we normally will assume that  $V_{BE} \approx 0.7$  V, which is similar to the approach used in the analysis of diode circuits (Chapter 4). For a *pnp* transistor, the  $i_C$ - $v_{EB}$  characteristic will look identical to that of Fig. 6.16 with  $v_{BE}$  replaced with  $v_{EB}$ .

<sup>7</sup>The  $i_C$ - $v_{BE}$  characteristic is the BJT's counterpart of the  $i_D$ - $v_{GS}$  characteristic of the MOSFET. They share an important attribute: In both cases the voltage has to exceed a "threshold" for the device to conduct appreciably. In the case of the MOSFET, there is a formal threshold voltage,  $V_t$ , which lies typically in the range of 0.4 V to 0.8 V. For the BJT, there is an "apparent threshold" of approximately 0.5 V. The  $i_D$ - $v_{GS}$  characteristic of the MOSFET is parabolic, and thus is less steep than the  $i_C$ - $v_{BE}$  characteristic of the BJT. As will be seen in Chapter 7, this difference has a direct and significant implication for the value of transconductance  $g_m$  realized with each device.



**Figure 6.16** The  $i_C-v_{BE}$  characteristic for an *npn* transistor.



**Figure 6.17** Effect of temperature on the  $i_C-v_{BE}$  characteristic. At a constant emitter current (broken line),  $v_{BE}$  changes by  $-2 \text{ mV}/^\circ\text{C}$ .

As in silicon diodes, the voltage across the emitter-base junction decreases by about 2 mV for each rise of  $1^\circ\text{C}$  in temperature, provided the junction is operating at a constant current. Figure 6.17 illustrates this temperature dependence by depicting  $i_C-v_{BE}$  curves for an *npn* transistor at three different temperatures.

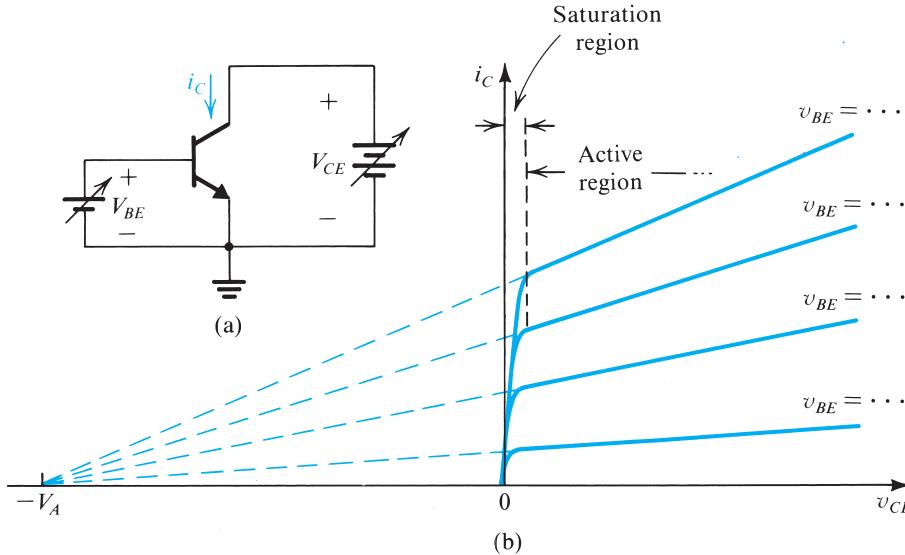
### EXERCISE

- 6.15** Consider a *pnp* transistor with  $v_{EB} = 0.7 \text{ V}$  at  $i_E = 1 \text{ mA}$ . Let the base be grounded, the emitter be fed by a 2-mA constant-current source, and the collector be connected to a  $-5\text{-V}$  supply through a  $1\text{-k}\Omega$  resistance. If the temperature increases by  $30^\circ\text{C}$ , find the changes in emitter and collector voltages. Neglect the effect of  $I_{CBO}$ .

**Ans.**  $-60 \text{ mV}$ ;  $0 \text{ V}$

### 6.2.3 Dependence of $i_C$ on the Collector Voltage—The Early Effect

When operated in the active region, practical BJTs show some dependence of the collector current on the collector voltage, with the result that, unlike the graph shown in Fig. 6.8, their  $i_C-v_{CB}$  characteristics are not perfectly horizontal straight lines. To see this dependence more



**Figure 6.18** (a) Conceptual circuit for measuring the  $i_C$ - $v_{CE}$  characteristics of the BJT. (b) The  $i_C$ - $v_{CE}$  characteristics of a practical BJT.

clearly, consider the conceptual circuit shown in Fig. 6.18(a). The transistor is connected in the **common-emitter configuration**; that is, here the emitter serves as a common terminal between the input and output ports. The voltage  $V_{BE}$  can be set to any desired value by adjusting the dc source connected between base and emitter. At each value of  $V_{BE}$ , the corresponding  $i_C$ - $v_{CE}$  characteristic curve can be measured point by point by varying the dc source connected between collector and emitter and measuring the corresponding collector current. The result is the family of  $i_C$ - $v_{CE}$  characteristic curves shown in Fig. 6.18(b) and known as **common-emitter characteristics**.

At low values of  $v_{CE}$  (lower than about 0.3 V), as the collector voltage goes below that of the base by more than 0.4 V, the collector-base junction becomes forward biased and the transistor leaves the active mode and enters the saturation mode. Shortly, we shall look at the details of the  $i_C$ - $v_{CE}$  curves in the saturation region. At this time, however, we wish to examine the characteristic curves in the active region in detail. We observe that the characteristic curves, though still straight lines, have finite slope. In fact, when extrapolated, the characteristic lines meet at a point on the negative  $v_{CE}$  axis, at  $v_{CE} = -V_A$ . The voltage  $V_A$ , a positive number, is a parameter for the particular BJT, with typical values in the range of 10 V to 100 V. As noted earlier, it is called the **Early voltage**, after J. M. Early, the engineering scientist who first studied this phenomenon.

At a given value of  $v_{BE}$ , increasing  $v_{CE}$  increases the reverse-bias voltage on the collector-base junction, and thus increases the width of the depletion region of this junction (refer to Fig. 6.4). This in turn results in a decrease in the **effective base width**  $W$ . Recalling that  $I_s$  is inversely proportional to  $W$  (Eq. 6.13), we see that  $I_s$  will increase and that  $i_C$  increases proportionally. This is the Early effect. For obvious reasons, it is also known as the **base-width modulation effect**.<sup>8</sup>

<sup>8</sup>Recall that the MOSFET's counterpart is the channel-length modulation effect. These two effects are remarkably similar and have been assigned the same name, Early effect.

The linear dependence of  $i_C$  on  $v_{CE}$  can be explicitly accounted for by assuming that  $I_S$  remains constant and including the factor  $(1 + v_{CE}/V_A)$  in the equation for  $i_C$  as follows:

$$\rightarrow i_C = I_S e^{v_{BE}/V_T} \left( 1 + \frac{v_{CE}}{V_A} \right) \quad (6.18)$$

The nonzero slope of the  $i_C-v_{CE}$  straight lines indicates that the **output resistance** looking into the collector is not infinite. Rather, it is finite and defined by

$$r_o \equiv \left[ \frac{\partial i_C}{\partial v_{CE}} \Big|_{v_{BE} = \text{constant}} \right]^{-1} \quad (6.19)$$

Using Eq. (6.18) we can show that

$$r_o = \frac{V_A + V_{CE}}{I_C} \quad (6.20)$$

where  $I_C$  and  $V_{CE}$  are the coordinates of the point at which the BJT is operating on the particular  $i_C-v_{CE}$  curve (i.e., the curve obtained for  $v_{BE}$  equal to constant value  $V_{BE}$  at which Eq. (6.19) is evaluated). Alternatively, we can write

$$\rightarrow r_o = \frac{V_A}{I'_C} \quad (6.21)$$

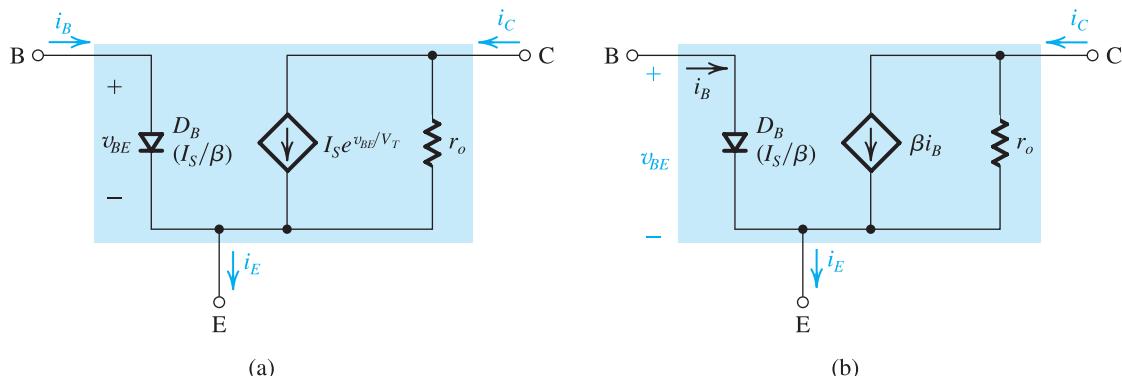
where  $I'_C$  is the value of the collector current with the Early effect neglected; that is,

$$I'_C = I_S e^{V_{BE}/V_T} \quad (6.22)$$

It is rarely necessary to include the dependence of  $i_C$  on  $v_{CE}$  in dc bias design and analysis that is performed by hand. Such an effect, however, can be easily included in the SPICE simulation of circuit operation, which is frequently used to “fine-tune” pencil-and-paper analysis or design.

The finite output resistance  $r_o$  can have a significant effect on the gain of transistor amplifiers. This is particularly the case in integrated-circuit amplifiers, as will be shown in Chapter 8. Fortunately, there are many situations in which  $r_o$  can be included relatively easily in pencil-and-paper analysis.

The output resistance  $r_o$  can be included in the circuit model of the transistor.<sup>9</sup> This is illustrated in Fig. 6.19, where we show the two large-signal circuit models of a



**Figure 6.19** Large-signal, equivalent-circuit models of an npn BJT operating in the active mode in the common-emitter configuration with the output resistance  $r_o$  included.

<sup>9</sup>In applying Eq. (6.21) to determine  $r_o$  we will usually drop the prime and simply use  $r_o = V_A/I_C$  where  $I_C$  is the collector current without the Early effect.

common-emitter *npn* transistor operating in the active mode, those in Fig 6.5(c) and (d), with the resistance  $r_o$  connected between the collector and the emitter terminals.

## EXERCISES

- 6.16** Use the circuit model in Fig. 6.19(a) to express  $i_C$  in terms of  $e^{v_{BE}/V_T}$  and  $v_{CE}$  and thus show that this circuit is a direct representation of Eq. (6.18).
- 6.17** Find the output resistance of a BJT for which  $V_A = 100$  V at  $I_C = 0.1, 1$ , and  $10$  mA.  
**Ans.**  $1\text{ M}\Omega$ ;  $100\text{ k}\Omega$ ;  $10\text{ k}\Omega$
- 6.18** Consider the circuit in Fig. 6.18(a). At  $V_{CE} = 1$  V,  $V_{BE}$  is adjusted to yield a collector current of  $1$  mA. Then, while  $V_{BE}$  is kept constant,  $V_{CE}$  is raised to  $11$  V. Find the new value of  $I_C$ . For this transistor,  $V_A = 100$  V.  
**Ans.**  $1.1$  mA

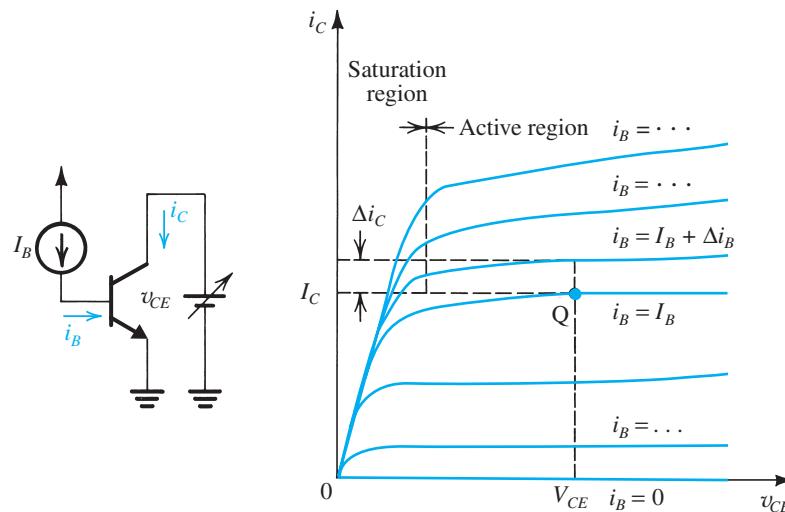
### 6.2.4 An Alternative Form of the Common-Emitter Characteristics

An alternative way of expressing the transistor common-emitter characteristics is illustrated in Fig. 6.20. Here the base current  $i_B$  rather than the base–emitter voltage  $v_{BE}$  is used as a parameter. That is, each  $i_C-v_{CE}$  curve is measured with the base fed with a constant current  $I_B$ . The resulting characteristics, shown in Fig. 6.20(b), look similar to those in Fig. 6.18. Figure 6.20(c) shows an expanded view of the characteristics in the saturation region.

**The Common-Emitter Current Gain  $\beta$**  In the active region of the characteristics shown in Fig. 6.20(b) we have identified a particular point Q. Note that this operating point for the transistor is characterized by a base current  $I_B$ , a collector current  $I_C$ , and a collector–emitter voltage  $V_{CE}$ . The ratio  $I_C/I_B$  is the transistor  $\beta$ . However, there is another way to measure  $\beta$ : change the base current by an increment  $\Delta i_B$  and measure the resulting increment  $\Delta i_C$ , while keeping  $V_{CE}$  constant. This is illustrated in Fig. 6.20(b). The ratio  $\Delta i_C/\Delta i_B$  should, according to our study thus far, yield an identical value for  $\beta$ . It turns out, however, that the latter value of  $\beta$  (called *incremental*, or *ac*,  $\beta$ ) is a little different from the dc  $\beta$  (i.e.,  $I_C/I_B$ ). Such a distinction, however, is too subtle for our needs in this book. We shall use  $\beta$  to denote both dc and incremental values.<sup>10</sup>

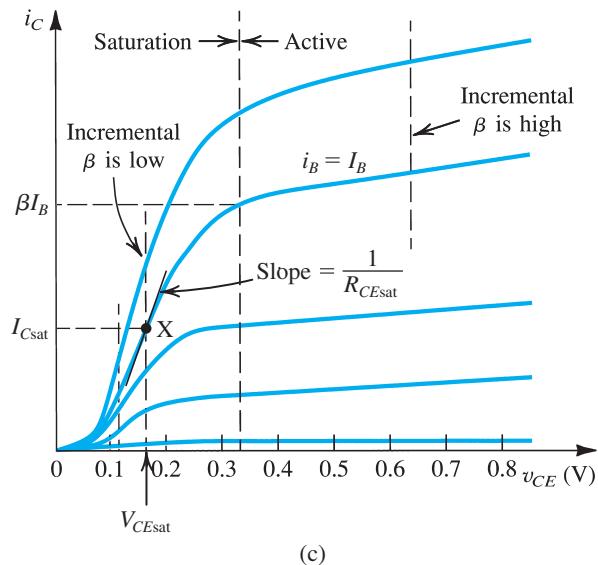
**The Saturation Voltage  $V_{CESat}$  and Saturation Resistance  $R_{CESat}$**  Refer next to the expanded view of the common-emitter characteristics in the saturation region shown in Fig. 6.20(c). The “bunching together” of the curves in the saturation region implies that the incremental  $\beta$  is lower there than in the active region. A possible operating point in the saturation region is that labeled X. It is characterized by a base current  $I_B$ , a collector current  $I_{Csat}$ , and a collector–emitter voltage  $V_{CESat}$ . From our previous discussion of saturation, recall that  $I_{Csat} = \beta_{\text{forced}} I_B$ , where  $\beta_{\text{forced}} < \beta$ .

<sup>10</sup> Manufacturers of bipolar transistors use  $h_{FE}$  to denote the dc value of  $\beta$  and  $h_{fe}$  to denote the incremental  $\beta$ . These symbols come from the *h*-parameter description of two-port networks (see Appendix C), with the subscript *F(f)* denoting forward and *E(e)* denoting common emitter.



(a)

(b)

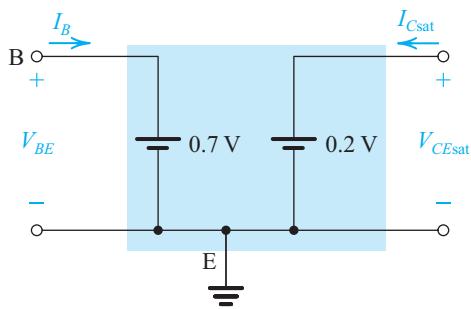


**Figure 6.20** Common-emitter characteristics. (a) Basic CE circuit; note that in (b) the horizontal scale is expanded around the origin to show the saturation region in some detail. A much greater expansion of the saturation region is shown in (c).

The  $i_C - v_{CE}$  curves in saturation are rather steep, indicating that the saturated transistor exhibits a low collector-to-emitter resistance  $R_{CESat}$ ,

$$R_{CESat} \equiv \left. \frac{\partial v_{CE}}{\partial i_C} \right|_{\substack{i_B = I_B \\ i_C = I_{Csat}}} \quad (6.23)$$

Typically,  $R_{CESat}$  ranges from a few ohms to a few tens of ohms.



**Figure 6.21** A simplified equivalent-circuit model of the saturated transistor.

That the collector-to-emitter resistance of a saturated BJT is small should have been anticipated from the fact that between C and E we now have two forward-conducting diodes in series<sup>11</sup> (see also Fig. 6.9).

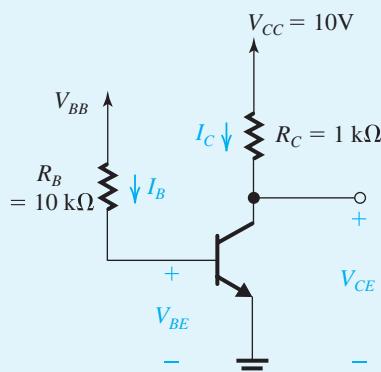
A simple model for the saturated BJT is shown in Fig. 6.21. Here  $V_{BE}$  is assumed constant (approximately 0.7 V) and  $V_{CE}$  also is assumed constant,  $V_{CEsat} \approx 0.2$  V. That is, we have neglected the small saturation resistance  $R_{CEsat}$  for the sake of making the model simple for hand calculations.

### Example 6.3

For the circuit in Fig. 6.22, it is required to determine the value of the voltage  $V_{BB}$  that results in the transistor operating

- (a) in the active mode with  $V_{CE} = 5$  V
- (b) at the edge of saturation
- (c) deep in saturation with  $\beta_{forced} = 10$

For simplicity, assume that  $V_{BE}$  remains constant at 0.7 V. The transistor  $\beta$  is specified to be 50.



**Figure 6.22** Circuit for Example 6.3.

<sup>11</sup>In the corresponding mode of operation for the MOSFET, the triode region, the resistance between drain and source is small because it is the resistance of the continuous (non-pinched-off) channel.

**Example 6.3** *continued***Solution**

(a) To operate in the active mode with  $V_{CE} = 5$  V,

$$\begin{aligned} I_C &= \frac{V_{CC} - V_{CE}}{R_C} \\ &= \frac{10 - 5}{1 \text{ k}\Omega} = 5 \text{ mA} \\ I_B &= \frac{I_C}{\beta} = \frac{5}{50} = 0.1 \text{ mA} \end{aligned}$$

Now the required value of  $V_{BB}$  can be found as follows:

$$\begin{aligned} V_{BB} &= I_B R_B + V_{BE} \\ &= 0.1 \times 10 + 0.7 = 1.7 \text{ V} \end{aligned}$$

(b) Operation at the edge of saturation is obtained with  $V_{CE} = 0.3$  V. Thus

$$I_C = \frac{10 - 0.3}{1} = 9.7 \text{ mA}$$

Since, at the edge of saturation,  $I_C$  and  $I_B$  are still related by  $\beta$ ,

$$I_B = \frac{9.7}{50} = 0.194 \text{ mA}$$

The required value of  $V_{BB}$  can be determined as

$$V_{BB} = 0.194 \times 10 + 0.7 = 2.64 \text{ V}$$

(c) To operate deep in saturation,

$$V_{CE} = V_{CESat} \simeq 0.2 \text{ V}$$

Thus,

$$I_C = \frac{10 - 0.2}{1} = 9.8 \text{ mA}$$

We then use the value of forced  $\beta$  to determine the required value of  $I_B$  as

$$I_B = \frac{I_C}{\beta_{\text{forced}}} = \frac{9.8}{10} = 0.98 \text{ mA}$$

and the required  $V_{BB}$  can now be found as

$$V_{BB} = 0.98 \times 10 + 0.7 = 10.5 \text{ V}$$

Observe that once the transistor is in saturation, increasing  $V_{BB}$  and thus  $I_B$  results in negligible change in  $I_C$  since  $V_{CESat}$  will change only slightly. Thus  $I_C$  is said to *saturate*, which is the origin of the name “saturation mode of operation.”

## EXERCISES

- 6.19** Repeat Example 6.3 for  $R_C = 10 \text{ k}\Omega$ .

**Ans.** 0.8 V; 0.894 V; 1.68 V

- 6.20** For the circuit in Fig. 6.22, find  $V_{CE}$  for  $V_{BB} = 0 \text{ V}$ .

**Ans.** +10 V

- 6.21** For the circuit in Fig. 6.22, let  $V_{BB}$  be set to the value obtained in Example 6.3, part (a), namely,  $V_{BB} = 1.7 \text{ V}$ . Verify that the transistor is indeed operating in the active mode. Now, while keeping  $V_{BB}$  constant, find the value to which  $R_C$  should be increased in order to obtain (a) operation at the edge of saturation and (b) operation deep in saturation with  $\beta_{\text{forced}} = 10$ .

**Ans.** (a) 1.94 k $\Omega$ ; (b) 9.8 k $\Omega$

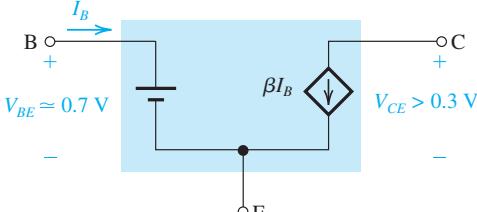
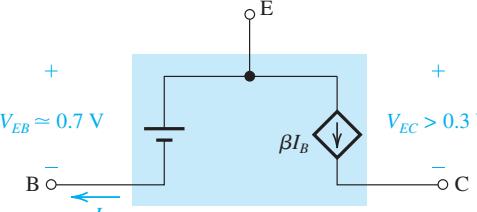
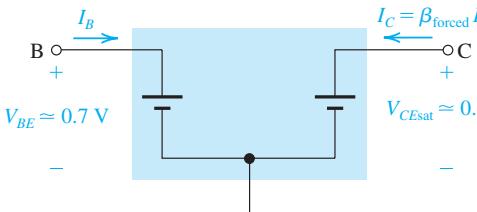
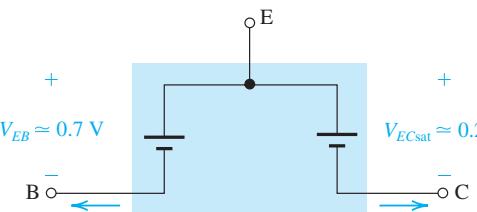
## 6.3 BJT Circuits at DC

We are now ready to consider the analysis of BJT circuits to which only dc voltages are applied. In the following examples we will use the simple model in which  $|V_{BE}|$  of a conducting transistor is 0.7 V and  $|V_{CE}|$  of a saturated transistor is 0.2 V, and we will neglect the Early effect. These models are shown in Table 6.3. Better models can, of course, be used to obtain more accurate results. This, however, is usually achieved at the expense of speed of analysis; more importantly, the attendant complexity could impede the circuit designer's ability to gain insight regarding circuit behavior. Accurate results using elaborate models can be obtained using circuit simulation with SPICE. This is almost always done in the final stages of a design and certainly before circuit fabrication. Computer simulation, however, is *not* a substitute for quick pencil-and-paper circuit analysis, an essential ability that aspiring circuit designers must master. The following series of examples is a step in that direction.

As will be seen, in analyzing a circuit the first question that one must answer is: *In which mode is the transistor operating?* In some cases, the answer will be obvious. For instance, a quick check of the terminal voltages will indicate whether the transistor is cut off or conducting. If it is conducting, we have to determine whether it is operating in the active mode or in saturation. In some cases, however, this may not be obvious. Needless to say, as the reader gains practice and experience in transistor circuit analysis and design, the answer will be apparent in a much larger proportion of problems. The answer, however, can always be determined by utilizing the following procedure.

Assume that the transistor is operating in the active mode and, using the active-mode model in Table 6.3, proceed to determine the various voltages and currents that correspond. Then check for consistency of the results with the assumption of active-mode operation; that is, is  $V_{CB}$  of an *n*p*n* transistor greater than -0.4 V (or  $V_{CB}$  of a *p*n*p* transistor lower than 0.4 V)? If the answer is yes, then our task is complete. If the answer is no, assume saturation-mode operation and, using the saturation-mode model in Table 6.3, proceed to determine currents and voltages

**Table 6.3** Simplified Models for the Operation of the BJT in DC Circuits

	<i>npn</i>	<i>pnp</i>
<b>Active</b> EBJ: Forward Biased  CBJ: Reverse Biased	 <p><math>V_{BE} \approx 0.7 \text{ V}</math></p>	 <p><math>V_{EB} \approx 0.7 \text{ V}</math></p>
<b>Saturation</b> EBJ: Forward Biased  CBJ: Forward Biased	 <p><math>I_C = \beta_{\text{forced}} I_B</math></p> <p><math>V_{CESat} \approx 0.2 \text{ V}</math></p>	 <p><math>V_{EB} \approx 0.7 \text{ V}</math></p> <p><math>V_{ECSat} \approx 0.2 \text{ V}</math></p>

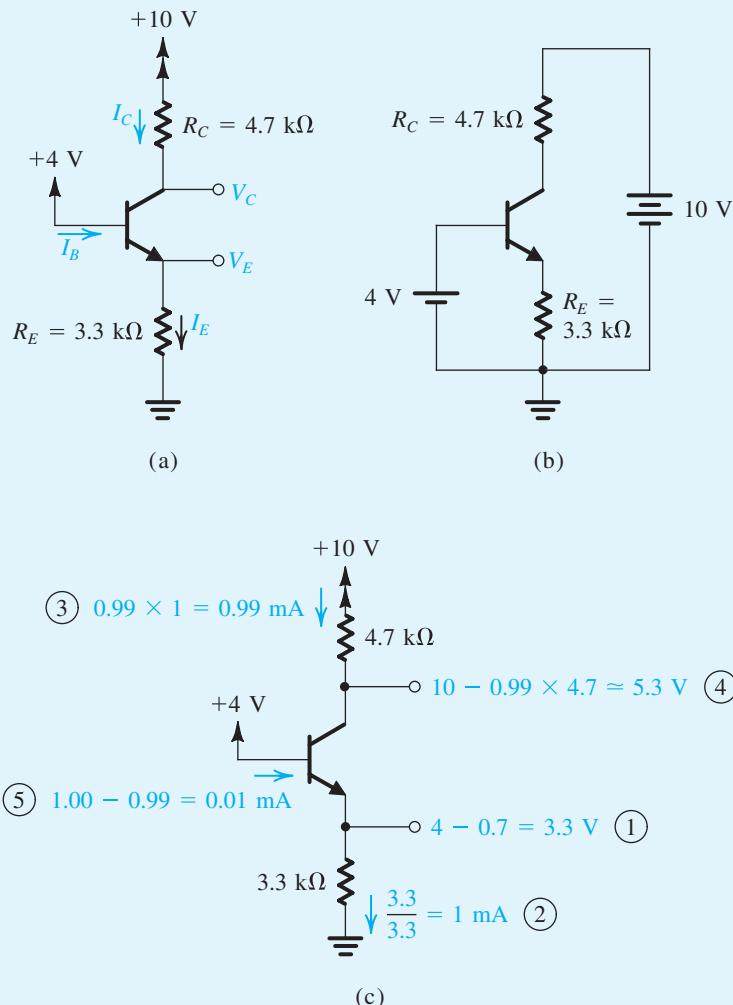
and then check for consistency of the results with the assumption of saturation-mode operation. Here the test is usually to compute the ratio  $I_C/I_B$  and to verify that it is lower than the transistor  $\beta$  (i.e.,  $\beta_{\text{forced}} < \beta$ ). Since  $\beta$  for a given transistor type varies over a wide range,<sup>12</sup> one must use the lowest specified  $\beta$  for this test. Finally, note that the order of these two assumptions can be reversed.

**A Note on Units** Except when otherwise specified, throughout this book we use a consistent set of units, namely, volts (V), millamps (mA), and kilohms ( $k\Omega$ ).

<sup>12</sup>That is, if one buys BJTs of a certain part number, the manufacturer guarantees only that their values of  $\beta$  fall within a certain range, say 50 to 150.

### Example 6.4

Consider the circuit shown in Fig. 6.23(a), which is redrawn in Fig. 6.23(b) to remind the reader of the convention employed throughout this book for indicating connections to dc sources. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that  $\beta$  is specified to be 100.



**Figure 6.23** Analysis of the circuit for Example 6.4: (a) circuit; (b) circuit redrawn to remind the reader of the convention used in this book to show connections to the dc sources; (c) analysis with the steps numbered.

**Example 6.4** *continued***Solution**

Glancing at the circuit in Fig. 6.23(a), we note that the base is connected to +4 V and the emitter is connected to ground through a resistance  $R_E$ . Therefore, it is reasonable to conclude that the base–emitter junction will be forward biased. Assuming that this is the case and assuming that  $V_{BE}$  is approximately 0.7 V, it follows that the emitter voltage will be

$$V_E = 4 - V_{BE} \simeq 4 - 0.7 = 3.3 \text{ V}$$

We are now in an opportune position; we know the voltages at the two ends of  $R_E$  and thus can determine the current  $I_E$  through it,

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1 \text{ mA}$$

Since the collector is connected through  $R_C$  to the +10-V power supply, it appears possible that the collector voltage will be higher than the base voltage, which implies active-mode operation. Assuming that this is the case, we can evaluate the collector current from

$$I_C = \alpha I_E$$

The value of  $\alpha$  is obtained from

$$\alpha = \frac{\beta}{\beta + 1} = \frac{100}{101} \simeq 0.99$$

Thus  $I_C$  will be given by

$$I_C = 0.99 \times 1 = 0.99 \text{ mA}$$

We are now in a position to use Ohm's law to determine the collector voltage  $V_C$ ,

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 \simeq +5.3 \text{ V}$$

Since the base is at +4 V, the collector–base junction is reverse biased by 1.3 V, and the transistor is indeed in the active mode as assumed.

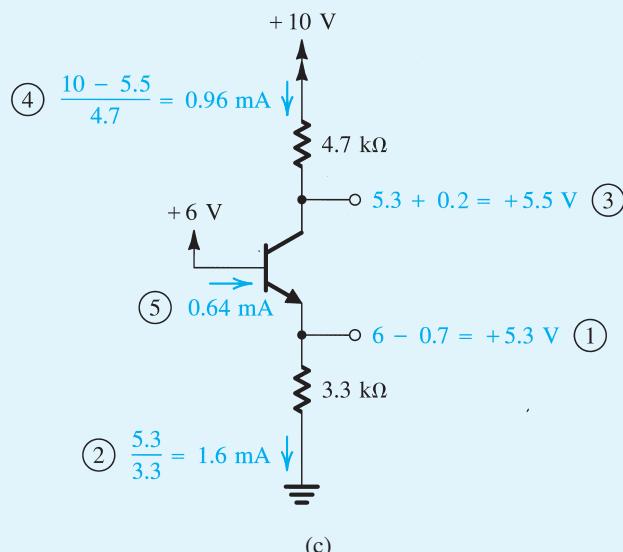
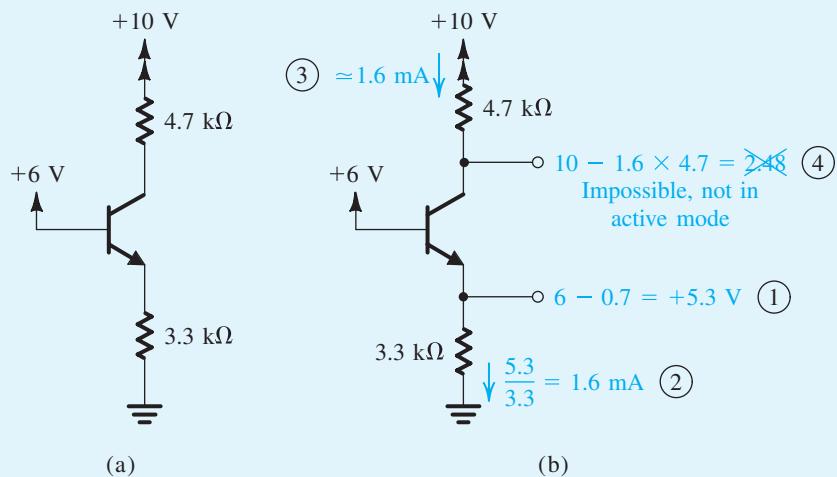
It remains only to determine the base current  $I_B$ , as follows:

$$I_B = \frac{I_E}{\beta + 1} = \frac{1}{101} \simeq 0.01 \text{ mA}$$

Before leaving this example, we wish to emphasize strongly the value of carrying out the analysis directly on the circuit diagram. Only in this way will one be able to analyze complex circuits in a reasonable length of time. Figure 6.23(c) illustrates the above analysis on the circuit diagram, with the order of the analysis steps indicated by the circled numbers.

### Example 6.5

We wish to analyze the circuit of Fig. 6.24(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 6.23 except that the voltage at the base is now +6 V. Assume that the transistor  $\beta$  is specified to be *at least* 50.



**Figure 6.24** Analysis of the circuit for Example 6.5. Note that the circled numbers indicate the order of the analysis steps.

**Example 6.5** *continued***Solution**

With +6 V at the base, the base–emitter junction will be forward biased; thus,

$$V_E = +6 - V_{BE} \simeq 6 - 0.7 = 5.3 \text{ V}$$

and

$$I_E = \frac{5.3}{3.3} = 1.6 \text{ mA}$$

Now, assuming active-mode operation,  $I_C = \alpha I_E \simeq I_E$ ; thus,

$$V_C = +10 - 4.7 \times I_C \simeq 10 - 7.52 = 2.48 \text{ V}$$

The details of the analysis performed above are illustrated in Fig. 6.24(b).

Since the collector voltage calculated is less than the base voltage by 3.52 V, it follows that our original assumption of active-mode operation is incorrect. In fact, the transistor has to be in the *saturation* mode. Assuming this to be the case, the values of  $V_E$  and  $I_E$  will remain unchanged. The collector voltage, however, becomes

$$V_C = V_E + V_{CE\text{sat}} \simeq 5.3 + 0.2 = +5.5 \text{ V}$$

from which we can determine  $I_C$  as

$$I_C = \frac{10 - 5.5}{4.7} = 0.96 \text{ mA}$$

and  $I_B$  can now be found as

$$I_B = I_E - I_C = 1.6 - 0.96 = 0.64 \text{ mA}$$

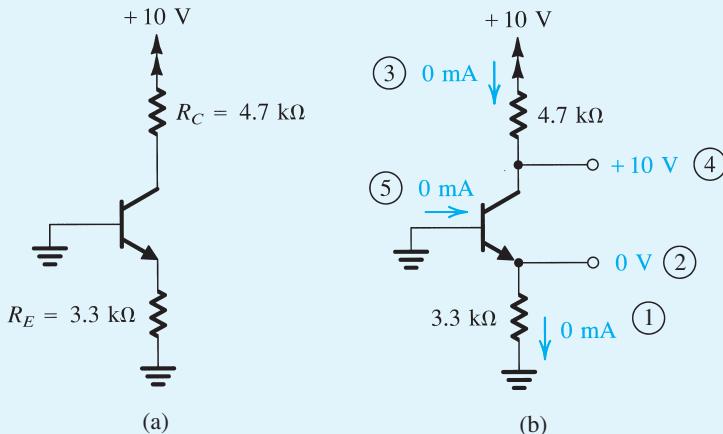
Thus the transistor is operating at a forced  $\beta$  of

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$

Since  $\beta_{\text{forced}}$  is less than the *minimum* specified value of  $\beta$ , the transistor is indeed saturated. We should emphasize here that in testing for saturation the minimum value of  $\beta$  should be used. By the same token, if we are designing a circuit in which a transistor is to be saturated, the design should be based on the minimum specified  $\beta$ . Obviously, if a transistor with this minimum  $\beta$  is saturated, then transistors with higher values of  $\beta$  will also be saturated. The details of the analysis are shown in Fig. 6.24(c), where the order of the steps used is indicated by the circled numbers.

### Example 6.6

We wish to analyze the circuit in Fig. 6.25(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that considered in Examples 6.4 and 6.5 except that now the base voltage is zero.



**Figure 6.25** Example 6.6: (a) circuit; (b) analysis, with the order of the analysis steps indicated by circled numbers.

### Solution

Since the base is at zero volts and the emitter is connected to ground through  $R_E$ , the base–emitter junction cannot conduct and the emitter current is zero. Also, the collector–base junction cannot conduct, since the *n*-type collector is connected through  $R_C$  to the positive power supply while the *p*-type base is at ground. It follows that the collector current will be zero. The base current will also have to be zero, and the transistor is in the *cutoff* mode of operation.

The emitter voltage will be zero, while the collector voltage will be equal to +10 V, since the voltage drops across  $R_E$  and  $R_C$  are zero. Figure 6.25(b) shows the analysis details.

### EXERCISES

- D6.22** For the circuit in Fig. 6.23(a), find the highest voltage to which the base can be raised while the transistor remains in the active mode. Assume  $\alpha \simeq 1$ .

**Ans.** +4.7 V

- D6.23** Redesign the circuit of Fig. 6.23(a) (i.e., find new values for  $R_E$  and  $R_C$ ) to establish a collector current of 0.5 mA and a reverse-bias voltage on the collector–base junction of 2 V. Assume  $\alpha \simeq 1$ .

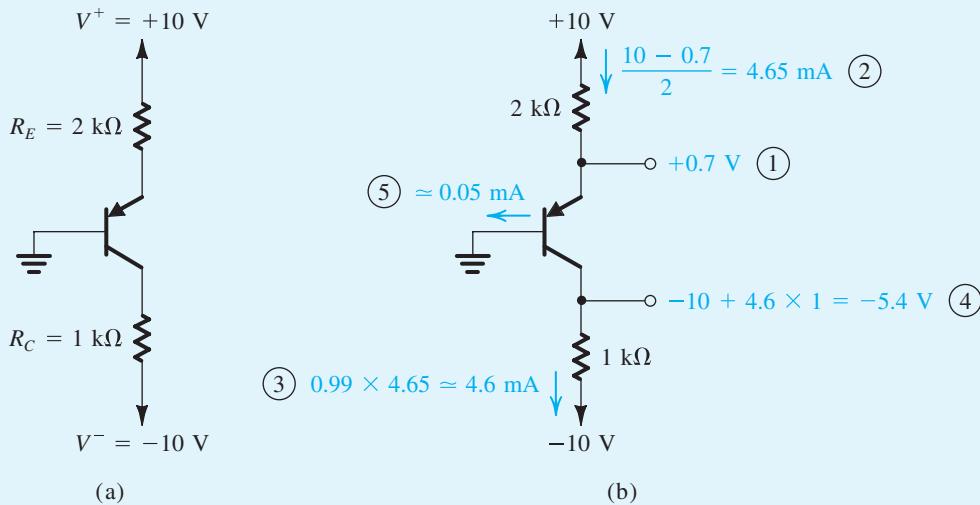
**Ans.**  $R_E = 6.6 \text{ k}\Omega$ ;  $R_C = 8 \text{ k}\Omega$

**D6.24** For the circuit in Fig. 6.24(a), find the value to which the base voltage should be changed so that the transistor operates in saturation with a forced  $\beta$  of 5.

**Ans.** +5.18 V

### Example 6.7

We want to analyze the circuit of Fig. 6.26(a) to determine the voltages at all nodes and the currents through all branches.



**Figure 6.26** Example 6.7: (a) circuit; (b) analysis, with the steps indicated by circled numbers.

### Solution

The base of this *pnp* transistor is grounded, while the emitter is connected to a positive supply ( $V^+ = +10 \text{ V}$ ) through  $R_E$ . It follows that the emitter-base junction will be forward biased with

$$V_E = V_{EB} \simeq 0.7 \text{ V}$$

Thus the emitter current will be given by

$$I_E = \frac{V^+ - V_E}{R_E} = \frac{10 - 0.7}{2} = 4.65 \text{ mA}$$

Since the collector is connected to a negative supply (more negative than the base voltage) through  $R_C$ , it is *possible* that this transistor is operating in the active mode. Assuming this to be the case, we obtain

$$I_C = \alpha I_E$$

Since no value for  $\beta$  has been given, we shall assume  $\beta = 100$ , which results in  $\alpha = 0.99$ . Since large variations in  $\beta$  result in small differences in  $\alpha$ , this assumption will not be critical as far as determining the value of  $I_C$  is concerned. Thus,

$$I_C = 0.99 \times 4.65 = 4.6 \text{ mA}$$

The collector voltage will be

$$\begin{aligned} V_C &= V^- + I_C R_C \\ &= -10 + 4.6 \times 1 = -5.4 \text{ V} \end{aligned}$$

Thus the collector-base junction is reverse biased by 5.4 V, and the transistor is indeed in the active mode, which supports our original assumption.

It remains only to calculate the base current,

$$I_B = \frac{I_E}{\beta + 1} = \frac{4.65}{101} \simeq 0.05 \text{ mA}$$

Obviously, the value of  $\beta$  critically affects the base current. Note, however, that in this circuit the value of  $\beta$  will have no effect on the mode of operation of the transistor. Since  $\beta$  is generally an ill-specified parameter, this circuit represents a good design. As a rule, one should strive to *design the circuit such that its performance is as insensitive to the value of  $\beta$  as possible*. The analysis details are illustrated in Fig. 6.26(b).

## EXERCISES

**D6.25** For the circuit in Fig. 6.26(a), find the largest value to which  $R_C$  can be raised while the transistor remains in the active mode.

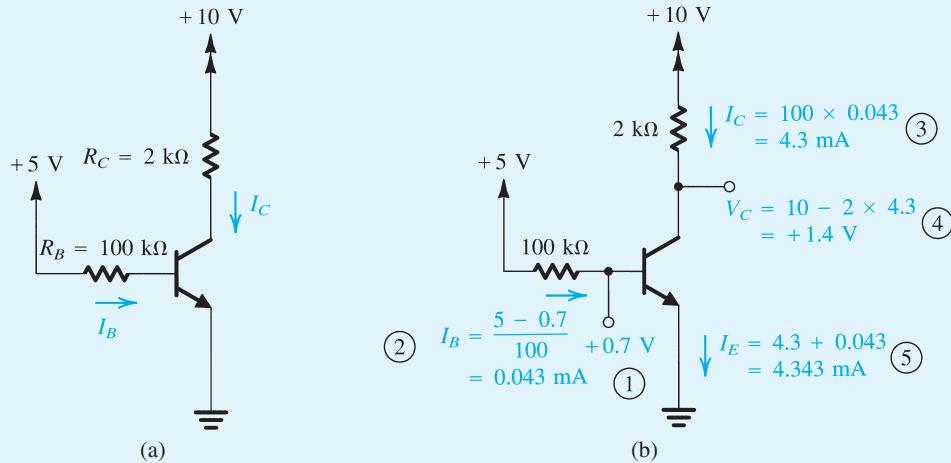
**Ans.** 2.26 kΩ

**D6.26** Redesign the circuit of Fig. 6.26(a) (i.e., find new values for  $R_E$  and  $R_C$ ) to establish a collector current of 1 mA and a reverse bias on the collector-base junction of 4 V. Assume  $\alpha \simeq 1$ .

**Ans.**  $R_E = 9.3 \text{ k}\Omega$ ;  $R_C = 6 \text{ k}\Omega$

**Example 6.8**

We want to analyze the circuit in Fig. 6.27(a) to determine the voltages at all nodes and the currents in all branches. Assume  $\beta = 100$ .



**Figure 6.27** Example 6.8: (a) circuit; (b) analysis, with the steps indicated by the circled numbers.

**Solution**

The base–emitter junction is clearly forward biased. Thus,

$$I_B = \frac{+5 - V_{BE}}{R_B} \simeq \frac{5 - 0.7}{100} = 0.043 \text{ mA}$$

Assume that the transistor is operating in the active mode. We now can write

$$I_C = \beta I_B = 100 \times 0.043 = 4.3 \text{ mA}$$

The collector voltage can now be determined as

$$V_C = 10 - I_C R_C = 10 - 4.3 \times 2 = +1.4 \text{ V}$$

Since the base voltage  $V_B$  is

$$V_B = V_{BE} \simeq +0.7 \text{ V}$$

it follows that the collector–base junction is reverse biased by 0.7 V and the transistor is indeed in the active mode. The emitter current will be given by

$$I_E = (\beta + 1)I_B = 101 \times 0.043 \simeq 4.3 \text{ mA}$$

We note from this example that the collector and emitter currents depend critically on the value of  $\beta$ . In fact, if  $\beta$  were 10% higher, the transistor would leave the active mode and enter saturation. Therefore this clearly is a *bad* design. The analysis details are illustrated in Fig. 6.27(b).

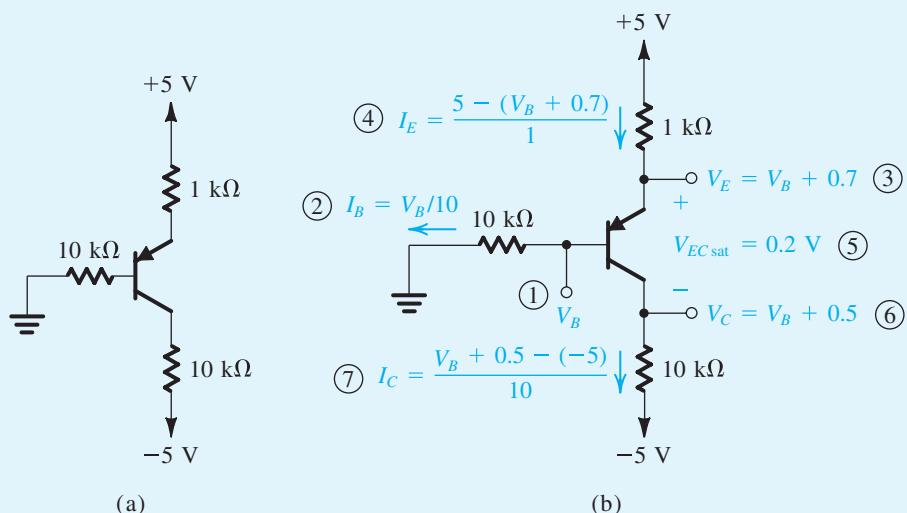
**EXERCISE**

**D6.27** The circuit of Fig. 6.27(a) is to be fabricated using a transistor type whose  $\beta$  is specified to be in the range of 50 to 150. That is, individual units of this same transistor type can have  $\beta$  values anywhere in this range. Redesign the circuit by selecting a new value for  $R_c$  so that all fabricated circuits are guaranteed to be in the active mode. What is the range of collector voltages that the fabricated circuits may exhibit?

**Ans.**  $R_c = 1.5 \text{ k}\Omega$ ;  $V_c = 0.3 \text{ V}$  to  $6.8 \text{ V}$

**Example 6.9**

We want to analyze the circuit of Fig. 6.28(a) to determine the voltages at all nodes and the currents through all branches. The minimum value of  $\beta$  is specified to be 30.



**Figure 6.28** Example 6.9: (a) circuit; (b) analysis with steps numbered.

**Solution**

A quick glance at this circuit reveals that the transistor will be either active or saturated. Assuming active-mode operation and neglecting the base current, we see that the base voltage will be approximately zero volts, the emitter voltage will be approximately  $+0.7 \text{ V}$ , and the emitter current will be approximately  $4.3 \text{ mA}$ . Since the maximum current that the collector can support while the transistor remains in the active mode is approximately  $0.5 \text{ mA}$ , it follows that the transistor is definitely saturated.

**Example 6.9** *continued*

Assuming that the transistor is saturated and denoting the voltage at the base by  $V_B$  (refer to Fig. 6.28b), it follows that

$$\begin{aligned} V_E &= V_B + V_{EB} \simeq V_B + 0.7 \\ V_C &= V_E - V_{EC\text{sat}} \simeq V_B + 0.7 - 0.2 = V_B + 0.5 \\ I_E &= \frac{+5 - V_E}{1} = \frac{5 - V_B - 0.7}{1} = 4.3 - V_B \text{ mA} \\ I_B &= \frac{V_B}{10} = 0.1V_B \text{ mA} \\ I_C &= \frac{V_C - (-5)}{10} = \frac{V_B + 0.5 + 5}{10} = 0.1V_B + 0.55 \text{ mA} \end{aligned}$$

Using the relationship  $I_E = I_B + I_C$ , we obtain

$$4.3 - V_B = 0.1V_B + 0.1V_B + 0.55$$

which results in

$$V_B = \frac{3.75}{1.2} \simeq 3.13 \text{ V}$$

Substituting in the equations above, we obtain

$$\begin{aligned} V_E &= 3.83 \text{ V} \\ V_C &= 3.63 \text{ V} \\ I_E &= 1.17 \text{ mA} \\ I_C &= 0.86 \text{ mA} \\ I_B &= 0.31 \text{ mA} \end{aligned}$$

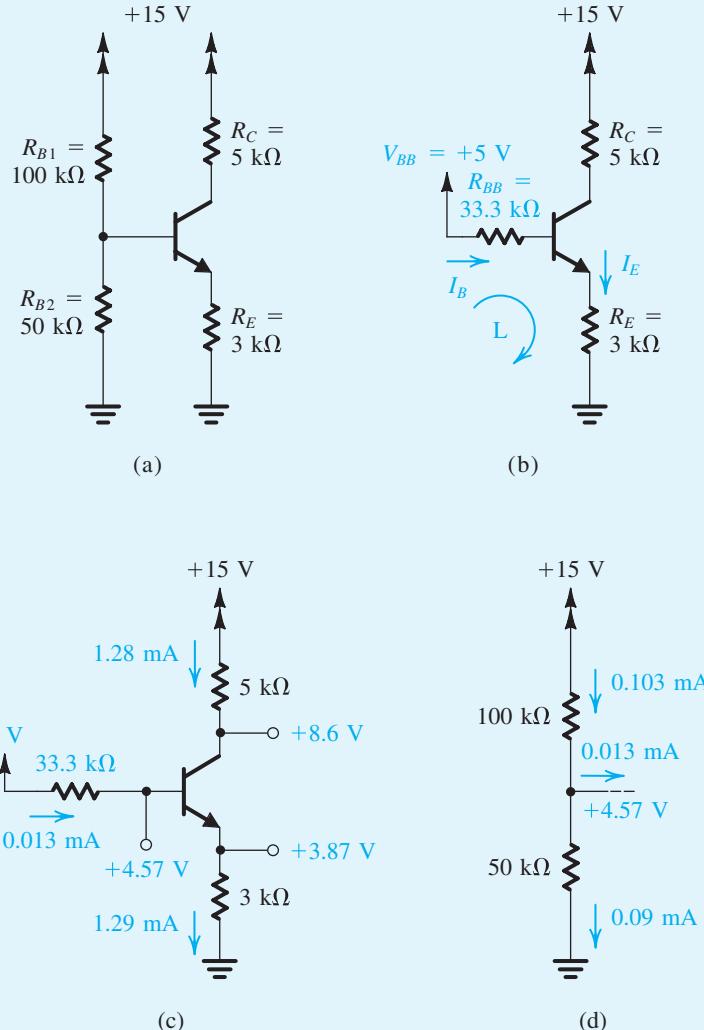
from which we see that the transistor is saturated, since the value of forced  $\beta$  is

$$\beta_{\text{forced}} = \frac{0.86}{0.31} \simeq 2.8$$

which is much smaller than the specified minimum  $\beta$ .

**Example 6.10**

We want to analyze the circuit of Fig. 6.29(a) to determine the voltages at all nodes and the currents through all branches. Assume  $\beta = 100$ .



**Figure 6.29** Circuits for Example 6.10.

### Solution

The first step in the analysis consists of simplifying the base circuit using Thévenin's theorem. The result is shown in Fig. 6.29(b), where

$$V_{BB} = +15 \frac{R_{B2}}{R_{B1} + R_{B2}} = 15 \frac{50}{100 + 50} = +5 \text{ V}$$

$$R_{BB} = R_{B1} \parallel R_{B2} = 100 \parallel 50 = 33.3 \text{ k}\Omega$$

**Example 6.10** *continued*

To evaluate the base or the emitter current, we have to write a loop equation around the loop labeled L in Fig. 6.29(b). Note, however, that the current through  $R_{BB}$  is different from the current through  $R_E$ . The loop equation will be

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E$$

Now, assuming active-mode operation, we replace  $I_B$  with

$$I_B = \frac{I_E}{\beta + 1}$$

and rearrange the equation to obtain

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + [R_{BB}/(\beta + 1)]}$$

For the numerical values given we have

$$I_E = \frac{5 - 0.7}{3 + (33.3/101)} = 1.29 \text{ mA}$$

The base current will be

$$I_B = \frac{1.29}{101} = 0.0128 \text{ mA}$$

The base voltage is given by

$$\begin{aligned} V_B &= V_{BE} + I_E R_E \\ &= 0.7 + 1.29 \times 3 = 4.57 \text{ V} \end{aligned}$$

We can evaluate the collector current as

$$I_C = \alpha I_E = 0.99 \times 1.29 = 1.28 \text{ mA}$$

The collector voltage can now be evaluated as

$$V_C = +15 - I_C R_C = 15 - 1.28 \times 5 = 8.6 \text{ V}$$

It follows that the collector is higher in potential than the base by 4.03 V, which means that the transistor is in the active mode, as had been assumed. The results of the analysis are given in Fig. 6.29(c, d).

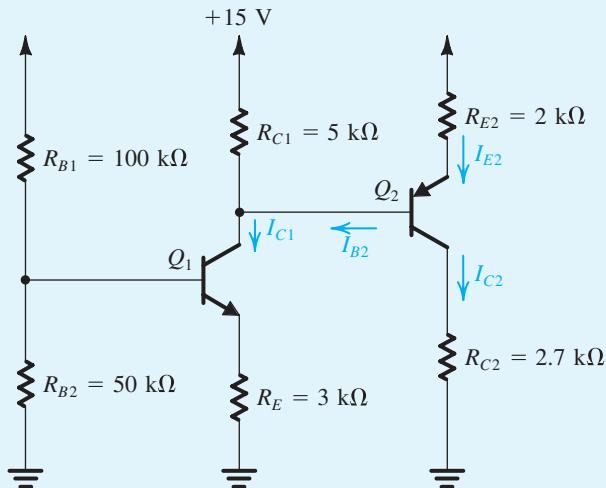
**EXERCISE**

- 6.28** If the transistor in the circuit of Fig. 6.29(a) is replaced with another having half the value of  $\beta$  (i.e.,  $\beta = 50$ ), find the new value of  $I_C$ , and express the change in  $I_C$  as a percentage.

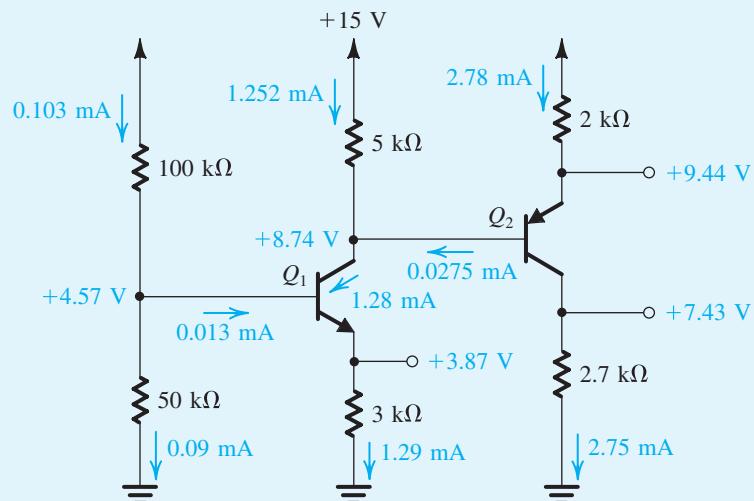
**Ans.**  $I_C = 1.15 \text{ mA}; -10\%$

**Example 6.11**

We wish to analyze the circuit in Fig. 6.30(a) to determine the voltages at all nodes and the currents through all branches.



(a)



(b)

**Figure 6.30** Circuits for Example 6.11.

**Example 6.11** *continued***Solution**

We first recognize that part of this circuit is identical to the circuit we analyzed in Example 6.10—namely, the circuit of Fig. 6.29(a). The difference, of course, is that in the new circuit we have an additional transistor  $Q_2$  together with its associated resistors  $R_{E2}$  and  $R_{C2}$ . Assume that  $Q_1$  is still in the active mode. The following values will be identical to those obtained in the previous example:

$$\begin{aligned} V_{B1} &= +4.57 \text{ V} & I_{E1} &= 1.29 \text{ mA} \\ I_{B1} &= 0.0128 \text{ mA} & I_{C1} &= 1.28 \text{ mA} \end{aligned}$$

However, the collector voltage will be different than previously calculated, since part of the collector current  $I_{C1}$  will flow in the base lead of  $Q_2$  ( $I_{B2}$ ). As a first approximation we may assume that  $I_{B2}$  is much smaller than  $I_{C1}$ ; that is, we may assume that the current through  $R_{C1}$  is almost equal to  $I_{C1}$ . This will enable us to calculate  $V_{C1}$ :

$$\begin{aligned} V_{C1} &\simeq +15 - I_{C1}R_{C1} \\ &= 15 - 1.28 \times 5 = +8.6 \text{ V} \end{aligned}$$

Thus  $Q_1$  is in the active mode, as had been assumed.

As far as  $Q_2$  is concerned, we note that its emitter is connected to +15 V through  $R_{E2}$ . It is therefore safe to assume that the emitter–base junction of  $Q_2$  will be forward biased. Thus the emitter of  $Q_2$  will be at a voltage  $V_{E2}$  given by

$$V_{E2} = V_{C1} + V_{EB}|_{Q_2} \simeq 8.6 + 0.7 = +9.3 \text{ V}$$

The emitter current of  $Q_2$  may now be calculated as

$$I_{E2} = \frac{+15 - V_{E2}}{R_{E2}} = \frac{15 - 9.3}{2} = 2.85 \text{ mA}$$

Since the collector of  $Q_2$  is returned to ground via  $R_{C2}$ , it is possible that  $Q_2$  is operating in the active mode. Assume this to be the case. We now find  $I_{C2}$  as

$$\begin{aligned} I_{C2} &= \alpha_2 I_{E2} \\ &= 0.99 \times 2.85 = 2.82 \text{ mA} \quad (\text{assuming } \beta_2 = 100) \end{aligned}$$

The collector voltage of  $Q_2$  will be

$$V_{C2} = I_{C2}R_{C2} = 2.82 \times 2.7 = 7.62 \text{ V}$$

which is lower than  $V_{B2}$  by 0.98 V. Thus  $Q_2$  is in the active mode, as assumed.

It is important at this stage to find the magnitude of the error incurred in our calculations by the assumption that  $I_{B2}$  is negligible. The value of  $I_{B2}$  is given by

$$I_{B2} = \frac{I_{E2}}{\beta_2 + 1} = \frac{2.85}{101} = 0.028 \text{ mA}$$

which is indeed much smaller than  $I_{C1}$  (1.28 mA). If desired, we can obtain more accurate results by iterating one more time, assuming  $I_{B2}$  to be 0.028 mA. The new values will be

$$\text{Current in } R_{C1} = I_{C1} - I_{B2} = 1.28 - 0.028 = 1.252 \text{ mA}$$

$$V_{C1} = 15 - 5 \times 1.252 = 8.74 \text{ V}$$

$$V_{E2} = 8.74 + 0.7 = 9.44 \text{ V}$$

$$I_{E2} = \frac{15 - 9.44}{2} = 2.78 \text{ mA}$$

$$I_{C2} = 0.99 \times 2.78 = 2.75 \text{ mA}$$

$$V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V}$$

$$I_{B2} = \frac{2.78}{101} = 0.0275 \text{ mA}$$

Note that the new value of  $I_{B2}$  is very close to the value used in our iteration, and no further iterations are warranted. The final results are indicated in Fig. 6.30(b).

The reader justifiably might be wondering about the necessity for using an iterative scheme in solving a linear (or linearized) problem. Indeed, we can obtain the exact solution (if we can call anything we are doing with a first-order model exact!) by writing appropriate equations. The reader is encouraged to find this solution and then compare the results with those obtained above. It is important to emphasize, however, that in most such problems it is quite sufficient to obtain an approximate solution, provided we can obtain it quickly and, of course, correctly.

In the above examples, we frequently used a precise value of  $\alpha$  to calculate the collector current. Since  $\alpha \simeq 1$ , the error in such calculations will be very small if one assumes  $\alpha = 1$  and  $I_C = I_E$ . Therefore, except in calculations that depend critically on the value of  $\alpha$  (e.g., the calculation of base current), one usually assumes  $\alpha \simeq 1$ .

## EXERCISES

- 6.29** For the circuit in Fig. 6.30, find the total current drawn from the power supply. Hence find the power dissipated in the circuit.

**Ans.** 4.135 mA; 62 mW

- 6.30** The circuit in Fig. E6.30 is to be connected to the circuit in Fig. 6.30(a) as indicated; specifically, the base of  $Q_3$  is to be connected to the collector of  $Q_2$ . If  $Q_3$  has  $\beta = 100$ , find the new value of  $V_{C2}$  and the values of  $V_{E3}$  and  $I_{C3}$ .

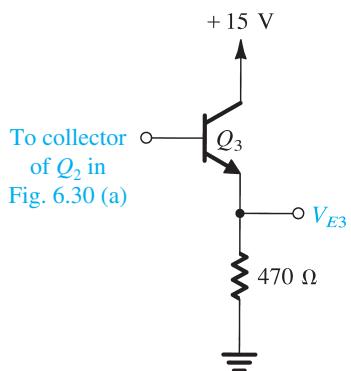
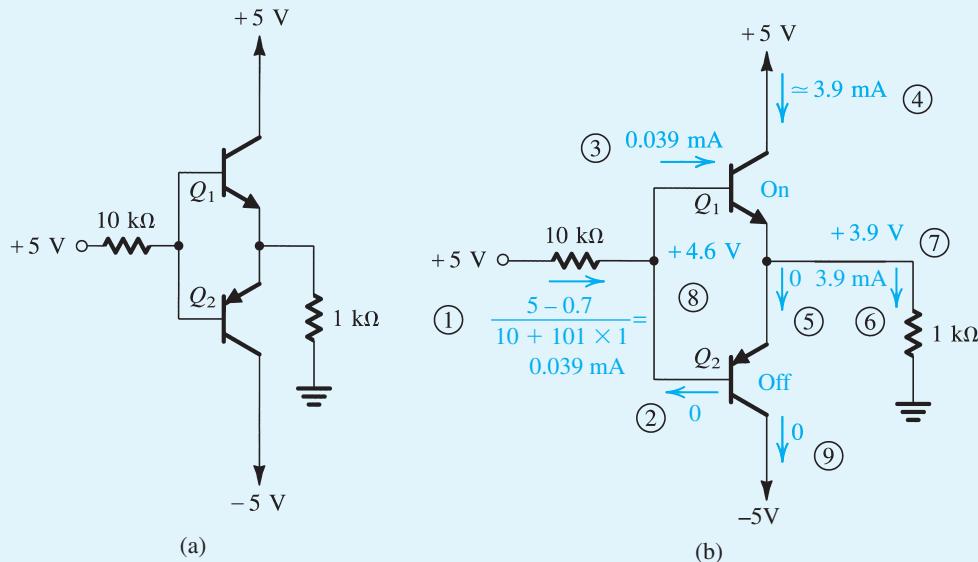


Figure E6.30

**Ans.** +7.06 V; +6.36 V; 13.4 mA

### Example 6.12

We desire to evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 6.31(a). Assume  $\beta = 100$ .



**Figure 6.31** Example 6.12: (a) circuit; (b) analysis with the steps numbered.

### Solution

By examining the circuit, we conclude that the two transistors  $Q_1$  and  $Q_2$  cannot be simultaneously conducting. Thus if  $Q_1$  is on,  $Q_2$  will be off, and vice versa. Assume that  $Q_2$  is on. It follows that current will flow from ground through the  $1\text{-k}\Omega$  resistor into the emitter of  $Q_2$ . Thus the base of  $Q_2$  will be at a negative voltage, and base current will be flowing out of the base through the  $10\text{-k}\Omega$  resistor and into the  $+5\text{-V}$  supply. This is impossible, since if the base is negative, current in the  $10\text{-k}\Omega$  resistor will have to flow into the base. Thus we conclude that our original assumption—that  $Q_2$  is on—is incorrect. It follows that  $Q_2$  will be off and  $Q_1$  will be on.

The question now is whether  $Q_1$  is active or saturated. The answer in this case is obvious: Since the base is fed with a  $+5\text{-V}$  supply and since base current flows into the base of  $Q_1$ , it follows that the base of  $Q_1$  will be at a voltage lower than  $+5\text{ V}$ . Thus the collector–base junction of  $Q_1$  is reverse biased and  $Q_1$  is in the active mode. It remains only to determine the currents and voltages using techniques already described in detail. The results are given in Fig. 6.31(b).

### EXERCISES

- 6.31** Solve the problem in Example 6.12 for the case of a voltage of  $-5\text{ V}$  feeding the bases. What voltage appears at the emitters?

**Ans.**  $-3.9\text{ V}$

- 6.32** Solve the problem in Example 6.12 with the voltage feeding the bases changed to  $+10\text{ V}$ . Assume that  $\beta_{\min} = 30$ , and find  $V_E$ ,  $V_B$ ,  $I_{C1}$ , and  $I_{C2}$ .

**Ans.**  $+4.8\text{ V}$ ;  $+5.5\text{ V}$ ;  $4.35\text{ mA}$ ;  $0$

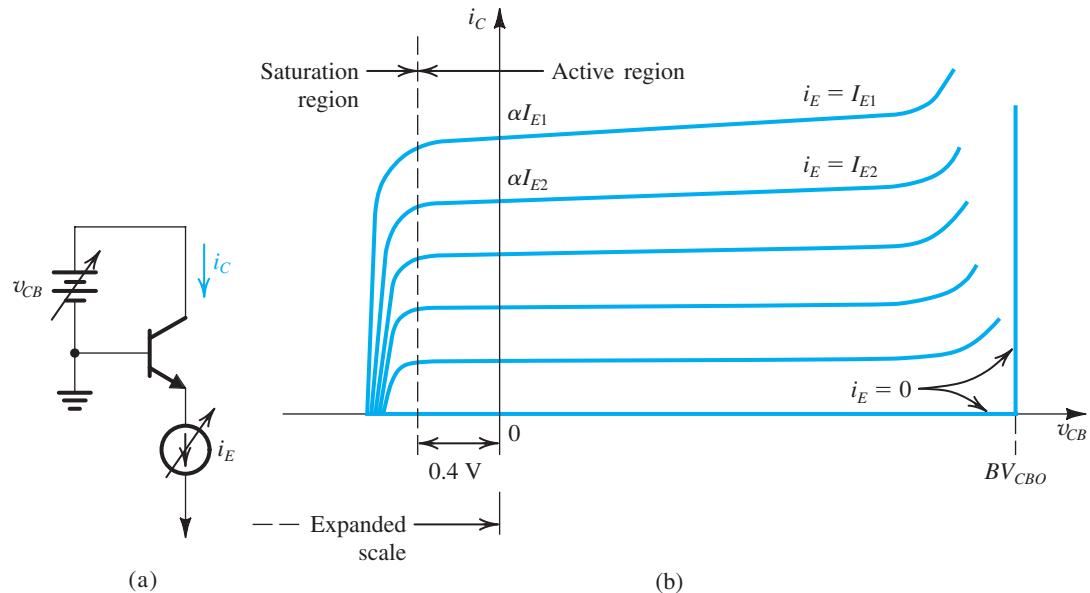
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## 6.4 Transistor Breakdown and Temperature Effects

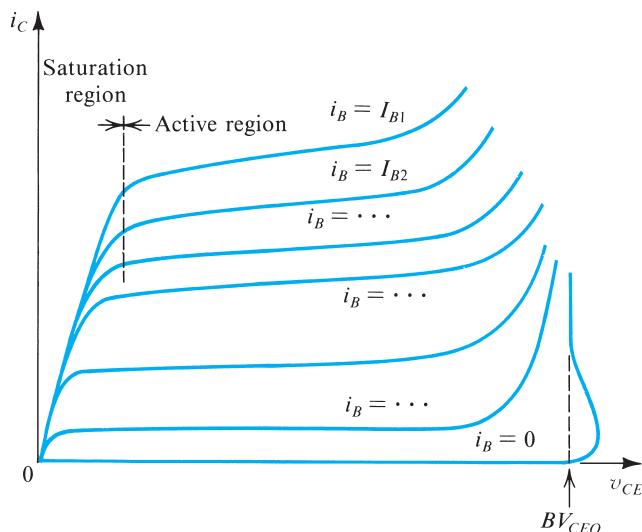
We conclude this chapter with a brief discussion of two important nonideal effects in the BJT: voltage breakdown, and the dependence of  $\beta$  on  $I_C$  and temperature.

### 6.4.1 Transistor Breakdown

The maximum voltages that can be applied to a BJT are limited by the EBJ and CBJ breakdown effects that follow the avalanche multiplication mechanism described in Section 3.5.3. Consider first the common-base configuration (Fig. 6.32(a)). The  $i_C - v_{CB}$  characteristics in Fig. 6.32(b) indicate that for  $i_E = 0$  (i.e., with the emitter open-circuited) the collector–base junction breaks down at a voltage denoted by  $BV_{CBO}$ . For  $i_E > 0$ , breakdown occurs at voltages smaller than  $BV_{CBO}$ . Typically, for discrete BJTs,  $BV_{CBO}$  is greater than  $50\text{ V}$ .



**Figure 6.32** The BJT common-base characteristics including the transistor breakdown region.



**Figure 6.33** The BJT common-emitter characteristics including the breakdown region.

Next consider the common-emitter characteristics of Fig. 6.33, which show breakdown occurring at a voltage  $BV_{CEO}$ . Here, although breakdown is still of the avalanche type, the effects on the characteristics are more complex than in the common-base configuration. We will not explain these in detail; it is sufficient to point out that typically  $BV_{CEO}$  is about half  $BV_{CBO}$ . On transistor data sheets,  $BV_{CEO}$  is sometimes referred to as the **sustaining voltage**  $LV_{CEO}$ .

Breakdown of the CBJ in either the common-base or common-emitter configuration is not destructive as long as the power dissipation in the device is kept within safe limits. This, however, is not the case with the breakdown of the emitter–base junction. The EBJ breaks down in an avalanche manner at a voltage  $BV_{EBO}$  much smaller than  $BV_{CBO}$ . Typically,  $BV_{EBO}$  is in the range of 6 V to 8 V, and the breakdown is destructive in the sense that the  $\beta$  of the transistor is permanently reduced. This does not prevent use of the EBJ as a zener diode to generate reference voltages in IC design. In such applications one is not concerned with the  $\beta$ -degradation effect. A circuit arrangement to prevent EBJ breakdown in IC amplifiers will be discussed in Chapter 13. Transistor breakdown and the maximum allowable power dissipation are important parameters in the design of power amplifiers (Chapter 12).

### EXERCISE

**6.33** What is the output voltage of the circuit in Fig. E6.33 if the transistor  $BV_{BCO} = 70$  V?

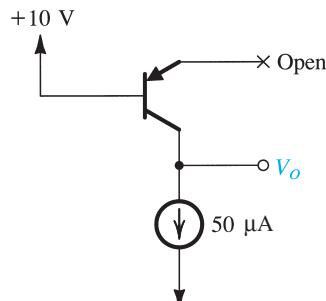


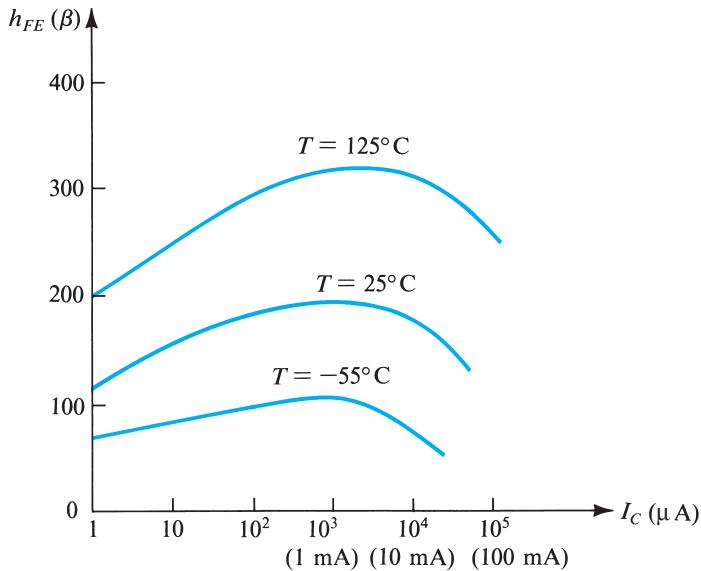
Figure E6.33

**Ans.** -60 V

### 6.4.2 Dependence of $\beta$ on $I_C$ and Temperature

Throughout this chapter we have assumed that the transistor common-emitter dc current gain,  $\beta$  or  $h_{FE}$ , is constant for a given transistor. In fact,  $\beta$  depends on the dc current at which the transistor is operating, as shown in Fig. 6.34. The physical processes that give rise to this dependence are beyond the scope of this book. Note, however, that there is a current range over which  $\beta$  is highest. Normally, one arranges to operate the transistor at a current within this range.

Figure 6.34 also shows the dependence of  $\beta$  on temperature. The fact that  $\beta$  increases with temperature can lead to serious problems in transistors that operate at large power levels (see Chapter 12).



**Figure 6.34** Typical dependence of  $\beta$  on  $I_C$  and on temperature in an integrated-circuit *npn* silicon transistor intended for operation around 1 mA.

## Summary

- Depending on the bias conditions on its two junctions, the BJT can operate in one of three possible modes: cutoff (both junctions reverse biased), active (the EBJ forward biased and the CBJ reverse biased), and saturation (both junctions forward biased). Refer to Table 6.1.
- For amplifier applications, the BJT is operated in the active mode. Switching applications make use of the cutoff and saturation modes.
- A BJT operating in the active mode provides a collector current  $i_C = I_s e^{[v_{BE}]/V_T}$ . The base current  $i_B = i_C/\beta$ , and the emitter current  $i_E = i_C + i_B$ . Also,  $i_C = \alpha i_E$ , and thus  $\beta = \alpha/(1 - \alpha)$  and  $\alpha = \beta/(\beta + 1)$ . See Table 6.2.
- To ensure operation in the active mode, the collector voltage of an *npn* transistor must be kept higher than approximately 0.4 V below the base voltage. For a *pnp* transistor, the collector voltage must be lower than approximately 0.4 V above the base voltage. Otherwise, the CBJ becomes forward biased, and the transistor enters the saturation region.
- At a constant collector current, the magnitude of the base-emitter voltage decreases by about 2 mV for every 1°C rise in temperature.
- The BJT will be at the edge of saturation when  $|v_{CE}|$  is reduced to about 0.3 V. In saturation,  $|v_{CE}| \approx 0.2$  V, and the ratio of  $i_C$  to  $i_B$  is lower than  $\beta$  (i.e.,  $\beta_{\text{forced}} < \beta$ ).
- In the active mode,  $i_C$  shows a slight dependence on  $v_{CE}$ . This phenomenon, known as the Early effect, is modeled by ascribing a finite (i.e., noninfinite) output resistance to the BJT:  $r_o = |V_A|/I'_C$ , where  $V_A$  is the Early voltage and  $I'_C$  is the dc collector current without the Early effect taken into account. In discrete circuits,  $r_o$  plays a minor role and can usually be neglected. This is *not* the case, however, in integrated-circuit design (Chapter 8).
- The dc analysis of transistor circuits is greatly simplified by assuming that  $|V_{BE}| \approx 0.7$  V. Refer to Table 6.3.
- If the BJT is conducting, one assumes it is operating in the active mode and, using the active-mode model, proceeds to determine all currents and voltages. The validity of the initial assumption is then checked by determining whether the CBJ is reverse biased. If it is, the analysis is complete; otherwise, we assume the BJT is operating in saturation and redo the analysis, using the saturation-mode model and checking at the end that  $I_C < \beta I_B$ .

## Computer Simulations Problems

**SIM** Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSPice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

### Section 6.1: Device Structure and Physical Operation

**6.1** The terminal voltages of various *npn* transistors are measured during operation in their respective circuits with the following results:

Case	E	B	C	Mode
1	0	0.7	0.7	
2	0	0.8	0.1	
3	-0.7	0	1.0	
4	-0.7	0	-0.6	
5	1.3	2.0	5.0	
6	0	0	5.0	

In this table, where the entries are in volts, 0 indicates the reference terminal to which the black (negative) probe of the voltmeter is connected. For each case, identify the mode of operation of the transistor.

**6.2** Two transistors, fabricated with the same technology but having different junction areas, when operated at a base-emitter voltage of 0.75 V, have collector currents of 0.5 mA and 2 mA. Find  $I_s$  for each device. What are the relative junction areas?

**6.3** In a particular technology, a small BJT operating at  $v_{BE} = 30V_T$  conducts a collector current of 200  $\mu$ A. What is the corresponding saturation current? For a transistor in the same technology but with an emitter junction that is 32 times larger, what is the saturation current? What current will this transistor conduct at  $v_{BE} = 30V_T$ ? What is the base-emitter voltage of the latter transistor at  $i_C = 1$  mA? Assume active-mode operation in all cases.

**6.4** Two transistors have EBJ areas as follows:  $A_{E1} = 200 \mu\text{m} \times 200 \mu\text{m}$  and  $A_{E2} = 0.4 \mu\text{m} \times 0.4 \mu\text{m}$ . If the two

transistors are operated in the active mode and conduct equal collector currents, what do you expect the difference in their  $v_{BE}$  values to be?

**6.5** Find the collector currents that you would expect for operation at  $v_{BE} = 700$  mV for transistors for which  $I_s = 10^{-13}$  A and  $I_s = 10^{-18}$  A. For the transistor with the larger EBJ, what is the  $v_{BE}$  required to provide a collector current equal to that provided by the smaller transistor at  $v_{BE} = 700$  mV? Assume active-mode operation in all cases.

**6.6** In this problem, we contrast two BJT integrated-circuit fabrication technologies: For the “old” technology, a typical *npn* transistor has  $I_s = 2 \times 10^{-15}$  A, and for the “new” technology, a typical *npn* transistor has  $I_s = 2 \times 10^{-18}$  A. These typical devices have vastly different junction areas and base width. For our purpose here we wish to determine the  $v_{BE}$  required to establish a collector current of 1 mA in each of the two typical devices. Assume active-mode operation.

**6.7** Consider an *npn* transistor whose base-emitter drop is 0.76 V at a collector current of 5 mA. What current will it conduct at  $v_{BE} = 0.70$  V? What is its base-emitter voltage for  $i_C = 5 \mu\text{A}$ ?

**6.8** In a particular BJT, the base current is 10  $\mu\text{A}$ , and the collector current is 800  $\mu\text{A}$ . Find  $\beta$  and  $\alpha$  for this device.

**6.9** Find the values of  $\beta$  that correspond to  $\alpha$  values of 0.5, 0.8, 0.9, 0.95, 0.98, 0.99, 0.995, and 0.999.

**6.10** Find the values of  $\alpha$  that correspond to  $\beta$  values of 1, 2, 10, 20, 50, 100, 200, 500, and 1000.

**\*6.11** Show that for a transistor with  $\alpha$  close to unity, if  $\alpha$  changes by a small per-unit amount ( $\Delta\alpha/\alpha$ ), the corresponding per-unit change in  $\beta$  is given approximately by

$$\frac{\Delta\beta}{\beta} \simeq \beta \left( \frac{\Delta\alpha}{\alpha} \right)$$

Now, for a transistor whose nominal  $\beta$  is 100, find the percentage change in its  $\alpha$  value corresponding to a drop in its  $\beta$  of 10%.

**6.12** An *npn* transistor of a type whose  $\beta$  is specified to range from 50 to 300 is connected in a circuit with emitter grounded, collector at +10 V, and a current of 10  $\mu\text{A}$  injected into the base. Calculate the range of collector and emitter currents that can result. What is the maximum power dissipated in the transistor? (Note: Perhaps you can see why this is a bad way to establish the operating current in the collector of a BJT.)

**6.13** A BJT is specified to have  $I_s = 5 \times 10^{-15}$  A and  $\beta$  that falls in the range of 50 to 200. If the transistor is operated in the active mode with  $v_{BE}$  set to 0.700 V, find the expected range of  $i_c$ ,  $i_b$ , and  $i_e$ .

**6.14** Measurements made on a number of transistors operating in the active mode with  $i_e = 1$  mA indicate base currents of 10  $\mu$ A, 20  $\mu$ A, and 50  $\mu$ A. For each device, find  $i_c$ ,  $\beta$ , and  $\alpha$ .

**6.15** Measurements of  $V_{BE}$  and two terminal currents taken on a number of *npn* transistors operating in the active mode are tabulated below. For each, calculate the missing current value as well as  $\alpha$ ,  $\beta$ , and  $I_s$  as indicated by the table.

Transistor	a	b	c	d	e
$V_{BE}$ (mV)	700	690	580	780	820
$I_c$ (mA)	1.000	1.000		10.10	
$I_b$ ( $\mu$ A)	10		5	120	1050
$I_e$ (mA)		1.020	0.235		75.00
$\alpha$					
$\beta$					
$I_s$					

**6.16** When operated in the active mode, a particular *npn* BJT conducts a collector current of 1 mA and has  $v_{BE} = 0.70$  V and  $i_b = 10 \mu$ A. Use these data to create specific transistor models of the form shown in Fig. 6.5(a) to (d).

**6.17** Using the *npn* transistor model of Fig. 6.5(b), consider the case of a transistor for which the base is connected to ground, the collector is connected to a 5-V dc source through a 2-k $\Omega$  resistor, and a 2-mA current source is connected to the emitter with the polarity so that current is drawn out of the emitter terminal. If  $\beta = 100$  and  $I_s = 5 \times 10^{-15}$  A, find the voltages at the emitter and the collector and calculate the base current.

**D 6.18** Consider an *npn* transistor operated in the active mode and represented by the model of Fig. 6.5(d). Let the transistor be connected as indicated by the equivalent circuit shown in Fig. 6.6(b). It is required to calculate the values of  $R_B$  and  $R_C$  that will establish a collector current  $I_c$  of 0.5 mA and a collector-to-emitter voltage  $V_{CE}$  of 1 V. The BJT is specified to have  $\beta = 50$  and  $I_s = 5 \times 10^{-15}$  A.

**6.19** An *npn* transistor has a CBJ with an area 100 times that of the EBJ. If  $I_s = 10^{-15}$  A, find the voltage drop across EBJ

and across CBJ when each is forward biased and conducting a current of 1 mA. Also find the forward current each junction would conduct when forward biased with 0.5 V.

**\*6.20** We wish to investigate the operation of the *npn* transistor in saturation using the model of Fig. 6.9. Let  $I_s = 10^{-15}$  A,  $v_{BE} = 0.7$  V,  $\beta = 100$ , and  $I_{SC}/I_s = 100$ . For each of three values of  $v_{CE}$  (namely, 0.4 V, 0.3 V, and 0.2 V), find  $v_{BC}$ ,  $i_{BC}$ ,  $i_{BE}$ ,  $i_b$ ,  $i_c$ , and  $i_c/i_b$ . Present your results in tabular form. Also find  $v_{CE}$  that results in  $i_c = 0$ .

**\*6.21** Use Eqs. (6.14), (6.15), and (6.16) to show that an *npn* transistor operated in saturation exhibits a collector-to-emitter voltage,  $V_{CEsat}$ , given by

$$V_{CEsat} = V_T \ln \left[ \left( \frac{I_{SC}}{I_s} \right) \frac{1 + \beta_{\text{forced}}}{1 - \beta_{\text{forced}}/\beta} \right]$$

Use this relationship to evaluate  $V_{CEsat}$  for  $\beta_{\text{forced}} = 50$ , 10, 5, and 1 for a transistor with  $\beta = 100$  and with a CBJ area 100 times that of the EBJ. Present your results in a table.

**6.22** Consider the *pnp* large-signal model of Fig. 6.11(b) applied to a transistor having  $I_s = 10^{-14}$  A and  $\beta = 50$ . If the emitter is connected to ground, the base is connected to a current source that pulls 10  $\mu$ A out of the base terminal, and the collector is connected to a negative supply of -5 V via a 8.2-k $\Omega$  resistor, find the collector voltage, the emitter current, and the base voltage.

**6.23** A *pnp* transistor has  $v_{EB} = 0.7$  V at a collector current of 1 mA. What do you expect  $v_{EB}$  to become at  $i_c = 10$  mA? At  $i_c = 100$  mA?

**6.24** A *pnp* transistor modeled with the circuit in Fig. 6.11(b) is connected with its base at ground, collector at -2.0 V, and a 1-mA current is injected into its emitter. If the transistor is said to have  $\beta = 10$ , what are its base and collector currents? In which direction do they flow? If  $I_s = 10^{-15}$  A, what voltage results at the emitter? What does the collector current become if a transistor with  $\beta = 1000$  is substituted? (Note: The fact that the collector current changes by less than 10% for a large change in  $\beta$  illustrates that this is a good way to establish a specific collector current.)

**6.25** A *pnp* power transistor operates with an emitter-to-collector voltage of 5 V, an emitter current of 5 A, and  $V_{EB} = 0.8$  V. For  $\beta = 20$ , what base current is required? What is  $I_s$  for this transistor? Compare the emitter-base junction area of this transistor with that of a small-signal

transistor that conducts  $i_c = 1 \text{ mA}$  with  $v_{EB} = 0.70 \text{ V}$ . How much larger is it?

**6.26** While Fig. 6.5 provides four possible large-signal equivalent circuits for the *npn* transistor, only two equivalent circuits for the *pnp* transistor are provided in Fig. 6.11. Supply the missing two.

**6.27** By analogy to the *npn* case shown in Fig. 6.9, give the equivalent circuit of a *pnp* transistor in saturation.

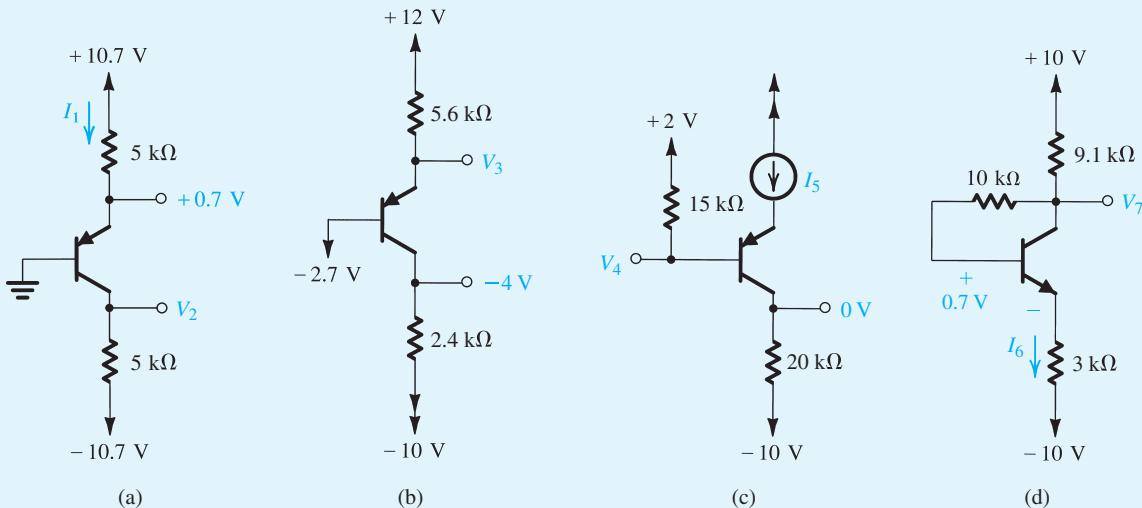


Figure P6.28

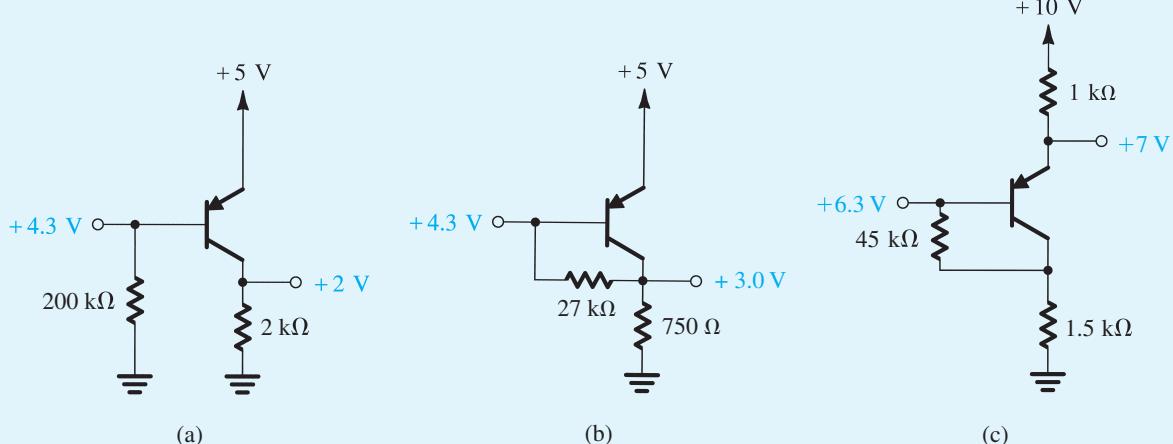


Figure P6.29

## Section 6.2: Current–Voltage Characteristics

**6.28** For the circuits in Fig. P6.28, assume that the transistors have very large  $\beta$ . Some measurements have been made on these circuits, with the results indicated in the figure. Find the values of the other labeled voltages and currents.

**6.29** Measurements on the circuits of Fig. P6.29 produce labeled voltages as indicated. Find the value of  $\beta$  for each transistor.

**6.30** A very simple circuit for measuring  $\beta$  of an *npn* transistor is shown in Fig. P6.30. In a particular design,  $V_{CC}$  is provided by a 9-V battery; M is a current meter with a 50- $\mu$ A full scale and relatively low resistance that you can neglect for our purposes here. Assuming that the transistor has  $V_{BE} = 0.7$  V at  $I_E = 1$  mA, what value of  $R_C$  would establish a resistor current of 1 mA? Now, to what value of  $\beta$  does a meter reading of full scale correspond? What is  $\beta$  if the meter reading is 1/5 of full scale? 1/10 of full scale?

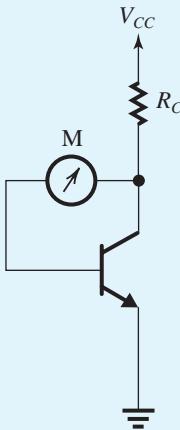


Figure P6.30

**6.31** Repeat Exercise 6.13 for the situation in which the power supplies are reduced to  $\pm 2.5$  V.

**D 6.32** Design the circuit in Fig. P6.32 to establish a current of 0.5 mA in the emitter and a voltage of  $-0.5$  V at the collector. The transistor  $v_{EB} = 0.64$  V at  $I_E = 0.1$  mA, and  $\beta = 100$ . To what value can  $R_C$  be increased while the collector current remains unchanged?

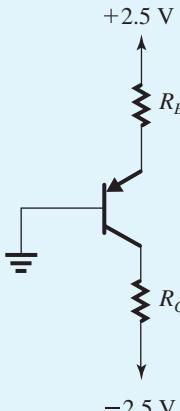


Figure P6.32

**D 6.33** Examination of the table of standard values for resistors with 5% tolerance in Appendix J reveals that the closest values to those found in the design of Example 6.2 are 5.1 k $\Omega$  and 6.8 k $\Omega$ . For these values, use approximate calculations (e.g.,  $V_{BE} \approx 0.7$  V and  $\alpha \approx 1$ ) to determine the values of collector current and collector voltage that are likely to result.

**D 6.34** Design the circuit in Fig. P6.34 to establish  $I_C = 0.2$  mA and  $V_c = 0.5$  V. The transistor exhibits  $v_{BE}$  of 0.8 V at  $i_c = 1$  mA, and  $\beta = 100$ .

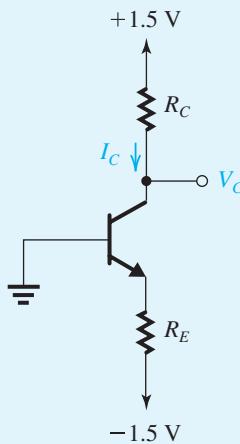


Figure P6.34

**6.35** For each of the circuits shown in Fig. P6.35, find the emitter, base, and collector voltages and currents. Use  $\beta = 50$ , but assume  $|V_{BE}| = 0.8$  V independent of current level.

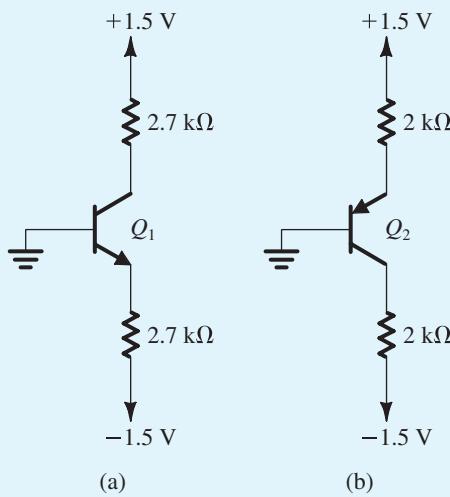


Figure P6.35

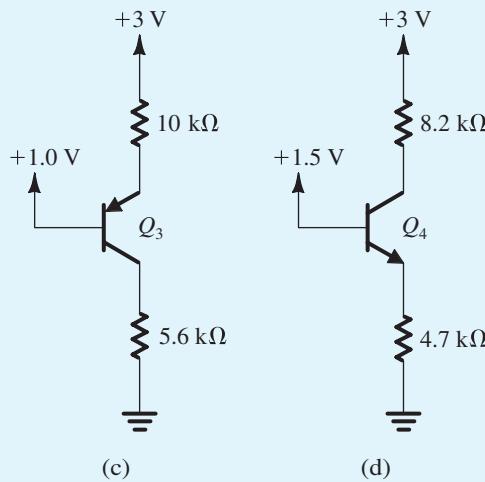


Figure P6.35 continued

**6.36** The current  $I_{CBO}$  of a small transistor is measured to be  $10\text{ nA}$  at  $25^\circ\text{C}$ . If the temperature of the device is raised to  $125^\circ\text{C}$ , what do you expect  $I_{CBO}$  to become?

**6.37** Augment the model of the *npn* BJT shown in Fig. 6.19(a) by a current source representing  $I_{CBO}$ . Assume that  $r_o$  is very large and thus can be neglected. In terms of this addition, what do the terminal currents  $i_B$ ,  $i_C$ , and  $i_E$  become? If the base lead is open-circuited while the emitter is connected to ground, and the collector is connected to a positive supply, find the emitter and collector currents.

**6.38** A BJT whose emitter current is fixed at  $1\text{ mA}$  has a base-emitter voltage of  $0.70\text{ V}$  at  $25^\circ\text{C}$ . What base-emitter voltage would you expect at  $0^\circ\text{C}$ ? At  $100^\circ\text{C}$ ?

**6.39** A particular *pnp* transistor operating at an emitter current of  $0.5\text{ mA}$  at  $20^\circ\text{C}$  has an emitter-base voltage of  $692\text{ mV}$ .

- What does  $v_{EB}$  become if the junction temperature rises to  $50^\circ\text{C}$ ?
- If the transistor is operated at a fixed emitter-base voltage of  $700\text{ mV}$ , what emitter current flows at  $20^\circ\text{C}$ ? At  $50^\circ\text{C}$ ?

**6.40** Consider a transistor for which the base-emitter voltage drop is  $0.7\text{ V}$  at  $10\text{ mA}$ . What current flows for  $v_{BE} = 0.5\text{ V}$ ? Evaluate the ratio of the slopes of the  $i_C-v_{BE}$  curve at  $v_{BE} = 700\text{ mV}$  and at  $v_{BE} = 500\text{ mV}$ . The large ratio confirms the point that the BJT has an “apparent threshold” at  $v_{BE} \approx 0.5\text{ V}$ .

**6.41** Use Eq. (6.18) to plot  $i_C$  versus  $v_{CE}$  for an *npn* transistor having  $I_s = 10^{-15}\text{ A}$  and  $V_A = 100\text{ V}$ . Provide curves for  $v_{BE} = 0.65, 0.70, 0.72, 0.73$ , and  $0.74$  volts. Show the characteristics for  $v_{CE}$  up to  $15\text{ V}$ .

**\*6.42** In the circuit shown in Fig. P6.42, current source  $I$  is  $1.1\text{ mA}$ , and at  $25^\circ\text{C}$   $v_{BE} = 680\text{ mV}$  at  $i_E = 1\text{ mA}$ . At  $25^\circ\text{C}$  with  $\beta = 100$ , what currents flow in  $R_1$  and  $R_2$ ? What voltage would you expect at node E? Noting that the temperature coefficient of  $v_{BE}$  for  $I_E$  constant is  $-2\text{ mV}/^\circ\text{C}$ , what is the TC of  $v_E$ ? For an ambient temperature of  $75^\circ\text{C}$ , what voltage would you expect at node E? Clearly state any simplifying assumptions you make.

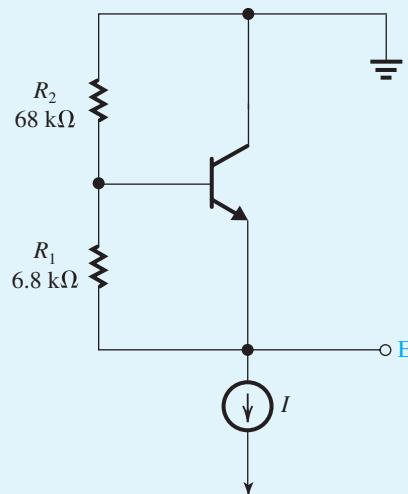


Figure P6.42

**6.43** For a particular *npn* transistor operating at a  $v_{BE}$  of  $680\text{ mV}$  and  $I_C = 1\text{ mA}$ , the  $i_C-v_{CE}$  characteristic has a slope of  $0.8 \times 10^{-5}\text{ }\mathcal{V}$ . To what value of output resistance does this correspond? What is the value of the Early voltage for this transistor? For operation at  $10\text{ mA}$ , what would the output resistance become?

**6.44** For a BJT having an Early voltage of  $50\text{ V}$ , what is its output resistance at  $1\text{ mA}$ ? At  $100\text{ }\mu\text{A}$ ?

**6.45** Measurements of the  $i_C-v_{CE}$  characteristic of a small-signal transistor operating at  $v_{BE} = 710\text{ mV}$  show that  $i_C = 1.1\text{ mA}$  at  $v_{CE} = 5\text{ V}$  and that  $i_C = 1.3\text{ mA}$  at  $v_{CE} = 15\text{ V}$ . What is the corresponding value of  $i_C$  near saturation? At what value of  $v_{CE}$  is  $i_C = 1.2\text{ mA}$ ? What is the value of the Early voltage for this transistor? What is the output resistance that corresponds to operation at  $v_{BE} = 710\text{ mV}$ ?

**6.46** Give the *pnp* equivalent circuit models that correspond to those shown in Fig. 6.19 for the *npn* case.

**6.47** A BJT operating at  $i_B = 10 \mu\text{A}$  and  $i_C = 1.0 \text{ mA}$  undergoes a reduction in base current of  $1.0 \mu\text{A}$ . It is found that when  $v_{CE}$  is held constant, the corresponding reduction in collector current is  $0.08 \text{ mA}$ . What are the values of  $\beta$  and the incremental  $\beta$  or  $\beta_{ac}$  that apply? If the base current is increased from  $10 \mu\text{A}$  to  $12 \mu\text{A}$  and  $v_{CE}$  is increased from  $8 \text{ V}$  to  $10 \text{ V}$ , what collector current results? Assume  $V_A = 100 \text{ V}$ .

**6.48** For the circuit in Fig. P6.48 let  $V_{CC} = 10 \text{ V}$ ,  $R_C = 1 \text{ k}\Omega$ , and  $R_B = 10 \text{ k}\Omega$ . The BJT has  $\beta = 50$ . Find the value of  $V_{BB}$  that results in the transistor operating

- in the active mode with  $V_C = 2 \text{ V}$ ;
- at the edge of saturation;
- deep in saturation with  $\beta_{\text{forced}} = 10$ .

Assume  $V_{BE} \approx 0.7 \text{ V}$ .

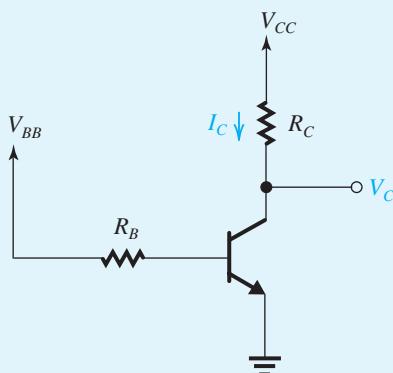


Figure P6.48

**SIM D \*6.49** Consider the circuit of Fig. P6.48 for the case  $V_{BB} = V_{CC}$ . If the BJT is saturated, use the equivalent circuit of Fig. 6.21 to derive an expression for  $\beta_{\text{forced}}$  in terms of  $V_{CC}$  and  $(R_B/R_C)$ . Also derive an expression for the total power dissipated in the circuit. For  $V_{CC} = 5 \text{ V}$ , design the circuit to obtain operation at a forced  $\beta$  as close to 10 as possible while limiting the power dissipation to no larger than  $20 \text{ mW}$ . Use 1% resistors (see Appendix J).

**6.50** The *pnp* transistor in the circuit in Fig. P6.50 has  $\beta = 50$ . Show that the BJT is operating in the saturation mode and find  $\beta_{\text{forced}}$  and  $V_C$ . To what value should  $R_B$  be increased in order for the transistor to operate at the edge of saturation?

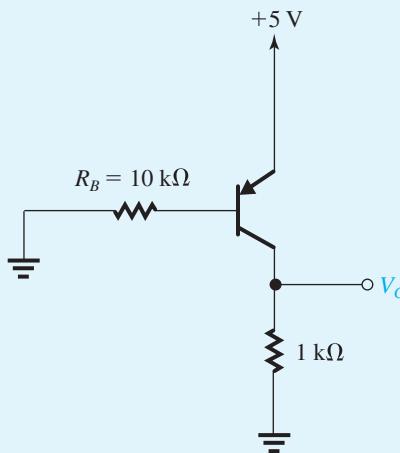


Figure P6.50

### Section 6.3: BJT Circuits at DC

**6.51** The transistor in the circuit of Fig. P6.51 has a very high  $\beta$ . Find  $V_E$  and  $V_C$  for  $V_B$  (a)  $+2.0 \text{ V}$ , (b)  $+1.7 \text{ V}$ , and (c)  $0 \text{ V}$ .

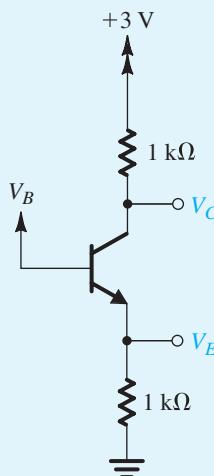


Figure P6.51

**6.52** The transistor in the circuit of Fig. P6.51 has a very high  $\beta$ . Find the highest value of  $V_B$  for which the transistor still operates in the active mode. Also, find the value of  $V_B$  for which the transistor operates in saturation with a forced  $\beta$  of 2.

**6.53** Consider the operation of the circuit shown in Fig. P6.53 for  $V_B$  at  $-1 \text{ V}$ ,  $0 \text{ V}$ , and  $+1 \text{ V}$ . Assume that  $\beta$  is very high. What values of  $V_E$  and  $V_C$  result? At what value of  $V_B$  does the emitter current reduce to one-tenth of

its value for  $V_B = 0$  V? For what value of  $V_B$  is the transistor just at the edge of conduction? ( $v_{BE} = 0.5$  V) What values of  $V_E$  and  $V_C$  correspond? For what value of  $V_B$  does the transistor reach the edge of saturation? What values of  $V_C$  and  $V_E$  correspond? Find the value of  $V_B$  for which the transistor operates in saturation with a forced  $\beta$  of 2.

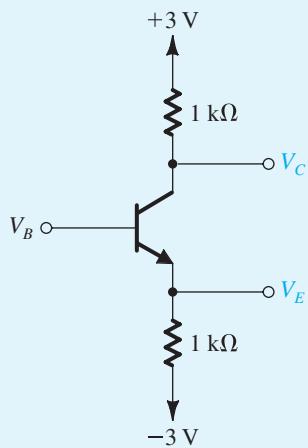


Figure P6.53

**6.54** For the transistor shown in Fig. P6.54, assume  $\alpha \approx 1$  and  $v_{BE} = 0.5$  V at the edge of conduction. What are the values of  $V_E$  and  $V_C$  for  $V_B = 0$  V? For what value of  $V_B$  does the transistor cut off? Saturate? In each case, what values of  $V_E$  and  $V_C$  result?

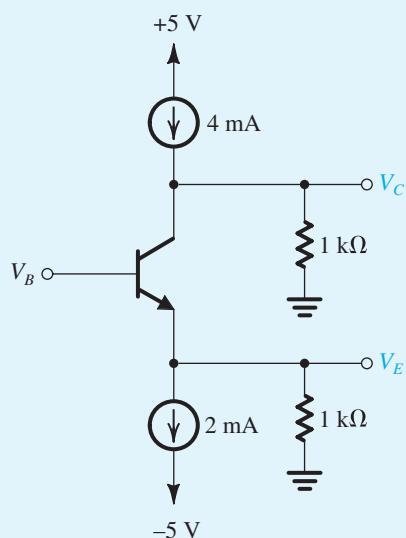


Figure P6.54

**D 6.55** Consider the circuit in Fig. P6.51 with the base voltage  $V_B$  obtained using a voltage divider across the 3-V supply. Assuming the transistor  $\beta$  to be very large (i.e., ignoring the base current), design the voltage divider to obtain  $V_B = 1.2$  V. Design for a 0.1-mA current in the voltage divider. Now, if the BJT  $\beta = 100$ , analyze the circuit to determine the collector current and the collector voltage.

**6.56** A single measurement indicates the emitter voltage of the transistor in the circuit of Fig. P5.56 to be 1.0 V. Under the assumption that  $|V_{BE}| = 0.7$  V, what are  $V_B$ ,  $I_B$ ,  $I_E$ ,  $I_C$ ,  $V_C$ ,  $\beta$ , and  $\alpha$ ? (Note: Isn't it surprising what a little measurement can lead to?)

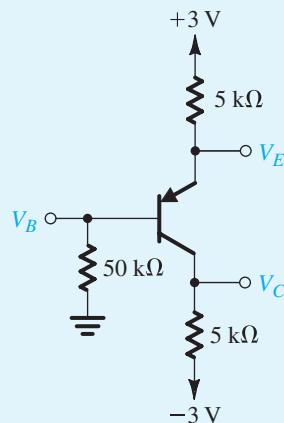


Figure P6.56

**D 6.57** Design a circuit using a *pnp* transistor for which  $\alpha \approx 1$  using two resistors connected appropriately to  $\pm 3$  V so that  $I_E = 0.5$  mA and  $V_{BC} = 1$  V. What exact values of  $R_E$  and  $R_C$  would be needed? Now, consult a table of standard 5% resistor values (e.g., that provided in Appendix J) to select suitable practical values. What values of resistors have you chosen? What are the values of  $I_E$  and  $V_{BC}$  that result?

**6.58** In the circuit shown in Fig. P6.58, the transistor has  $\beta = 40$ . Find the values of  $V_B$ ,  $V_E$ , and  $V_C$ . If  $R_B$  is raised to 100 kΩ, what voltages result? With  $R_B = 100$  kΩ, what value of  $\beta$  would return the voltages to the values first calculated?

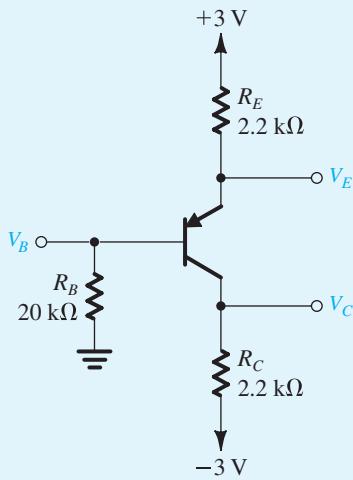


Figure P6.58

**6.59** In the circuit shown in Fig. P6.58, the transistor has  $\beta = 50$ . Find the values of  $V_B$ ,  $V_E$ , and  $V_C$ , and verify that the transistor is operating in the active mode. What is the largest value that  $R_C$  can have while the transistor remains in the active mode?

**SIM 6.60** For the circuit in Fig. P6.60, find  $V_B$ ,  $V_E$ , and  $V_C$  for  $R_B = 100 \text{ k}\Omega$ ,  $10 \text{ k}\Omega$ , and  $1 \text{ k}\Omega$ . Let  $\beta = 100$ .

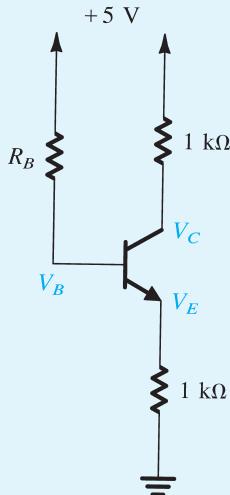


Figure P6.60

**6.61** For the circuits in Fig. P6.61, find values for the labeled node voltages and branch currents. Assume  $\beta$  to be very high.

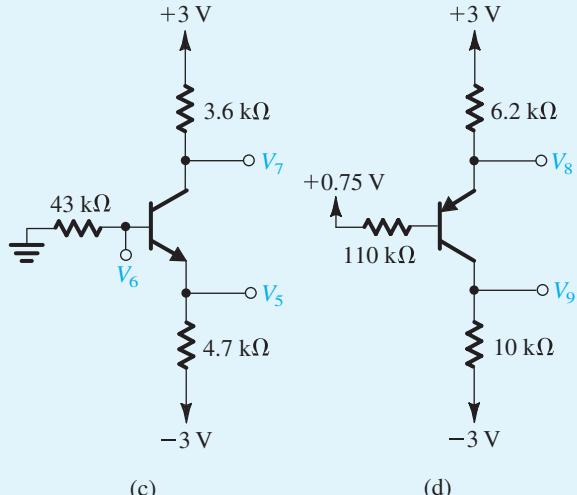
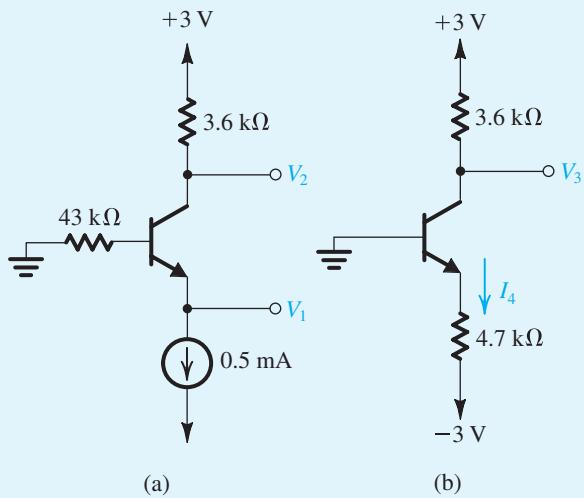


Figure P6.61

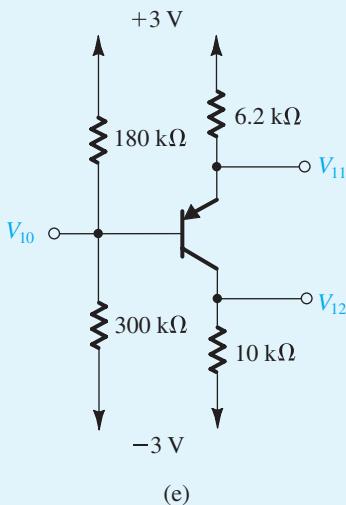


Figure P6.61 continued

**\*6.62** Repeat the analysis of the circuits in Problem 6.61 using  $\beta=100$ . Find all the labeled node voltages and branch currents.

**D \*\*6.63** It is required to design the circuit in Fig. P6.63 so that a current of 1 mA is established in the emitter and a voltage of  $-1$  V appears at the collector. The transistor type used has a nominal  $\beta$  of 100. However, the  $\beta$  value can be as low as 50 and as high as 150. Your design should ensure that the specified emitter current is obtained when  $\beta=100$  and that at the extreme values of  $\beta$  the emitter current does not change by more than 10% of its nominal value. Also, design for as large a value for  $R_B$  as possible. Give the values of  $R_B$ ,  $R_E$ , and  $R_C$  to the nearest kilohm. What is the expected range of collector current and collector voltage corresponding to the full range of  $\beta$  values?

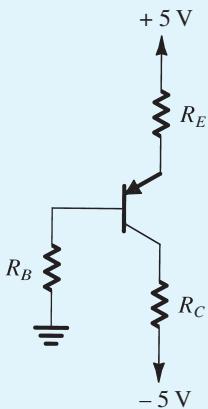


Figure P6.63

**D 6.64** The *pnp* transistor in the circuit of Fig. P6.64 has  $\beta=50$ . Find the value for  $R_C$  to obtain  $V_C = +2$  V. What happens if the transistor is replaced with another having  $\beta=100$ ? Give the value of  $V_C$  in the latter case.

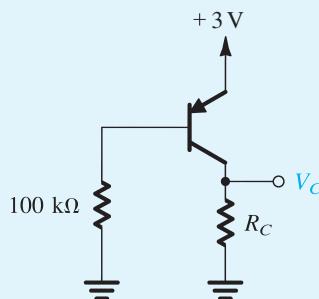


Figure P6.64

**\*\*\*6.65** Consider the circuit shown in Fig. P6.65. It resembles that in Fig. 6.30 but includes other features. First, note diodes  $D_1$  and  $D_2$  are included to make design (and analysis) easier and to provide temperature compensation for the emitter-base voltages of  $Q_1$  and  $Q_2$ . Second, note resistor  $R$ , whose purpose is to provide negative feedback (more on this later in the book!). Using  $|V_{BE}| = 0.7$  V independent of current, and  $\beta=\infty$ , find the voltages  $V_{B1}$ ,  $V_{E1}$ ,  $V_{C1}$ ,  $V_{B2}$ ,  $V_{E2}$ , and  $V_{C2}$ , initially with  $R$  open-circuited and then with  $R$  connected. Repeat for  $\beta=100$ , with  $R$  open-circuited initially, then connected.

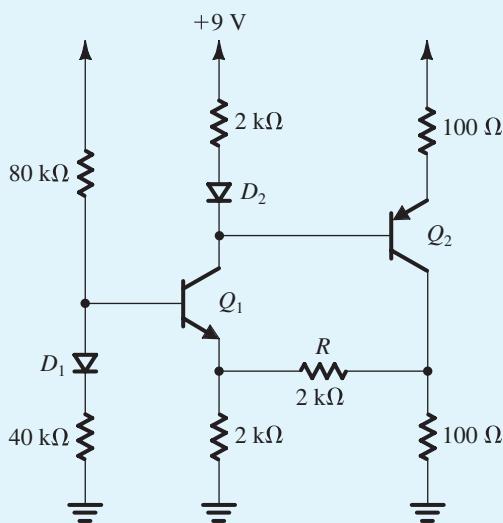


Figure P6.65

\*6.66 For the circuit shown in Fig. P6.66, find the labeled node voltages for:

- (a)  $\beta = \infty$
- (b)  $\beta = 100$

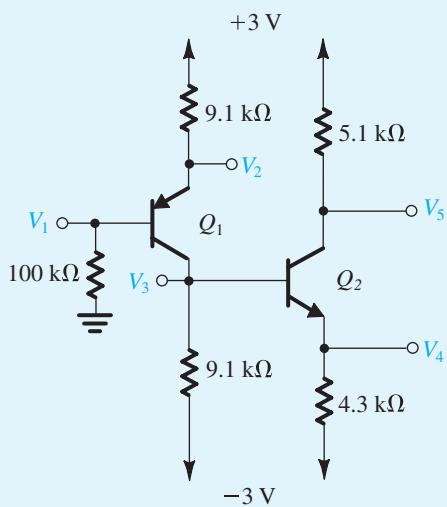


Figure P6.66

D \*6.67 Using  $\beta = \infty$ , design the circuit shown in Fig. P6.67 so that the emitter currents of  $Q_1$ ,  $Q_2$ , and  $Q_3$

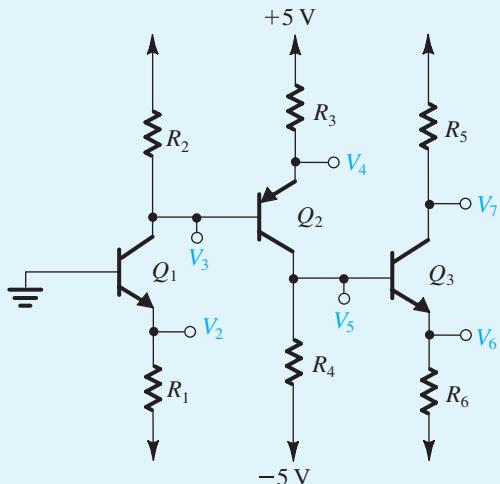


Figure P6.67

are 0.5 mA, 0.5 mA, and 1 mA, respectively, and  $V_3 = 0$ ,  $V_5 = -2$  V, and  $V_7 = 1$  V. For each resistor, select the nearest standard value utilizing the table of standard values for 5% resistors in Appendix J. Now, for  $\beta = 100$ , find the values of  $V_3$ ,  $V_4$ ,  $V_5$ ,  $V_6$ , and  $V_7$ .

\*6.68 For the circuit in Fig. P6.68, find  $V_B$  and  $V_E$  for  $v_I = 0$  V, +2 V, -2.5 V, and -5 V. The BJTs have  $\beta = 50$ .

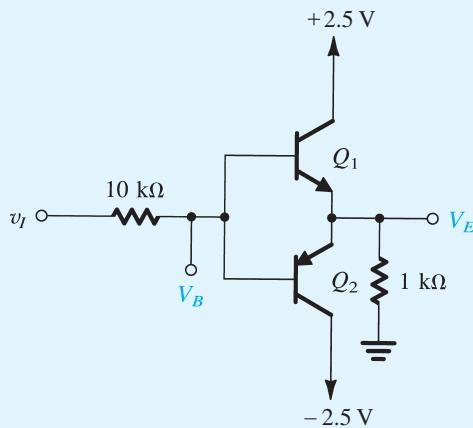


Figure P6.68

\*\*6.69 All the transistors in the circuits of Fig. P6.69 are specified to have a minimum  $\beta$  of 50. Find approximate values for the collector voltages and calculate forced  $\beta$  for each of the transistors. (Hint: Initially, assume all transistors are operating in saturation, and verify the assumption.)

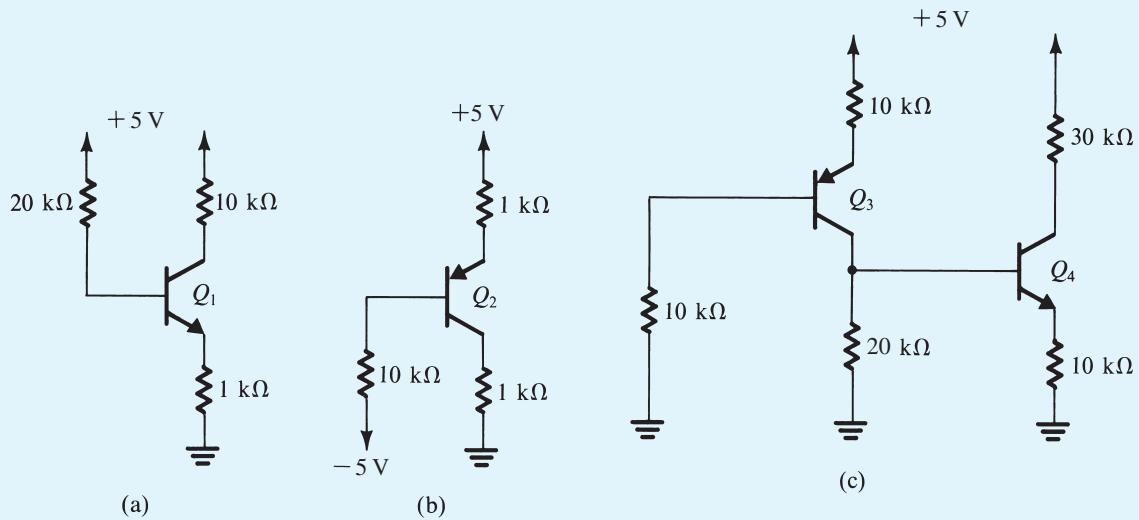


Figure P6.69

## CHAPTER 7

# Transistor Amplifiers

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**7.3 Basic Configurations 423**

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## IN THIS CHAPTER YOU WILL LEARN

1. How the transistor (a MOSFET or a BJT) can be used to make an amplifier.
  2. How to obtain linear amplification from the fundamentally nonlinear MOS and bipolar transistor.
  3. How to model the linear operation of a transistor around a bias point by an equivalent circuit that can be used in the analysis and design of transistor amplifiers.
  4. The three basic ways to connect a MOSFET or a BJT to construct amplifiers with different properties.
  5. Practical circuits for MOS and bipolar transistor amplifiers that can be constructed using discrete components.
- 

## Introduction

Having studied the two major transistor types, the MOSFET (Chapter 5) and the BJT (Chapter 6), we now begin the study of their application. There are two distinctly different kinds of transistor application: as a switch, in the design of digital circuits (Chapters 14–16) and as a controlled source, in the design of amplifiers for analog circuits. This chapter and the subsequent six focus on the latter application, namely, the use of the transistor in the design of a variety of amplifier types.

Since the basic principles that underlie the use of the MOSFET and the BJT in amplifier design are the same, the two devices are studied together in this chapter. Besides providing some economy in presentation, this unified study enables us to make important comparisons between MOS and bipolar amplifiers.

The bulk of this chapter is concerned with the fundamental principles and concepts that are the basis for the application of transistors in amplifier design: We study in detail the models that are used to represent both transistor types in the analysis and design of small-signal linear amplifiers. We also study the three basic configurations in which each of the two transistor types can be connected to realize an amplifier.

The chapter concludes with examples of discrete-circuit amplifiers. These are circuits that can be assembled using discrete transistors, resistors, and capacitors on printed-circuit boards (PCBs). They predominantly use BJTs, and their design differs in significant ways from the design of integrated-circuit (IC) amplifiers. The latter predominantly use MOSFETs, and their study begins in Chapter 8. However, the fundamental principles and concepts introduced in this chapter apply equally well to both discrete and integrated amplifiers.

## 7.1 Basic Principles

### 7.1.1 The Basis for Amplifier Operation

The basis for the application of the transistor (a MOSFET or a BJT) in amplifier design is that when the device is operated in the active region, a voltage-controlled current source is realized. Specifically, when a MOSFET is operated in the saturation or pinch-off region, also referred to in this chapter as the active region, the voltage between gate and source,  $v_{GS}$ , controls the drain current  $i_D$  according to the square-law relationship which, for an NMOS transistor, is expressed as

$$i_D = \frac{1}{2} k_n (v_{GS} - V_m)^2 \quad (7.1)$$

We note that in this first-order model of MOSFET operation, the drain current  $i_D$  does not depend on the drain voltage  $v_{DS}$  because the channel is pinched off at the drain end,<sup>1</sup> thus “isolating” the drain.

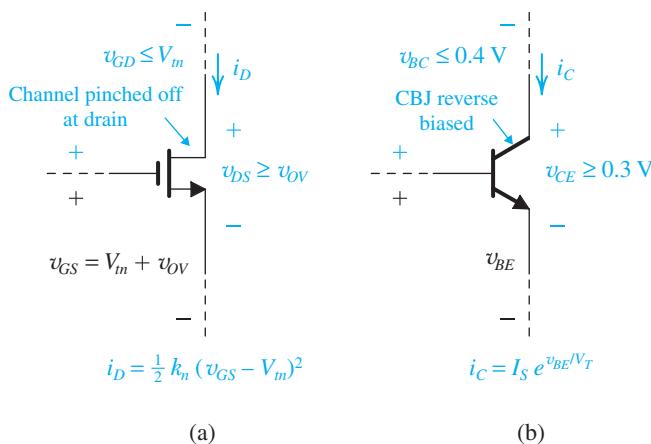
Similarly, when a BJT is operated in the active region, the base-emitter voltage  $v_{BE}$  controls the collector current  $i_C$  according to the exponential relationship which, for an *npn* transistor, is expressed as

$$i_C = I_S e^{v_{BE}/V_T} \quad (7.2)$$

Here, this first-order model of BJT operation indicates that the collector current  $i_C$  does not depend on the collector voltage  $v_{CE}$  because the collector-base junction is reverse biased, thus “isolating” the collector.

Figure 7.1 shows an NMOS transistor and an *npn* transistor operating in the active mode. Observe that for the NMOS transistor, the pinch-off condition is ensured by keeping  $v_{DS} \geq v_{OV}$ . Since the overdrive voltage  $v_{OV} = v_{GS} - V_m$ , this condition implies that  $v_{GD} \leq V_m$ , which indeed ensures channel pinch-off at the drain end.

Similarly, for the *npn* transistor in Fig. 7.1(b), the CBJ reverse-bias condition is ensured by keeping  $v_{CE} \geq 0.3$  V. Since  $v_{BE}$  is usually in the vicinity of 0.7 V,  $v_{BC}$  is thus kept



**Figure 7.1** Operating (a) an NMOS transistor and (b) an *npn* transistor in the active mode. Note that  $v_{GS} = V_m + v_{OV}$  and  $v_{DS} \geq v_{OV}$ ; thus  $v_{GD} \leq V_m$ , which ensures channel pinch-off at the drain end. Similarly,  $v_{BE} \approx 0.7$  V, and  $v_{CE} \geq 0.3$  V results in  $v_{BC} \leq 0.4$  V, which is sufficient to keep the CBJ from conducting.

<sup>1</sup>To focus on essentials, we shall neglect the Early effect until a later point.

smaller than 0.4 V, which is sufficient to prevent this relatively large-area junction from conducting.

Although we used NMOS and *npn* transistors to illustrate the conditions for active-mode operation, similar conditions apply for PMOS and *pnp* transistors, as studied in Chapters 5 and 6, respectively.

Finally, we note that the control relationships in Eqs. (7.1) and (7.2) are nonlinear. Nevertheless, we shall shortly devise a technique for obtaining almost-linear amplification from these fundamentally nonlinear devices.

### 7.1.2 Obtaining a Voltage Amplifier

From the above we see that the transistor is basically a transconductance amplifier: that is, an amplifier whose input signal is a voltage and whose output signal is a current. More commonly, however, one is interested in voltage amplifiers. A simple way to convert a transconductance amplifier to a voltage amplifier is to pass the output current through a resistor and take the voltage across the resistor as the output. Doing this for a MOSFET results in the simple amplifier circuit shown in Fig. 7.2(a). Here  $v_{GS}$  is the input voltage,  $R_D$  (known as a **load resistance**) converts the drain current  $i_D$  to a voltage ( $i_D R_D$ ), and  $V_{DD}$  is the supply voltage that powers up the amplifier and, together with  $R_D$ , establishes operation in the active region, as will be shown shortly.

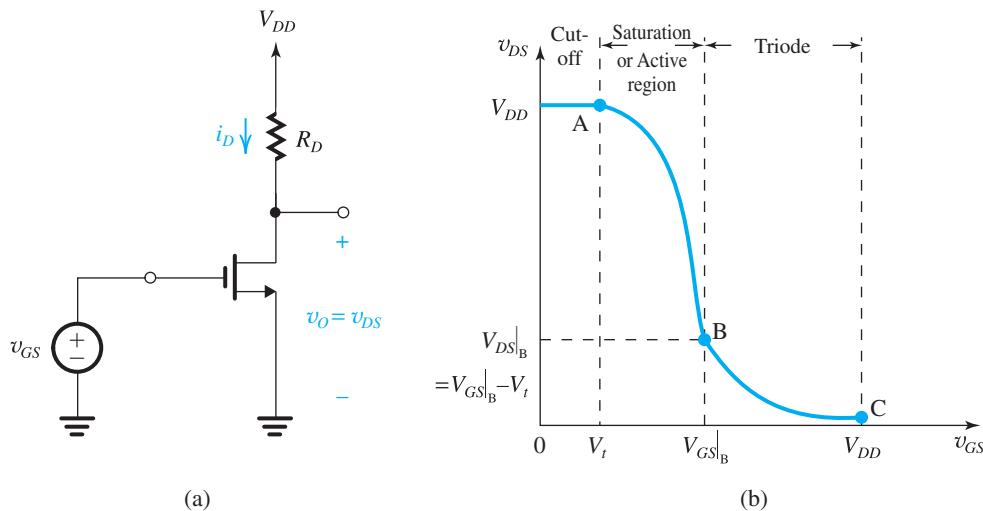
In the amplifier circuit of Fig. 7.2(a) the output voltage is taken between the drain and ground, rather than simply across  $R_D$ . This is done because of the need to maintain a common ground reference between the input and the output. The output voltage  $v_{DS}$  is given by

$$v_{DS} = V_{DD} - i_D R_D \quad (7.3)$$

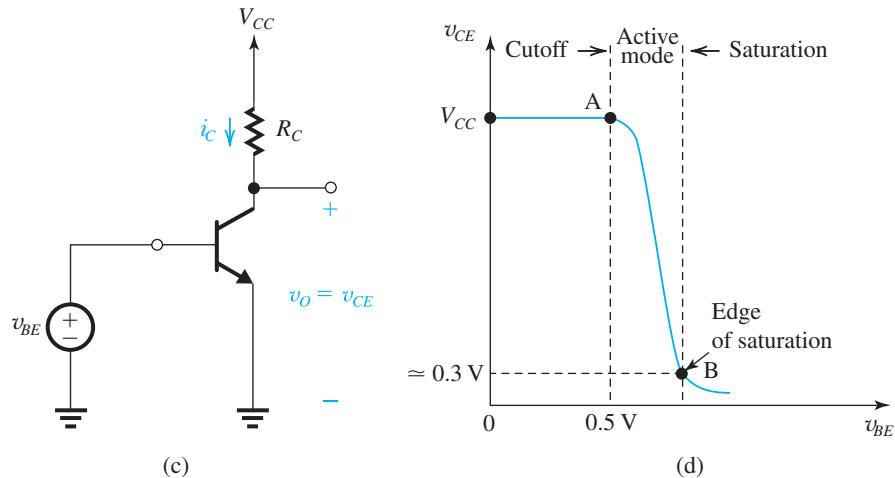
Thus it is an inverted version (note the minus sign) of  $i_D R_D$  that is shifted by the constant value of the supply voltage  $V_{DD}$ .

An exactly similar arrangement applies for the BJT amplifier, as illustrated in Fig. 7.2(c). Here the output voltage  $v_{CE}$  is given by

$$v_{CE} = V_{CC} - i_C R_C \quad (7.4)$$



**Figure 7.2** (a) An NMOS amplifier and (b) its VTC; and (c) an *npn* amplifier and (d) its VTC.

Figure 7.2 *continued*

### 7.1.3 The Voltage-Transfer Characteristic (VTC)

A useful tool that provides insight into the operation of an amplifier circuit is its voltage-transfer characteristic (VTC). This is simply a plot (or a clearly labeled sketch) of the output voltage versus the input voltage. For the MOS amplifier in Fig. 7.2(a), this is the plot of  $v_{DS}$  versus  $v_{GS}$  shown in Fig. 7.2(b).

Observe that for  $v_{GS} < V_t$ , the transistor is cut off,  $i_D = 0$  and, from Eq. (7.3),  $v_{DS} = V_{DD}$ . As  $v_{GS}$  exceeds  $V_t$ , the transistor turns on and  $v_{DS}$  decreases. However, since initially  $v_{DS}$  is still high, the MOSFET will be operating in saturation or the active region. This continues as  $v_{GS}$  is increased until the value of  $v_{GS}$  is reached that results in  $v_{DS}$  becoming lower than  $v_{GS}$  by  $V_t$  volts [point B on the VTC in Fig. 7.2(b)]. For  $v_{GS}$  greater than that at point B, the transistor operates in the triode region and  $v_{DS}$  decreases more slowly.

The VTC in Fig. 7.2(b) indicates that the segment of greatest slope (hence potentially the largest amplifier gain) is that labeled AB, which corresponds to operation in the active region. When a MOSFET is operated as an amplifier, its operating point is confined to the segment AB at all times. An expression for the segment AB can be obtained by substituting for  $i_D$  in Eq. (7.3) by its active-region value from Eq. (7.1), thus

$$v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_t)^2 \quad (7.5)$$

This is obviously a nonlinear relationship. Nevertheless, linear (or almost-linear) amplification can be obtained by using the technique of biasing the MOSFET. Before considering biasing, however, it is useful to determine the coordinates of point B, which is at the boundary between the saturation and the triode regions of operation. These can be obtained by substituting in Eq. (7.5),  $v_{GS} = V_{GS}|_B$  and  $v_{DS} = V_{DS}|_B = V_{GS}|_B - V_t$ . The result is

$$V_{GS}|_B = V_t + \frac{\sqrt{2k_n R_D V_{DD} + 1} - 1}{k_n R_D} \quad (7.6)$$

Point B can be alternatively characterized by the overdrive voltage

$$V_{OV}|_B \equiv V_{GS}|_B - V_t = \frac{\sqrt{2k_nR_DV_{DD}+1}-1}{k_nR_D} \quad (7.7)$$

and

$$V_{DS}|_B = V_{OV}|_B \quad (7.8)$$

### EXERCISE

- 7.1** Consider the amplifier of Fig. 7.2(a) with  $V_{DD} = 1.8$  V,  $R_D = 17.5$  k $\Omega$ , and with a MOSFET specified to have  $V_t = 0.4$  V,  $k_n = 4$  mA/V $^2$ , and  $\lambda = 0$ . Determine the coordinates of the end points of the active-region segment of the VTC. Also, determine  $V_{DS}|_C$  assuming  $V_{GS}|_C = V_{DD}$ .

**Ans.** A: 0.4 V, 1.8 V; B: 0.613 V, 0.213 V;  $V_{DS}|_C = 18$  mV

An exactly similar development applies to the BJT case. This is illustrated in Fig. 7.2(c) and (d). In this case, over the active-region or amplifier segment AB, the output voltage  $v_{CE}$  is related to the input voltage  $v_{BE}$  by

$$v_{CE} = V_{CC} - R_C I_S e^{v_{BE}/V_T} \quad (7.9)$$

Here also, the input–output relationship is nonlinear. Nevertheless, linear (or almost-linear) amplification can be obtained by using the biasing technique discussed next.

#### 7.1.4 Obtaining Linear Amplification by Biasing the Transistor

Biasing enables us to obtain almost-linear amplification from the MOSFET and the BJT. The technique is illustrated for the MOSFET case in Fig. 7.3(a). A dc voltage  $V_{GS}$  is selected to obtain operation at a point Q on the segment AB of the VTC. How to select an appropriate location for the bias point Q will be discussed shortly. For the time being, observe that the coordinates of Q are the dc voltages  $V_{GS}$  and  $V_{DS}$ , which are related by

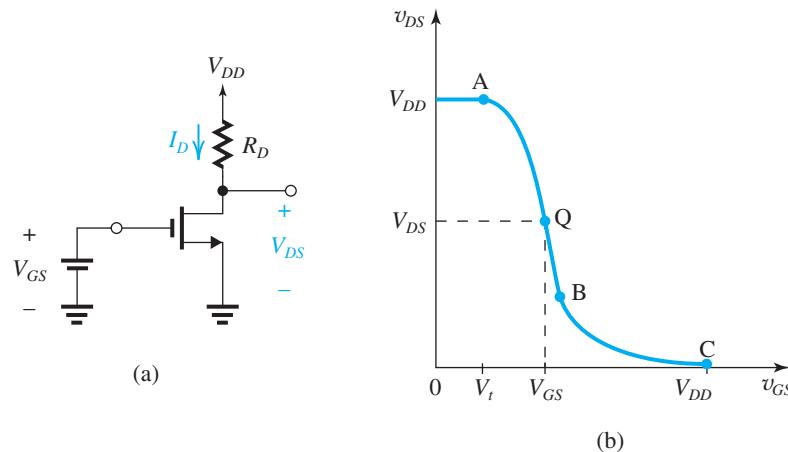
$$V_{DS} = V_{DD} - \frac{1}{2}k_nR_D(V_{GS} - V_t)^2 \quad (7.10)$$

Point Q is known as the **bias point** or the **dc operating point**. Also, since at Q no signal component is present, it is also known as the **quiescent point** (which is the origin of the symbol Q).

Next, the signal to be amplified,  $v_{gs}$ , a function of time  $t$ , is superimposed on the bias voltage  $V_{GS}$ , as shown in Fig. 7.4(a). Thus the total instantaneous value of  $v_{GS}$  becomes

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

The resulting  $v_{DS}(t)$  can be obtained by substituting for  $v_{GS}(t)$  into Eq. (7.5). Graphically, we can use the VTC to obtain  $v_{DS}(t)$  point by point, as illustrated in Fig. 7.4(b). Here we show



**Figure 7.3** Biasing the MOSFET amplifier at a point Q located on the segment AB of the VTC.

the case of  $v_{gs}$  being a triangular wave of “small” amplitude. Specifically, the amplitude of  $v_{gs}$  is small enough to restrict the excursion of the instantaneous operating point to a short, almost-linear segment of the VTC around the bias point Q. The shorter the segment, the greater the linearity achieved, and the closer to an ideal triangular wave the signal component at the output,  $v_{ds}$ , will be. This is the essence of obtaining linear amplification from the nonlinear MOSFET.

Before leaving Fig. 7.4(b) we wish to draw the reader’s attention to the consequence of increasing the amplitude of the signal  $v_{gs}$ . As the instantaneous operating point will no longer be confined to the almost-linear segment of the VTC, the output signal  $v_{ds}$  will deviate from its ideal triangular shape; that is, it will exhibit nonlinear distortion. Worse yet, if the input signal amplitude becomes sufficiently large, the instantaneous operating point may leave the segment AB altogether. If this happens at the negative peaks of  $v_{gs}$ , the transistor will cut off for a portion of the cycle and the positive peaks of  $v_{ds}$  will be “clipped off.” If it occurs at the positive peaks of  $v_{gs}$ , the transistor will enter the triode region for a portion of the cycle, and the negative peaks of  $v_{ds}$  will become flattened. It follows that the selection of the location of the bias point Q can have a profound effect on the maximum allowable amplitude of  $v_{ds}$ , referred to as the *allowable signal swing at the output*. We will have more to say later on this important point.

An exactly parallel development can be applied to the BJT amplifier. In fact, all we need to do is replace the NMOS transistor in Figs. 7.3 and 7.4 with an *npn* transistor and change the voltage and current symbols to their BJT counterparts. The resulting bias point Q will be characterized by dc voltages  $V_{BE}$  and  $V_{CE}$ , which are related by

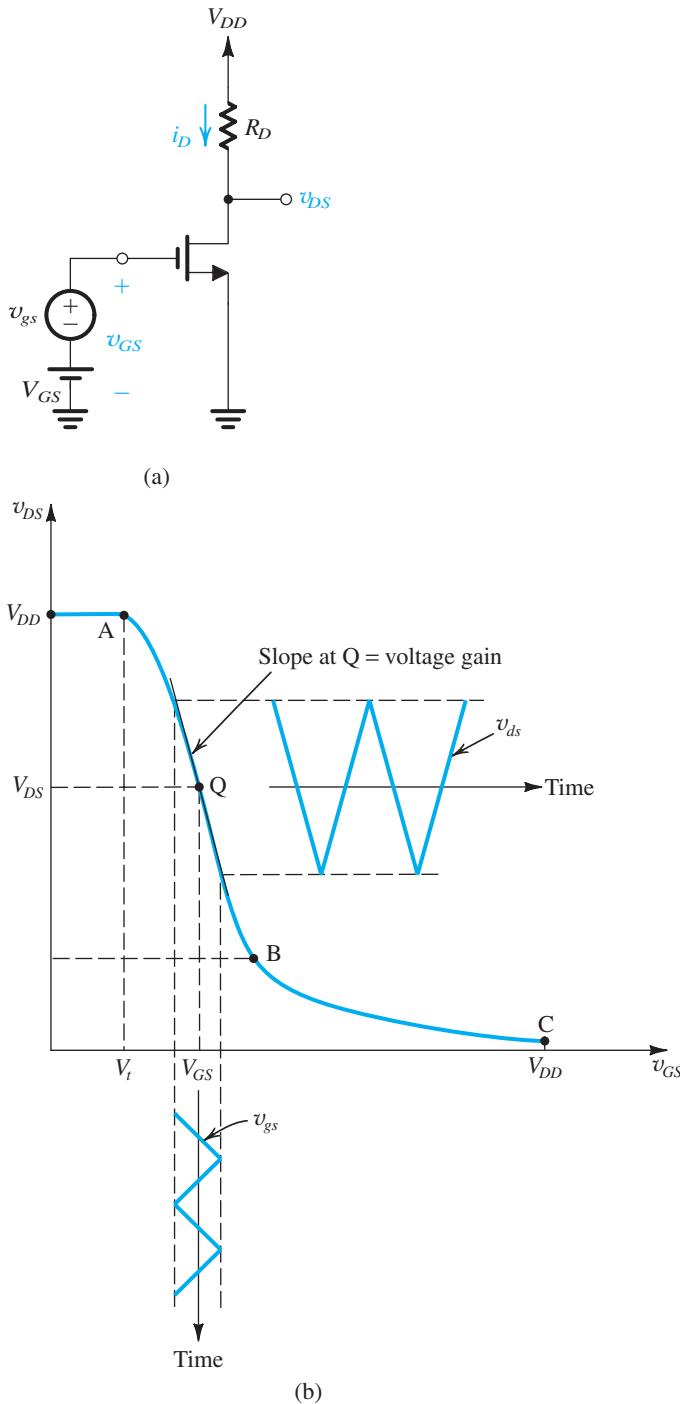
$$V_{CE} = V_{CC} - R_C I_S e^{V_{BE}/V_T} \quad (7.11)$$

and a dc current  $I_C$ ,

$$I_C = I_S e^{V_{BE}/V_T} \quad (7.12)$$

Also, superimposing a small-signal  $v_{be}$  on the dc bias voltage  $V_{BE}$  results in

$$v_{BE}(t) = V_{BE} + v_{be}(t)$$



**Figure 7.4** The MOSFET amplifier with a small time-varying signal  $v_{gs}(t)$  superimposed on the dc bias voltage  $V_{GS}$ . The MOSFET operates on a short almost-linear segment of the VTC around the bias point Q and provides an output voltage  $v_{ds} = A_v v_{gs}$ .

which can be substituted into Eq. (7.9) to obtain the total instantaneous value of the output voltage  $v_{CE}(t)$ . Here again, almost-linear operation is obtained by keeping  $v_{be}$  small enough to restrict the excursion of the instantaneous operating point to a short, almost-linear segment of the VTC around the bias point Q. Similar comments also apply to the maximum allowable signal swing at the output.

### 7.1.5 The Small-Signal Voltage Gain

**The MOSFET Case** Consider the MOSFET amplifier in Fig. 7.4(a). If the input signal  $v_{gs}$  is kept small, the corresponding signal at the output  $v_{ds}$  will be nearly proportional to  $v_{gs}$  with the constant of proportionality being the slope of the almost-linear segment of the VTC around Q. This is the voltage gain of the amplifier, and its value can be determined by evaluating the slope of the tangent to the VTC at the bias point Q,

$$\rightarrow A_v = \left. \frac{dv_{DS}}{dv_{GS}} \right|_{v_{GS}=V_{GS}} \quad (7.13)$$

Utilizing Eq. (7.5) we obtain

$$A_v = -k_n(V_{GS} - V_t)R_D \quad (7.14)$$

which can be expressed in terms of the overdrive voltage at the bias point,  $V_{OV}$ , as

$$\rightarrow A_v = -k_n V_{OV} R_D \quad (7.15)$$

We make the following observations on this expression for the voltage gain.

1. The gain is negative, which signifies that the amplifier is inverting; that is, there is a  $180^\circ$  phase shift between the input and the output. This inversion is obvious in Fig. 7.4(b) and should have been anticipated from Eq. (7.5).
2. The gain is proportional to the load resistance  $R_D$ , to the transistor transconductance parameter  $k_n$ , and to the overdrive voltage  $V_{OV}$ . This all makes intuitive sense.

Another simple and insightful expression for the voltage gain  $A_v$  can be derived by recalling that the dc current in the drain at the bias point is related to  $V_{OV}$  by

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

This equation can be combined with Eq. (7.15) to obtain

$$\rightarrow A_v = -\frac{I_D R_D}{V_{OV}/2} \quad (7.16)$$

That is, the gain is simply the ratio of the dc voltage drop across the load resistance  $R_D$  to  $V_{OV}/2$ . It can be expressed in the alternative form

$$\rightarrow A_v = -\frac{V_{DD} - V_{DS}}{V_{OV}/2} \quad (7.17)$$

Since the maximum slope of the VTC in Fig. 7.4(b) occurs at point B, the maximum gain magnitude  $|A_{vmax}|$  is obtained by biasing the transistor at point B,

$$|A_{vmax}| = \frac{V_{DD} - V_{DS}|_B}{V_{OV}|_B/2}$$

and since  $V_{DS}|_B = V_{OV}|_B$ ,

$$|A_{v_{max}}| = \frac{V_{DD} - V_{OV}|_B}{V_{OV}|_B/2} \quad (7.18)$$

where  $V_{OV}|_B$  is given by Eq. (7.7). Of course, this result is only of theoretical importance since biasing at B would leave no room for negative signal swing at the output. Nevertheless, the result in Eq. (7.18) is valuable as it provides an upper bound on the magnitude of voltage gain achievable from this basic amplifier circuit. As an example, for a discrete-circuit amplifier operated with  $V_{DD} = 5$  V and  $V_{OV}|_B = 0.5$  V, the maximum achievable gain is 18 V/V. An integrated-circuit amplifier utilizing a modern submicron MOSFET operated with  $V_{DD} = 1.3$  V and with  $V_{OV}|_B = 0.2$  V realizes a maximum gain of 11 V/V.

Finally, note that to maximize the gain, the bias point Q should be as close to point B as possible, consistent with the required signal swing at the output. This point will be explored further in the end-of-chapter problems.

### Example 7.1

Consider the amplifier circuit shown in Fig. 7.4(a). The transistor is specified to have  $V_t = 0.4$  V,  $k'_n = 0.4$  mA/V<sup>2</sup>,  $W/L = 10$ , and  $\lambda = 0$ . Also, let  $V_{DD} = 1.8$  V,  $R_D = 17.5$  kΩ, and  $V_{GS} = 0.6$  V.

- (a) For  $v_{gs} = 0$  (and hence  $v_{ds} = 0$ ), find  $V_{OV}$ ,  $I_D$ ,  $V_{DS}$ , and  $A_v$ .
- (b) What is the maximum symmetrical signal swing allowed at the drain? Hence, find the maximum allowable amplitude of a sinusoidal  $v_{gs}$ .

#### Solution

- (a) With  $V_{GS} = 0.6$  V,  $V_{OV} = 0.6 - 0.4 = 0.2$  V. Thus,

$$\begin{aligned} I_D &= \frac{1}{2} k'_n \left( \frac{W}{L} \right) V_{OV}^2 \\ &= \frac{1}{2} \times 0.4 \times 10 \times 0.2^2 = 0.08 \text{ mA} \\ V_{DS} &= V_{DD} - R_D I_D \\ &= 1.8 - 17.5 \times 0.08 = 0.4 \text{ V} \end{aligned}$$

Since  $V_{DS}$  is greater than  $V_{OV}$ , the transistor is indeed operating in saturation. The voltage gain can be found from Eq. (7.15),

$$\begin{aligned} A_v &= -k_n V_{OV} R_D \\ &= -0.4 \times 10 \times 0.2 \times 17.5 \\ &= -14 \text{ V/V} \end{aligned}$$

An identical result can be found using Eq. (7.17).

- (b) Since  $V_{OV} = 0.2$  V and  $V_{DS} = 0.4$  V, we see that the maximum allowable negative signal swing at the drain is 0.2 V. In the positive direction, a swing of +0.2 V would not cause the transistor to

**Example 7.1** *continued*

cut off (since the resulting  $v_{ds}$  would be still lower than  $V_{DD}$ ) and thus is allowed. Thus the maximum symmetrical signal swing allowable at the drain is  $\pm 0.2$  V. The corresponding amplitude of  $v_{gs}$  can be found from

$$\hat{v}_{gs} = \frac{\hat{v}_{ds}}{|A_v|} = \frac{0.2 \text{ V}}{14} = 14.2 \text{ mV}$$

Since  $\hat{v}_{gs} \ll V_{OV}$ , the operation will be reasonably linear (more on this in later sections).

Greater insight into the issue of allowable signal swing can be obtained by examining the signal waveforms shown in Fig. 7.5. Note that for the MOSFET to remain in saturation at the negative peak of  $v_{ds}$ , we must ensure that

$$v_{DS\min} \geq v_{GS\max} - V_t$$

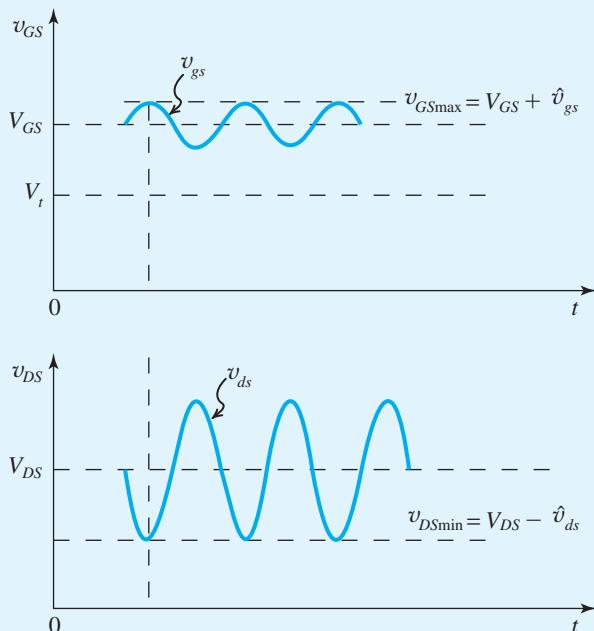
that is,

$$0.4 - |A_v| \hat{v}_{gs} \geq 0.6 + \hat{v}_{gs} - 0.4$$

which results in

$$\hat{v}_{gs} \leq \frac{0.2}{|A_v| + 1} = 13.3 \text{ mV}$$

This result differs slightly from the one obtained earlier.



**Figure 7.5** Signal waveforms at gate and drain for the amplifier in Example 7.1. Note that to ensure operation in the saturation region at all times,  $v_{DS\min} \geq v_{GS\max} - V_t$ .

## EXERCISE

- D7.2** For the amplifier circuit studied in Example 7.1, create two alternative designs, each providing a voltage gain of  $-10$  by (a) changing  $R_D$  while keeping  $V_{ov}$  constant and (b) changing  $V_{ov}$  while keeping  $R_D$  constant. For each design, specify  $V_{GS}$ ,  $I_D$ ,  $R_D$ , and  $V_{DS}$ .

**Ans.** (a)  $0.6\text{ V}, 0.08\text{ mA}, 12.5\text{ k}\Omega, 0.8\text{ V}$ ; (b)  $0.54\text{ V}, 0.04\text{ mA}, 17.5\text{ k}\Omega, 1.1\text{ V}$

**The BJT Case** A similar development can be used to obtain the small-signal voltage gain of the BJT amplifier shown in Fig. 7.6,

$$A_v = \left. \frac{dv_{CE}}{dv_{BE}} \right|_{v_{BE}=V_{BE}} \quad (7.19)$$

Utilizing Eq. (7.9) together with Eq. (7.12), we obtain

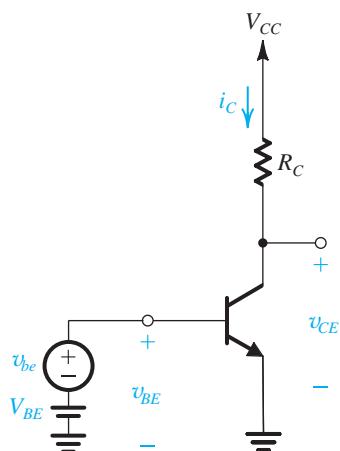
$$A_v = -\left( \frac{I_C}{V_T} \right) R_C \quad (7.20)$$

We make the following observations on this expression for the voltage gain:

1. The gain is negative, which signifies that the amplifier is inverting; that is, there is a  $180^\circ$  phase shift between the input and the output. This inversion should have been anticipated from Eq. (7.9).
2. The gain is proportional to the collector bias current  $I_C$  and to the load resistance  $R_C$ .

Additional insight into the voltage gain  $A_v$  can be obtained by expressing Eq. (7.20) as

$$A_v = -\frac{I_C R_C}{V_T} \quad (7.21)$$



**Figure 7.6** BJT amplifier biased at a point Q, with a small voltage signal  $v_{be}$  superimposed on the dc bias voltage  $V_{BE}$ . The resulting output signal  $v_{ce}$  appears superimposed on the dc collector voltage  $V_{CE}$ . The amplitude of  $v_{ce}$  is larger than that of  $v_{be}$  by the voltage gain  $A_v$ .

That is, the gain is the ratio of the dc voltage drop across the load resistance  $R_C$  to the physical constant  $V_T$  (recall that the thermal voltage  $V_T \simeq 25$  mV at room temperature). This relationship is similar in form to that for the MOSFET (Eq. 7.16) except that here the denominator is a physical constant ( $V_T$ ) rather than a design parameter ( $V_{ov}/2$ ). Usually,  $V_{ov}/2$  is larger than ( $V_T$ ), thus we can obtain higher voltage gain from the BJT amplifier than from the MOSFET amplifier. This should not be surprising, as the exponential  $i_C-v_{BE}$  relationship is much steeper than the square-law relationship  $i_D-v_{GS}$ .

The gain  $A_v$  in Eq. (7.21) can be expressed alternately as

$$\Rightarrow A_v = -\frac{V_{CC} - V_{CE}}{V_T} \quad (7.22)$$

from which we see that maximum gain is achieved when  $V_{CE}$  is at its minimum value of about 0.3 V,

$$\Rightarrow |A_{vmax}| = \frac{V_{CC} - 0.3}{V_T} \quad (7.23)$$

Here again, this is only a theoretical maximum, since biasing the BJT at the edge of saturation leaves no room for negative signal swing at the output. Equation (7.23) nevertheless provides an upper bound on the voltage gain achievable from the basic BJT amplifier. As an example, for  $V_{CC} = 5$  V, the maximum gain is 188 V/V, considerably larger than in the MOSFET case. For modern low-voltage technologies, a  $V_{CC}$  of 1.3 V provides a gain of 40 V/V, again much larger than the MOSFET case. The reader should not, however, jump to the conclusion that the BJT is preferred to the MOSFET in the design of modern integrated-circuit amplifiers; in fact, the opposite is true, as we shall see in Chapter 8 and beyond.

Finally, we conclude from Eq. (7.22) that to maximize  $|A_v|$  the transistor should be biased at the lowest possible  $V_{CE}$  consistent with the desired value of negative signal swing at the output.

### Example 7.2

Consider an amplifier circuit using a BJT having  $I_s = 10^{-15}$  A, a collector resistance  $R_C = 6.8$  k $\Omega$ , and a power supply  $V_{CC} = 10$  V.

- Determine the value of the bias voltage  $V_{BE}$  required to operate the transistor at  $V_{CE} = 3.2$  V. What is the corresponding value of  $I_C$ ?
- Find the voltage gain  $A_v$  at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on  $V_{BE}$ , find the amplitude of the output sine-wave signal (assume linear operation).
- Find the positive increment in  $v_{BE}$  (above  $V_{BE}$ ) that drives the transistor to the edge of saturation, where  $v_{CE} = 0.3$  V.
- Find the negative increment in  $v_{BE}$  that drives the transistor to within 1% of cutoff (i.e., to  $v_{CE} = 0.99V_{CC}$ ).

**Solution**

(a)

$$\begin{aligned}I_C &= \frac{V_{CC} - V_{CE}}{R_C} \\&= \frac{10 - 3.2}{6.8} = 1 \text{ mA}\end{aligned}$$

The value of  $V_{BE}$  can be determined from

$$1 \times 10^{-3} = 10^{-15} e^{V_{BE}/V_T}$$

which results in

$$V_{BE} = 690.8 \text{ mV}$$

(b)

$$\begin{aligned}A_v &= -\frac{V_{CC} - V_{CE}}{V_T} \\&= \frac{10 - 3.2}{0.025} = -272 \text{ V/V} \\v_{ce} &= 272 \times 0.005 = 1.36 \text{ V}\end{aligned}$$

(c) For  $v_{CE} = 0.3 \text{ V}$ ,

$$i_C = \frac{10 - 0.3}{6.8} = 1.617 \text{ mA}$$

To increase  $i_C$  from 1 mA to 1.617 mA,  $v_{BE}$  must be increased by

$$\begin{aligned}\Delta v_{BE} &= V_T \ln\left(\frac{1.617}{1}\right) \\&= 12 \text{ mV}\end{aligned}$$

(d) For  $v_{CE} = 0.99V_{CC} = 9.9 \text{ V}$ ,

$$i_C = \frac{10 - 9.9}{6.8} = 0.0147 \text{ mA}$$

To decrease  $i_C$  from 1 mA to 0.0147 mA,  $v_{BE}$  must change by

$$\begin{aligned}\Delta v_{BE} &= V_T \ln\left(\frac{0.0147}{1}\right) \\&= -105.5 \text{ mV}\end{aligned}$$

## EXERCISE

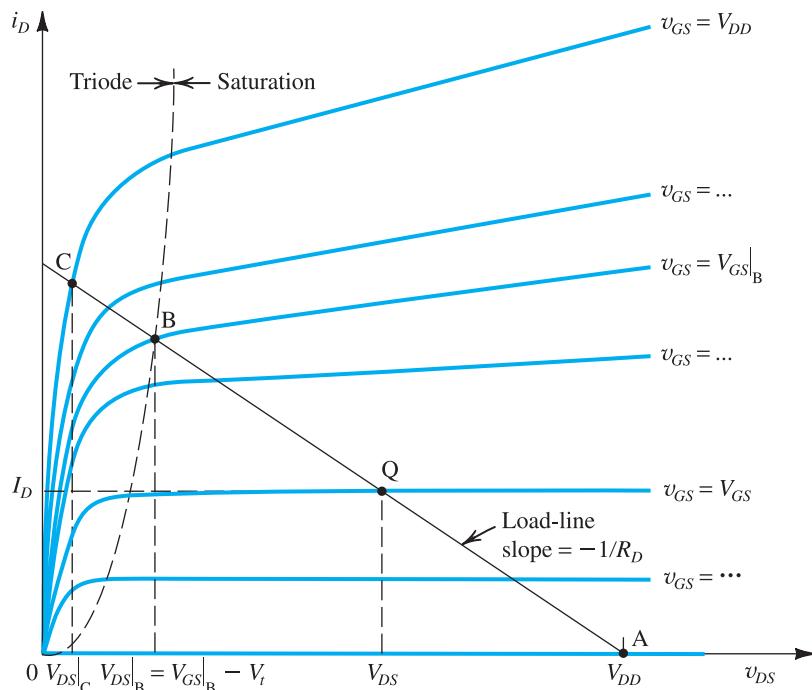
- 7.3 For the situation described in Example 7.2, while keeping  $I_C$  unchanged at 1 mA, find the value of  $R_C$  that will result in a voltage gain of  $-320 \text{ V/V}$ . What is the largest negative signal swing allowed at the output (assume that  $v_{CE}$  is not to decrease below 0.3 V)? What (approximately) is the corresponding input signal amplitude? (Assume linear operation.)

**Ans.**  $8 \text{ k}\Omega$ ; 1.7 V; 5.3 mV

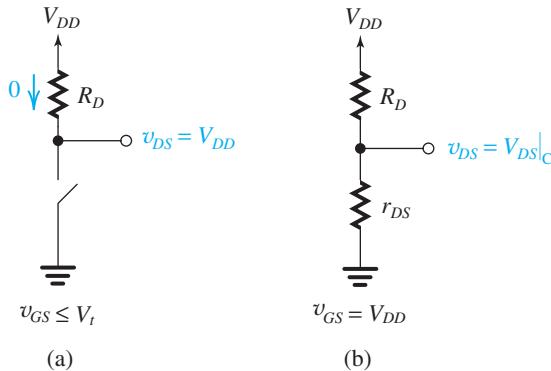
### 7.1.6 Determining the VTC by Graphical Analysis

Figure 7.7 shows a graphical method for determining the VTC of the amplifier of Fig. 7.4(a). Although graphical analysis of transistor circuits is rarely employed in practice, it is useful to us at this stage for gaining greater insight into circuit operation, especially in answering the question of where to locate the bias point Q.

The graphical analysis is based on the observation that for each value of  $v_{GS}$ , the circuit will be operating at the point of intersection of the  $i_D - v_{DS}$  graph corresponding to the particular



**Figure 7.7** Graphical construction to determine the voltage-transfer characteristic of the amplifier in Fig. 7.4(a).



**Figure 7.8** Operation of the MOSFET in Fig. 7.4(a) as a switch: (a) open, corresponding to point A in Fig. 7.7; (b) closed, corresponding to point C in Fig. 7.7. The closure resistance is approximately equal to  $r_{DS}$  because  $V_{DS}$  is usually very small.

value of  $v_{GS}$  and the straight line representing Eq. (7.3), which can be rewritten in the form

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS} \quad (7.24)$$

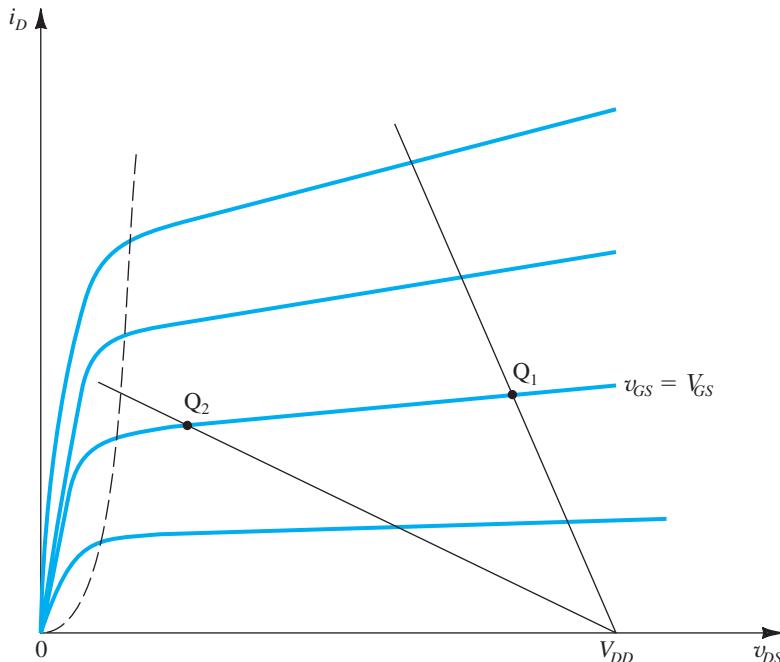
The straight line representing this relationship is superimposed on the  $i_D - v_{DS}$  characteristics in Fig. 7.7. It intersects the horizontal axis at  $v_{DS} = V_{DD}$  and has a slope of  $-1/R_D$ . Since this straight line represents in effect the load resistance  $R_D$ , it is called the **load line**. The VTC is then determined point by point. Note that we have labeled four important points: point A at which  $v_{GS} = V_t$ , point Q at which the MOSFET can be biased for amplifier operation ( $v_{GS} = V_{GS}$  and  $v_{DS} = V_{DS}$ ), point B at which the MOSFET leaves saturation and enters the triode region, and point C, which is deep into the triode region and for which  $v_{GS} = V_{DD}$ . If the MOSFET is to be used as a switch, then operating points A and C are applicable: At A the transistor is off (open switch), and at C the transistor operates as a low-valued resistance  $r_{DS}$  and has a small voltage drop (closed switch). The incremental resistance at point C is also known as the **closure resistance**. The operation of the MOSFET as a switch is illustrated in Fig. 7.8. A detailed study of the application of the MOSFET as a switch is undertaken in Chapter 14, dealing with CMOS digital logic circuits.

The graphical analysis method above can be applied to determine the VTC of the BJT amplifier in Fig. 7.2(c). Here point A, Fig. 7.2(d), corresponds to the BJT just turning on ( $v_{BE} \approx 0.5$  V) and point B corresponds to the BJT leaving the active region and entering the saturation region. If the BJT is to be operated as a switch, the two modes of operation are cutoff (open switch) and saturation (closed switch). As discussed in Section 6.2, in saturation, the BJT has a small closure resistance  $R_{CE\text{sat}}$  as well as an offset voltage. More seriously, switching the BJT out of its saturation region can require a relatively long delay time to ensure the removal of the charge stored in the BJT base region. This phenomenon has made the BJT much less attractive in digital logic applications relative to the MOSFET.<sup>2</sup>

### 7.1.7 Deciding on a Location for the Bias Point Q

For the MOSFET amplifier, the bias point Q is determined by the value of  $V_{GS}$  and that of the load resistance  $R_D$ . Two important considerations in deciding on the location of Q

<sup>2</sup>The only exception is a nonsaturating form of BJT logic circuits known as emitter-coupled logic (ECL).



**Figure 7.9** Two load lines and corresponding bias points. Bias point  $Q_1$  does not leave sufficient room for positive signal swing at the drain (too close to  $V_{DD}$ ). Bias point  $Q_2$  is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

are the required gain and the desired signal swing at the output. To illustrate, consider the VTC shown in Fig. 7.4(b). Here the value of  $R_D$  is fixed and the only variable remaining is the value of  $V_{GS}$ . Since the slope increases as we move closer to point B, we obtain higher gain by locating Q as close to B as possible. However, the closer Q is to the boundary point B, the smaller the allowable magnitude of negative signal swing. Thus, as often happens in engineering design, we encounter a situation requiring a trade-off. The answer here is relatively simple: For a given  $R_D$ , locate Q as close to the triode region (point B) as possible to obtain high gain but sufficiently distant to allow for the required negative signal swing.

In deciding on a value for  $R_D$ , it is useful to refer to the  $i_D - v_{DS}$  plane. Figure 7.9 shows two load lines resulting in two extreme bias points: Point  $Q_1$  is too close to  $V_{DD}$ , resulting in a severe constraint on the positive signal swing of  $v_{ds}$ . Exceeding the allowable positive maximum results in the positive peaks of the signal being clipped off, since the MOSFET will turn off for the part of each cycle near the positive peak. We speak of this situation by saying that the circuit does not have sufficient “headroom.” Similarly, point  $Q_2$  is too close to the boundary of the triode region, thus severely limiting the allowable negative signal swing of  $v_{ds}$ . Exceeding this limit would result in the transistor entering the triode region for part of each cycle near the negative peaks, resulting in a distorted output signal. In this situation we say that the circuit does not have sufficient “legroom.” We will have more to say on bias design in Section 7.4.

Finally, we note that exactly similar considerations apply to the case of the BJT amplifier.

## 7.2 Small-Signal Operation and Models

In our study of the operation of the MOSFET and BJT amplifiers in Section 7.1 we learned that linear amplification can be obtained by biasing the transistor to operate in the active region and by keeping the input signal small. In this section, we explore the small-signal operation in greater detail.

### 7.2.1 The MOSFET Case

Consider the conceptual amplifier circuit shown in Fig. 7.10. Here the MOS transistor is biased by applying a dc voltage<sup>3</sup>  $V_{GS}$ , and the input signal to be amplified,  $v_{gs}$ , is superimposed on the dc bias voltage  $V_{GS}$ . The output voltage is taken at the drain.

**The DC Bias Point** The dc bias current  $I_D$  can be found by setting the signal  $v_{gs}$  to zero; thus,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 = \frac{1}{2} k_n V_{OV}^2 \quad (7.25)$$

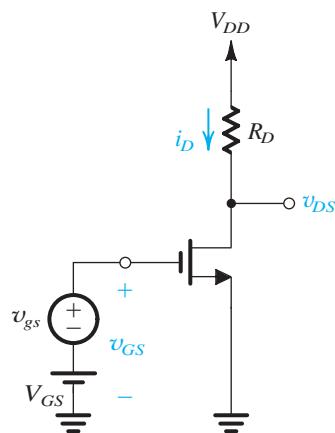
where we have neglected channel-length modulation (i.e., we have assumed  $\lambda = 0$ ). Here  $V_{OV} = V_{GS} - V_t$  is the overdrive voltage at which the MOSFET is biased to operate. The dc voltage at the drain,  $V_{DS}$ , will be

$$V_{DS} = V_{DD} - R_D I_D \quad (7.26)$$

To ensure saturation-region operation, we must have

$$V_{DS} > V_{OV}$$

Furthermore, since the total voltage at the drain will have a signal component superimposed on  $V_{DS}$ ,  $V_{DS}$  has to be sufficiently greater than  $V_{OV}$  to allow for the required negative signal swing.



**Figure 7.10** Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

<sup>3</sup>Practical biasing arrangements will be studied in Section 7.4.

**The Signal Current in the Drain Terminal** Next, consider the situation with the input signal  $v_{gs}$  applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \quad (7.27)$$

resulting in a total instantaneous drain current  $i_D$ ,

$$\begin{aligned} i_D &= \frac{1}{2} k_n (V_{GS} + v_{gs} - V_t)^2 \\ &= \frac{1}{2} k_n (V_{GS} - V_t)^2 + k_n (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n v_{gs}^2 \end{aligned} \quad (7.28)$$

The first term on the right-hand side of Eq. (7.28) can be recognized as the dc bias current  $I_D$  (Eq. 7.25). The second term represents a current component that is directly proportional to the input signal  $v_{gs}$ . The third term is a current component that is proportional to the square of the input signal. This last component is undesirable because it represents *nonlinear distortion*. To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2} k_n v_{gs}^2 \ll k_n (V_{GS} - V_t) v_{gs}$$

resulting in

$$v_{gs} \ll 2(V_{GS} - V_t) \quad (7.29)$$

or, equivalently,

$$v_{gs} \ll 2V_{OV} \quad (7.30)$$

If this **small-signal condition** is satisfied, we may neglect the last term in Eq. (7.28) and express  $i_D$  as

$$i_D \simeq I_D + i_d \quad (7.31)$$

where

$$i_d = k_n (V_{GS} - V_t) v_{gs}$$

The parameter that relates  $i_d$  and  $v_{gs}$  is the MOSFET **transconductance**  $g_m$ ,

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n (V_{GS} - V_t) \quad (7.32)$$

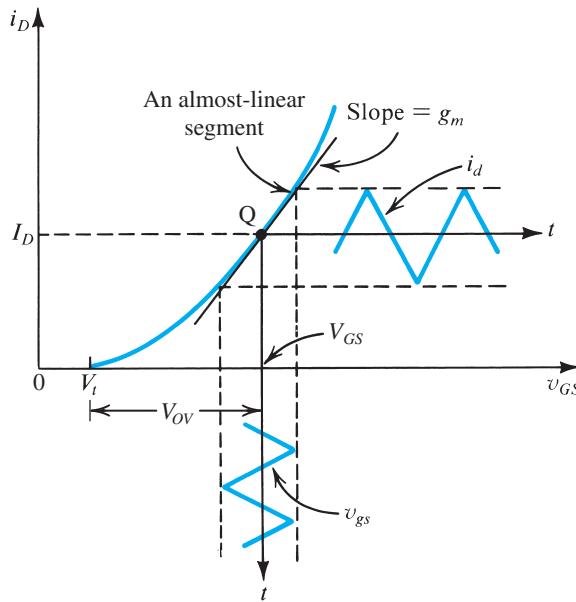
or in terms of the overdrive voltage  $V_{OV}$ ,

$$g_m = k_n V_{OV} \quad (7.33)$$

Figure 7.11 presents a graphical interpretation of the small-signal operation of the MOSFET amplifier. Note that  $g_m$  is equal to the slope of the  $i_D-v_{GS}$  characteristic at the bias point,

$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=V_{GS}} \quad (7.34)$$

This is the formal definition of  $g_m$ , which can be shown to yield the expressions given in Eqs. (7.32) and (7.33).



**Figure 7.11** Small-signal operation of the MOSFET amplifier.

**The Voltage Gain** Returning to the circuit of Fig. 7.10, we can express the total instantaneous drain voltage  $v_{DS}$  as follows:

$$v_{DS} = V_{DD} - R_D i_D$$

Under the small-signal condition, we have

$$v_{DS} = V_{DD} - R_D (I_D + i_d)$$

which can be rewritten as

$$v_{DS} = V_{DS} - R_D i_d$$

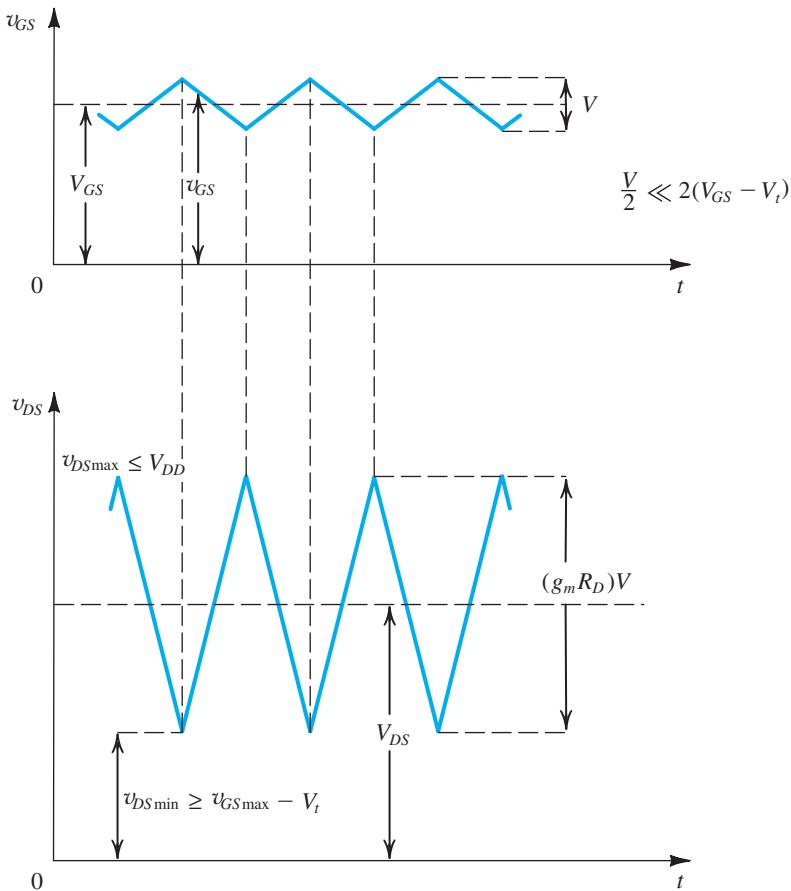
Thus the signal component of the drain voltage is

$$v_{ds} = -i_d R_D = -g_m v_{gs} R_D \quad (7.35)$$

which indicates that the voltage gain is given by

$$A_v \equiv \frac{v_{ds}}{v_{gs}} = -g_m R_D \quad (7.36)$$

The minus sign in Eq. (7.36) indicates that the output signal  $v_{ds}$  is  $180^\circ$  out of phase with respect to the input signal  $v_{gs}$ . This is illustrated in Fig. 7.12, which shows  $v_{GS}$  and  $v_{DS}$ . The input signal is assumed to have a triangular waveform with an amplitude much smaller than  $2(V_{GS} - V_t)$ , the small-signal condition in Eq. (7.29), to ensure linear operation. For operation in the saturation (active) region at all times, the minimum value of  $v_{DS}$  should not fall below the corresponding value of  $v_{GS}$  by more than  $V_t$ . Also, the maximum value of  $v_{DS}$  should be



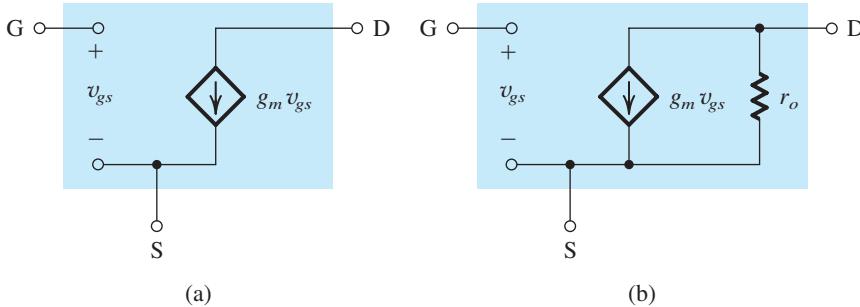
**Figure 7.12** Total instantaneous voltages  $v_{GS}$  and  $v_{DS}$  for the circuit in Fig. 7.10.

smaller than  $V_{DD}$ ; otherwise the FET will enter the cutoff region and the peaks of the output signal waveform will be clipped off.

Finally, we note that by substituting for  $g_m$  from Eq. (7.33) the voltage-gain expression in Eq. (7.36) becomes identical to that derived in Section 7.1—namely, Eq. (7.15).

**Separating the DC Analysis and the Signal Analysis** From the preceding analysis, we see that under the small-signal approximation, signal quantities are superimposed on dc quantities. For instance, the total drain current  $i_D$  equals the dc current  $I_D$  plus the signal current  $i_d$ , the total drain voltage  $v_{DS} = V_{DS} + v_{ds}$ , and so on. It follows that the analysis and design can be greatly simplified by separating dc or bias calculations from small-signal calculations. That is, once a stable dc operating point has been established and all dc quantities calculated, we may then perform signal analysis ignoring dc quantities.

**Small-Signal Equivalent-Circuit Models** From a signal point of view, the FET behaves as a voltage-controlled current source. It accepts a signal  $v_{gs}$  between gate and source and provides a current  $g_m v_{gs}$  at the drain terminal. The input resistance of this controlled source is very high—ideally, infinite. The output resistance—that is, the resistance looking into the



**Figure 7.13** Small-signal models for the MOSFET: (a) neglecting the dependence of  $i_D$  on  $v_{DS}$  in the active region (the channel-length modulation effect) and (b) including the effect of channel-length modulation, modeled by output resistance  $r_o = |V_A|/I_D$ . These models apply equally well for both NMOS and PMOS transistors.

drain—also is high, and we have assumed it to be infinite thus far. Putting all of this together, we arrive at the circuit in Fig. 7.13(a), which represents the small-signal operation of the MOSFET and is thus a **small-signal model** or a **small-signal equivalent circuit**.

In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent-circuit model shown in Fig. 7.13(a). The rest of the circuit remains unchanged except that *ideal constant dc voltage sources are replaced by short circuits*. This is a result of the fact that the voltage across an ideal constant dc voltage source does not change, and thus there will always be a zero voltage signal across a constant dc voltage source. A dual statement applies for constant dc current sources; namely, the signal current of an ideal constant dc current source will always be zero, and thus *an ideal constant dc current source can be replaced by an open circuit* in the small-signal equivalent circuit of the amplifier. The circuit resulting can then be used to perform any required signal analysis, such as calculating voltage gain.

The most serious shortcoming of the small-signal model of Fig. 7.13(a) is that it assumes the drain current in saturation to be independent of the drain voltage. From our study of the MOSFET characteristics in saturation, we know that the drain current does in fact depend on  $v_{DS}$  in a linear manner. Such dependence was modeled by a finite resistance  $r_o$  between drain and source, whose value was given by Eq. (5.27) in Section 5.2.4, which we repeat here (with the prime on  $I_D$  dropped) as

$$r_o = \frac{|V_A|}{I_D} \quad (7.37)$$

where  $V_A = 1/\lambda$  is a MOSFET parameter that either is specified or can be measured. It should be recalled that for a given process technology,  $V_A$  is proportional to the MOSFET channel length. The current  $I_D$  is the value of the dc drain current without the channel-length modulation taken into account; that is,

$$I_D = \frac{1}{2} k_n V_{OV}^2 \quad (7.38)$$

Typically,  $r_o$  is in the range of 10 kΩ to 1000 kΩ. It follows that the accuracy of the small-signal model can be improved by including  $r_o$  in parallel with the controlled source, as shown in Fig. 7.13(b).

It is important to note that the small-signal model parameters  $g_m$  and  $r_o$  depend on the dc bias point of the MOSFET.

Returning to the amplifier of Fig. 7.10, we find that replacing the MOSFET with the small-signal model of Fig. 7.13(b) results in the voltage-gain expression

$$\mathbf{A}_v = \frac{v_{ds}}{v_{gs}} = -g_m(R_D \parallel r_o) \quad (7.39)$$

Thus, the finite output resistance  $r_o$  results in a reduction in the magnitude of the voltage gain.

Although the analysis above is performed on an NMOS transistor, the results, and the equivalent-circuit models of Fig. 7.13, apply equally well to PMOS devices, except for using  $|V_{GS}|, |V_t|, |V_{OV}|$ , and  $|V_A|$  and replacing  $k_n$  with  $k_p$ .

**The Transconductance  $g_m$**  We shall now take a closer look at the MOSFET transconductance given by Eq. (7.32), which we rewrite with  $k_n = k'_n(W/L)$  as follows:

$$\mathbf{g}_m = k'_n(W/L)(V_{GS} - V_t) = k'_n(W/L)V_{OV} \quad (7.40)$$

This relationship indicates that  $g_m$  is proportional to the process transconductance parameter  $k'_n = \mu_n C_{ox}$  and to the  $W/L$  ratio of the MOS transistor; hence to obtain relatively large transconductance the device must be short and wide. We also observe that for a given device the transconductance is proportional to the overdrive voltage,  $V_{OV} = V_{GS} - V_t$ , the amount by which the bias voltage  $V_{GS}$  exceeds the threshold voltage  $V_t$ . Note, however, that increasing  $g_m$  by biasing the device at a larger  $V_{GS}$  has the disadvantage of reducing the allowable voltage signal swing at the drain.

Another useful expression for  $g_m$  can be obtained by substituting for  $V_{OV}$  in Eq. (7.40) by  $\sqrt{2I_D/(k'_n(W/L))}$  [from Eq. (7.25)]:

$$\mathbf{g}_m = \sqrt{2k'_n} \sqrt{W/L} \sqrt{I_D} \quad (7.41)$$

This expression shows two things:

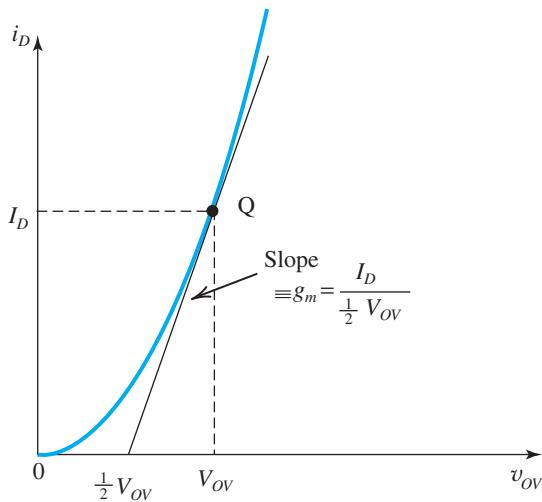
1. For a given MOSFET,  $g_m$  is proportional to the square root of the dc bias current.
2. At a given bias current,  $g_m$  is proportional to  $\sqrt{W/L}$ .

In contrast, as we shall see shortly, the transconductance of the bipolar junction transistor (BJT) is proportional to the bias current and is independent of the physical size and geometry of the device.

To gain some insight into the values of  $g_m$  obtained in MOSFETs consider an integrated-circuit device operating at  $I_D = 0.5$  mA and having  $k'_n = 120 \mu\text{A/V}^2$ . Equation (7.41) shows that for  $W/L = 1$ ,  $g_m = 0.35$  mA/V, whereas a device for which  $W/L = 100$  has  $g_m = 3.5$  mA/V. In contrast, a BJT operating at a collector current of 0.5 mA has  $g_m = 20$  mA/V.

Yet another useful expression for  $g_m$  of the MOSFET can be obtained by substituting for  $k'_n(W/L)$  in Eq. (7.40) by  $2I_D/(V_{GS} - V_t)^2$ :

$$\mathbf{g}_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}} \quad (7.42)$$



**Figure 7.14** The slope of the tangent at the bias point Q intersects the  $v_{OV}$  axis at  $\frac{1}{2}V_{OV}$ . Thus,  $g_m = I_D / (\frac{1}{2}V_{OV})$ .

A convenient graphical construction that clearly illustrates this relationship is shown in Fig. 7.14.

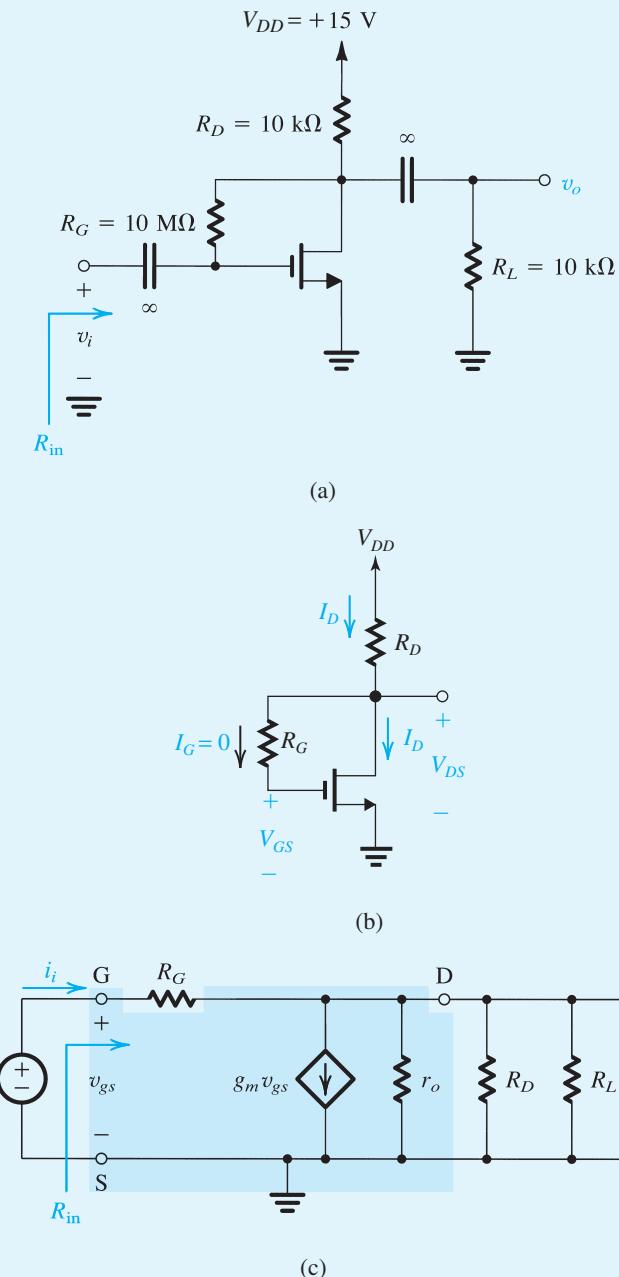
In summary, there are three different relationships for determining  $g_m$ —Eqs. (7.40), (7.41), and (7.42)—and there are three design parameters— $(W/L)$ ,  $V_{OV}$ , and  $I_D$ , any two of which can be chosen independently. That is, the designer may choose to operate the MOSFET with a certain overdrive voltage  $V_{OV}$  and at a particular current  $I_D$ ; the required  $W/L$  ratio can then be found and the resulting  $g_m$  determined.<sup>4</sup>

### Example 7.3

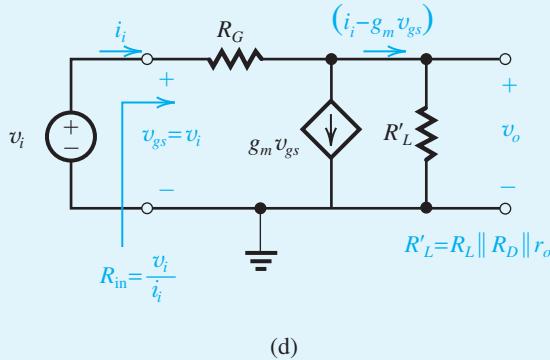
Figure 7.15(a) shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance  $R_G$  for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal  $v_i$  is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance  $R_L$  via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has  $V_t = 1.5$  V,  $k'_n (W/L) = 0.25$  mA/V<sup>2</sup>, and  $V_A = 50$  V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

<sup>4</sup>This assumes that the circuit designer is also designing the device, as is typically the case in IC design. On the other hand, a circuit designer working with a discrete-circuit MOSFET obviously does not have the freedom to change its  $W/L$  ratio. Thus, in this case there are only two design parameters— $V_{OV}$  and  $I_D$ , and only one can be specified by the designer.

## Example 7.3 continued



**Figure 7.15** Example 7.3: (a) amplifier circuit; (b) circuit for determining the dc operating point; (c) the amplifier small-signal equivalent circuit; (d) a simplified version of the circuit in (c).

**Figure 7.15** continued

### Solution

We first determine the dc operating point. For this purpose, we eliminate the input signal  $v_i$ , and open-circuit the two coupling capacitors (since they block dc currents). The result is the circuit shown in Fig. 7.14(b). We note that since  $I_G = 0$ , the dc voltage drop across  $R_G$  will be zero, and

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D \quad (7.43)$$

With  $V_{DS} = V_{GS}$ , the NMOS transistor will be operating in saturation. Thus,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \quad (7.44)$$

where, for simplicity, we have neglected the effect of channel-length modulation on the dc operating point. Substituting  $V_{DD} = 15$  V,  $R_D = 10$  k $\Omega$ ,  $k_n = 0.25$  mA/V $^2$ , and  $V_t = 1.5$  V in Eqs. (7.43) and (7.44), and substituting for  $V_{GS}$  from Eq. (7.43) into Eq. (7.44) results in a quadratic equation in  $I_D$ . Solving the latter and discarding the root that is not physically meaningful yields the solution

$$I_D = 1.06 \text{ mA}$$

which corresponds to

$$V_{GS} = V_{DS} = 4.4 \text{ V}$$

and

$$V_{OV} = 4.4 - 1.5 = 2.9 \text{ V}$$

Next we proceed with the small-signal analysis of the amplifier. Toward that end we replace the MOSFET with its small-signal model to obtain the small-signal equivalent circuit of the amplifier, shown in Fig. 7.15(c). Observe that we have replaced the coupling capacitors with short circuits. The dc voltage supply  $V_{DD}$  has also been replaced with a short circuit to ground.

**Example 7.3** *continued*

The values of the transistor small-signal parameters  $g_m$  and  $r_o$  can be determined by using the dc bias quantities found above, as follows:

$$\begin{aligned} g_m &= k_n V_{OV} \\ &= 0.25 \times 2.9 = 0.725 \text{ mA/V} \\ r_o &= \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ k}\Omega \end{aligned}$$

Next we use the equivalent circuit of Fig. 7.15(c) to determine the input resistance  $R_{in} \equiv v_i/i_i$  and the voltage gain  $A_v = v_o/v_i$ . Toward that end we simplify the circuit by combining the three parallel resistances  $r_o$ ,  $R_D$ , and  $R_L$  in a single resistance  $R'_L$ ,

$$\begin{aligned} R'_L &= R_L || R_D || r_o \\ &= 10 || 10 || 47 = 4.52 \text{ k}\Omega \end{aligned}$$

as shown in Fig. 7.15(d). For the latter circuit we can write the two equations

$$v_o = (i_i - g_m v_{gs}) R'_L \quad (7.45)$$

and

$$i_i = \frac{v_{gs} - v_o}{R_G} \quad (7.46)$$

Substituting for  $i_i$  from Eq. (7.46) into Eq. (7.45) results in the following expression for the voltage gain  $A_v \equiv v_o/v_i = v_o/v_{gs}$ :

$$A_v = -g_m R'_L \frac{1 - (1/g_m R_G)}{1 + (R'_L/R_G)}$$

Since  $R_G$  is very large,  $g_m R_G \gg 1$  and  $R'_L/R_G \ll 1$  (the reader can easily verify this), and the gain expression can be approximated as

$$A_v \simeq -g_m R'_L \quad (7.47)$$

Substituting  $g_m = 0.725 \text{ mA/V}$  and  $R'_L = 4.52 \text{ k}\Omega$  yields

$$A_v = -3.3 \text{ V/V}$$

To obtain the input resistance, we substitute in Eq. (7.46) for  $v_o = A_v v_{gs} = -g_m R'_L v_{gs}$ , then use  $R_{in} \equiv v_i/i_i = v_{gs}/i_i$  to obtain

$$R_{in} = \frac{R_G}{1 + g_m R'_L} \quad (7.48)$$

This is an interesting relationship: The input resistance decreases as the gain ( $g_m R'_L$ ) is increased. The value of  $R_{in}$  can now be determined; it is

$$R_{in} = \frac{10 \text{ M}\Omega}{1 + 3.3} = 2.33 \text{ M}\Omega$$

which is still very large.

The largest allowable input signal  $\hat{v}_i$  is constrained by the need to keep the transistor in saturation at all times; that is,

$$v_{DS} \geq v_{GS} - V_t$$

Enforcing this condition with equality at the point  $v_{GS}$  is maximum and  $v_{DS}$  is minimum, we write

$$v_{DS\min} = v_{GS\max} - V_t$$

$$V_{DS} - |A_v| \hat{v}_i = V_{GS} + \hat{v}_i - V_t$$

Since  $V_{DS} = V_{GS}$ , we obtain

$$\hat{v}_i = \frac{V_t}{|A_v| + 1}$$

This is a general relationship that applies to this circuit irrespective of the component values. Observe that it simply states that the maximum signal swing is determined by the fact that the bias arrangement makes  $V_D = V_G$  and thus, to keep the MOSFET out of the triode region, the signal between D and G is constrained to be equal to  $V_t$ . For our particular design,

$$\hat{v}_i = \frac{1.5}{3.3 + 1} = 0.35 \text{ V}$$

Since  $V_{OV} = 2.9 \text{ V}$ , a  $v_i$  of 0.35 is indeed much smaller than  $2V_{OV} = 5.8 \text{ V}$ ; thus the assumption of linear operation is justified.

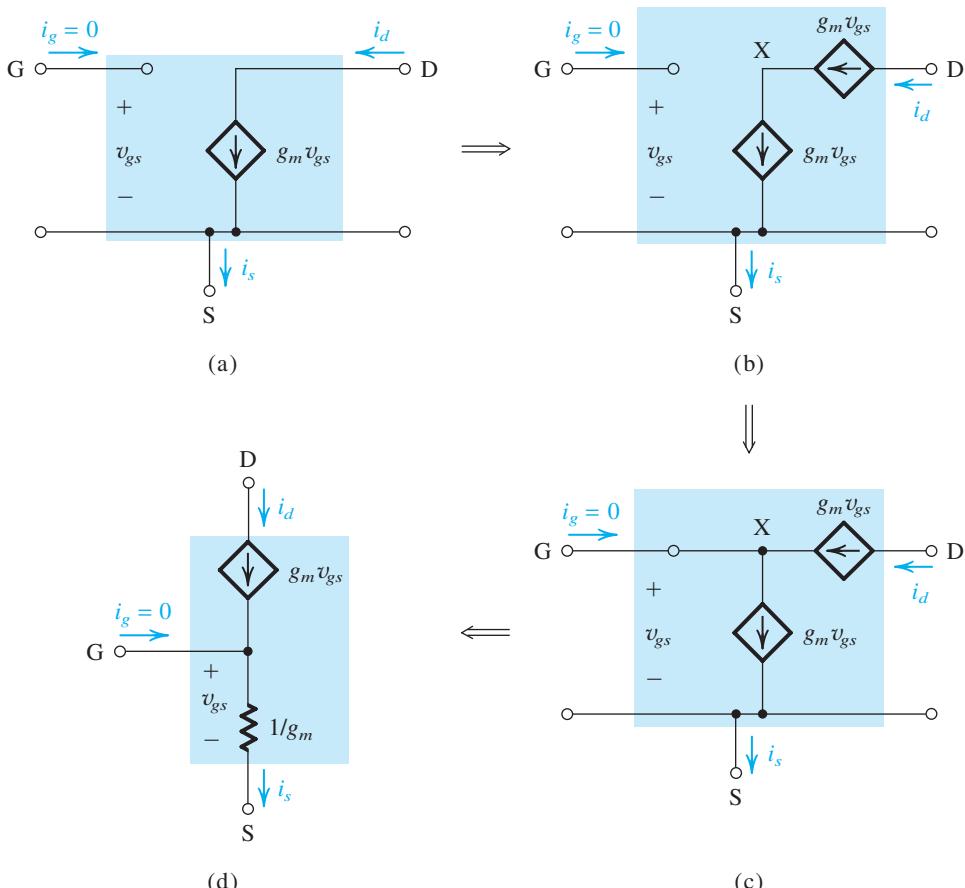
A modification of this circuit that increases the allowable signal swing is investigated in Problem 7.103.

### EXERCISE

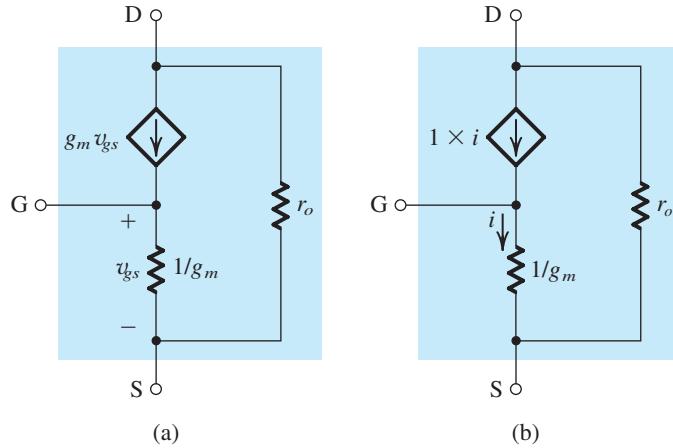
- D7.4** Consider the amplifier circuit of Fig. 7.15(a) without the load resistance  $R_L$  and with channel-length modulation neglected. Let  $V_{DD} = 5 \text{ V}$ ,  $V_t = 0.7 \text{ V}$ , and  $k_n = 1 \text{ mA/V}^2$ . Find  $V_{OV}$ ,  $I_D$ ,  $R_D$ , and  $R_G$  to obtain a voltage gain of  $-25 \text{ V/V}$  and an input resistance of  $0.5 \text{ M}\Omega$ . What is the maximum allowable input signal,  $\hat{v}_i$ ?

**Ans.**  $0.319 \text{ V}$ ;  $50.9 \mu\text{A}$ ;  $78.5 \text{ k}\Omega$ ;  $13 \text{ M}\Omega$ ;  $27 \text{ mV}$

**The T Equivalent-Circuit Model** Through a simple circuit transformation it is possible to develop an alternative equivalent-circuit model for the MOSFET. The development of such a model, known as the T model, is illustrated in Fig. 7.16. Figure 7.16(a) shows the equivalent circuit studied above without  $r_o$ . In Fig. 7.16(b) we have added a second  $g_m v_{gs}$  current source in series with the original controlled source. This addition obviously does not change the terminal currents and is thus allowed. The newly created circuit node, labeled X, is joined to the gate terminal G in Fig. 7.16(c). Observe that the gate current does not change—that is, it remains equal to zero—and thus this connection does not alter the terminal characteristics. We now note that we have a controlled current source  $g_m v_{gs}$  connected across its control voltage  $v_{gs}$ . We can replace this controlled source by a resistance as long as this resistance draws an equal current as the source. (See the source-absorption theorem in Appendix D.) Thus the value of the resistance is  $v_{gs}/g_m v_{gs} = 1/g_m$ . This replacement is shown in Fig. 7.16(d), which depicts



**Figure 7.16** Development of the T equivalent-circuit model for the MOSFET. For simplicity,  $r_o$  has been omitted; however, it may be added between D and S in the T model of (d).



**Figure 7.17** (a) The T model of the MOSFET augmented with the drain-to-source resistance  $r_o$ . (b) An alternative representation of the T model.

the alternative model. Observe that  $i_g$  is still zero,  $i_d = g_m v_{gs}$ , and  $i_s = v_{gs}/(1/g_m) = g_m v_{gs}$ , all the same as in the original model in Fig. 7.16(a).

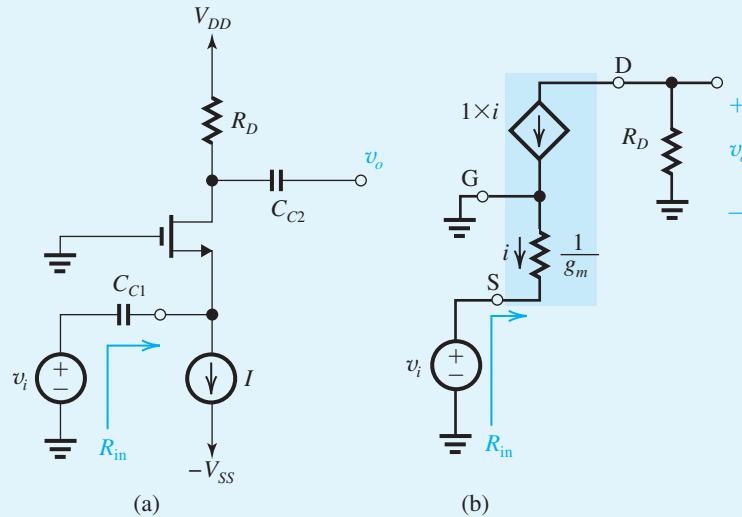
The model of Fig. 7.16(d) shows that the resistance between gate and source looking into the source is  $1/g_m$ . This observation and the T model prove useful in many applications. Note that the resistance between gate and source, looking into the gate, is infinite.

In developing the T model we did not include  $r_o$ . If desired, this can be done by incorporating in the circuit of Fig. 7.16(d) a resistance  $r_o$  between drain and source, as shown in Fig. 7.17(a). An alternative representation of the T model, in which the voltage-controlled current source is replaced with a current-controlled current source, is shown in Fig. 7.17(b).

Finally, we should note that in order to distinguish the model of Fig. 7.13(b) from the equivalent T model, the former is sometimes referred to as the **hybrid- $\pi$  model**, a carryover from the bipolar transistor literature. The origin of this name will be explained shortly.

#### Example 7.4

Figure 7.18(a) shows a MOSFET amplifier biased by a constant-current source  $I$ . Assume that the values of  $I$  and  $R_D$  are such that the MOSFET operates in the saturation region. The input signal  $v_i$  is coupled to the source terminal by utilizing a large capacitor  $C_{C1}$ . Similarly, the output signal at the drain is taken through a large coupling capacitor  $C_{C2}$ . Find the input resistance  $R_{in}$  and the voltage gain  $v_o/v_i$ . Neglect channel-length modulation.

**Example 7.4** *continued***Figure 7.18** (a) Amplifier circuit for Example 7.4. (b) Small-signal equivalent circuit of the amplifier in (a).**Solution**

Replacing the MOSFET with its T equivalent-circuit model results in the amplifier equivalent circuit shown in Fig. 7.18(b). Observe that the dc current source  $I$  is replaced with an open circuit and the dc voltage source  $V_{DD}$  is replaced by a short circuit. The large coupling capacitors have been replaced by short circuits. From the equivalent-circuit model we determine

$$R_{in} = \frac{v_i}{-i} = 1/g_m$$

and

$$v_o = -iR_D = \left( \frac{v_i}{1/g_m} \right) R_D = g_m R_D v_i$$

Thus,

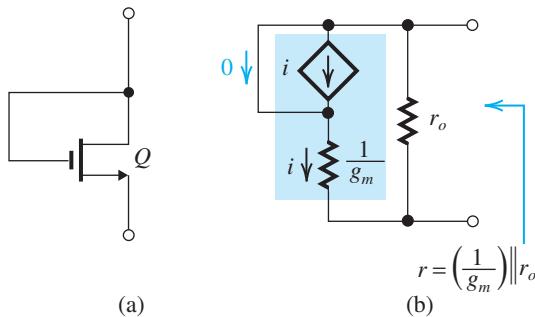
$$A_v \equiv \frac{v_o}{v_i} = g_m R_D$$

We note that this amplifier, known as the common-gate amplifier because the gate at ground potential is common to both the input and output ports, has a low input resistance ( $1/g_m$ ) and a noninverting gain. We shall study this amplifier type in Section 7.3.5.

## EXERCISE

- 7.5** Use the T model of Fig. 7.17(b) to show that a MOSFET whose drain is connected to its gate exhibits an incremental resistance equal to  $[(1/g_m) \parallel r_o]$ .

**Ans.** See Fig. E7.5.



**Figure E7.5** Circuits for Exercise 7.5. Note that the bias arrangement of  $Q$  is not shown.

**Modeling the Body Effect** As mentioned earlier (see Section 5.4), the body effect occurs in a MOSFET when the source is not tied to the substrate (which is always connected to the most negative power supply in the integrated circuit for *n*-channel devices and to the most positive for *p*-channel devices). Thus the substrate (body) will be at signal ground, but since the source is not, a signal voltage  $v_{bs}$  develops between the body (B) and the source (S). The substrate then acts as a “second gate” or a **backgate** for the MOSFET. Thus the signal  $v_{bs}$  gives rise to a drain-current component, which we shall write as  $g_{mb}v_{bs}$ , where  $g_{mb}$  is the **body transconductance**, defined as

$$g_{mb} \equiv \left. \frac{\partial i_D}{\partial v_{BS}} \right|_{\substack{v_{GS} = \text{constant} \\ v_{DS} = \text{constant}}} \quad (7.49)$$

Recalling that  $i_D$  depends on  $v_{BS}$  through the dependence of  $V_t$  on  $V_{BS}$ , we can show that

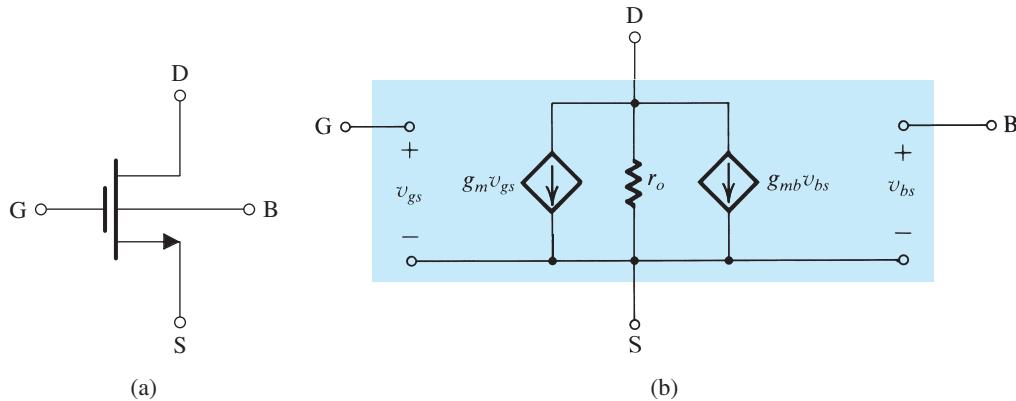
$$g_{mb} = \chi g_m \quad (7.50)$$

where

$$\chi \equiv \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} \quad (7.51)$$

Typically the value of  $\chi$  lies in the range 0.1 to 0.3.

Figure 7.19 shows the MOSFET model augmented to include the controlled source  $g_{mb}v_{bs}$  that models the body effect. Ideally, this is the model to be used whenever the source is not connected to the substrate. It has been found, however, that except in some very particular



**Figure 7.19** Small-signal, equivalent-circuit model of a MOSFET in which the source is not connected to the body.

situations, the body effect can generally be ignored in the initial, pencil-and-paper design of MOSFET amplifiers.

Finally, although the analysis above was performed on an NMOS transistor, the results and the equivalent circuit of Fig. 7.19 apply equally well to PMOS transistors, except for using  $|V_{GS}|$ ,  $|V_t|$ ,  $|V_{OV}|$ ,  $|V_A|$ ,  $|V_{SB}|$ ,  $|\gamma|$ , and  $|\lambda|$  and replacing  $k'_n$  with  $k'_p$  in the appropriate formula.

## EXERCISES

- 7.6** For the amplifier in Fig. 7.4, let  $V_{DD} = 5$  V,  $R_D = 10$  k $\Omega$ ,  $V_t = 1$  V,  $k'_n = 20 \mu\text{A/V}^2$ ,  $W/L = 20$ ,  $V_{GS} = 2$  V, and  $\lambda = 0$ .

- (a) Find the dc current  $I_D$  and the dc voltage  $V_{DS}$ .
- (b) Find  $g_m$ .
- (c) Find the voltage gain.
- (d) If  $v_{gs} = 0.2 \sin \omega t$  volts, find  $v_{ds}$  assuming that the small-signal approximation holds. What are the minimum and maximum values of  $v_{ds}$ ?
- (e) Use Eq. (7.28) to determine the various components of  $i_D$ . Using the identity  $(\sin^2 \omega t = \frac{1}{2} - \frac{1}{2} \cos 2\omega t)$ , show that there is a slight shift in  $I_D$  (by how much?) and that there is a second-harmonic component (i.e., a component with frequency  $2\omega$ ). Express the amplitude of the second-harmonic component as a percentage of the amplitude of the fundamental. (This value is known as the second-harmonic distortion.)

**Ans.** (a)  $200 \mu\text{A}$ ,  $3$  V; (b)  $0.4 \text{ mA/V}$ ; (c)  $-4 \text{ V/V}$ ; (d)  $v_{ds} = -0.8 \sin \omega t$  volts,  $2.2$  V,  $3.8$  V; (e)  $i_D = (204 + 80 \sin \omega t - 4 \cos 2\omega t) \mu\text{A}$ ,  $5\%$

- 7.7** An NMOS transistor has  $\mu_n C_{ox} = 60 \mu\text{A/V}^2$ ,  $W/L = 40$ ,  $V_t = 1$  V, and  $V_A = 15$  V. Find  $g_m$  and  $r_o$  when (a) the bias voltage  $V_{GS} = 1.5$  V, (b) the bias current  $I_D = 0.5$  mA.

**Ans.** (a)  $1.2 \text{ mA/V}$ ,  $50 \text{ k}\Omega$ ; (b)  $1.55 \text{ mA/V}$ ,  $30 \text{ k}\Omega$

- 7.8** A MOSFET is to operate at  $I_D = 0.1$  mA and is to have  $g_m = 1$  mA/V. If  $k'_n = 50 \mu\text{A}/\text{V}^2$ , find the required  $W/L$  ratio and the overdrive voltage.

**Ans.** 100; 0.2 V

- 7.9** For a fabrication process for which  $\mu_p \simeq 0.4 \mu_n$ , find the ratio of the width of a PMOS transistor to the width of an NMOS transistor so that the two devices have equal  $g_m$  for the same bias conditions. The two devices have equal channel lengths.

**Ans.** 2.5

- 7.10** A PMOS transistor has  $V_t = -1$  V,  $k'_p = 60 \mu\text{A}/\text{V}^2$ , and  $W/L = 16 \mu\text{m}/0.8 \mu\text{m}$ . Find  $I_D$  and  $g_m$  when the device is biased at  $V_{GS} = -1.6$  V. Also, find the value of  $r_o$  if  $\lambda$  (at  $L = 1 \mu\text{m}$ ) =  $-0.04 \text{ V}^{-1}$ .

**Ans.** 216  $\mu\text{A}$ ; 0.72 mA/V; 92.6 k $\Omega$

- 7.11** Derive an expression for  $(g_m r_o)$  in terms of  $V_A$  and  $V_{OV}$ . As we shall see in Chapter 8, this is an important transistor parameter and is known as the intrinsic gain. Evaluate the value of  $g_m r_o$  for an NMOS transistor fabricated in a 0.8- $\mu\text{m}$  CMOS process for which  $V'_A = 12.5 \text{ V}/\mu\text{m}$  of channel length. Let the device have minimum channel length and be operated at an overdrive voltage of 0.2 V.

**Ans.**  $g_m r_o = 2V_A/V_{OV}$ ; 100 V/V

## 7.2.2 The BJT Case

We next consider the small-signal operation of the BJT and develop small-signal equivalent-circuit models that represent its operation at a given bias point. The following development parallels what we used for the MOSFET except that here we have an added complication: The BJT draws a finite base current. As will be seen shortly, this phenomenon (finite  $\beta$ ) manifests itself as a finite input resistance looking into the base of the BJT (as compared to the infinite input resistance looking into the gate of the MOSFET).

Consider the *conceptual* amplifier circuit shown in Fig. 7.20(a). Here the base-emitter junction is forward biased by a dc voltage  $V_{BE}$ . The reverse bias of the collector-base junction is established by connecting the collector to another power supply of voltage  $V_{CC}$  through a resistor  $R_C$ . The input signal to be amplified is represented by the voltage source  $v_{be}$  that is superimposed on  $V_{BE}$ .

**The DC Bias Point** We consider first the dc bias conditions by setting the signal  $v_{be}$  to zero. The circuit reduces to that in Fig. 7.20(b), and we can write the following relationships for the dc currents and voltages:

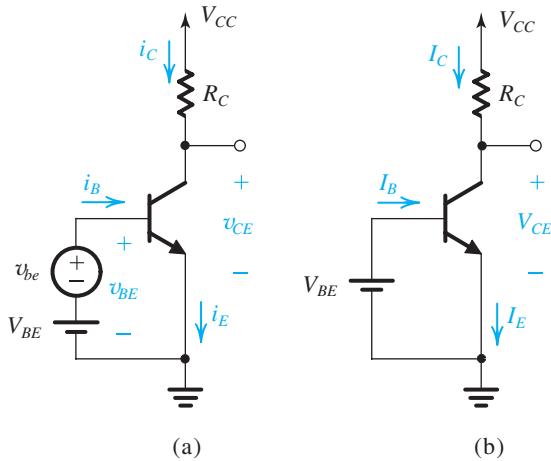
$$I_C = I_S e^{V_{BE}/V_T} \quad (7.52)$$

$$I_E = I_C/\alpha \quad (7.53)$$

$$I_B = I_C/\beta \quad (7.54)$$

$$V_{CE} = V_{CC} - I_C R_C \quad (7.55)$$

For active-mode operation,  $V_{CE}$  should be greater than  $(V_{BE} - 0.4)$  by an amount that allows for the required negative signal swing at the collector.



**Figure 7.20** (a) Conceptual circuit to illustrate the operation of the transistor as an amplifier. (b) The circuit of (a) with the signal source  $v_{be}$  eliminated for dc (bias) analysis.

**The Collector Current and the Transconductance** If a signal  $v_{be}$  is applied as shown in Fig. 7.20(a), the total instantaneous base–emitter voltage  $v_{BE}$  becomes

$$v_{BE} = V_{BE} + v_{be}$$

Correspondingly, the collector current becomes

$$\begin{aligned} i_C &= I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE} + v_{be})/V_T} \\ &= I_S e^{V_{BE}/V_T} e^{v_{be}/V_T} \end{aligned}$$

Use of Eq. (7.52) yields

$$i_C = I_C e^{v_{be}/V_T} \quad (7.56)$$

Now, if  $v_{be} \ll V_T$ , we may approximate Eq. (7.56) as

$$i_C \simeq I_C \left( 1 + \frac{v_{be}}{V_T} \right) \quad (7.57)$$

Here we have expanded the exponential in Eq. (7.56) in a series and retained only the first two terms. That is, we have assumed that

$$v_{be} \ll V_T \quad (7.58)$$

so that we can neglect the higher-order terms in the exponential series expansion. The condition in Eq. (7.58) is the **small-signal approximation** for the BJT and corresponds to that in Eq. (7.29) for the MOSFET case. The small-signal approximation for the BJT is valid only for  $v_{be}$  less than 5 mV or 10 mV, at most. Under this approximation, the total collector current is given by Eq. (7.57) and can be rewritten

$$i_C = I_C + \frac{I_C}{V_T} v_{be} \quad (7.59)$$

Thus the collector current is composed of the dc bias value  $I_C$  and a signal component  $i_c$ ,

$$i_c = \frac{I_C}{V_T} v_{be} \quad (7.60)$$

This equation relates the signal current in the collector to the corresponding base-emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be} \quad (7.61) \quad \text{◀}$$

where  $g_m$  is the **transconductance**, and from Eq. (7.60), it is given by

$$g_m = \frac{I_C}{V_T} \quad (7.62) \quad \text{◀}$$

We observe that the transconductance of the BJT is directly proportional to the collector bias current  $I_C$ . Thus to obtain a constant predictable value for  $g_m$ , we need a constant predictable  $I_C$ . Also, we note that BJTs have relatively high transconductance in comparison to MOSFETs: for instance, at  $I_C = 1$  mA,  $g_m \simeq 40$  mA/V. Finally, unlike the MOSFET, whose  $g_m$  depends on the device dimensions ( $W$  and  $L$ ),  $g_m$  of a BJT depends only on the dc collector current at which it is biased to operate.

A graphical interpretation for  $g_m$  is given in Fig. 7.21, where it is shown that  $g_m$  is equal to the slope of the tangent to the  $i_c-v_{BE}$  characteristic curve at  $i_c = I_C$  (i.e., at the bias point Q). Thus,

$$g_m = \left. \frac{\partial i_c}{\partial v_{BE}} \right|_{i_c = I_C} \quad (7.63) \quad \text{◀}$$

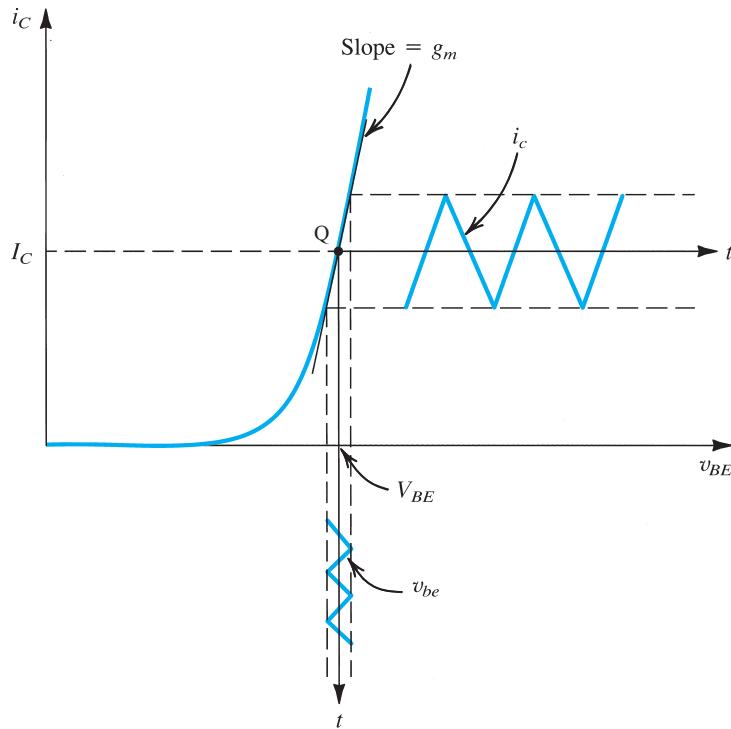
The small-signal approximation implies keeping the signal amplitude sufficiently small that *operation is restricted to an almost-linear segment of the  $i_c-v_{BE}$  exponential curve*. Increasing the signal amplitude will result in the collector current having components nonlinearly related to  $v_{be}$ .

## EXERCISES

**7.12** Use Eq. (7.63) to derive the expression for  $g_m$  in Eq. (7.62).

**7.13** Calculate the value of  $g_m$  for a BJT biased at  $I_C = 0.5$  mA.

**Ans.** 20 mA/V



**Figure 7.21** Linear operation of the transistor under the small-signal condition: A small-signal  $v_{be}$  with a triangular waveform is superimposed on the dc voltage  $V_{BE}$ . It gives rise to a collector-signal current  $i_c$ , also of triangular waveform, superimposed on the dc current  $I_C$ . Here,  $i_c = g_m v_{be}$ , where  $g_m$  is the slope of the  $i_C - v_{BE}$  curve at the bias point Q.

**The Base Current and the Input Resistance at the Base** To determine the resistance seen by  $v_{be}$ , we first evaluate the total base current  $i_B$  using Eq. (7.59), as follows:

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta} \frac{I_C}{V_T} v_{be}$$

Thus,

$$i_B = I_B + i_b \quad (7.64)$$

where  $I_B$  is equal to  $I_C/\beta$  and the signal component  $i_b$  is given by

$$i_b = \frac{1}{\beta} \frac{I_C}{V_T} v_{be} \quad (7.65)$$

Substituting for  $I_C/V_T$  by  $g_m$  gives

$$i_b = \frac{g_m}{\beta} v_{be} \quad (7.66)$$

The small-signal input resistance between base and emitter, *looking into the base*, is denoted by  $r_\pi$  and is defined as

$$r_\pi \equiv \frac{v_{be}}{i_b} \quad (7.67)$$

Using Eq. (7.66) gives

$$r_\pi = \frac{\beta}{g_m} \quad (7.68)$$

Thus  $r_\pi$  is directly dependent on  $\beta$  and is inversely proportional to the bias current  $I_C$ . Substituting for  $g_m$  in Eq. (7.68) from Eq. (7.62) and replacing  $I_C/\beta$  by  $I_B$  gives an alternative expression for  $r_\pi$ ,

$$r_\pi = \frac{V_T}{I_B} \quad (7.69)$$

Here, we recall that because the gate current of the MOSFET is zero (at dc and low frequencies) the input resistance at the gate is infinite; that is, in the MOSFET there is no counterpart to  $r_\pi$ .<sup>5</sup>

### EXERCISE

- 7.14** A BJT amplifier is biased to operate at a constant collector current  $I_C = 0.5$  mA irrespective of the value  $\beta$ . If the transistor manufacturer specifies  $\beta$  to range from 50 to 200, give the expected range of  $g_m$ ,  $I_B$ , and  $r_\pi$ .

**Ans.**  $g_m$  is constant at 20 mA/V;  $I_B = 10 \mu\text{A}$  to  $2.5 \mu\text{A}$ ;  $r_\pi = 2.5 \text{k}\Omega$  to  $10 \text{k}\Omega$

**The Emitter Current and the Input Resistance at the Emitter** The total emitter current  $i_E$  can be determined using Eq. (7.59) as

$$i_E = \frac{i_c}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

Thus,

$$i_E = I_E + i_e \quad (7.70)$$

where  $I_E$  is equal to  $I_C/\alpha$  and the signal current  $i_e$  is given by

$$i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be} \quad (7.71)$$

---

<sup>5</sup>At high frequencies, the input capacitance at the MOSFET gate makes the input current finite (see Chapter 10).

If we denote the small-signal resistance between base and emitter *looking into the emitter* by  $r_e$ , it can be defined as

$$r_e \equiv \frac{v_{be}}{i_e} \quad (7.72)$$

Using Eq. (7.71) we find that  $r_e$ , called the **emitter resistance**, is given by

➤  $r_e = \frac{V_T}{I_E}$  (7.73)

Comparison with Eq. (7.62) reveals that

➤  $r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m}$  (7.74)

The relationship between  $r_\pi$  and  $r_e$  can be found by combining their respective definitions in Eqs. (7.67) and (7.72) as

$$v_{be} = i_b r_\pi = i_e r_e$$

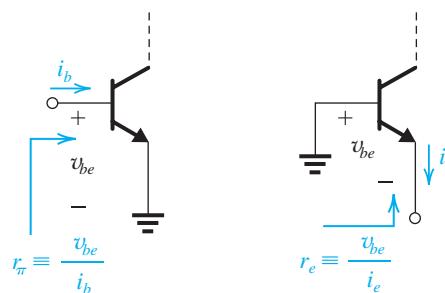
Thus,

$$r_\pi = (i_e / i_b) r_e$$

which yields

➤  $r_\pi = (\beta + 1) r_e$  (7.75)

Figure 7.22 illustrates the definition of  $r_\pi$  and  $r_e$ .



**Figure 7.22** Illustrating the definition of  $r_\pi$  and  $r_e$ .

Finally, a comparison with the MOSFET would be useful: For the MOSFET,  $\alpha = 1$  and the resistance looking into the source is simply  $1/g_m$ .

## SHOCKLEY AND SILICON VALLEY:

In 1956 William Bradford Shockley started a new company, Shockley Semiconductor Laboratory in Mountain View, California (near Stanford, his birthplace). While at Bell Labs, together with John Bardeen and Walter Brattain, he had invented the BJT. At Shockley, the initial concentration was on developing semiconductor devices, particularly a new four-layer diode. But Shockley's scientific genius and ability to select and attract good team members, first demonstrated at Bell Labs, was not accompanied by comparable talent for management. Consequently, in 1957, eight of his team members (the so-called Traitorous Eight, including Gordon Moore and Robert Noyce) left Shockley to create Fairchild Semiconductor. It was a propitious time: The first *Sputnik* was launched a month later, and the ensuing space race accelerated demand for solid-state circuits. Decades passed, and in 2002 a group of some 30 individuals who had been associated with Silicon Valley since 1956 met at Stanford University to reminisce about Shockley's contributions to the information technology age. They unanimously concluded that Shockley was the man who brought silicon to Silicon Valley!

## EXERCISE

- 7.15** A BJT having  $\beta = 100$  is biased at a dc collector current of 1 mA. Find the value of  $g_m$ ,  $r_e$ , and  $r_\pi$  at the bias point.

**Ans.** 40 mA/V; 25  $\Omega$ ; 2.5 k $\Omega$

**The Voltage Gain** The total collector voltage  $v_{CE}$  is

$$\begin{aligned} v_{CE} &= V_{CC} - i_C R_C \\ &= V_{CC} - (I_C + i_c) R_C \\ &= (V_{CC} - I_C R_C) - i_c R_C \\ &= V_{CE} - i_c R_C \end{aligned} \quad (7.76)$$

Thus, superimposed on the collector bias voltage  $V_{CE}$  we have signal voltage  $v_{ce}$  given by

$$\begin{aligned} v_{ce} &= -i_c R_C = -g_m v_{be} R_C \\ &= (-g_m R_C) v_{be} \end{aligned} \quad (7.77)$$

from which we find the voltage gain  $A_v$  of this amplifier as

$$A_v \equiv \frac{v_{ce}}{v_{be}} = -g_m R_C \quad (7.78)$$

Here again we note that because  $g_m$  is directly proportional to the collector bias current, the gain will be as stable as the collector bias current is made. Substituting for  $g_m$  from Eq. (7.62)

enables us to express the gain in the form

$$A_v = -\frac{I_C R_C}{V_T} \quad (7.79)$$

which is identical to the expression we derived in Section 7.1 (Eq. 7.21). Finally, we note that the gain expression in Eq. (7.78) is identical in form to that for the MOSFET amplifier (namely,  $-g_m R_D$ ).

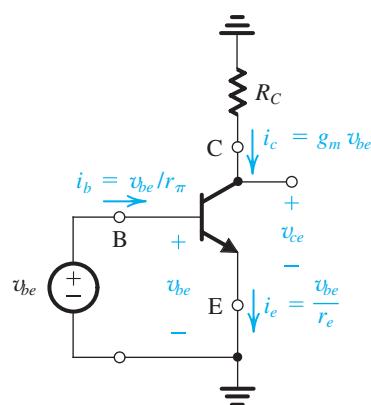
### EXERCISE

- 7.16** In the circuit of Fig. 7.20(a),  $V_{BE}$  is adjusted to yield a dc collector current of 1 mA. Let  $V_{CC} = 15$  V,  $R_C = 10$  k $\Omega$ , and  $\beta = 100$ . Find the voltage gain  $v_{ce}/v_{be}$ . If  $v_{be} = 0.005 \sin \omega t$  volt, find  $v_c(t)$  and  $i_B(t)$ .

**Ans.**  $-400$  V/V;  $5 - 2 \sin \omega t$  volts;  $10 + 2 \sin \omega t$   $\mu$ A

**Separating the Signal and the DC Quantities** The analysis above indicates that every current and voltage in the amplifier circuit of Fig. 7.20(a) is composed of two components: a dc component and a signal component. For instance,  $v_{BE} = V_{BE} + v_{be}$ ,  $I_C = I_C + i_c$ , and so on. The dc components are determined from the dc circuit given in Fig. 7.20(b) and from the relationships imposed by the transistor (Eqs. 7.52 through 7.54). On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources, as shown in Fig. 7.23. Observe that since the voltage of an ideal dc supply does not change, the signal voltage across it will be zero. For this reason we have replaced  $V_{CC}$  and  $V_{BE}$  with short circuits. Had the circuit contained ideal dc current sources, these would have been replaced by open circuits. Note, however, that the circuit of Fig. 7.23 is useful only insofar as it shows the various signal currents and voltages; it is *not* an actual amplifier circuit, since the dc bias circuit is not shown.

Figure 7.23 also shows the expressions for the current increments ( $i_c$ ,  $i_b$ , and  $i_e$ ) obtained when a small signal  $v_{be}$  is applied. These relationships can be represented by a circuit. Such



**Figure 7.23** The amplifier circuit of Fig. 7.20(a) with the dc sources ( $V_{BE}$  and  $V_{CC}$ ) eliminated (short-circuited). Thus only the signal components are present. Note that this is a representation of the signal operation of the BJT and not an actual amplifier circuit.

a circuit should have three terminals—C, B, and E—and should yield the same terminal currents indicated in Fig. 7.23. The resulting circuit is then *equivalent to the transistor as far as small-signal operation is concerned*, and thus it can be considered an equivalent small-signal circuit model.

**The Hybrid- $\pi$  Model** An equivalent-circuit model for the BJT is shown in Fig. 7.24(a). This model represents the BJT as a voltage-controlled current source and explicitly includes the input resistance looking into the base,  $r_\pi$ . The model obviously yields  $i_c = g_m v_{be}$  and  $i_b = v_{be}/r_\pi$ . Not so obvious, however, is the fact that the model also yields the correct expression for  $i_e$ . This can be shown as follows: At the emitter node we have

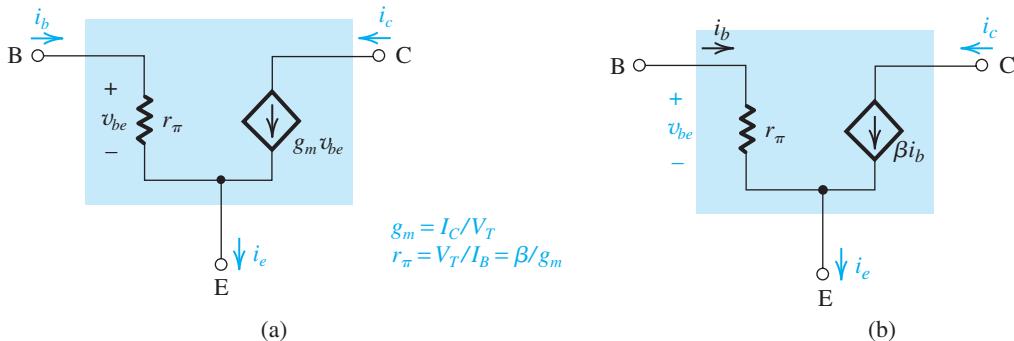
$$\begin{aligned} i_e &= \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi} (1 + g_m r_\pi) \\ &= \frac{v_{be}}{r_\pi} (1 + \beta) = v_{be} / \left( \frac{r_\pi}{1 + \beta} \right) \\ &= v_{be}/r_e \end{aligned}$$

A slightly different equivalent-circuit model can be obtained by expressing the current of the controlled source ( $g_m v_{be}$ ) in terms of the base current  $i_b$  as follows:

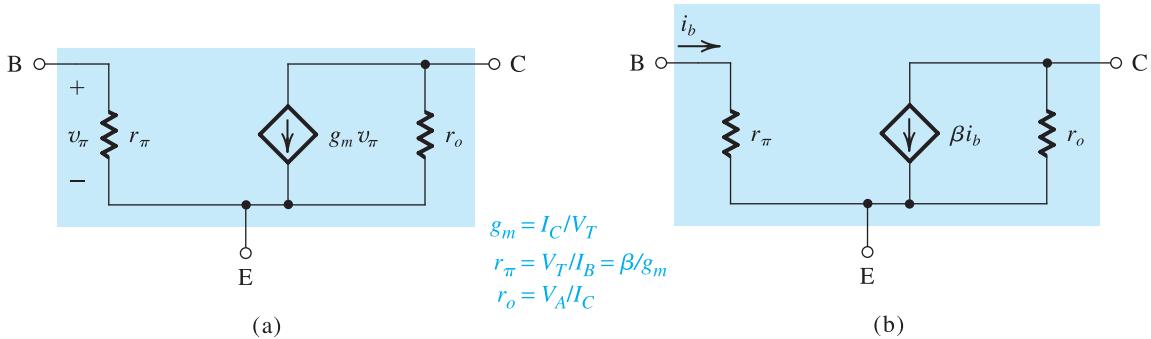
$$\begin{aligned} g_m v_{be} &= g_m (i_b r_\pi) \\ &= (g_m r_\pi) i_b = \beta i_b \end{aligned}$$

This results in the alternative equivalent-circuit model shown in Fig. 7.24(b). Here the transistor is represented as a current-controlled current source, with the control current being  $i_b$ .

As we have done in the case of the MOSFET's small-signal models, we can account for the Early effect (the slight dependence of  $i_C$  on  $v_{CE}$  due to basewidth modulation) by adding the resistance  $r_o = V_A/I_C$  between collector and emitter, as shown in Fig. 7.25. Note that to conform with the literature, we have renamed  $v_{be}$  as  $v_\pi$ . The two models of Fig. 7.25 are versions of the hybrid- $\pi$  model, the most widely used model for the BJT. The equivalent circuit of Fig. 7.25(a) corresponds to that of the MOSFET [Fig. 7.13(b)] except for  $r_\pi$ , which accounts for the finite base current (or finite  $\beta$ ) of the BJT. However, the equivalent circuit of Fig. 7.25(b) has no MOS counterpart.



**Figure 7.24** Two slightly different versions of the hybrid- $\pi$  model for the small-signal operation of the BJT. The equivalent circuit in (a) represents the BJT as a voltage-controlled current source (a transconductance amplifier), and that in (b) represents the BJT as a current-controlled current source (a current amplifier).



**Figure 7.25** The hybrid- $\pi$  small-signal model, in its two versions, with the resistance  $r_o$  included.

It is important to note that the small-signal equivalent circuits of Fig. 7.25 model the operation of the BJT *at a given bias point*. This should be obvious from the fact that the model parameters  $g_m$ ,  $r_\pi$ , and  $r_o$  depend on the value of the dc bias current  $I_C$ , as indicated in Fig. 7.25. That is, these equivalent circuits model the *incremental operation* of the BJT around the bias point.

As in the case of the MOSFET amplifier, including  $r_o$  in the BJT model causes the voltage gain of the conceptual amplifier of Fig. 7.20(a) to become

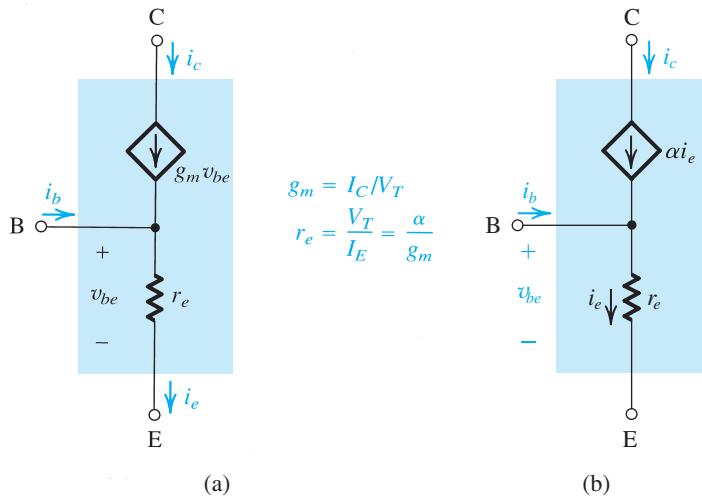
$$\frac{v_o}{v_{be}} = -g_m(R_C \parallel r_o) \quad (7.80)$$

Thus, the magnitude of the gain is reduced somewhat.

## EXERCISE

- 7.17** For the model in Fig. 7.24(b) show that  $i_c = g_m v_{be}$  and  $i_e = v_{be}/r_e$ .

**The T Model** Although the hybrid- $\pi$  model (in one of its two variants shown in Fig. 7.24) can be used to carry out small-signal analysis of any transistor circuit, there are situations in which an alternative model, shown in Fig. 7.26, is much more convenient. This model, called, as in the case of the MOSFET, the **T model**, is shown in two versions in Fig. 7.26. The model of Fig. 7.26(a) represents the BJT as a voltage-controlled current source with the control voltage being  $v_{be}$ . Here, however, the resistance between base and emitter, looking into the emitter, is explicitly shown. From Fig. 7.26(a) we see clearly that the model yields the correct expressions for  $i_c$  and  $i_e$ . It can also be shown to yield the correct expression for  $i_b$  (see Exercise 7.18 on the next page).



**Figure 7.26** Two slightly different versions of what is known as the *T model* of the BJT. The circuit in (a) is a voltage-controlled current source representation and that in (b) is a current-controlled current source representation. These models explicitly show the emitter resistance  $r_e$  rather than the base resistance  $r_\pi$  featured in the hybrid- $\pi$  model.

If in the model of Fig. 7.26(a) the current of the controlled source is expressed in terms of the emitter current as

$$\begin{aligned} g_m v_{be} &= g_m (i_e r_e) \\ &= (g_m r_e) i_e = \alpha i_e \end{aligned}$$

we obtain the alternative T model shown in Fig. 7.26(b). Here the BJT is represented as a current-controlled current source but with the control signal being  $i_e$ .

Finally, the T models can be augmented by  $r_o$  to account for the dependence of  $i_c$  to  $v_{ce}$  (the Early effect) to obtain the equivalent circuits shown in Fig. 7.27.

### EXERCISE

- 7.18** Show that for the T model in Fig. 7.24(a),  $i_b = v_{be}/r_\pi$ .

**Small-Signal Models of the pnp Transistor** Although the small-signal models in Figs. 7.25 and 7.27 were developed for the case of the *npn* transistor, they apply equally well to the *pnp* transistor *with no change in polarities*.

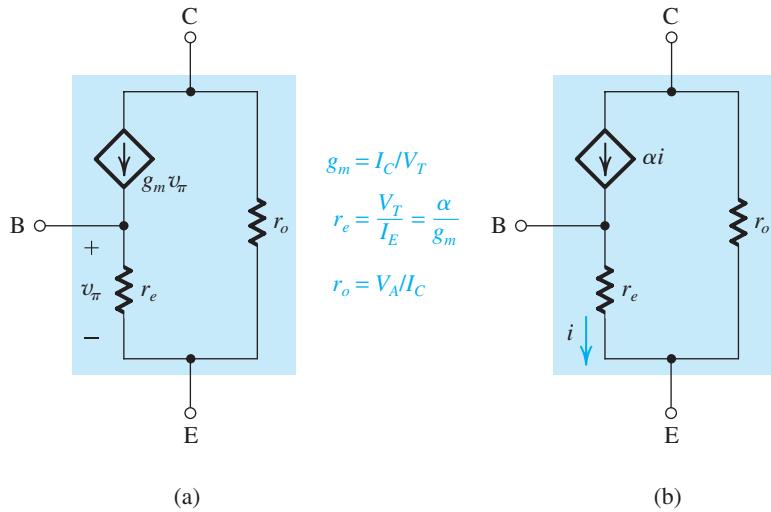


Figure 7.27 The T models of the BJT.

### Example 7.5

We wish to analyze the transistor amplifier shown in Fig. 7.28(a) to determine its voltage gain  $v_o/v_i$ . Assume  $\beta = 100$  and neglect the Early effect.

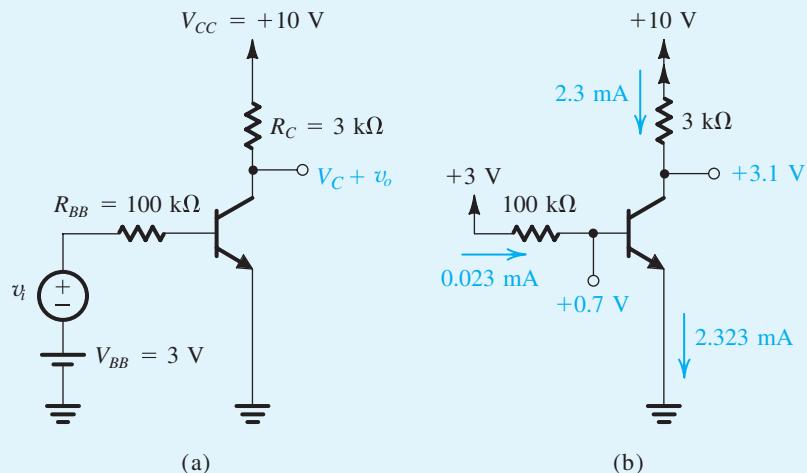


Figure 7.28 Example 7.5: (a) amplifier circuit; (b) circuit for dc analysis; (c) amplifier circuit with dc sources replaced by short circuits; (d) amplifier circuit with transistor replaced by its hybrid- $\pi$ , small-signal model.

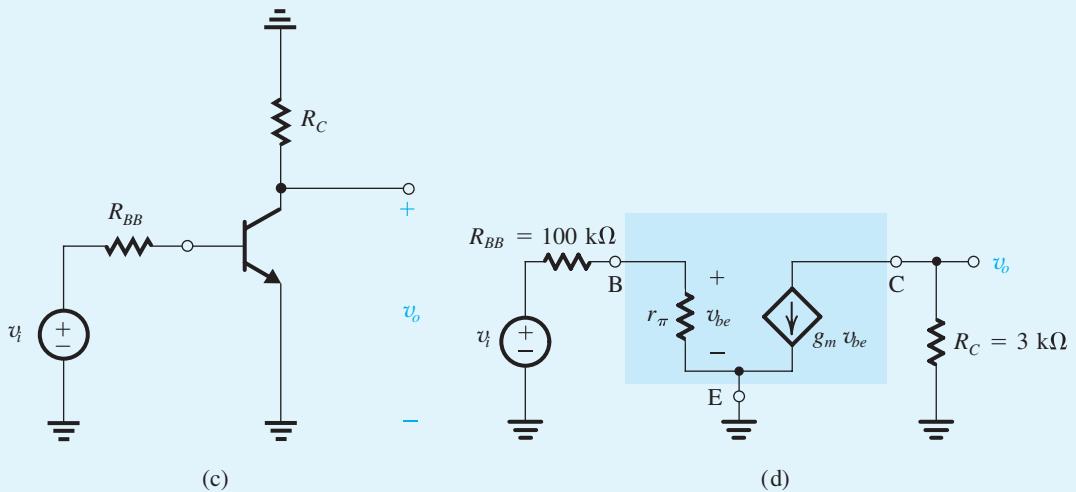


Figure 7.28 continued

**Solution**

We shall follow a five-step process:

1. The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that  $v_i = 0$  and thus obtain the dc circuit shown in Fig. 7.28(b). The dc base current will be

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}}$$

$$\approx \frac{3 - 0.7}{100} = 0.023 \text{ mA}$$

The dc collector current will be

$$I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA}$$

The dc voltage at the collector will be

$$V_C = V_{CC} - I_C R_C$$

$$= +10 - 2.3 \times 3 = +3.1 \text{ V}$$

Since  $V_B$  at  $+0.7 \text{ V}$  is less than  $V_C$ , it follows that in the quiescent condition the transistor will be operating in the active mode. The dc analysis is illustrated in Fig. 7.28(b).

**Example 7.5** *continued*

2. Having determined the operating point, we can now proceed to determine the small-signal model parameters:

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{(2.3/0.99) \text{ mA}} = 10.8 \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega$$

3. Replacing  $V_{BB}$  and  $V_{CC}$  with short circuits results in the circuit in Fig. 7.28(c).  
 4. To carry out the small-signal analysis it is equally convenient to employ either of the two hybrid- $\pi$ , equivalent-circuit models of Fig. 7.24 to replace the transistor in the circuit of Fig. 7.28(c). Using the first results in the amplifier equivalent circuit given in Fig. 7.28(d).  
 5. Analysis of the equivalent circuit in Fig. 7.28(d) proceeds as follows:

$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}}$$

$$= v_i \frac{1.09}{101.09} = 0.011 v_i \quad (7.81)$$

The output voltage  $v_o$  is given by

$$v_o = -g_m v_{be} R_C$$

$$= -92 \times 0.011 v_i \times 3 = -3.04 v_i$$

Thus the voltage gain will be

$$A_v = \frac{v_o}{v_i} = -3.04 \text{ V/V} \quad (7.82)$$

**Example 7.6**

To gain more insight into the operation of transistor amplifiers, we wish to consider the waveforms at various points in the circuit analyzed in the previous example. For this purpose assume that  $v_i$  has a triangular waveform. First determine the maximum amplitude that  $v_i$  is allowed to have. Then, with the amplitude of  $v_i$  set to this value, give the waveforms of the total quantities  $i_B(t)$ ,  $v_{BE}(t)$ ,  $i_C(t)$ , and  $v_C(t)$ .

### Solution

One constraint on signal amplitude is the small-signal approximation, which stipulates that  $v_{be}$  should not exceed about 10 mV. If we take the triangular waveform  $v_{be}$  to be 20 mV peak-to-peak and work backward, Eq. (7.81) can be used to determine the maximum possible peak of  $v_i$ ,

$$\hat{v}_i = \frac{\hat{v}_{be}}{0.011} = \frac{10}{0.011} = 0.91 \text{ V}$$

To check whether the transistor remains in the active mode with  $v_i$  having a peak value  $\hat{v}_i = 0.91 \text{ V}$ , we have to evaluate the collector voltage. The voltage at the collector will consist of a triangular wave  $v_o$  superimposed on the dc value  $V_C = 3.1 \text{ V}$ . The peak voltage of the triangular waveform will be

$$\hat{v}_o = \hat{v}_i \times \text{gain} = 0.91 \times 3.04 = 2.77 \text{ V}$$

It follows that when the output swings negative, the collector voltage reaches a minimum of  $3.1 - 2.77 = 0.33 \text{ V}$ , which is lower than the base voltage by less than 0.4 V. Thus the transistor will remain in the active mode with  $v_i$  having a peak value of 0.91 V. Nevertheless, to be on the safe side, we will use a somewhat lower value for  $\hat{v}_i$  of approximately 0.8 V, as shown in Fig. 7.29(a), and complete the analysis of this problem utilizing the equivalent circuit in Fig. 7.28(d). The signal current in the base will be triangular, with a peak value  $\hat{i}_b$  of

$$\hat{i}_b = \frac{\hat{v}_i}{R_{BB} + r_\pi} = \frac{0.8}{100 + 1.09} = 0.008 \text{ mA}$$

This triangular-wave current will be superimposed on the quiescent base current  $I_B$ , as shown in Fig. 7.29(b). The base-emitter voltage will consist of a triangular-wave component superimposed on the dc  $V_{BE}$  that is approximately 0.7 V. The peak value of the triangular waveform will be

$$\hat{v}_{be} = \hat{v}_i \frac{r_\pi}{r_\pi + R_{BB}} = 0.8 \frac{1.09}{100 + 1.09} = 8.6 \text{ mV}$$

The total  $v_{BE}$  is sketched in Fig. 7.29(c).

The signal current in the collector will be triangular in waveform, with a peak value  $\hat{i}_c$  given by

$$\hat{i}_c = \beta \hat{i}_b = 100 \times 0.008 = 0.8 \text{ mA}$$

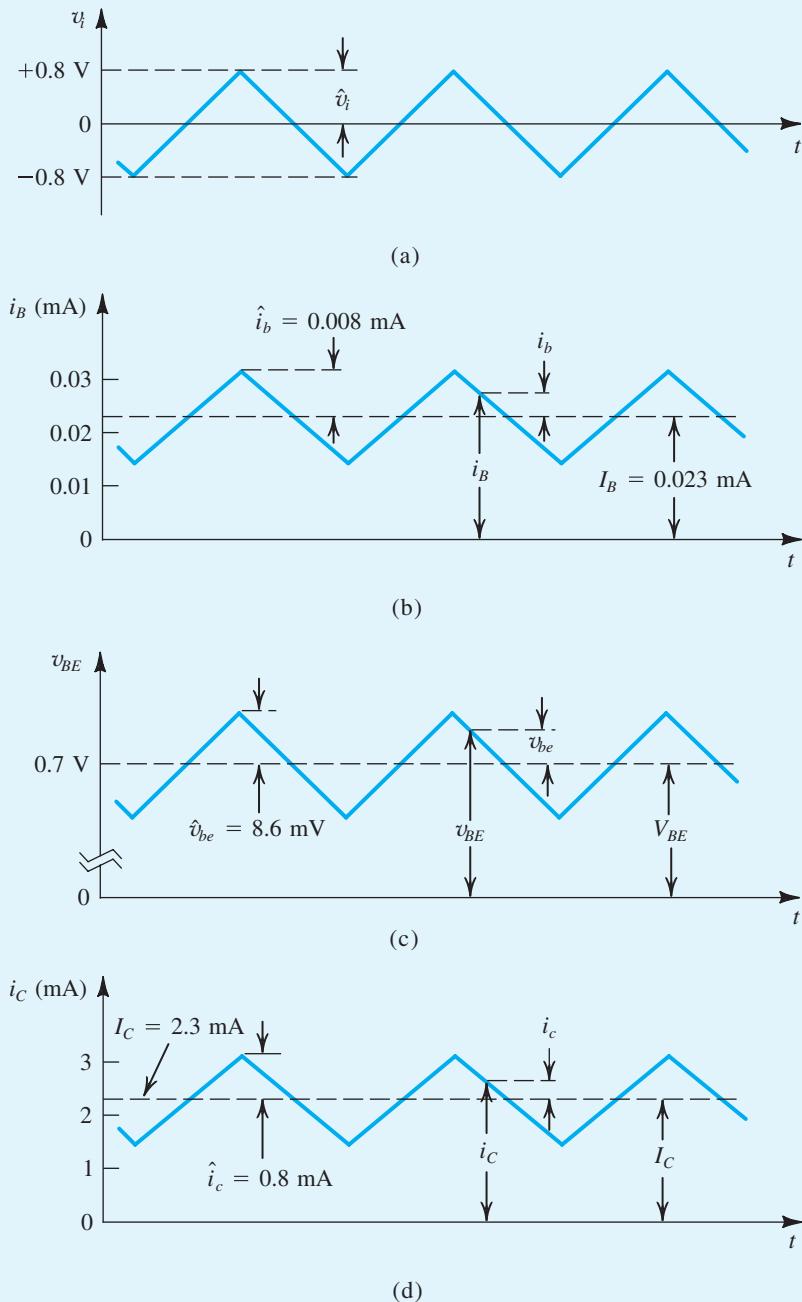
This current will be superimposed on the quiescent collector current  $I_C$  ( $= 2.3 \text{ mA}$ ), as shown in Fig. 7.29(d).

The signal voltage at the collector can be obtained by multiplying  $v_i$  by the voltage gain; that is,

$$\hat{v}_o = 3.04 \times 0.8 = 2.43 \text{ V}$$

Figure 7.29(e) shows a sketch of the total collector voltage  $v_c$  versus time. Note the phase reversal between the input signal  $v_i$  and the output signal  $v_o$ .

Finally, we observe that each of the total quantities is the sum of a dc quantity (found from the dc circuit in Fig. 7.28b), and a signal quantity (found from the circuit in Fig. 7.28d).

**Example 7.6** *continued***Figure 7.29** Signal waveforms in the circuit of Fig. 7.28.

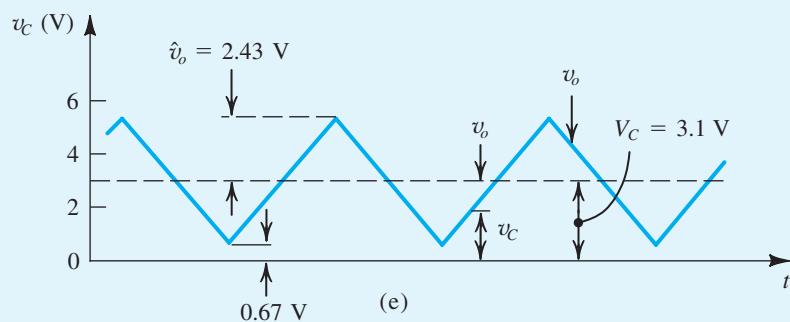
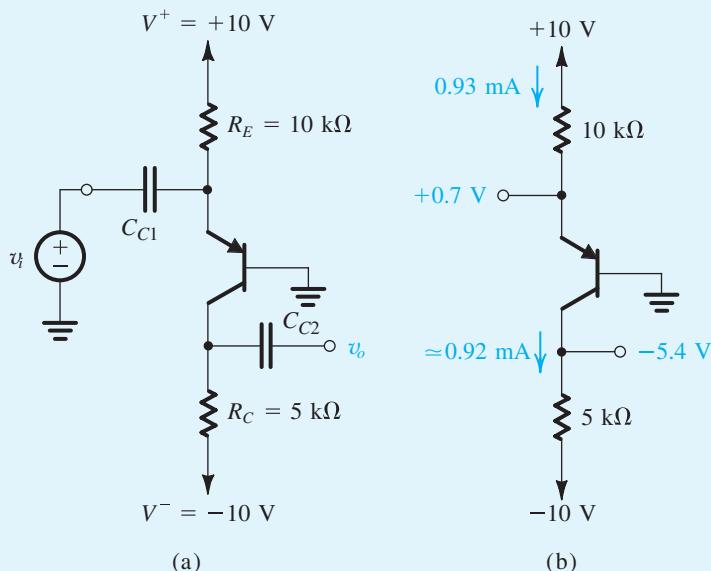


Figure 7.29 continued

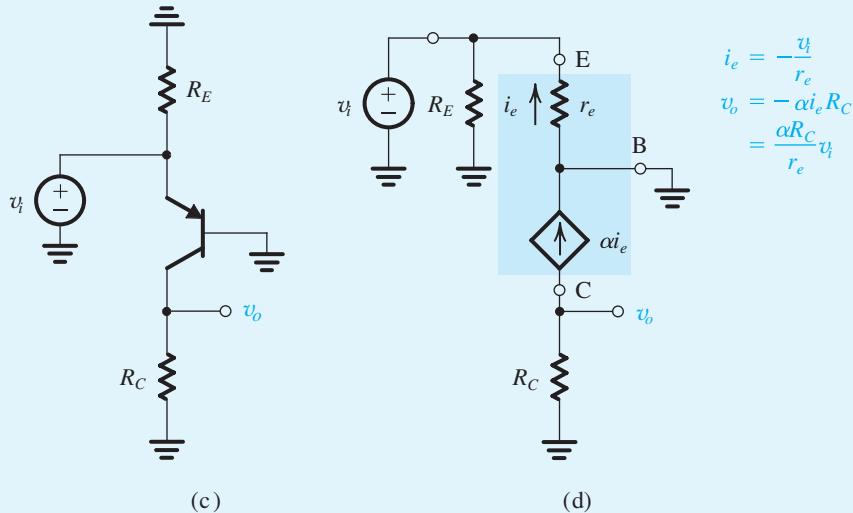
### Example 7.7

We need to analyze the circuit of Fig. 7.30(a) to determine the voltage gain and the signal waveforms at various points. The capacitor  $C_{C1}$  is a coupling capacitor whose purpose is to couple the signal  $v_i$  to the emitter while blocking dc. In this way the dc bias established by  $V^+$  and  $V^-$  together with  $R_E$  and  $R_C$  will



**Figure 7.30** Example 7.7: (a) circuit; (b) dc analysis; (c) circuit with the dc sources eliminated; (d) small-signal analysis using the T model for the BJT.

### Example 7.7 continued



**Figure 7.30** *continued*

not be disturbed when the signal  $v_i$  is connected. For the purpose of this example,  $C_{C1}$  will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor  $C_{C2}$  is used to couple the output signal  $v_o$  to other parts of the system. You may neglect the Early effect.

## Solution

Here again we shall follow a five-step process:

1. Figure 7.30(b) shows the circuit with the signal source and the coupling capacitors eliminated. The dc operating point can be determined as follows:

$$I_E = \frac{+10 - V_E}{R_E} \simeq \frac{+10 - 0.7}{10} = 0.93 \text{ mA}$$

Assuming  $\beta = 100$ , then  $\alpha = 0.99$ , and

$$V_C = -10 + I_C R_C \\ = -10 + 0.92 \times 5 = -5.4 \text{ V}$$

Thus the transistor is in the active mode.

2. We now determine the small-signal parameters as follows:

$$g_m = \frac{I_C}{V_T} = \frac{0.92}{0.025} = 36.8 \text{ mA/V}$$

$$r_e = \frac{V_T}{I_E} = \frac{0.025}{0.92} = 27.2 \Omega$$

$$\beta = 100 \quad \alpha = 0.99$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{36.8} = 2.72 \text{ k}\Omega$$

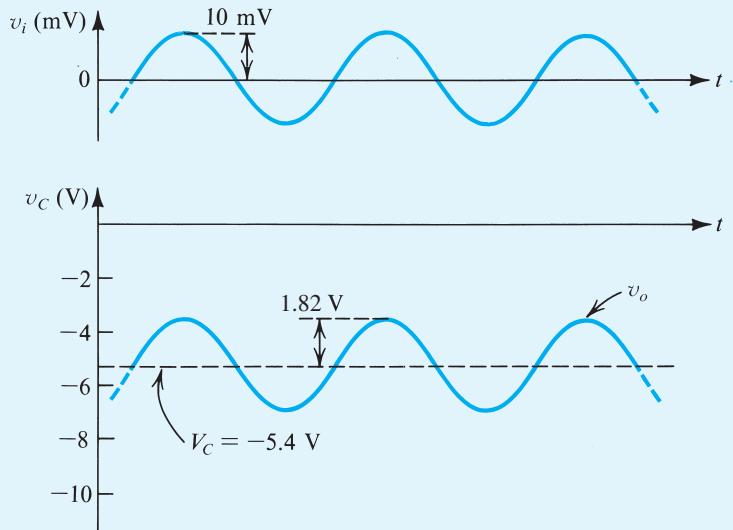
3. To prepare the circuit for small-signal analysis, we replace the dc sources with short circuits. The resulting circuit is shown in Fig. 7.30(c). Observe that we have also eliminated the two coupling capacitors, since they are assumed to be acting as perfect short circuits.
4. We are now ready to replace the BJT with one of the four equivalent-circuit models of Figs. 7.24 and 7.26. Although any of the four will work, the T models of Fig. 7.26 will be more convenient because the base is grounded. Selecting the version in Fig. 7.26(b) results in the amplifier equivalent circuit shown in Fig. 7.30(d).
5. Analysis of the circuit in Fig. 7.30(d) to determine the output voltage  $v_o$  and hence the voltage gain  $v_o/v_i$  is straightforward and is given in the figure. The result is

$$A_v = \frac{v_o}{v_i} = \frac{\alpha R_C}{r_e} = \frac{0.99 \times 5}{0.0272} = 182 \text{ V/V}$$

Note that the voltage gain is positive, indicating that the output is in phase with the input signal. This property is due to the fact that the input signal is applied to the emitter rather than to the base, as was done in Example 7.5. We should emphasize that the positive gain has nothing to do with the fact that the transistor used in this example is of the *pnp* type.

Returning to the question of allowable signal magnitude, we observe from Fig. 7.30(d) that  $v_{eb} = v_i$ . Thus, if small-signal operation is desired (for linearity), then the peak of  $v_i$  should be limited to approximately 10 mV. With  $\hat{V}_i$  set to this value, as shown for a sine-wave input in Fig. 7.31, the peak amplitude at the collector,  $\hat{V}_o$ , will be

$$\hat{V}_o = 182 \times 0.01 = 1.82 \text{ V}$$

**Example 7.7** *continued*

**Figure 7.31** Input and output waveforms for the circuit of Fig. 7.30. Observe that this amplifier is noninverting, a property of the grounded-base configuration.

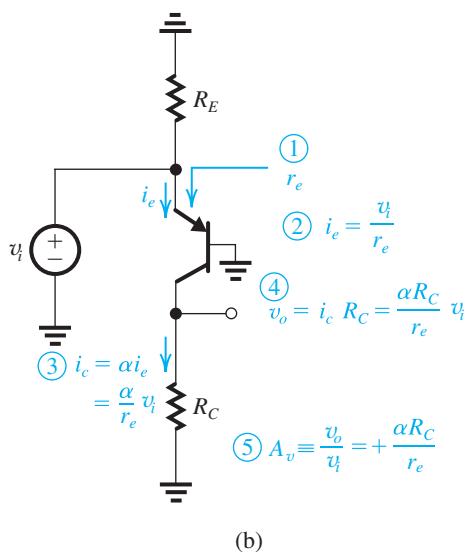
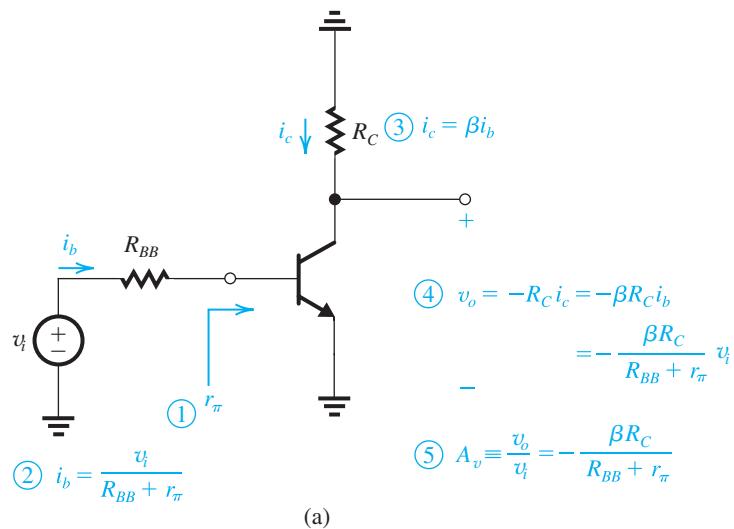
**EXERCISE**

- 7.19** To increase the voltage gain of the amplifier analyzed in Example 7.7, the collector resistance  $R_C$  is increased to  $7.5 \text{ k}\Omega$ . Find the new values of  $V_C$ ,  $A_v$ , and the peak amplitude of the output sine wave corresponding to an input sine wave  $v_i$  of 10-mV peak.

**Ans.**  $-3.1 \text{ V}$ ;  $276 \text{ V/V}$ ;  $2.76 \text{ V}$

**Performing Small-Signal Analysis Directly on the Circuit Diagram** In most cases one should explicitly replace each BJT with its small-signal model and analyze the resulting circuit, as we have done in the examples above. This systematic procedure is particularly recommended for beginning students. Experienced circuit designers, however, often perform a first-order analysis directly on the circuit. Figure 7.32 illustrates this process for the two

circuits we analyzed in Examples 7.5 and 7.7. The reader is urged to follow this direct analysis procedure (the steps are numbered). Observe that the equivalent-circuit model is *implicitly* utilized; we are only saving the step of drawing the circuit with the BJT replaced by its model. Direct analysis, however, has an additional very important benefit: It provides insight regarding the signal transmission through the circuit. Such insight can prove invaluable in design, particularly at the stage of selecting a circuit configuration appropriate for a given application. Direct analysis can be utilized also for MOS amplifier circuits.



**Figure 7.32** Performing signal analysis directly on the circuit diagram with the BJT small-signal model implicitly employed: (a) circuit for Example 7.5; (b) circuit for Example 7.7.

## EXERCISE

**7.20** The transistor in Fig. E7.20 is biased with a constant current source  $I = 1 \text{ mA}$  and has  $\beta = 100$  and  $V_A = 100 \text{ V}$ .

- Neglecting the Early effect, find the dc voltages at the base, emitter, and collector.
- Find  $g_m$ ,  $r_\pi$ , and  $r_o$ .
- If terminal Z is connected to ground, X to a signal source  $v_{\text{sig}}$  with a source resistance  $R_{\text{sig}} = 2 \text{ k}\Omega$ , and Y to an 8-k $\Omega$  load resistance, use the hybrid- $\pi$  model shown earlier (Fig. 7.25) to draw the small-signal equivalent circuit of the amplifier. (Note that the current source  $I$  should be replaced with an open circuit.) Calculate the overall voltage gain  $v_y/v_{\text{sig}}$ . If  $r_o$  is neglected, what is the error in estimating the gain magnitude? (Note: An infinite capacitance is used to indicate that the capacitance is sufficiently large that it acts as a short circuit at all signal frequencies of interest. However, the capacitor still blocks dc.)

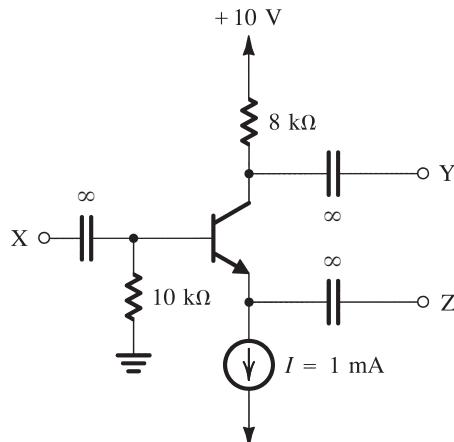


Figure E7.20

**Ans.** (a)  $-0.1 \text{ V}$ ,  $-0.8 \text{ V}$ ,  $+2.1 \text{ V}$ ; (b)  $40 \text{ mA/V}$ ,  $2.5 \text{ k}\Omega$ ,  $100 \text{ k}\Omega$ ; (c)  $-77 \text{ V/V}$ ,  $+3.9\%$

### 7.2.3 Summary Tables

We conclude this section by presenting three useful summary tables: Table 7.1 lists the five steps to be followed in the analysis of a MOSFET or a BJT amplifier circuit. Table 7.2 presents the MOSFET small-signal, equivalent-circuit models, together with the formulas for calculating the parameter values of the models. Finally, Table 7.3 supplies the corresponding data for the BJT.

**Table 7.1** Systematic Procedure for the Analysis of Transistor Amplifier Circuits

1. Eliminate the signal source and determine the dc operating point of the transistor.
2. Calculate the values of the parameters of the small-signal model.
3. Eliminate the dc sources by replacing each dc voltage source by a short circuit and each dc current source by an open circuit.
4. Replace the transistor with one of its small-signal, equivalent-circuit models. Although any of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point will be made clearer in the next section.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance).

**Table 7.2** Small-Signal Models of the MOSFET*Small-Signal Parameters***NMOS transistors****■ Transconductance:**

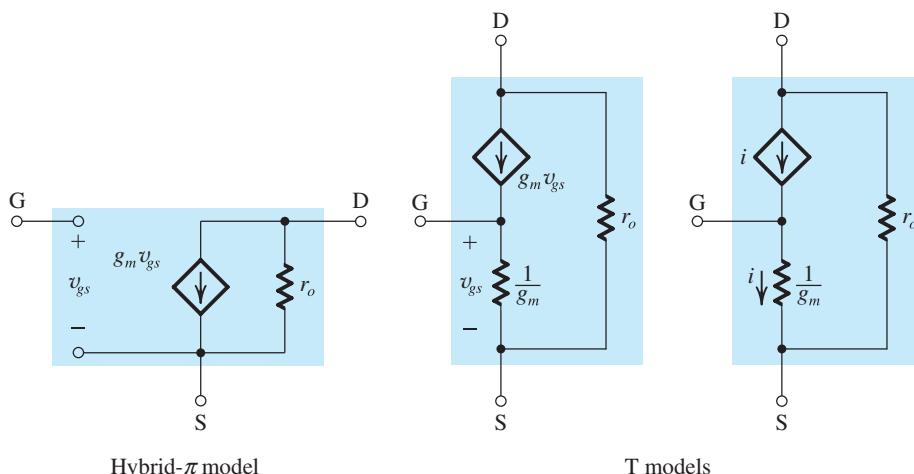
$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ov} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{ov}}$$

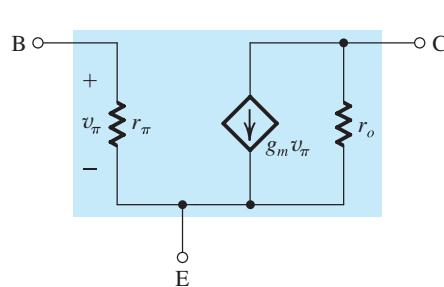
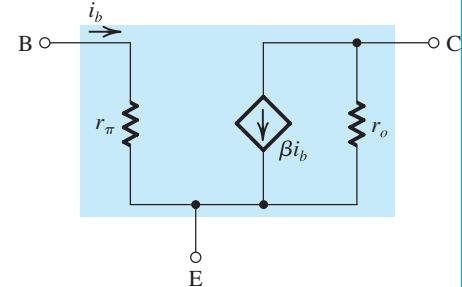
**■ Output resistance:**

$$r_o = V_A/I_D = 1/\lambda I_D$$

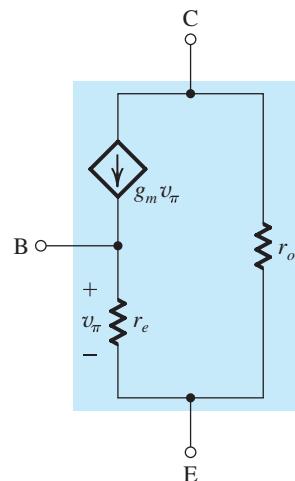
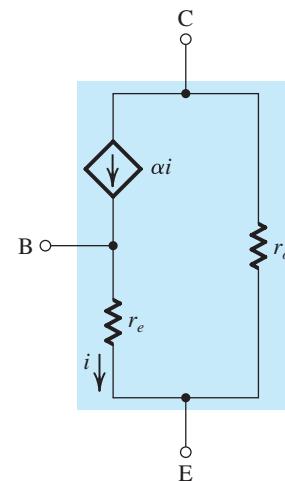
**PMOS transistors**

Same formulas as for NMOS *except* using  $|V_{ov}|$ ,  $|V_A|$ ,  $|\lambda|$  and replacing  $\mu_n$  with  $\mu_p$ .

*Small-Signal, Equivalent-Circuit Models*

**Table 7.3** Small-Signal Models of the BJTHybrid- $\pi$  Model■ ( $g_m v_\pi$ ) Version■ ( $\beta i_b$ ) Version

T Model

■ ( $g_m v_\pi$ ) Version■ ( $\alpha i$ ) Version

Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T}$$

$$r_e = \frac{V_T}{I_E} = \alpha \frac{V_T}{I_C}$$

$$r_\pi = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C}$$

$$r_o = \frac{|V_A|}{I_C}$$

In Terms of  $g_m$ 

$$r_e = \frac{\alpha}{g_m}$$

$$r_\pi = \frac{\beta}{g_m}$$

In Terms of  $r_e$ 

$$g_m = \frac{\alpha}{r_e}$$

$$r_\pi = (\beta + 1)r_e$$

$$g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships between  $\alpha$  and  $\beta$ 

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta + 1 = \frac{1}{1 - \alpha}$$

## 7.3 Basic Configurations

It is useful at this point to take stock of where we are and where we are going in our study of transistor amplifiers. In Section 7.1 we examined the underlying principle for the application of the MOSFET, and of the BJT, as an amplifier. There we found that almost-linear amplification can be obtained by dc biasing the transistor at an appropriate point in its active region of operation, and by keeping the input signal ( $v_{gs}$  or  $v_{be}$ ) small. We then developed, in Section 7.2, circuit models that represent the small-signal operation of each of the two transistor types (Tables 7.2 and 7.3), thus providing a systematic procedure (Table 7.1) for the analysis of transistor amplifiers.

We are now ready to consider the various possible configurations of MOSFET and BJT amplifiers, and we will do that in the present section. To focus our attention on the salient features of the various configurations, we shall present them in their most simple, or “stripped-down,” version. Thus, we will not show the dc biasing arrangements, leaving the study of bias design to the next section. Finally, in Section 7.5 we will bring everything together and present practical *discrete-circuit amplifiers*, namely, amplifier circuits that can be constructed using discrete components. The study of integrated-circuit amplifiers begins in Chapter 8.

### 7.3.1 The Three Basic Configurations

There are three basic configurations for connecting a MOSFET or a BJT as an amplifier. Each of these configurations is obtained by connecting one of the device terminals to ground, thus creating a two-port network with the grounded terminal being *common* to the input and output ports. The resulting configurations are shown in Fig. 7.33(a–c) for the MOSFET and in Fig. 7.33(d–f) for the BJT.

In the circuit of Fig. 7.33(a) the source terminal is connected to ground, the input voltage signal  $v_i$  is applied between the gate and ground, and the output voltage signal  $v_o$  is taken between the drain and ground, across the resistance  $R_D$ . This configuration, therefore, is called the **grounded-source or common-source (CS)** amplifier. It is by far the most popular MOS amplifier configuration, and we utilized it in Sections 7.1 and 7.2 to study MOS amplifier operation. A parallel set of remarks apply to the BJT counterpart, the **grounded-emitter or common-emitter (CE)** amplifier in Fig. 7.33(d).

The **common-gate (CG)** or grounded-gate amplifier is shown in Fig. 7.33(b), and its BJT counterpart, the **common-base (CB)** or grounded-base amplifier in Fig. 7.33(e). Here the gate (base) is grounded, the input signal  $v_i$  is applied to the source (emitter), and the output signal  $v_o$  is taken at the drain (collector) across the resistance  $R_D$  ( $R_C$ ). We encountered a CG amplifier in Example 7.4 and a CB amplifier in Example 7.7.

Finally, Fig. 7.33(c) shows the **common drain (CD)** or grounded-drain amplifier, and Fig. 7.33(f) shows its BJT counterpart, the **common-collector (CC)** or grounded collector amplifier. Here the drain (collector) terminal is grounded, the input signal  $v_i$  is applied between gate (base) and ground, and the output voltage  $v_o$  is taken between the source (emitter) and ground, across a resistance  $R_L$ . For reasons that will become apparent shortly, this pair of configurations is more commonly called the **source follower** and the **emitter follower**.

Our study of the three basic amplifier configurations of the MOSFET and of the BJT will reveal that each has distinctly different attributes, hence areas of application. As well, it will be shown that although each pair of configurations, (e.g., CS and CE), has many common attributes, important differences remain.

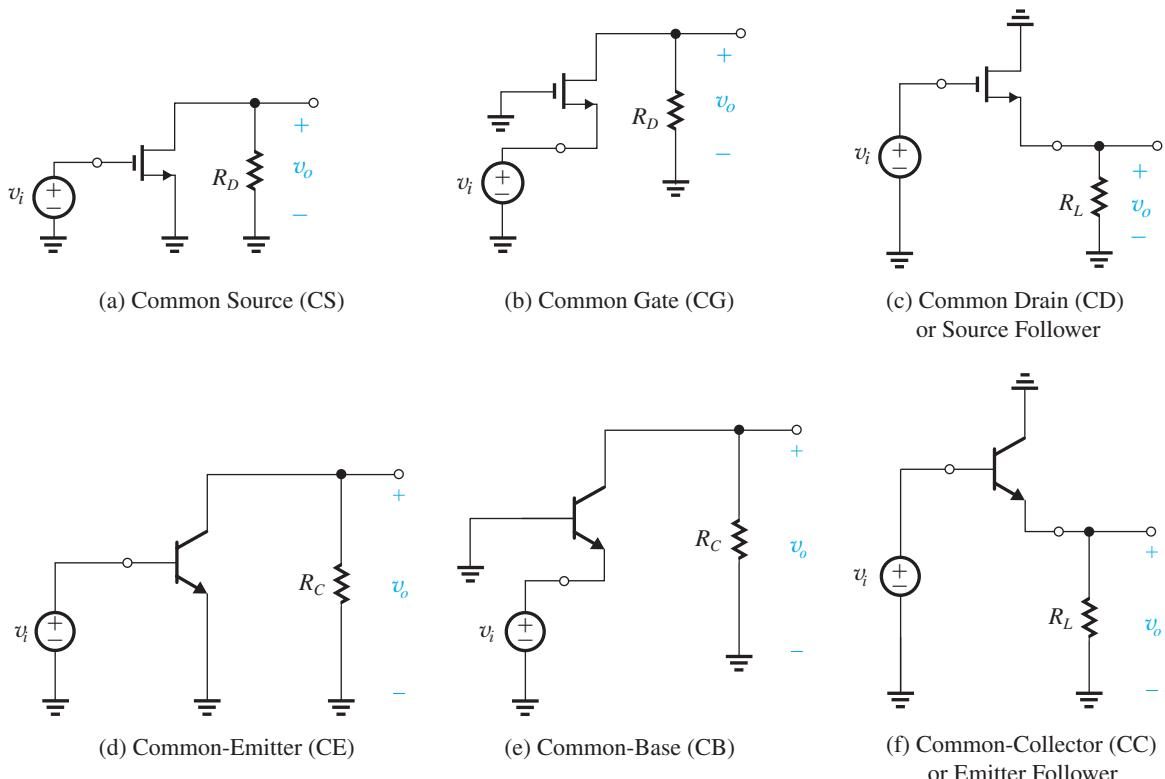


Figure 7.33 The basic configurations of transistor amplifiers. (a)–(c) For the MOSFET; (d)–(f) for the BJT.

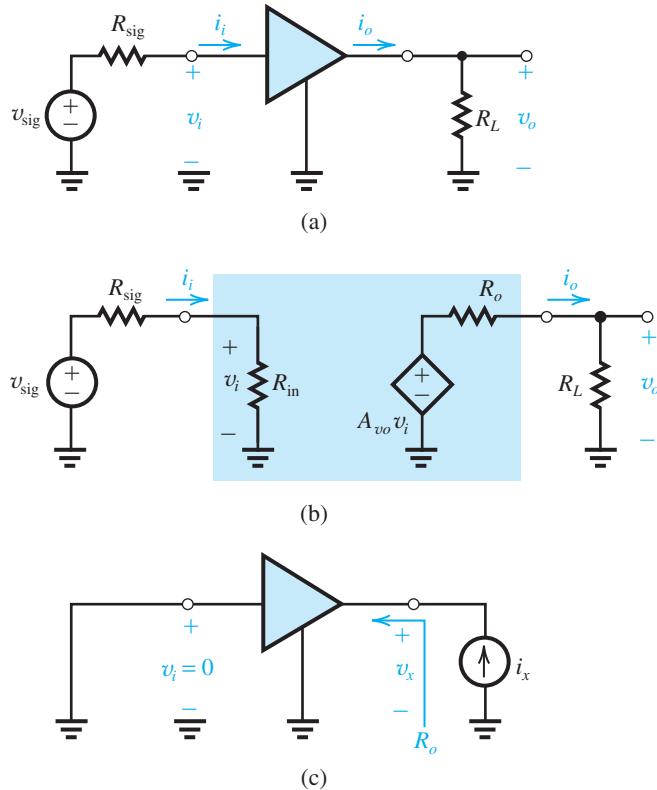
Our next step is to replace the transistor in each of the six circuits in Fig. 7.33 by an appropriate equivalent-circuit model (from Tables 7.2 and 7.3) and analyze the resulting circuits to determine important characteristic parameters of the particular amplifier configuration. To simplify matters, we shall not include  $r_o$  in the initial analysis. At the end of the section we will offer a number of comments about when to include  $r_o$  in the analysis, and on the expected magnitude of its effect.

### 7.3.2 Characterizing Amplifiers

Before we begin our study of the different transistor amplifier configurations, we consider how to characterize the performance of an amplifier as a circuit building block. An introduction to this topic was presented in Section 1.5.

Figure 7.34(a) shows an amplifier fed with a signal source having an open-circuit voltage  $v_{\text{sig}}$  and an internal resistance  $R_{\text{sig}}$ . These can be the parameters of an actual signal source or, in a cascade amplifier, the Thévenin equivalent of the output circuit of another amplifier stage preceding the one under study. The amplifier is shown with a load resistance  $R_L$  connected to the output terminal. Here,  $R_L$  can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

Figure 7.34(b) shows the amplifier circuit with the amplifier block replaced by its equivalent-circuit model. The input resistance  $R_{\text{in}}$  represents the loading effect of the amplifier



**Figure 7.34** Characterization of the amplifier as a functional block: (a) An amplifier fed with a voltage signal  $v_{\text{sig}}$  having a source resistance  $R_{\text{sig}}$ , and feeding a load resistance  $R_L$ ; (b) equivalent-circuit representation of the circuit in (a); (c) determining the amplifier output resistance  $R_o$ .

input on the signal source. It is found from

$$R_{\text{in}} \equiv \frac{v_i}{i_i}$$

and together with the resistance  $R_{\text{sig}}$  forms a voltage divider that reduces  $v_{\text{sig}}$  to the value  $v_i$  that appears at the amplifier input,

$$v_i = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} v_{\text{sig}} \quad (7.83)$$

Most of the amplifier circuits studied in this section are **unilateral**. That is, they do not contain internal feedback, and thus  $R_{\text{in}}$  will be independent of  $R_L$ . However, in general  $R_{\text{in}}$  may depend on the load resistance  $R_L$ . Indeed one of the six configurations studied in this section, the emitter follower, exhibits such dependence.

The second parameter in characterizing amplifier performance is the **open-circuit voltage gain**  $A_{vo}$ , defined as

$$A_{vo} \equiv \left. \frac{v_o}{v_i} \right|_{R_L=\infty}$$

The third and final parameter is the output resistance  $R_o$ . Observe from Fig. 7.34(b) that  $R_o$  is the resistance seen looking back into the amplifier output terminal with  $v_i$  set to zero. Thus  $R_o$  can be determined, at least conceptually, as indicated in Fig. 7.34(c) with

$$R_o = \frac{v_x}{i_x}$$

Because  $R_o$  is determined with  $v_i = 0$ , the value of  $R_o$  does not depend on  $R_{\text{sig}}$ .

The controlled source  $A_{vo}v_i$  and the output resistance  $R_o$  represent the Thévenin equivalent of the amplifier output circuit, and the output voltage  $v_o$  can be found from

$$v_o = \frac{R_L}{R_L + R_o} A_{vo} v_i \quad (7.84)$$

Thus the **voltage gain of the amplifier proper**,  $A_v$ , can be found as

➤  $A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \quad (7.85)$

and the **overall voltage gain**,  $G_v$ ,

$$G_v \equiv \frac{v_o}{v_{\text{sig}}}$$

can be determined by combining Eqs. (7.83) and (7.85):

➤  $G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_{vo} \frac{R_L}{R_L + R_o} \quad (7.86)$

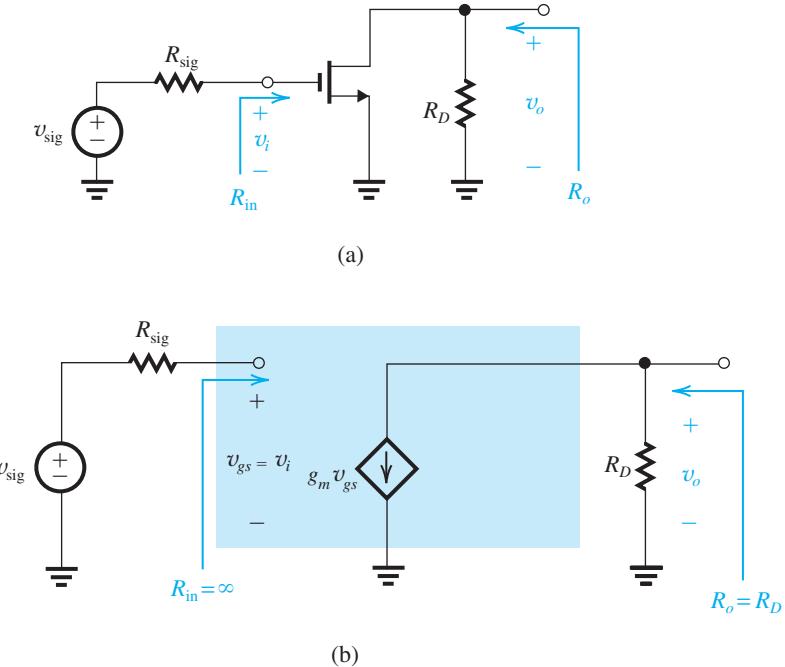
### 7.3.3 The Common-Source (CS) and Common-Emitter (CE) Amplifiers

Of the three basic transistor amplifier configurations, the common-source (common-emitter, for BJT), is the most widely used. Typically, in an amplifier formed by cascading a number of gain stages, the bulk of the voltage gain is obtained by using one or more common-source (or common-emitter, for BJT) stages in cascade.

**Characteristic Parameters of the CS Amplifier** Figure 7.35(a) shows a common-source amplifier (with the biasing arrangement omitted) fed with a signal source  $v_{\text{sig}}$  having a source resistance  $R_{\text{sig}}$ . We wish to analyze this circuit to determine  $R_{\text{in}}$ ,  $A_{vo}$ , and  $R_o$ . For this purpose, we assume that  $R_D$  is part of the amplifier; thus if a load resistance  $R_L$  is connected to the amplifier output,  $R_L$  appears in parallel with  $R_D$ . In such a case, we wish to determine  $A_v$  and  $G_v$  as well.

Replacing the MOSFET with its hybrid- $\pi$  model (without  $r_o$ ), we obtain the CS amplifier equivalent circuit in Fig. 7.35(b) for which, tracing the signal from input to output, we can write by inspection

$$\begin{aligned} R_{\text{in}} &= \infty \\ v_i &= v_{\text{sig}} \\ v_{gs} &= v_i \\ v_o &= -g_m v_{gs} R_D \end{aligned} \quad (7.87)$$



**Figure 7.35** (a) Common-source amplifier fed with a signal  $v_{\text{sig}}$  from a generator with a resistance  $R_{\text{sig}}$ . The bias circuit is omitted. (b) The common-source amplifier with the MOSFET replaced with its hybrid- $\pi$  model.

Thus,

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_m R_D \quad (7.88)$$

$$R_o = R_D \quad (7.89)$$

If a load resistance  $R_L$  is connected across  $R_D$ , the voltage gain  $A_v$  can be obtained from

$$A_v = A_{vo} \frac{R_L}{R_L + R_o} \quad (7.90)$$

where  $A_{vo}$  is given by Eq. (7.88) and  $R_o$  by Eq. (7.89), or alternatively by simply adding  $R_L$  in parallel with  $R_D$  in Eq. (7.88), thus

$$A_v = -g_m (R_D \parallel R_L) \quad (7.91)$$

The reader can easily show that the expression obtained from Eq. (7.90) is identical to that in Eq. (7.91). Finally, since  $R_{\text{in}} = \infty$  and thus  $v_i = v_{\text{sig}}$ , the overall voltage gain  $G_v$  is equal to  $A_v$ ,

$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = -g_m (R_D \parallel R_L) \quad (7.92)$$

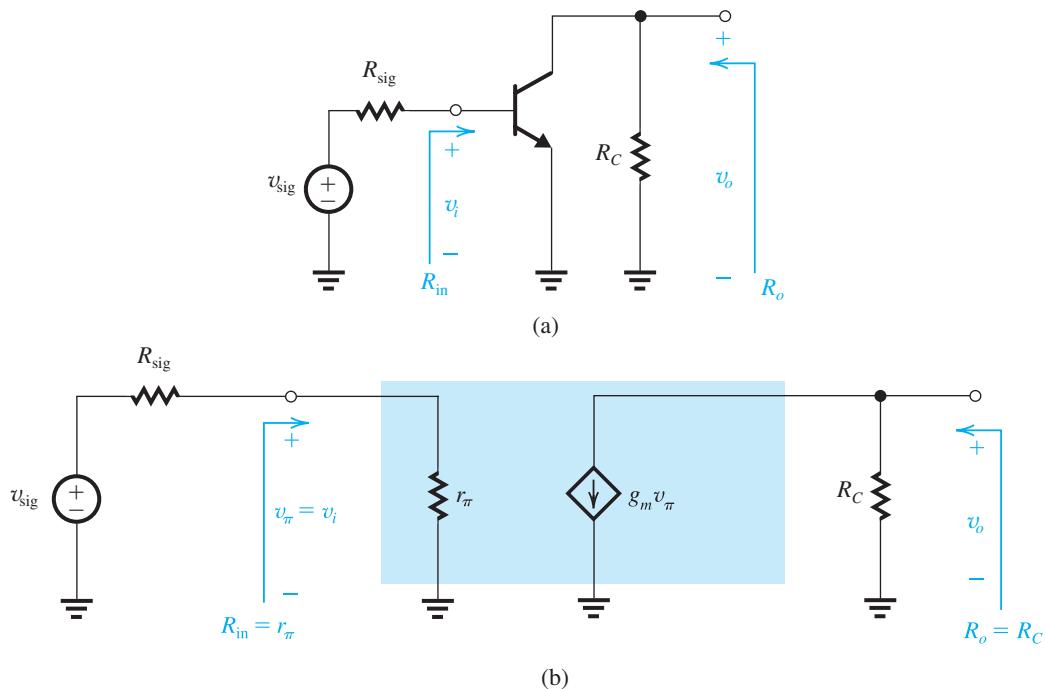
## EXERCISE

- 7.21** A CS amplifier utilizes a MOSFET biased at  $I_D = 0.25$  mA with  $V_{OV} = 0.25$  V and  $R_D = 20$  k $\Omega$ . The amplifier is fed with a signal source having  $R_{sig} = 100$  k $\Omega$ , and a 20-k $\Omega$  load is connected to the output. Find  $R_{in}$ ,  $A_{vo}$ ,  $R_o$ ,  $A_v$ , and  $G_v$ . If, to maintain reasonable linearity, the peak of the input sine-wave signal is limited to 10% of  $2V_{OV}$ , what is the peak of the sine-wave voltage at the output?

**Ans.**  $\infty$ ; -40 V/V; 20 k $\Omega$ ; -20 V/V; -20 V/V; 1 V

**Characteristic Parameters of the CE Amplifier** Figure 7.36(a) shows a common-emitter amplifier. Its equivalent circuit, obtained by replacing the BJT with its hybrid- $\pi$  model (without  $r_o$ ), is shown in Fig. 7.36(b). The latter circuit can be analyzed to obtain the characteristic parameters of the CE amplifier. The analysis parallels that for the MOSFET above except that here we have the added complexity of a finite input resistance  $r_\pi$ . Tracing the signal through the amplifier from input to output, we can write by inspection

$$R_{in} = r_\pi$$



**Figure 7.36** (a) Common-emitter amplifier fed with a signal  $v_{sig}$  from a generator with a resistance  $R_{sig}$ . The bias circuit is omitted. (b) The common-emitter amplifier circuit with the BJT replaced by its hybrid- $\pi$  model.

Then we write

$$v_i = \frac{r_\pi}{r_\pi + R_{\text{sig}}} v_{\text{sig}} \quad (7.93)$$

$$\begin{aligned} v_\pi &= v_i \\ v_o &= -g_m v_\pi R_C \end{aligned}$$

Thus,

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_m R_C \quad (7.94)$$

$$R_o = R_C \quad (7.95)$$

With a load resistance  $R_L$  connected across  $R_C$ ,

$$A_v = -g_m (R_C \parallel R_L) \quad (7.96)$$

and the overall voltage gain  $G_v$  can be found from

$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = \frac{v_i}{v_{\text{sig}}} \frac{v_o}{v_i}$$

Thus,

$$G_v = -\frac{r_\pi}{r_\pi + R_{\text{sig}}} g_m (R_C \parallel R_L) \quad (7.97)$$

It is important to note here the effect of the finite input resistance ( $r_\pi$ ) in reducing the magnitude of the voltage gain by the voltage-divider ratio  $r_\pi/(r_\pi + R_{\text{sig}})$ . The extent of the gain reduction depends on the relative values of  $r_\pi$  and  $R_{\text{sig}}$ . However, there is a compensating effect in the CE amplifier:  $g_m$  of the BJT is usually much higher than the corresponding value of the MOSFET.

### Example 7.8

A CE amplifier utilizes a BJT with  $\beta = 100$  is biased at  $I_C = 1 \text{ mA}$  and has a collector resistance  $R_C = 5 \text{ k}\Omega$ . Find  $R_{\text{in}}$ ,  $R_o$ , and  $A_{vo}$ . If the amplifier is fed with a signal source having a resistance of  $5 \text{ k}\Omega$ , and a load resistance  $R_L = 5 \text{ k}\Omega$  is connected to the output terminal, find the resulting  $A_v$  and  $G_v$ . If  $\hat{v}_\pi$  is to be limited to  $5 \text{ mV}$ , what are the corresponding  $\hat{v}_{\text{sig}}$  and  $\hat{v}_o$  with the load connected?

#### Solution

At  $I_C = 1 \text{ mA}$ ,

$$\begin{aligned} g_m &= \frac{I_C}{V_T} = \frac{1 \text{ mA}}{0.025 \text{ V}} = 40 \text{ mA/V} \\ r_\pi &= \frac{\beta}{g_m} = \frac{100}{40 \text{ mA/V}} = 2.5 \text{ k}\Omega \end{aligned}$$

**Example 7.8** *continued*

The amplifier characteristic parameters can now be found as

$$\begin{aligned} R_{\text{in}} &= r_{\pi} = 2.5 \text{ k}\Omega \\ A_{vo} &= -g_m R_C \\ &= -40 \text{ mA/V} \times 5 \text{ k}\Omega \\ &= -200 \text{ V/V} \\ R_o &= R_C = 5 \text{ k}\Omega \end{aligned}$$

With a load resistance  $R_L = 5 \text{ k}\Omega$  connected at the output, we can find  $A_v$  by either of the following two approaches:

$$\begin{aligned} A_v &= A_{vo} \frac{R_L}{R_L + R_o} \\ &= -200 \times \frac{5}{5+5} = -100 \text{ V/V} \end{aligned}$$

or

$$\begin{aligned} A_v &= -g_m (R_C \parallel R_L) \\ &= -40(5 \parallel 5) = -100 \text{ V/V} \end{aligned}$$

The overall voltage gain  $G_v$  can now be determined as

$$\begin{aligned} G_v &= \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_v \\ &= \frac{2.5}{2.5+5} \times -100 = -33.3 \text{ V/V} \end{aligned}$$

If the maximum amplitude of  $v_{\pi}$  is to be 5 mV, the corresponding value of  $\hat{v}_{\text{sig}}$  will be

$$\hat{v}_{\text{sig}} = \left( \frac{R_{\text{in}} + R_{\text{sig}}}{R_{\text{in}}} \right) \hat{v}_{\pi} = \frac{2.5 + 5}{2.5} \times 5 = 15 \text{ mV}$$

and the amplitude of the signal at the output will be

$$\hat{v}_o = G_v \hat{v}_{\text{sig}} = 33.3 \times 0.015 = 0.5 \text{ V}$$

**EXERCISE**

- 7.22** The designer of the amplifier in Example 7.8 decides to lower the bias current to half its original value in order to raise the input resistance and hence increase the fraction of  $v_{\text{sig}}$  that appears at the input of the amplifier proper. In an attempt to maintain the voltage gain, the designer decides to double the value of  $R_C$ . For the new design, determine  $R_{\text{in}}$ ,  $A_{vo}$ ,  $R_o$ ,  $A_v$ , and  $G_v$ . If the peak amplitude of  $v_\pi$  is to be limited to 5 mV, what are the corresponding values of  $\hat{v}_{\text{sig}}$  and  $\hat{v}_o$  (with the load connected)?

**Ans.** 5 k $\Omega$ ; -200 V/V; 10 k $\Omega$ ; -66.7 V/V; -33.3 V/V; 10 mV; 0.33 V

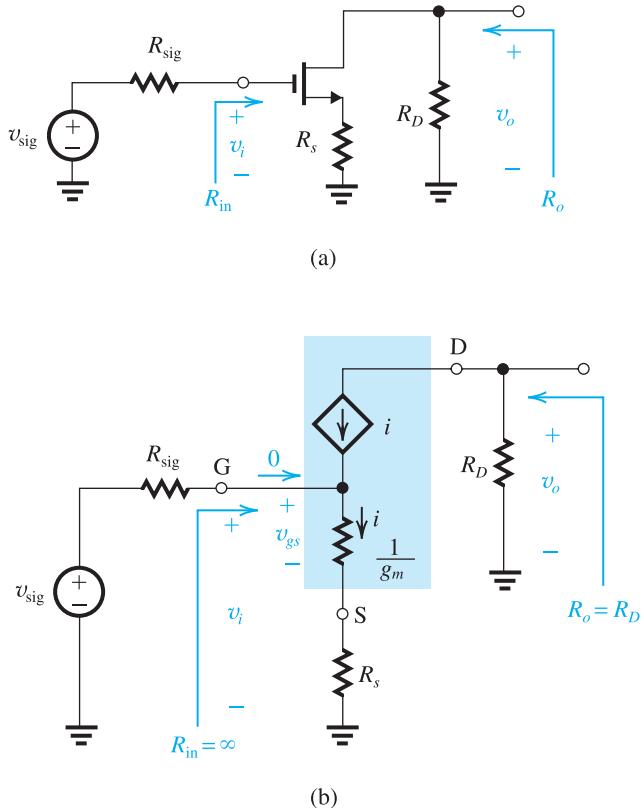
*Comment:* Although a larger fraction of the input signal reaches the amplifier input, linearity considerations cause the output signal to be in fact smaller than in the original design!

**Final Remarks**

1. The CS and CE amplifiers are the most useful of all transistor amplifier configurations. They exhibit a moderate to high input resistance (infinite for the CS), a moderate to high output resistance, and reasonably high voltage gain.
2. The input resistance of the CE amplifier,  $R_{\text{in}} = r_\pi = \beta/g_m$ , is inversely proportional to the dc bias current  $I_C$ . To increase  $R_{\text{in}}$  one is tempted to lower the bias current  $I_C$ ; however, this also lowers  $g_m$  and hence the voltage gain. This is a significant design trade-off. If a much higher input resistance is desired, then a modification of the CE configuration (to be discussed in Section 7.3.4) can be applied, or an emitter-follower stage can be inserted between the signal source and the CE amplifier (see Section 7.3.6).
3. Reducing  $R_D$  or  $R_C$  to lower the output resistance of the CS or CE amplifier, respectively, is usually not a viable proposition because the voltage gain is also reduced. Alternatively, if a very low output resistance (in the ohms or tens-of-ohms range) is needed, a source-follower or an emitter-follower stage can be utilized between the output of the CS or CE amplifier and the load resistance (see Section 7.3.6).
4. Although the CS and the CE configurations are the workhorses of transistor amplifiers, both suffer from a limitation on their high-frequency response. As will be shown in Chapter 10, combining the CS (CE) amplifier with a CG (CB) amplifier can extend the bandwidth considerably. The CG and CB amplifiers are studied in Section 7.3.5.

### 7.3.4 The Common-Source (Common-Emitter) Amplifier with a Source (Emitter) Resistance

It is often beneficial to insert a resistance  $R_s$  (a resistance  $R_e$ ) in the source lead (the emitter lead) of a common-source (common-emitter) amplifier. Figure 7.37(a) shows a CS amplifier with a resistance  $R_s$  in its source lead. The corresponding small-signal equivalent circuit is shown



**Figure 7.37** The CS amplifier with a source resistance  $R_s$ : (a) circuit without bias details; (b) equivalent circuit with the MOSFET represented by its T model.

in Fig. 7.37(b), where we have utilized the T model for the MOSFET. The T model is used in preference to the hybrid- $\pi$  model because it makes the analysis in this case considerably simpler. In general, whenever a resistance is connected in the source lead, the T model is preferred. The source resistance then simply appears in series with the model resistance  $1/g_m$  and can be added to it.

From Fig. 7.37(b) we see that as expected, the input resistance  $R_{\text{in}}$  is infinite and thus  $v_i = v_{\text{sig}}$ . Unlike the CS amplifier, however, here only a fraction of  $v_i$  appears between gate and source as  $v_{gs}$ . The voltage divider composed of  $1/g_m$  and  $R_s$ , which appears across the amplifier input, can be used to determine  $v_{gs}$ , as follows:

$$v_{gs} = v_i \frac{1/g_m}{1/g_m + R_s} = \frac{v_i}{1 + g_m R_s} \quad (7.98)$$

Thus we can use the value of  $R_s$  to control the magnitude of the signal  $v_{gs}$  and thereby ensure that  $v_{gs}$  does not become too large and cause unacceptably high nonlinear distortion. This is the first benefit of including resistor  $R_s$ . Other benefits will be encountered in later sections and chapters. For instance, it will be shown in Chapter 10 that  $R_s$  causes the useful bandwidth of the amplifier to be extended. The mechanism by which  $R_s$  causes such improvements in amplifier performance is *negative feedback*. To see how  $R_s$  introduces negative feedback, refer to Fig. 7.37(a): If with  $v_{\text{sig}}$  and hence  $v_i$  kept constant, the drain current increases for some

reason, the source current also will increase, resulting in an increased voltage drop across  $R_s$ . Thus the source voltage rises, and the gate-to-source voltage decreases. The latter effect causes the drain current to decrease, counteracting the initially assumed change, an indication of the presence of negative feedback. In Chapter 11 we shall study negative feedback formally. There we will learn that the improvements that negative feedback provides are obtained at the expense of a reduction in gain. We will now show this to be the case in the circuit of Fig. 7.37.

The output voltage  $v_o$  is obtained by multiplying the controlled-source current  $i$  by  $R_D$ ,

$$v_o = -iR_D$$

The current  $i$  in the source lead can be found by dividing  $v_i$  by the total resistance in the source,

$$i = \frac{v_i}{1/g_m + R_s} = \left( \frac{g_m}{1 + g_m R_s} \right) v_i \quad (7.99)$$

Thus, the voltage gain  $A_{vo}$  can be found as

$$A_{vo} \equiv \frac{v_o}{v_i} = -\frac{g_m R_D}{1 + g_m R_s} \quad (7.100)$$

which can also be expressed as

$$A_{vo} = -\frac{R_D}{1/g_m + R_s} \quad (7.101)$$

Equation (7.100) indicates that including the resistance  $R_s$  reduces the voltage gain by the factor  $(1 + g_m R_s)$ . This is the price paid for the improvements that accrue as a result of  $R_s$ . It is interesting to note that in Chapter 11, we will find that the factor  $(1 + g_m R_s)$  is the “amount of negative feedback” introduced by  $R_s$ . It is also the same factor by which linearity, bandwidth, and other performance parameters improve. Because of the negative-feedback action of  $R_s$  it is known as a **source-degeneration resistance**.

There is another useful interpretation of the expression for the drain current in Eq. (7.99): The quantity between brackets on the right-hand side can be thought of as the “effective transconductance with  $R_s$  included.” Thus, including  $R_s$  reduces the transconductance by the factor  $(1 + g_m R_s)$ . This, of course, is simply the result of the fact that only a fraction  $1/(1 + g_m R_s)$  of  $v_i$  appears as  $v_{gs}$  (see Eq. 7.98).

The alternative gain expression in Eq. (7.101) has a powerful and insightful interpretation: The voltage gain between gate and drain is equal to the ratio of the total resistance in the drain ( $R_D$ ) to the total resistance in the source ( $1/g_m + R_s$ ),

$$\text{Voltage gain from gate to drain} = -\frac{\text{Total resistance in drain}}{\text{Total resistance in source}} \quad (7.102)$$

This is a general expression. For instance, setting  $R_s = 0$  in Eq. (7.101) yields  $A_{vo}$  of the CS amplifier.

Finally, we consider the situation of a load resistance  $R_L$  connected at the output. We can obtain the gain  $A_v$  using the open-circuit voltage gain  $A_{vo}$  together with the output resistance  $R_o$ , which can be found by inspection to be

$$R_o = R_D$$

Alternatively,  $A_v$  can be obtained by simply replacing  $R_D$  in Eq. (7.101) or (7.100) by  $(R_D \parallel R_L)$ ; thus,

➤

$$A_v = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_s} \quad (7.103)$$

or

➤

$$A_v = -\frac{R_D \parallel R_L}{1/g_m + R_s} \quad (7.104)$$

Observe that Eq. (7.104) is a direct application of the ratio of total resistance rule of Eq. (7.102). Finally, note that because  $R_{in}$  is infinite,  $v_i = v_{sig}$  and the overall voltage gain  $G_v$  is equal to  $A_v$ .

### EXERCISE

- 7.23** In Exercise 7.21 we applied an input signal  $v_{sig}$  of 50 mV peak and obtained an output signal of approximately 1 V peak. Assume that for some reason we now have an input signal  $v_{sig}$  that is 0.2 V peak and that we wish to modify the circuit to keep  $v_{gs}$  unchanged, and thus keep the nonlinear distortion from increasing. What value should we use for  $R_s$ ? What value of  $G_v$  will result? What will the peak signal at the output become? Assume  $r_o = \infty$ .

**Ans.** 1.5 kΩ; -5 V/V; 1 V

We next turn our attention to the BJT case. Figure 7.38(a) shows a CE amplifier with a resistance  $R_e$  in its emitter. The corresponding equivalent circuit, utilizing the T model, is shown in Fig. 7.38(b). Note that in the BJT case also, as a general rule, the T model results in a simpler analysis and should be employed whenever there is a resistance in series with the emitter.

To determine the amplifier input resistance  $R_{in}$ , we note from Fig. 7.38(b) that

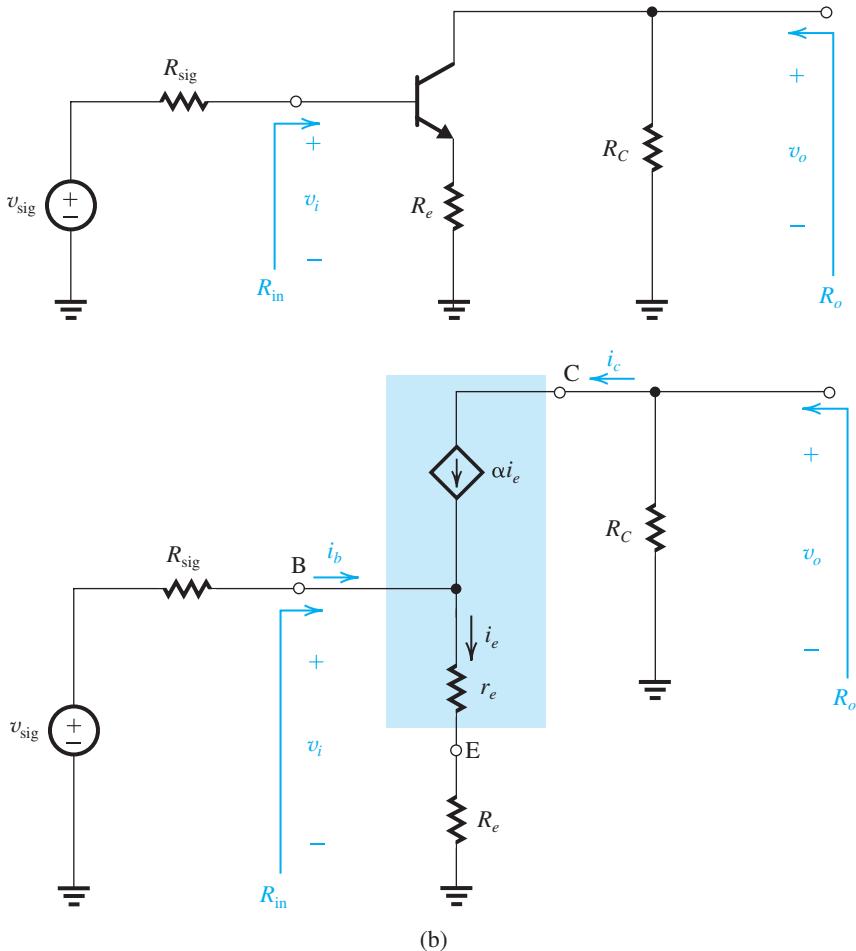
$$R_{in} \equiv \frac{v_i}{i_b}$$

where

$$i_b = (1 - \alpha)i_e = \frac{i_e}{\beta + 1} \quad (7.105)$$

and

$$i_e = \frac{v_i}{r_e + R_e} \quad (7.106)$$



**Figure 7.38** The CE amplifier with an emitter resistance  $R_e$ ; (a) circuit without bias details; (b) equivalent circuit with the BJT replaced with its T model.

Thus,

$$R_{in} = (\beta + 1)(r_e + R_e) \quad (7.107)$$

This is a very important result. It states that *the input resistance looking into the base is  $(\beta + 1)$  times the total resistance in the emitter*, and is known as the **resistance-reflection rule**. The factor  $(\beta + 1)$  arises because the base current is  $1/(\beta + 1)$  times the emitter current. The expression for  $R_{in}$  in Eq. (7.107) shows clearly that including a resistance  $R_e$  in the emitter can substantially increase  $R_{in}$ , a very desirable result. Indeed, the value of  $R_{in}$  is increased by the ratio

$$\begin{aligned} \frac{R_{in}(\text{with } R_e \text{ included})}{R_{in}(\text{without } R_e)} &= \frac{(\beta + 1)(r_e + R_e)}{(\beta + 1)r_e} \\ &= 1 + \frac{R_e}{r_e} \simeq 1 + g_m R_e \end{aligned} \quad (7.108)$$

Thus the circuit designer can use the value of  $R_e$  to control the value of  $R_{in}$ .

To determine the voltage gain  $A_{vo}$ , we see from Fig. 7.38(b) that

$$\begin{aligned} v_o &= -i_c R_C \\ &= -\alpha i_e R_C \end{aligned}$$

Substituting for  $i_e$  from Eq. (7.106) gives

$$A_{vo} = -\alpha \frac{R_C}{r_e + R_e} \quad (7.109)$$

This is a very useful result: It states that the gain from base to collector is  $\alpha$  times the ratio of the total resistance in the collector to the total resistance in the emitter (in this case,  $r_e + R_e$ ),

$$\text{Voltage gain from base to collector} = -\alpha \frac{\text{Total resistance in collector}}{\text{Total resistance in emitter}} \quad (7.110)$$

This is the BJT version of the MOSFET expression in Eq. (7.102) except that here we have the additional factor  $\alpha$ . This factor arises because  $i_c = \alpha i_e$ , unlike the MOSFET case where  $i_d = i_s$ . Usually,  $\alpha \approx 1$  and can be dropped from Eq. (7.110).

The open-circuit voltage gain in Eq. (7.109) can be expressed alternatively as

$$A_{vo} = -\frac{\alpha}{r_e} \frac{R_C}{1 + R_e/r_e}$$

Thus,

$$A_{vo} = -\frac{g_m R_C}{1 + R_e/r_e} \approx -\frac{g_m R_C}{1 + g_m R_e} \quad (7.111)$$

Thus, including  $R_e$  reduces the voltage gain by the factor  $(1 + g_m R_e)$ , which is the same factor by which  $R_{in}$  is increased. This points out an interesting trade-off between gain and input resistance, a trade-off that the designer can exercise through the choice of an appropriate value for  $R_e$ .

The output resistance  $R_o$  can be found from the circuit in Fig. 7.38(b) by inspection:

$$R_o = R_C$$

If a load resistance  $R_L$  is connected at the amplifier output,  $A_v$  can be found as

$$\begin{aligned} A_v &= A_{vo} \frac{R_L}{R_L + R_o} \\ &= -\alpha \frac{R_C}{r_e + R_e} \frac{R_L}{R_L + R_C} \\ &= -\alpha \frac{R_C \| R_L}{r_e + R_e} \end{aligned} \quad (7.112)$$

which could have been written directly using Eq. (7.110). The overall voltage gain  $G_v$  can now be found:

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} \times -\alpha \frac{R_C \| R_L}{r_e + R_e}$$

Substituting for  $R_{\text{in}}$  from Eq. (7.107) and replacing  $\alpha$  with  $\beta/(\beta + 1)$  results in

$$G_v = -\beta \frac{R_C \| R_L}{R_{\text{sig}} + (\beta + 1)(r_e + R_e)} \quad (7.113)$$

Careful examination of this expression reveals that the denominator comprises the total resistance in the base circuit [recall that  $(\beta + 1)(r_e + R_e)$  is the reflection of  $(r_e + R_e)$  from the emitter side to the base side]. Thus the expression in Eq. (7.113) states that the voltage gain from base to collector is equal to  $\beta$  times the ratio of the total resistance in the collector to the total resistance in the base. The factor  $\beta$  appears because it is the ratio of the collector current to the base current. This general and useful expression has no counterpart in the MOS case. We observe that the overall voltage gain  $G_v$  is lower than the value without  $R_e$ , namely,

$$G_v = -\beta \frac{R_C \| R_L}{R_{\text{sig}} + (\beta + 1)r_e} \quad (7.114)$$

because of the additional term  $(\beta + 1)r_e$  in the denominator. The gain, however, is now less sensitive to the value of  $\beta$ , a desirable result because of the typical wide variability in the value of  $\beta$ .

Another important consequence of including the resistance  $R_e$  in the emitter is that it enables the amplifier to handle larger input signals without incurring nonlinear distortion. This is because only a fraction of the input signal at the base,  $v_i$ , appears between the base and the emitter. Specifically, from the circuit in Fig. 7.38(b), we see that

$$\frac{v_\pi}{v_i} = \frac{r_e}{r_e + R_e} \approx \frac{1}{1 + g_m R_e} \quad (7.115)$$

Thus, for the same  $v_\pi$ , the signal at the input terminal of the amplifier,  $v_i$ , can be greater than for the CE amplifier by the factor  $(1 + g_m R_e)$ .

To summarize, including a resistance  $R_e$  in the emitter of the CE amplifier results in the following characteristics:

1. The input resistance  $R_{\text{in}}$  is increased by the factor  $(1 + g_m R_e)$ .
2. The voltage gain from base to collector,  $A_v$ , is reduced by the factor  $(1 + g_m R_e)$ .
3. For the same nonlinear distortion, the input signal  $v_i$  can be increased by the factor  $(1 + g_m R_e)$ .
4. The overall voltage gain is less dependent on the value of  $\beta$ .
5. The high-frequency response is significantly improved (as we shall see in Chapter 10).

With the exception of gain reduction, these characteristics represent performance improvements. Indeed, the reduction in gain is the price paid for obtaining the other performance improvements. In many cases this is a good bargain; it is the underlying philosophy for the use of negative feedback. That the resistance  $R_e$  introduces negative feedback in the amplifier circuit can be verified by utilizing a procedure similar to that we used above for the MOSFET case. In Chapter 11, where we shall study negative feedback formally, we will find that the factor  $(1 + g_m R_e)$ , which appears repeatedly, is the “amount of negative feedback” introduced by  $R_e$ . Finally, we note that the negative-feedback action of  $R_e$  gives it the name **emitter degeneration resistance**.

**Example 7.9**

For the CE amplifier specified in Example 7.8, what value of  $R_e$  is needed to raise  $R_{in}$  to a value four times that of  $R_{sig}$ ? With  $R_e$  included, find  $A_{vo}$ ,  $R_o$ ,  $A_v$ , and  $G_v$ . Also, if  $\hat{v}_\pi$  is limited to 5 mV, what are the corresponding values of  $\hat{v}_{sig}$  and  $\hat{v}_o$ ?

**Solution**

To obtain  $R_{in} = 4R_{sig} = 4 \times 5 = 20 \text{ k}\Omega$ , the required  $R_e$  is found from

$$20 = (\beta + 1)(r_e + R_e)$$

With  $\beta = 100$ ,

$$r_e + R_e \simeq 200 \Omega$$

Thus,

$$\begin{aligned} R_e &= 200 - 25 = 175 \Omega \\ A_{vo} &= -\alpha \frac{R_C}{r_e + R_e} \\ &\simeq -\frac{5000}{25 + 175} = -25 \text{ V/V} \\ R_o &= R_C = 5 \text{ k}\Omega \text{ (unchanged)} \\ A_v &= A_{vo} \frac{R_L}{R_L + R_o} = -25 \times \frac{5}{5+5} = -12.5 \text{ V/V} \\ G_v &= \frac{R_{in}}{R_{in} + R_{sig}} A_v = -\frac{20}{20+5} \times 12.5 = -10 \text{ V/V} \end{aligned}$$

For  $\hat{v}_\pi = 5 \text{ mV}$ ,

$$\begin{aligned} \hat{v}_i &= \hat{v}_\pi \left( \frac{r_e + R_e}{r_e} \right) \\ &= 5 \left( 1 + \frac{175}{25} \right) = 40 \text{ mV} \\ \hat{v}_{sig} &= \hat{v}_i \frac{R_{in} + R_{sig}}{R_{in}} \\ &= 40 \left( 1 + \frac{5}{20} \right) = 50 \text{ mV} \\ \hat{v}_o &= \hat{v}_{sig} \times |G_v| \\ &= 50 \times 10 = 500 \text{ mV} = 0.5 \text{ V} \end{aligned}$$

Thus, while  $|G_v|$  has decreased to about a third of its original value, the amplifier is able to produce as large an output signal as before for the same nonlinear distortion.

## EXERCISE

- 7.24** Show that with  $R_e$  included, and  $v_\pi$  limited to a maximum value  $\hat{v}_\pi$ , the maximum allowable input signal,  $\hat{v}_{\text{sig}}$ , is given by

$$\hat{v}_{\text{sig}} = \hat{v}_\pi \left( 1 + \frac{R_e}{r_e} + \frac{R_{\text{sig}}}{r_\pi} \right)$$

If the transistor is biased at  $I_C = 0.5 \text{ mA}$  and has a  $\beta$  of 100, what value of  $R_e$  is needed to permit an input signal  $\hat{v}_{\text{sig}}$  of 100 mV from a source with a resistance  $R_{\text{sig}} = 10 \text{ k}\Omega$  while limiting  $\hat{v}_\pi$  to 10 mV? What is  $R_{\text{in}}$  for this amplifier? If the total resistance in the collector is 10 k $\Omega$ , what  $G_v$  value results?

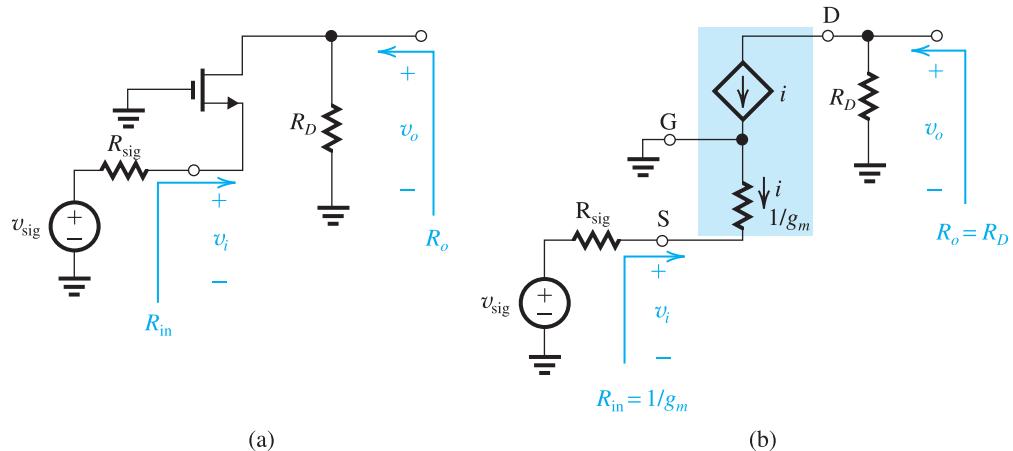
**Ans.** 350  $\Omega$ ; 40.4 k $\Omega$ ; -19.8 V/V

### 7.3.5 The Common-Gate (CG) and the Common-Base (CB) Amplifiers

Figure 7.39(a) shows a common-gate amplifier with the biasing circuit omitted. The amplifier is fed with a signal source characterized by  $v_{\text{sig}}$  and  $R_{\text{sig}}$ . Since  $R_{\text{sig}}$  appears in series with the source, it is more convenient to represent the transistor with the T model than with the  $\pi$  model. Doing this, we obtain the amplifier equivalent circuit shown in Fig. 7.39(b).

From inspection of the equivalent circuit of Fig. 7.39(b), we see that the input resistance

$$R_{\text{in}} = \frac{1}{g_m} \quad (7.116)$$



**Figure 7.39** (a) Common-gate (CG) amplifier with bias arrangement omitted. (b) Equivalent circuit of the CG amplifier with the MOSFET replaced with its T model.

This should have been expected, since we are looking into the source and the gate is grounded. Typically  $1/g_m$  is a few hundred ohms; thus the CG amplifier has a low input resistance.

To determine the voltage gain  $A_{vo}$ , we write at the drain node

$$v_o = -iR_D$$

and substitute for the source current  $i$  from

$$i = -\frac{v_i}{1/g_m}$$

to obtain

➤  $A_{vo} \equiv \frac{v_o}{v_i} = g_m R_D$  (7.117)

which except for the positive sign is identical to the expression for  $A_{vo}$  of the CS amplifier.

The output resistance of the CG circuit can be found by inspection of the circuit in Fig. 7.39(b) as

$$R_o = R_D \quad (7.118)$$

which is the same as in the case of the CS amplifier.

Although the gain of the CG amplifier proper has the same magnitude as that of the CS amplifier, this is usually not the case as far as the overall voltage gain is concerned. The low input resistance of the CG amplifier can cause the input signal to be severely attenuated. Specifically,

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{1/g_m}{1/g_m + R_{sig}} \quad (7.119)$$

from which we see that except for situations in which  $R_{sig}$  is on the order of  $1/g_m$ , the signal transmission factor  $v_i/v_{sig}$  can be very small and the overall voltage gain  $G_v$  can be correspondingly small. Specifically, with a resistance  $R_L$  connected at the output

$$G_v = \frac{1/g_m}{R_{sig} + 1/g_m} [g_m (R_D \parallel R_L)]$$

Thus,

➤  $G_v = \frac{(R_D \parallel R_L)}{R_{sig} + 1/g_m}$  (7.120)

Observe that the overall voltage gain is simply the ratio of the total resistance in the drain circuit to the total resistance in the source circuit. If  $R_{sig}$  is of the same order as  $R_D$  and  $R_L$ ,  $G_v$  will be very small.

Because of its low input resistance, the CG amplifier alone has very limited application. One such application is to amplify high-frequency signals that come from sources with relatively low resistances. These include cables, where it is usually necessary for the input resistance of the amplifier to match the characteristic resistance of the cable. As will be shown in Chapter 10, the CG amplifier has excellent high-frequency response. Thus it can be combined with the CS amplifier in a very beneficial way that takes advantage of the best features of each of the two configurations. A very significant circuit of this kind will be studied in Chapter 8.

## EXERCISE

- 7.25** A CG amplifier is required to match a signal source with  $R_{\text{sig}} = 100 \Omega$ . At what current  $I_D$  should the MOSFET be biased if it is operated at an overdrive voltage of 0.20 V? If the total resistance in the drain circuit is 2 k $\Omega$ , what overall voltage gain is realized?

**Ans.** 1 mA; 10 V/V

Very similar results can be obtained for the CB amplifier shown in Fig. 7.40(a). Specifically, from the equivalent circuit in Fig. 7.40(b) we can find

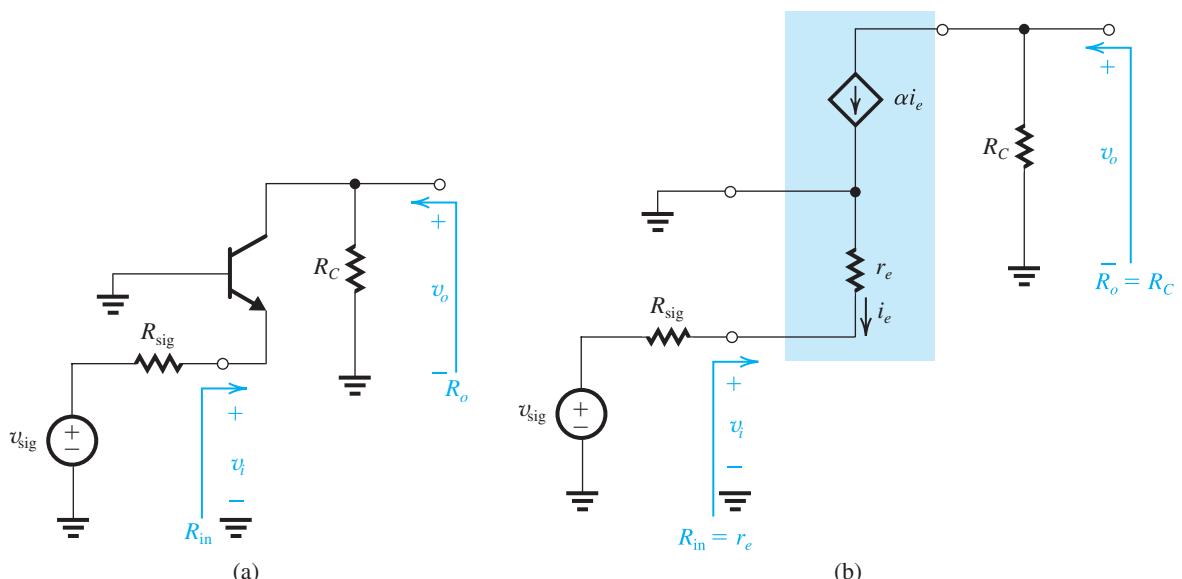
$$R_{\text{in}} = r_e = \frac{\alpha}{g_m} \simeq 1/g_m \quad (7.121)$$

$$A_{vo} = \frac{\alpha}{r_e} R_C = g_m R_C \quad (7.122)$$

$$R_o = R_C \quad (7.123)$$

and with a load resistance  $R_L$  connected to the output, the overall voltage gain is given by

$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = \alpha \frac{R_C \| R_L}{R_{\text{sig}} + r_e} \quad (7.124)$$



**Figure 7.40** (a) CB amplifier with bias details omitted; (b) amplifier equivalent circuit with the BJT represented by its T model.

Since  $\alpha \simeq 1$ , we see that as in the case of the CG amplifier, the overall voltage gain is simply the ratio of the total resistance in the collector to the total resistance in the emitter. We also note that the overall voltage gain is almost independent of the value of  $\beta$  (except through the small dependence of  $\alpha$  on  $\beta$ ), a desirable property. Observe that for  $R_{\text{sig}}$  of the same order as  $R_C$  and  $R_L$ , the gain will be very small.

In summary, the CB and CG amplifiers exhibit a very low input resistance ( $1/g_m$ ), an open-circuit voltage gain that is positive and equal in magnitude to that of the CE (CG) amplifier ( $g_m R_C$  or  $g_m R_D$ ), and, like the CE (CS) amplifier, a relatively high output resistance ( $R_C$  or  $R_D$ ). Because of its very low input resistance, the CB (CG) circuit *alone* is not attractive as a voltage amplifier except in specialized applications, such as the cable amplifier mentioned above. The CB (CG) amplifier has excellent high-frequency performance, which as we shall see in Chapters 8 and 10, makes it useful in combination with other circuits in the implementation of high-frequency amplifiers.

## EXERCISES

- 7.26** Consider a CB amplifier utilizing a BJT biased at  $I_C = 1 \text{ mA}$  and with  $R_C = 5 \text{ k}\Omega$ . Determine  $R_{\text{in}}$ ,  $A_{vo}$ , and  $R_o$ . If the amplifier is loaded in  $R_L = 5 \text{ k}\Omega$ , what value of  $A_v$  results? What  $G_v$  is obtained if  $R_{\text{sig}} = 5 \text{ k}\Omega$ ?

**Ans.**  $25 \Omega$ ;  $200 \text{ V/V}$ ;  $5 \text{ k}\Omega$ ;  $100 \text{ V/V}$ ;  $0.5 \text{ V/V}$

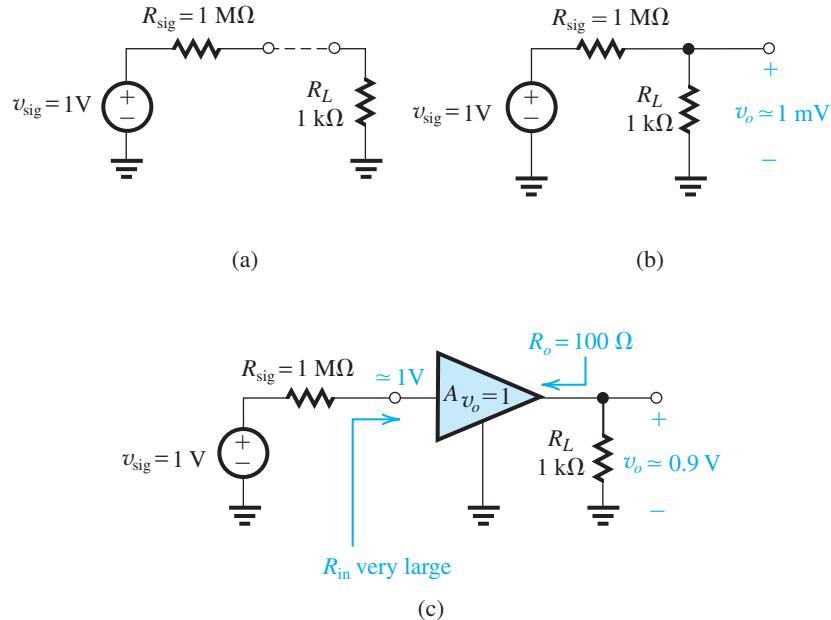
- 7.27** A CB amplifier is required to amplify a signal delivered by a coaxial cable having a characteristic resistance of  $50 \Omega$ . What bias current  $I_C$  should be utilized to obtain  $R_{\text{in}}$  that is matched to the cable resistance? To obtain an overall voltage gain of  $G_v$  of  $40 \text{ V/V}$ , what should the total resistance in the collector (i.e.,  $R_C \parallel R_L$ ) be?

**Ans.**  $0.5 \text{ mA}$ ;  $4 \text{ k}\Omega$

### 7.3.6 The Source and Emitter Followers

The last of the basic transistor amplifier configurations is the common-drain (common-collector) amplifier, an important circuit that finds application in the design of both small-signal amplifiers and amplifiers that are required to handle large signals and deliver substantial amounts of signal power to a load. This latter variety will be studied in Chapter 12. The common-drain amplifier is more commonly known as the *source follower*, and the common-collector amplifier is more commonly known as the *emitter follower*. The reason behind these names will become apparent shortly.

**The Need for Voltage Buffers** Before embarking on the analysis of the source and the emitter followers, it is useful to look at one of their more common applications. Consider the situation depicted in Fig. 7.41(a). A signal source delivering a signal of reasonable strength (1 V) with an internal resistance of  $1 \text{ M}\Omega$  is to be connected to a  $1\text{-k}\Omega$  load resistance. Connecting the source to the load directly as in Fig. 7.41(b) would result in severe attenuation



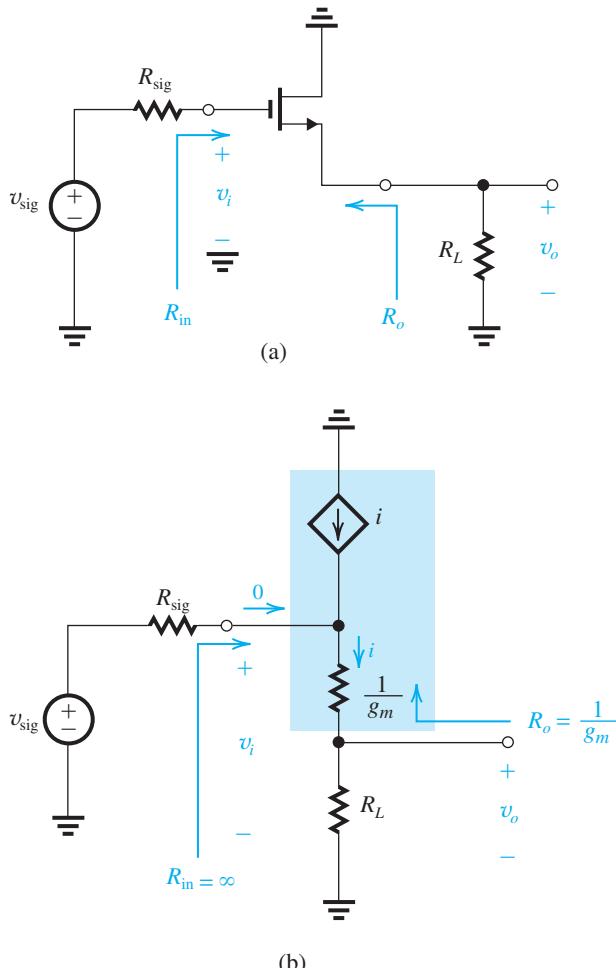
**Figure 7.41** Illustrating the need for a unity-gain voltage buffer amplifier.

of the signal; the signal appearing across the load will be only  $1/(1000 + 1)$  of the input signal, or about 1 mV. An alternative course of action is suggested in Fig. 7.41(c). Here we have interposed an amplifier between the source and the load. Our amplifier, however, is unlike the amplifiers we have been studying in this chapter thus far; it has a voltage gain of only unity. This is because our signal is already of sufficient strength and we do not need to increase its amplitude. Note, however, that our amplifier has a very high input resistance, thus almost all of  $v_{\text{sig}}$  (i.e., 1 V) will appear at the input of the amplifier proper. Since the amplifier has a low output resistance ( $100 \Omega$ ), 90% of this signal (0.9 V) will appear at the output, obviously a very significant improvement over the situation without the amplifier. As will be seen next, the source follower can easily implement the unity-gain buffer amplifier shown in Fig. 7.41(c).

**Characteristic Parameters of the Source Follower** Figure 7.42(a) shows a source follower with the bias circuit omitted. The source follower is fed with a signal generator ( $v_{\text{sig}}$ ,  $R_{\text{sig}}$ ) and has a load resistance  $R_L$  connected between the source terminal and ground. We shall assume that  $R_L$  includes both the actual load and any other resistance that may be present between the source terminal and ground (e.g., for biasing purposes). Normally, the actual load resistance would be much lower in value than such other resistances and thus would dominate.

Since the MOSFET has a resistance  $R_L$  connected in its source terminal, it is most convenient to use the T model, as shown in Fig. 7.40(b). From the latter circuit we can write by inspection

$$R_{\text{in}} = \infty$$



**Figure 7.42** (a) Common-drain amplifier or source follower with the bias circuit omitted. (b) Equivalent circuit of the source follower obtained by replacing the MOSFET with its T model.

and obtain  $A_v$  from the voltage divider formed by  $1/g_m$  and  $R_L$  as

$$\mathbf{A_v} \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m} \quad (7.125)$$

Setting  $R_L = \infty$  we obtain

$$\mathbf{A_{vo}} = 1 \quad (7.126)$$

The output resistance  $R_o$  is found by setting  $v_i = 0$  (i.e., by grounding the gate). Now looking back into the output terminal, excluding  $R_L$ , we simply see  $1/g_m$ , thus

$$\mathbf{R_o} = 1/g_m \quad (7.127)$$

The unity open-circuit voltage gain together with  $R_o$  in Eq. (7.127) can be used to find  $A_v$  when a load resistance  $R_L$  is connected. The result is simply the expression in Eq. (7.125).

Finally, because of the infinite  $R_{in}$ ,  $v_i = v_{sig}$ , and the overall voltage gain is

$$G_v = A_v = \frac{R_L}{R_L + 1/g_m} \quad (7.128)$$

Thus  $G_v$  will be lower than unity. However, because  $1/g_m$  is usually low, the voltage gain can be close to unity. The unity open-circuit voltage gain in Eq. (7.126) indicates that the voltage at the source terminal will follow that at the input, hence the name *source follower*.

In conclusion, the source follower features a very high input resistance (ideally, infinite), a relatively low output resistance ( $1/g_m$ ), and an open-circuit voltage gain that is near unity (ideally, unity). Thus the source follower is ideally suited for implementing the unity-gain voltage buffer of Fig. 7.41(c). The source follower is also used as the output (i.e., last) stage in a multistage amplifier, where its function is to equip the overall amplifier with a low output resistance, thus enabling it to supply relatively large load currents without loss of gain (i.e., with little reduction of output signal level). The design of output stages is studied in Chapter 12.

## EXERCISES

**D7.28** It is required to design a source follower that implements the buffer amplifier shown in Fig. 7.41(c).

If the MOSFET is operated with an overdrive voltage  $V_{ov} = 0.25$  V, at what drain current should it be biased? Find the output signal amplitude and the signal amplitude between gate and source.

**Ans.** 1.25 mA; 0.91 V; 91 mV

**D7.29** A MOSFET is connected in the source-follower configuration and employed as the output stage of a cascade amplifier. It is required to provide an output resistance of  $200\ \Omega$ . If the MOSFET has  $k'_n = 0.4\ \text{mA/V}^2$  and is operated at  $V_{ov} = 0.25$  V, find the required  $W/L$  ratio. Also specify the dc bias current  $I_D$ . If the amplifier load resistance varies over the range  $1\ \text{k}\Omega$  to  $10\ \text{k}\Omega$ , what is the range of  $G_v$  of the source follower?

**Ans.** 50; 0.625 mA; 0.83 V/V to 0.98 V/V

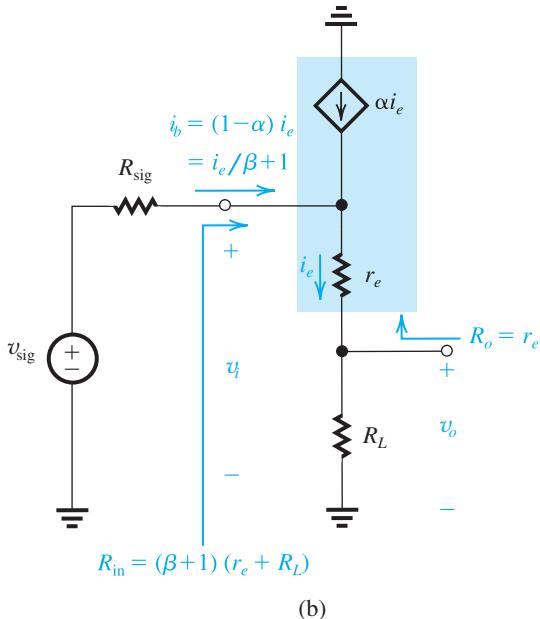
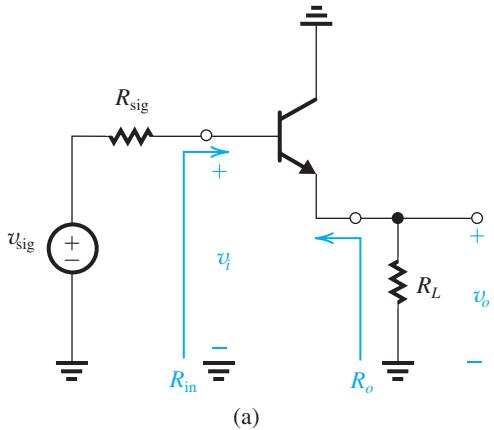
**Characteristic Parameters of the Emitter Follower** Although the emitter follower does not have an infinite input resistance (as in the case of the source follower), it is still widely used as a voltage buffer. In fact, it is a very versatile and popular circuit. We will therefore study it in some detail.

Figure 7.43(a) shows an emitter follower with the equivalent circuit shown in Fig. 7.43(b). The input resistance  $R_{in}$  is found from

$$R_{in} = \frac{v_i}{i_b}$$

Substituting for  $i_b = i_e/(\beta + 1)$  where  $i_e$  is given by

$$i_e = \frac{v_i}{r_e + R_L}$$



**Figure 7.43** (a) Common-collector amplifier or emitter follower with the bias circuit omitted. (b) Equivalent circuit obtained by replacing the BJT with its T model.

we obtain

$$\rightarrow R_{in} = (\beta + 1)(r_e + R_L) \quad (7.129)$$

a result that we could have written directly, utilizing the resistance-reflection rule. Note that as expected the emitter follower takes the low load resistance and reflects it to the base side, where the signal source is, after increasing its value by a factor  $(\beta + 1)$ . It is this impedance transformation property of the emitter follower that makes it useful in

connecting a low-resistance load to a high-resistance source, that is, to implement a buffer amplifier.

The voltage gain  $A_v$  is given by

$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + r_e} \quad (7.130)$$

Setting  $R_L = \infty$  yields  $A_{vo}$ ,

$$A_{vo} = 1 \quad (7.131)$$

Thus, as expected, the open-circuit voltage gain of the emitter follower proper is unity, which means that the signal voltage at the emitter *follows* that at the base, which is the origin of the name “emitter follower.”

To determine  $R_o$ , refer to Fig. 7.43(b) and look back into the emitter (i.e., behind or excluding  $R_L$ ) while setting  $v_i = 0$  (i.e., grounding the base). You will see  $r_e$  of the BJT, thus

$$R_o = r_e \quad (7.132)$$

This result together with  $A_{vo} = 1$  yields  $A_v$  in Eq. (7.130), thus confirming our earlier analysis.

We next determine the overall voltage gain  $G_v$ , as follows:

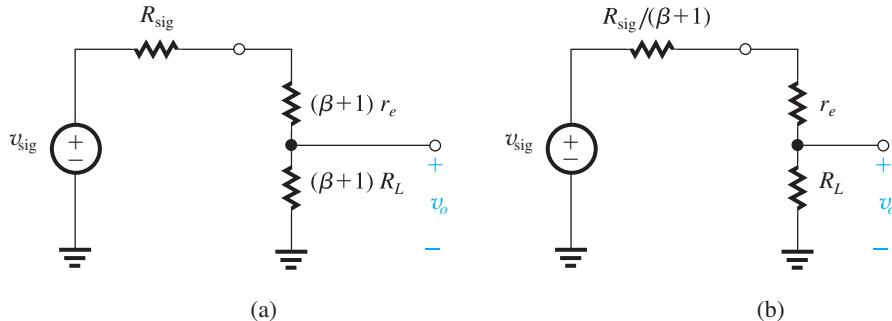
$$\begin{aligned} \frac{v_i}{v_{sig}} &= \frac{R_{in}}{R_{in} + R_{sig}} \\ &= \frac{(\beta + 1)(r_e + R_L)}{(\beta + 1)(r_e + R_L) + R_{sig}} \\ G_v \equiv \frac{v_o}{v_{sig}} &= \frac{v_i}{v_{sig}} \times A_v \end{aligned}$$

Substituting for  $A_v$  from Eq. (7.130) results in

$$G_v = \frac{(\beta + 1)R_L}{(\beta + 1)R_L + (\beta + 1)r_e + R_{sig}} \quad (7.133)$$

This equation indicates that the overall gain, though lower than one, can be close to one if  $(\beta + 1)R_L$  is larger or comparable in value to  $R_{sig}$ . This again confirms the action of the emitter follower in delivering a large proportion of  $v_{sig}$  to a low-valued load resistance  $R_L$  even though  $R_{sig}$  can be much larger than  $R_L$ . The key point is that  $R_L$  is multiplied by  $(\beta + 1)$  before it is “presented to the source.” Figure 7.44(a) shows an equivalent circuit of the emitter follower obtained by simply reflecting  $r_e$  and  $R_L$  to the base side. The overall voltage gain  $G_v \equiv v_o/v_{sig}$  can be determined directly and very simply from this circuit by using the voltage divider rule. The result is the expression for  $G_v$  already given in Eq. (7.133).

Dividing all resistances in the circuit of Fig. 7.44(a) by  $\beta + 1$  does not change the voltage ratio  $v_o/v_{sig}$ . Thus we obtain another equivalent circuit, shown in Fig. 7.44(b), that can be used to determine  $G_v \equiv v_o/v_{sig}$  of the emitter follower. A glance at this circuit reveals that it is simply the equivalent circuit obtained by reflecting  $v_{sig}$  and  $R_{sig}$  from the base side to the emitter side. In this reflection,  $v_{sig}$  does not change, but  $R_{sig}$  is divided by  $\beta + 1$ . Thus, we



**Figure 7.44** Simple equivalent circuits for the emitter follower obtained by (a) reflecting  $r_e$  and  $R_L$  to the base side, and (b) reflecting  $v_{sig}$  and  $R_{sig}$  to the emitter side. Note that the circuit in (b) can be obtained from that in (a) by simply dividing all resistances by  $(\beta + 1)$ .

either reflect to the base side and obtain the circuit in Fig. 7.44(a) or reflect to the emitter side and obtain the circuit in Fig. 7.44(b). From the latter,  $G_v$  can be found as

$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = \frac{R_L}{R_L + r_e + R_{\text{sig}}/(\beta + 1)} \quad (7.134)$$

Observe that this expression is the same as that in Eq. (7.133) except for dividing both the numerator and denominator by  $\beta + 1$ .

The expression for  $G_v$  in Eq. (7.134) has an interesting interpretation: The emitter follower reduces  $R_{sig}$  by the factor  $(\beta + 1)$  before “presenting it to the load resistance  $R_L$ ”: an impedance transformation that has the same buffering effect.

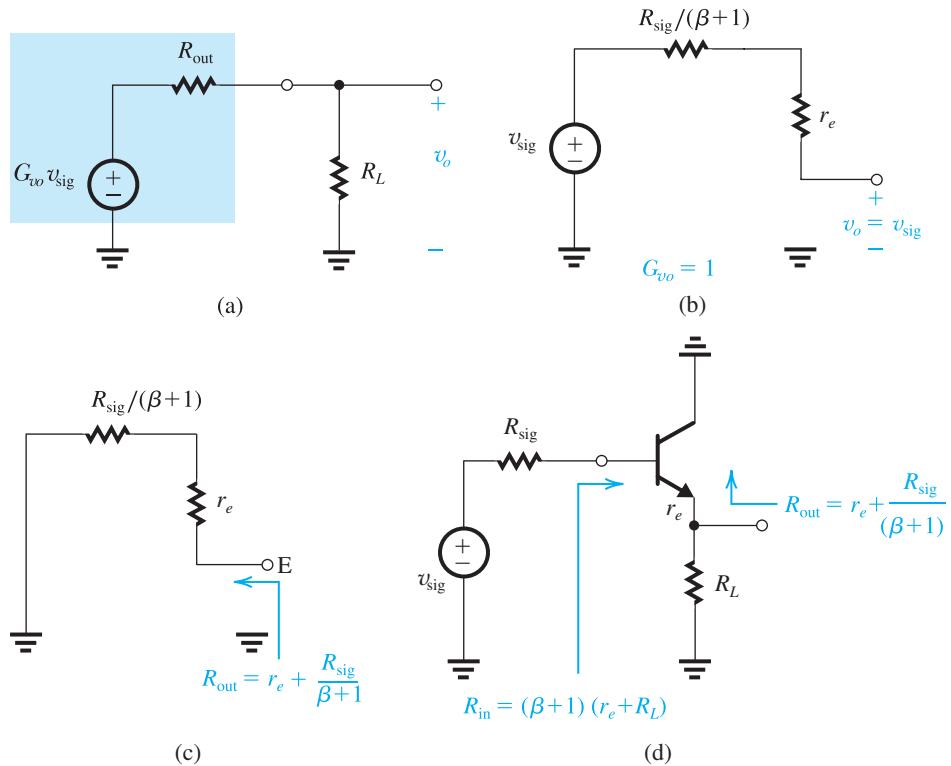
At this point it is important to note that although the emitter follower does not provide voltage gain it has a current gain of  $\beta + 1$ .

**Thévenin Representation of the Emitter-Follower Output** A more general representation of the emitter-follower output is shown in Fig. 7.45(a). Here  $G_{vo}$  is the overall open-circuit voltage gain that can be obtained by setting  $R_L = \infty$  in the circuit of Fig. 7.44(b), as illustrated in Fig. 7.45(b). The result is  $G_{vo} = 1$ . The output resistance  $R_{out}$  is different from  $R_o$ . To determine  $R_{out}$  we set  $v_{sig}$  to zero (rather than setting  $v_i$  to zero). Again we can use the equivalent circuit in Fig. 7.44(b) to do this, as illustrated in Fig. 7.45(c). We see that

$$R_{\text{out}} = r_e + \frac{R_{\text{sig}}}{\beta + 1} \quad (7.135)$$

Finally, we show in Fig. 7.45(d) the emitter-follower circuit together with its  $R_{in}$  and  $R_{out}$ . Observe that  $R_{in}$  is determined by reflecting  $r_e$  and  $R_L$  to the base side (by multiplying their values by  $\beta + 1$ ). To determine  $R_{out}$ , grab hold of the emitter and walk (or just look!) backward while  $v_{sig} = 0$ . You will see  $r_e$  in series with  $R_{sig}$ , which because it is in the base must be divided by  $(\beta + 1)$ .

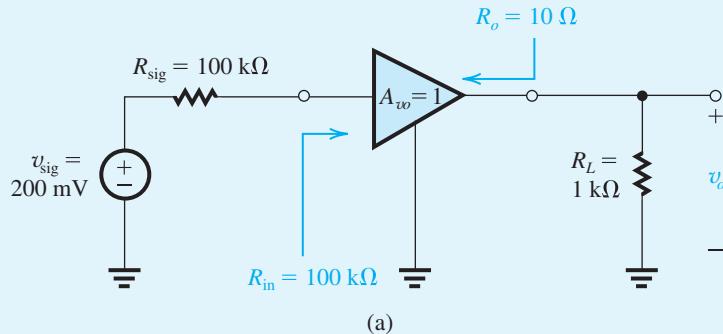
We note that unlike the amplifier circuits we studied earlier, the emitter follower is *not* unilateral. This is manifested by the fact that  $R_{in}$  depends on  $R_L$  and  $R_{out}$  depends on  $R_{sig}$ .



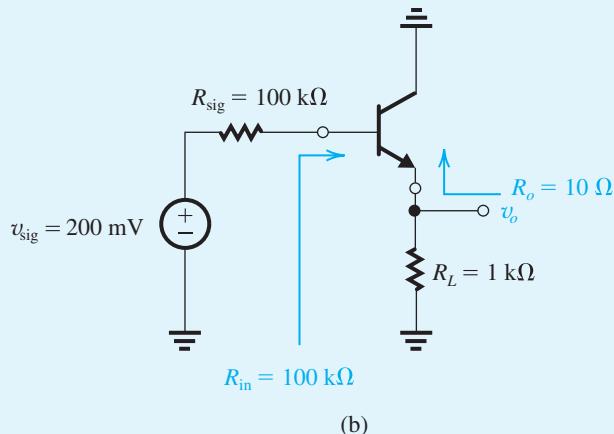
**Figure 7.45** (a) Thévenin representation of the output of the emitter follower. (b) Obtaining  $G_{vo}$  from the equivalent circuit in Fig. 7.44(b). (c) Obtaining  $R_{out}$  from the equivalent circuit in Fig. 7.44(b) with  $v_{sig}$  set to zero. (d) The emitter follower with  $R_{in}$  and  $R_{out}$  determined simply by looking into the input and output terminals, respectively.

### Example 7.10

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current  $I_E$  and the minimum value the transistor  $\beta$  must have. Determine the maximum allowed value of  $v_{sig}$  if  $v_\pi$  is to be limited to 5 mV in order to obtain reasonably linear operation. With  $v_{sig} = 200$  mV, determine the signal voltage at the output if  $R_L$  is changed to 2 k $\Omega$ , and to 0.5 k $\Omega$ .



**Figure 7.46** Circuit for Example 7.10.

**Example 7.10** *continued***Figure 7.46** *continued***Solution**

The emitter-follower circuit is shown in Fig. 7.46(b). To obtain  $R_o = 10 \Omega$ , we bias the transistor to obtain  $r_e = 10 \Omega$ . Thus,

$$10 \Omega = \frac{V_T}{I_E}$$

$$I_E = 2.5 \text{ mA}$$

The input resistance  $R_{in}$  will be

$$R_{in} = (\beta + 1)(r_e + R_L)$$

$$100 = (\beta + 1)(0.01 + 1)$$

Thus, the BJT should have a  $\beta$  with a minimum value of 98. A higher  $\beta$  would obviously be beneficial.

The overall voltage gain can be determined from

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L}{R_L + r_e + \frac{R_{sig}}{(\beta + 1)}}$$

Assuming  $\beta = 100$ , the value of  $G_v$  obtained is

$$G_v = 0.5$$

Thus when  $v_{\text{sig}} = 200 \text{ mV}$ , the signal at the output will be 100 mV. Since the 100 mV appears across the 1-k $\Omega$  load, the signal across the base-emitter junction can be found from

$$\begin{aligned} v_{\pi} &= \frac{v_o}{R_L} \times r_e \\ &= \frac{100}{1000} \times 10 = 1 \text{ mV} \end{aligned}$$

If  $\hat{v}_{\pi} = 5 \text{ mV}$  then  $v_{\text{sig}}$  can be increased by a factor of 5, resulting in  $\hat{v}_{\text{sig}} = 1 \text{ V}$ .

To obtain  $v_o$  as the load is varied, we use the Thévenin equivalent of the emitter follower, shown in Fig. 7.45(a) with  $G_{vo} = 1$  and

$$R_{\text{out}} = \frac{R_{\text{sig}}}{\beta + 1} + r_e = \frac{100}{101} + 0.01 = 1 \text{ k}\Omega$$

to obtain

$$v_o = v_{\text{sig}} \frac{R_L}{R_L + R_{\text{out}}}$$

For  $R_L = 2 \text{ k}\Omega$ ,

$$v_o = 200 \text{ mV} \times \frac{2}{2+1} = 133.3 \text{ mV}$$

and for  $R_L = 0.5 \text{ k}\Omega$ ,

$$v_o = 200 \text{ mV} \times \frac{0.5}{0.5+1} = 66.7 \text{ mV}$$

## EXERCISE

- 7.30** An emitter follower utilizes a transistor with  $\beta = 100$  and is biased at  $I_C = 5 \text{ mA}$ . It operates between a source having a resistance of 10 k $\Omega$  and a load of 1 k $\Omega$ . Find  $R_{\text{in}}$ ,  $G_{vo}$ ,  $R_{\text{out}}$ , and  $G_v$ . What is the peak amplitude of  $v_{\text{sig}}$  that results in  $v_{\pi}$  having a peak amplitude of 5 mV? Find the resulting peak amplitude at the output.

**Ans.** 101.5 k $\Omega$ ; 1 V/V; 104  $\Omega$ ; 0.91 V/V; 1.1 V; 1 V

### 7.3.7 Summary Tables and Comparisons

For easy reference and to enable comparisons, we present in Tables 7.4 and 7.5 the formulas for determining the characteristic parameters for the various configurations of MOSFET and BJT amplifiers, respectively. In addition to the remarks made throughout this section about the characteristics and areas of applicability of the various configurations, we make the following concluding points:

1. MOS amplifiers provide much higher, ideally infinite input resistances (except, of course, for the CG configuration). This is a definite advantage over BJT amplifiers.
2. BJTs exhibit higher  $g_m$  values than MOSFETs, resulting in higher gains.
3. For discrete-circuit amplifiers—that is, those that are assembled from discrete components on a printed-circuit board (PCB)—the BJT remains the device of choice. This is because discrete BJTs are much easier to handle physically than discrete MOSFETs and, more important, a very wide variety of discrete BJTs is available commercially. The remainder of this chapter is concerned with discrete-circuit amplifiers.
4. Integrated-circuit (IC) amplifiers predominantly use MOSFETs, although BJTs are utilized in certain niche areas. Chapters 8 to 13 are mainly concerned with IC amplifiers.
5. The CS and CE configurations are the best suited for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.
6. Including a resistance  $R_s$  in the source of the CS amplifier (a resistance  $R_e$  in the emitter of the CE amplifier) provides a number of performance improvements at the expense of gain reduction.

**Table 7.4** Characteristics of MOSFET Amplifiers

Amplifier type	Characteristics <sup>a</sup>				
	$R_{in}$	$A_{vo}$	$R_o$	$A_v$	$G_v$
Common source (Fig. 7.35)	$\infty$	$-g_m R_D$	$R_D$	$-g_m (R_D \parallel R_L)$	$-g_m (R_D \parallel R_L)$
Common source with $R_s$ (Fig. 7.37)	$\infty$	$-\frac{g_m R_D}{1 + g_m R_s}$	$R_D$	$\frac{-g_m (R_D \parallel R_L)}{1 + g_m R_s}$ $-\frac{R_D \parallel R_L}{1/g_m + R_s}$	$-\frac{g_m (R_D \parallel R_L)}{1 + g_m R_s}$ $-\frac{R_D \parallel R_L}{1/g_m + R_s}$
Common gate (Fig. 7.39)	$\frac{1}{g_m}$	$g_m R_D$	$R_D$	$g_m (R_D \parallel R_L)$	$\frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$
Source follower (Fig. 7.42)	$\infty$	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$

<sup>a</sup> For the interpretation of  $R_{in}$ ,  $A_{vo}$ , and  $R_o$ , refer to Fig. 7.34(b).

**Table 7.5** Characteristics of BJT Amplifiers<sup>a,b</sup>

	$R_{in}$	$A_{vo}$	$R_o$	$A_v$	$G_v$
Common emitter (Fig. 7.36)	$(\beta + 1)r_e$	$-g_m R_C$	$R_C$	$-g_m(R_C \parallel R_L)$ $-\alpha \frac{R_C \parallel R_L}{r_e}$	$-\beta \frac{R_C \parallel R_L}{R_{sig} + (\beta + 1)r_e}$
Common emitter with $R_e$ (Fig. 7.38)	$(\beta + 1)(r_e + R_e)$	$-\frac{g_m R_C}{1 + g_m R_e}$	$R_C$	$\frac{-g_m(R_C \parallel R_L)}{1 + g_m R_e}$ $-\alpha \frac{R_C \parallel R_L}{r_e + R_e}$	$-\beta \frac{R_C \parallel R_L}{R_{sig} + (\beta + 1)(r_e + R_e)}$
Common base (Fig. 7.40)	$r_e$	$g_m R_C$	$R_C$	$g_m(R_C \parallel R_L)$ $\alpha \frac{R_C \parallel R_L}{r_e}$	$\alpha \frac{R_C \parallel R_L}{R_{sig} + r_e}$
Emitter follower (Fig. 7.43)	$(\beta + 1)(r_e + R_L)$	1	$r_e$	$\frac{R_L}{R_L + r_e}$	$\frac{R_L}{R_L + r_e + R_{sig}/(\beta + 1)}$ $G_{vo} = 1$ $R_{out} = r_e + \frac{R_{sig}}{\beta + 1}$

<sup>a</sup> For the interpretation of  $R_m$ ,  $A_{vo}$ , and  $R_o$  refer to Fig. 7.34.

<sup>b</sup> Setting  $\beta = \infty$  ( $\alpha = 1$ ) and replacing  $r_e$  with  $1/g_m$ ,  $R_C$  with  $R_D$ , and  $R_e$  with  $R_s$  results in the corresponding formulas for MOSFET amplifiers (Table 7.4).

7. The low input resistance of the CG and CB amplifiers makes them useful only in specific applications. As we shall see in Chapter 10, these two configurations exhibit a much better high-frequency response than that available from the CS and CE amplifiers. This makes them useful as high-frequency amplifiers, especially when combined with the CS or CE circuit. We shall study one such combination in Chapter 8.
8. The source follower (emitter follower) finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load, and as the output stage in a multistage amplifier, where its purpose is to equip the amplifier with a low output resistance.

### 7.3.8 When and How to Include the Output Resistance $r_o$

So far we have been neglecting the output resistance  $r_o$  of the MOSFET and the BJT. We have done this for two reasons:

1. To keep things simple and focus attention on the significant features of each of the basic configurations, and
2. Because our main interest in this chapter is discrete-circuit design, where the circuit resistances (e.g.,  $R_C$ ,  $R_D$ , and  $R_L$ ) are usually much smaller than  $r_o$ .

### LEE DE FOREST—A FATHER OF THE ELECTRONICS AGE:

In 1906 self-employed inventor Lee de Forest (1873–1961) created a three-terminal vacuum tube; it was the first electronic amplifier of weak signals. The device was known initially as the de Forest valve. The patent filed in 1907, however, used the name Audion, with the “-ion” indicating that the device was not completely evacuated. By 1919, engineers had realized that complete evacuation of internal gases produced a more reliable device.

De Forest's first amplifier became known as the vacuum tube triode. Through its impact on radio, telephony, motion picture sound, and television, this invention, one of de Forest's 180 patents, is credited with introducing the electronics age. The vacuum tube, in a variety of types, remained the device for implementing amplifiers until the appearance of transistors in the early 1950s.

Nevertheless, in some instances it is relatively easy to include  $r_o$  in the analysis. Specifically:

1. In the CS and CE amplifiers, it can be seen that  $r_o$  of the transistor appears in parallel with  $R_D$  and  $R_C$ , respectively, and can be simply included in the corresponding formulas in Tables 7.4 and 7.5 by replacing  $R_D$  with  $(R_D \parallel r_o)$  and  $R_C$  with  $(R_C \parallel r_o)$ . The effect will be a reduction in the magnitude of gain, of perhaps 5% to 10%.
2. In the source and emitter followers, it can be seen that the transistor  $r_o$  appears in parallel with  $R_L$  and can be taken into account by replacing  $R_L$  in the corresponding formulas with  $(R_L \parallel r_o)$ . Thus, here too, the effect of taking  $r_o$  into account is a small reduction in gain. More significant, however, taking  $r_o$  into account reduces the open-circuit voltage gain  $A_{vo}$  from unity to

$$A_{vo} = \frac{r_o}{r_o + (1/g_m)} \quad (7.136)$$

There are configurations in which taking  $r_o$  into account complicates the analysis considerably. These are the CS (CE) amplifiers with a source (emitter) resistance, and the CG (CB) amplifier. Fortunately, for discrete implementation of these configurations, the effect of neglecting  $r_o$  is usually small (which can be verified by computer simulation).

Finally, a very important point: *In the analysis and design of IC amplifiers,  $r_o$  must always be taken into account.* This is because, as will be seen in the next chapter, all the circuit resistances are of the same order of magnitude as  $r_o$ ; thus, neglecting  $r_o$  can result in completely erroneous results.

## 7.4 Biasing

As discussed in Section 7.1, an essential step in the design of a transistor amplifier is the establishment of an appropriate dc operating point for the transistor. This is the step known as biasing or bias design. In this section, we study the biasing methods commonly employed in discrete-circuit amplifiers. Biasing of integrated-circuit amplifiers will be studied in Chapter 8.

Bias design aims to establish in the drain (collector) a dc current that is predictable and insensitive to variations in temperature and to the large variations in parameter values between devices of the same type. For instance, discrete BJTs belonging to the same manufacturer's part number can exhibit  $\beta$  values that range, say, from 50 to 150. Nevertheless, the bias design

for an amplifier utilizing this particular transistor type may specify that the dc collector current shall always be within, say,  $\pm 10\%$  of the nominal value of, say, 1 mA. A similar statement can be made about the desired insensitivity of the dc drain current to the wide variations encountered in  $V_t$  of discrete MOSFETs.

A second consideration in bias design is locating the dc operating point in the active region of operation of the transistor so as to obtain high voltage gain while allowing for the required output signal swing without the transistor leaving the active region at any time (in order to avoid nonlinear distortion). We discussed this point in Section 7.1.7.

Although we shall consider the biasing of MOSFET and BJT amplifiers separately, the resulting circuits are very similar. Also, it will be seen that good bias designs incorporate a feedback mechanism that works to keep the dc bias point as constant as possible.

In order to keep matters simple and thus focus our attention on significant issues, we will neglect the Early effect; that is assume  $\lambda = 0$  or  $V_A = \infty$ . This is certainly allowed in initial designs of discrete circuits. Of course, the design can be fine-tuned at a later point with the assistance of a circuit-simulation program such as SPICE.

### 7.4.1 The MOSFET Case

**Biasing by Fixing  $V_{GS}$**  The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage  $V_{GS}$  to the value required<sup>6</sup> to provide the desired  $I_D$ . This voltage value can be derived from the power-supply voltage  $V_{DD}$  through the use of an appropriate voltage divider, as shown in Fig. 7.47(a). Alternatively, it can be derived from another suitable reference voltage that might be available in the system. Independent of how the voltage  $V_{GS}$  may be generated, this is *not* a good approach to biasing a MOSFET. To understand the reason for this statement, recall that

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

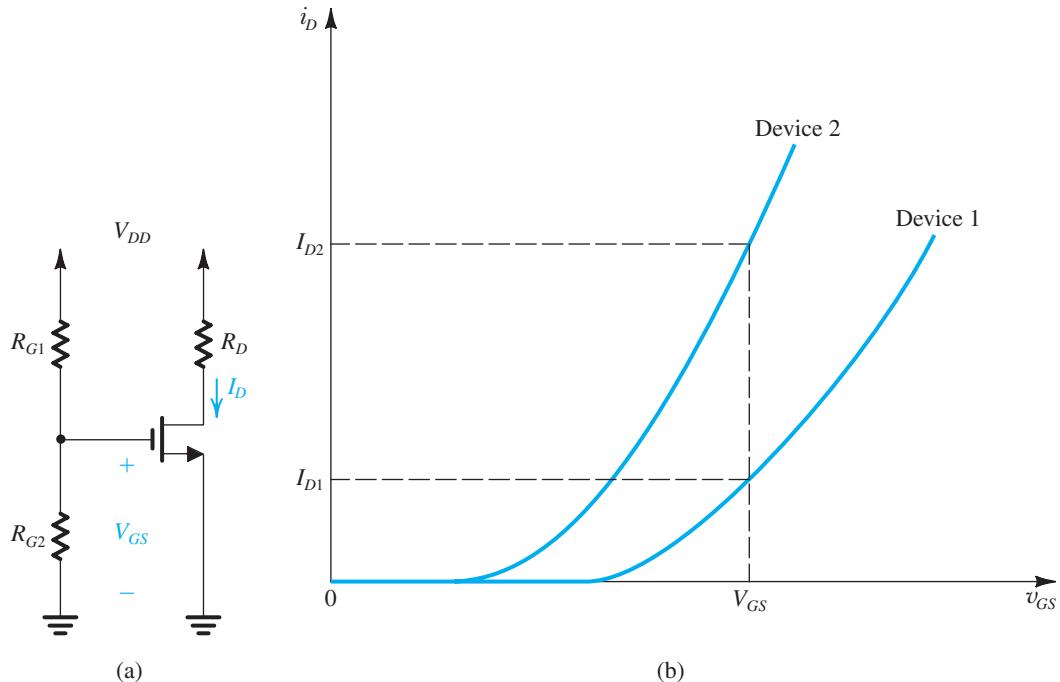
and note that the values of the threshold voltage  $V_t$ , the oxide-capacitance  $C_{ox}$ , and (to a lesser extent) the transistor aspect ratio  $W/L$  vary widely among devices of supposedly the same size and type. This is certainly the case for discrete devices, in which large spreads in the values of these parameters occur among devices of the same manufacturer's part number. The spread can also be large in integrated circuits, especially among devices fabricated on different wafers and certainly between different batches of wafers. Furthermore, both  $V_t$  and  $\mu_n$  depend on temperature, with the result that if we fix the value of  $V_{GS}$ , the drain current  $I_D$  becomes very much temperature dependent.

To emphasize the point that biasing by fixing  $V_{GS}$  is not a good technique, we show in Fig. 7.47 two  $i_D-v_{GS}$  characteristic curves representing extreme values in a batch of MOSFETs of the same type. Observe that for the fixed value of  $V_{GS}$ , the resultant spread in the values of the drain current can be substantial.

**Biasing by Fixing  $V_G$  and Connecting a Resistance in the Source** An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate,  $V_G$ , and connecting a resistance in the source lead, as shown in Fig. 7.48(a). For this circuit

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<sup>6</sup>That is indeed what we were doing in Section 7.1. However, the amplifier circuits studied there were conceptual ones, not actual practical circuits. Our purpose in this section is to study the latter.



**Figure 7.47** (a) Biasing the MOSFET with a constant  $V_{GS}$  generated from  $V_{DD}$  using a voltage divider ( $R_{G1}, R_{G2}$ ); (b) the use of fixed bias (constant  $V_{GS}$ ) can result in a large variability in the value of  $I_D$ . Devices 1 and 2 represent extremes among units of the same type.

we can write

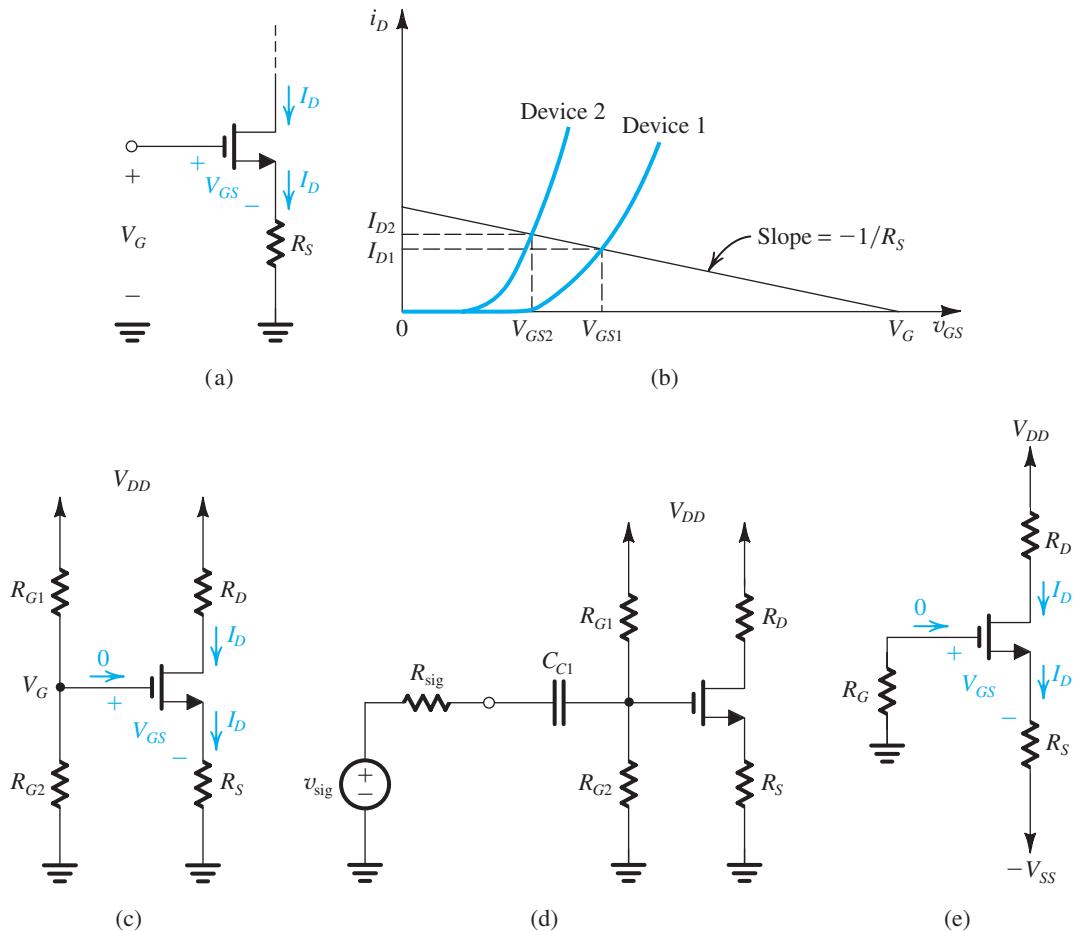
$$V_G = V_{GS} + R_s I_D \quad (7.137)$$

Now, if  $V_G$  is much greater than  $V_{GS}$ ,  $I_D$  will be mostly determined by the values of  $V_G$  and  $R_s$ . However, even if  $V_G$  is not much larger than  $V_{GS}$ , resistor  $R_s$  provides *negative feedback*, which acts to stabilize the value of the bias current  $I_D$ . To see how this comes about, consider what happens when  $I_D$  increases for whatever reason. Equation (7.137) indicates that since  $V_G$  is constant,  $V_{GS}$  will have to decrease. This in turn results in a decrease in  $I_D$ , a change that is opposite to that initially assumed. Thus the action of  $R_s$  works to keep  $I_D$  as constant as possible.<sup>7</sup>

Figure 7.48(b) provides a graphical illustration of the effectiveness of this biasing scheme. Here too we show the  $i_D-v_{GS}$  characteristics for two devices that represent the extremes of a batch of MOSFETs. Superimposed on the device characteristics is a straight line that represents the constraint imposed by the bias circuit—namely, Eq. (7.137). The intersection of this straight line with the  $i_D-v_{GS}$  characteristic curve provides the coordinates ( $I_D$  and  $V_{GS}$ ) of the bias point. Observe that compared to the case of fixed  $V_{GS}$ , here the variability obtained in  $I_D$  is much smaller. Also, note that the variability decreases as  $V_G$  and  $R_s$  are made larger (thus providing a bias line that is less steep).

Two possible practical discrete implementations of this bias scheme are shown in Fig. 7.48(c) and (e). The circuit in Fig. 7.48(c) utilizes one power-supply  $V_{DD}$  and derives  $V_G$

<sup>7</sup>The action of  $R_s$  in stabilizing the value of the bias current  $I_D$  is not unlike that of the resistance  $R_s$ , which we included in the source lead of a CS amplifier in Section 7.3.4. In the latter case also,  $R_s$  works to reduce the change in  $i_D$  with the result that the amplifier gain is reduced.



**Figure 7.48** Biasing using a fixed voltage at the gate,  $V_G$ , and a resistance in the source lead,  $R_s$ : (a) basic arrangement; (b) reduced variability in  $I_D$ ; (c) practical implementation using a single supply; (d) coupling of a signal source to the gate using a capacitor  $C_{C1}$ ; (e) practical implementation using two supplies.

through a voltage divider ( $R_{G1}, R_{G2}$ ). Since  $I_G = 0$ ,  $R_{G1}$  and  $R_{G2}$  can be selected to be very large (in the megohm range), allowing the MOSFET to present a large input resistance to a signal source that may be connected to the gate through a coupling capacitor, as shown in Fig. 7.48(d). Here capacitor  $C_{C1}$  blocks dc and thus allows us to couple the signal  $v_{sig}$  to the amplifier input without disturbing the MOSFET dc bias point. The value of  $C_{C1}$  should be selected large enough to approximate a short circuit at all signal frequencies of interest. We shall study capacitively coupled MOSFET amplifiers, which are suitable only in discrete-circuit design, in Section 7.5. Finally, note that in the circuit of Fig. 7.48(c), resistor  $R_D$  is selected to be as large as possible to obtain high gain but small enough to allow for the desired signal swing at the drain while keeping the MOSFET in saturation at all times.

When two power supplies are available, as is often the case, the somewhat simpler bias arrangement of Fig. 7.48(e) can be utilized. This circuit is an implementation of Eq. (7.137), with  $V_G$  replaced by  $V_{SS}$ . Resistor  $R_G$  establishes a dc ground at the gate and presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

**Example 7.11**

It is required to design the circuit of Fig. 7.48(c) to establish a dc drain current  $I_D = 0.5$  mA. The MOSFET is specified to have  $V_t = 1$  V and  $k'_n W/L = 1$  mA/V<sup>2</sup>. For simplicity, neglect the channel-length modulation effect (i.e., assume  $\lambda = 0$ ). Use a power-supply  $V_{DD} = 15$  V. Calculate the percentage change in the value of  $I_D$  obtained when the MOSFET is replaced with another unit having the same  $k'_n W/L$  but  $V_t = 1.5$  V.

**Solution**

As a rule of thumb for designing this classical biasing circuit, we choose  $R_D$  and  $R_s$  to provide one-third of the power-supply voltage  $V_{DD}$  as a drop across each of  $R_D$ , the transistor (i.e.,  $V_{DS}$ ), and  $R_s$ . For  $V_{DD} = 15$  V, this choice makes  $V_D = +10$  V and  $V_s = +5$  V. Now, since  $I_D$  is required to be 0.5 mA, we can find the values of  $R_D$  and  $R_s$  as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10 \text{ k}\Omega$$

$$R_s = \frac{V_s}{R_s} = \frac{5}{0.5} = 10 \text{ k}\Omega$$

The required value of  $V_{GS}$  can be determined by first calculating the overdrive voltage  $V_{OV}$  from

$$I_D = \frac{1}{2} k'_n (W/L) V_{OV}^2$$

$$0.5 = \frac{1}{2} \times 1 \times V_{OV}^2$$

which yields  $V_{OV} = 1$  V, and thus,

$$V_{GS} = V_t + V_{OV} = 1 + 1 = 2 \text{ V}$$

Now, since  $V_s = +5$  V,  $V_G$  must be

$$V_G = V_s + V_{GS} = 5 + 2 = 7 \text{ V}$$

To establish this voltage at the gate we may select  $R_{G1} = 8 \text{ M}\Omega$  and  $R_{G2} = 7 \text{ M}\Omega$ . The final circuit is shown in Fig. 7.49. Observe that the dc voltage at the drain (+10 V) allows for a positive signal swing of +5 V (i.e., up to  $V_{DD}$ ) and a negative signal swing of 4 V [i.e., down to  $(V_G - V_t)$ ].

If the NMOS transistor is replaced with another having  $V_t = 1.5$  V, the new value of  $I_D$  can be found as follows:

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \quad (7.138)$$

$$V_G = V_{GS} + I_D R_s$$

$$7 = V_{GS} + 10 I_D \quad (7.139)$$

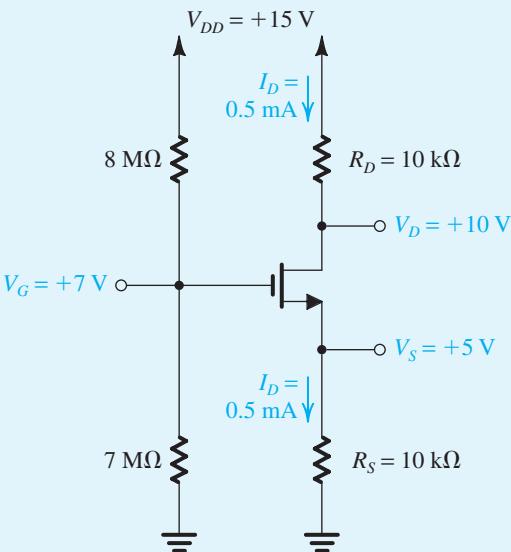


Figure 7.49 Circuit for Example 7.11.

Solving Eqs. (7.138) and (7.139) together yields

$$I_D = 0.455 \text{ mA}$$

Thus the change in  $I_D$  is

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

which is  $\frac{-0.045}{0.5} \times 100 = -9\%$  change.

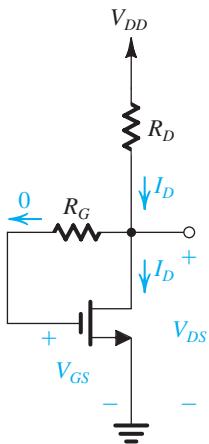
## EXERCISES

- 7.31** Consider the MOSFET in Example 7.11 when fixed- $V_{GS}$  bias is used. Find the required value of  $V_{GS}$  to establish a dc bias current  $I_D = 0.5 \text{ mA}$ . Recall that the device parameters are  $V_t = 1 \text{ V}$ ,  $k'_n W/L = 1 \text{ mA/V}^2$ , and  $\lambda = 0$ . What is the percentage change in  $I_D$  obtained when the transistor is replaced with another having  $V_t = 1.5 \text{ V}$ ?

**Ans.**  $V_{GS} = 2 \text{ V}; -75\%$

- D7.32** Design the circuit of Fig. 7.48(e) to operate at a dc drain current of 0.5 mA and  $V_D = +2 \text{ V}$ . Let  $V_t = 1 \text{ V}$ ,  $k'_n W/L = 1 \text{ mA/V}^2$ ,  $\lambda = 0$ ,  $V_{DD} = V_{SS} = 5 \text{ V}$ . Use standard 5% resistor values (see Appendix J), and give the resulting values of  $I_D$ ,  $V_D$ , and  $V_S$ .

**Ans.**  $R_D = R_S = 6.2 \text{ k}\Omega$ ;  $I_D = 0.49 \text{ mA}$ ,  $V_S = -1.96 \text{ V}$ , and  $V_D = +1.96 \text{ V}$ .  $R_G$  can be selected in the range of 1 MΩ to 10 MΩ.



**Figure 7.50** Biasing the MOSFET using a large drain-to-gate feedback resistance,  $R_G$ .

**Biasing Using a Drain-to-Gate Feedback Resistor** A simple and effective discrete-circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in Fig. 7.50. Here the large feedback resistance  $R_G$  (usually in the megohm range) forces the dc voltage at the gate to be equal to that at the drain (because  $I_G = 0$ ). Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D \quad (7.140)$$

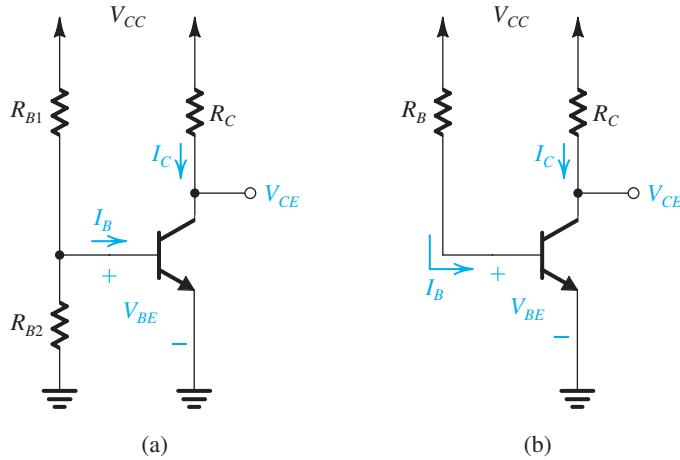
which is identical in form to Eq. (7.137), which describes the operation of the bias scheme discussed above [that in Fig. 7.48(a)]. Thus, here too, if  $I_D$  for some reason changes, say increases, then Eq. (7.140) indicates that  $V_{GS}$  must decrease. The decrease in  $V_{GS}$  in turn causes a decrease in  $I_D$ , a change that is opposite in direction to the one originally assumed. Thus the negative feedback or degeneration provided by  $R_G$  works to keep the value of  $I_D$  as constant as possible.

The circuit of Fig. 7.50 can be utilized as an amplifier by applying the input voltage signal to the gate via a coupling capacitor so as not to disturb the dc bias conditions already established. The amplified output signal at the drain can be coupled to another part of the circuit, again via a capacitor. We considered such an amplifier circuit in Section 7.2 (Example 7.3).

### EXERCISE

- D7.33** Design the circuit in Fig. 7.50 to operate at a dc drain current of 0.5 mA. Assume  $V_{DD} = +5$  V,  $k'_n W/L = 1$  mA/V<sup>2</sup>,  $V_t = 1$  V, and  $\lambda = 0$ . Use a standard 5% resistance value for  $R_D$ , and give the actual values obtained for  $I_D$  and  $V_D$ .

**Ans.**  $R_D = 6.2$  k $\Omega$ ;  $I_D \simeq 0.49$  mA;  $V_D \simeq 1.96$  V



**Figure 7.51** Two obvious schemes for biasing the BJT: (a) by fixing  $V_{BE}$ ; (b) by fixing  $I_B$ . Both result in wide variations in  $I_C$  and hence in  $V_{CE}$  and therefore are considered to be “bad.” Neither scheme is recommended.

### 7.4.2 The BJT Case

Before presenting the “good” biasing schemes, we should point out why two obvious arrangements are *not* good. First, attempting to bias the BJT by fixing the voltage  $V_{BE}$  by, for instance, using a voltage divider across the power supply  $V_{CC}$ , as shown in Fig. 7.51(a), is not a viable approach: The very sharp exponential relationship  $i_C - v_{BE}$  means that any small and inevitable differences in  $V_{BE}$  from the desired value will result in large differences in  $I_C$  and in  $V_{CE}$ . Second, biasing the BJT by establishing a constant current in the base, as shown in Fig. 7.51(b), where  $I_B \simeq (V_{CC} - 0.7)/R_B$ , is also not a recommended approach. Here the typically large variations in the value of  $\beta$  among units of the same device type will result in correspondingly large variations in  $I_C$  and hence in  $V_{CE}$ .

**The Classical Discrete-Circuit Bias Arrangement** Figure 7.52(a) shows the arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a single power supply is available. The technique consists of supplying the base of the transistor with a fraction of the supply voltage  $V_{CC}$  through the voltage divider  $R_1, R_2$ . In addition, a resistor  $R_E$  is connected to the emitter. This circuit is very similar to one we used for the MOSFET [Fig. 7.48(c)]. Here, however, the design must take into account the finite base current.

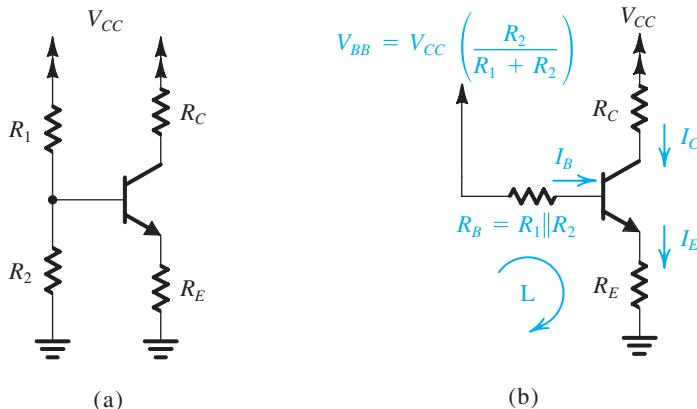
Figure 7.52(b) shows the same circuit with the voltage-divider network replaced by its Thévenin equivalent,

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \quad (7.141)$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \quad (7.142)$$

The current  $I_E$  can be determined by writing a Kirchhoff loop equation for the base–emitter–ground loop, labeled L, and substituting  $I_B = I_E/(\beta + 1)$ :

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta + 1)} \quad (7.143)$$



**Figure 7.52** Classical biasing for BJTs using a single power supply: (a) circuit; (b) circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

To make  $I_E$  insensitive to temperature and  $\beta$  variation,<sup>8</sup> we design the circuit to satisfy the following two constraints:

$$V_{BB} \gg V_{BE} \quad (7.144)$$

$$R_E \gg \frac{R_B}{\beta + 1} \quad (7.145)$$

Condition (7.144) ensures that small variations in  $V_{BE}$  ( $\approx 0.7$  V) will be swamped by the much larger  $V_{BB}$ . There is a limit, however, on how large  $V_{BB}$  can be: For a given value of the supply voltage  $V_{CC}$ , the higher the value we use for  $V_{BB}$ , the lower will be the sum of voltages across  $R_C$  and the collector–base junction ( $V_{CB}$ ). On the other hand, we want the voltage across  $R_C$  to be large in order to obtain high voltage gain and large signal swing (before transistor cutoff). We also want  $V_{CB}$  (or  $V_{CE}$ ) to be large, to provide a large signal swing (before transistor saturation). Thus, as is the case in any design, we have a set of conflicting requirements, and the solution must be a trade-off. As a rule of thumb, one designs for  $V_{BB}$  about  $\frac{1}{3}V_{CC}$ ,  $V_{CB}$  (or  $V_{CE}$ ) about  $\frac{1}{3}V_{CC}$ , and  $I_C R_C$  about  $\frac{1}{3}V_{CC}$ .

Condition (7.145) makes  $I_E$  insensitive to variations in  $\beta$  and could be satisfied by selecting  $R_B$  small. This in turn is achieved by using low values for  $R_1$  and  $R_2$ . Lower values for  $R_1$  and  $R_2$ , however, will mean a higher current drain from the power supply, and will result in a lowering of the input resistance of the amplifier (if the input signal is coupled to the base),<sup>9</sup> which is the trade-off involved in this part of the design. It should be noted that condition (7.145) means that we want to make the base voltage independent of the value of  $\beta$  and determined solely by the voltage divider. This will obviously be satisfied if the current in the divider is made much larger than the base current. Typically one selects  $R_1$  and  $R_2$  such that their current is in the range of  $I_E$  to  $0.1I_E$ .

Further insight regarding the mechanism by which the bias arrangement of Fig. 7.52(a) stabilizes the dc emitter (and hence collector) current is obtained by considering the feedback

<sup>8</sup>Bias design seeks to stabilize either  $I_E$  or  $I_C$  since  $I_C = \alpha I_E$  and  $\alpha$  varies very little. That is, a stable  $I_E$  will result in an equally stable  $I_C$ , and vice versa.

<sup>9</sup>If the input signal is coupled to the transistor base, the two bias resistances  $R_1$  and  $R_2$  effectively appear in parallel between the base and ground. Thus, low values for  $R_1$  and  $R_2$  will result in lowering  $R_{in}$ .

action provided by  $R_E$ . Consider that for some reason the emitter current increases. The voltage drop across  $R_E$ , and hence  $V_E$ , will increase correspondingly. Now, if the base voltage is determined primarily by the voltage divider  $R_1, R_2$ , which is the case if  $R_B$  is small, it will remain constant, and the increase in  $V_E$  will result in a corresponding decrease in  $V_{BE}$ . This in turn reduces the collector (and emitter) current, a change opposite to that originally assumed. Thus  $R_E$  provides a *negative feedback* action that stabilizes the bias current. This should remind the reader of the resistance  $R_e$  that we included in the emitter lead of the CE amplifier in Section 7.3.4. Also, the feedback action of  $R_E$  in the circuit of Fig. 7.52(a) is similar to the feedback action of  $R_S$  in the circuit of Fig. 7.48(c). We shall study negative feedback formally in Chapter 11.

### Example 7.12

We wish to design the bias network of the amplifier in Fig. 7.52 to establish a current  $I_E = 1 \text{ mA}$  using a power supply  $V_{CC} = +12 \text{ V}$ . The transistor is specified to have a nominal  $\beta$  value of 100.

#### Solution

We shall follow the rule of thumb mentioned above and allocate one-third of the supply voltage to the voltage drop across  $R_2$  and another one-third to the voltage drop across  $R_C$ , leaving one-third for possible negative signal swing at the collector. Thus,

$$\begin{aligned}V_B &= +4 \text{ V} \\V_E &= 4 - V_{BE} \simeq 3.3 \text{ V}\end{aligned}$$

and  $R_E$  is determined from

$$R_E = \frac{V_E}{I_E} = \frac{3.3}{1} = 3.3 \text{ k}\Omega$$

From the discussion above we select a voltage-divider current of  $0.1I_E = 0.1 \times 1 = 0.1 \text{ mA}$ . Neglecting the base current, we find

$$R_1 + R_2 = \frac{12}{0.1} = 120 \text{ k}\Omega$$

and

$$\frac{R_2}{R_1 + R_2} V_{CC} = 4 \text{ V}$$

Thus  $R_2 = 40 \text{ k}\Omega$  and  $R_1 = 80 \text{ k}\Omega$ .

At this point, it is desirable to find a more accurate estimate for  $I_E$ , taking into account the nonzero base current. Using Eq. (7.143),

$$I_E = \frac{4 - 0.7}{\frac{(80 \parallel 40)(\text{k}\Omega)}{3.3(\text{k}\Omega) + \frac{101}{101}}} = 0.93 \text{ mA}$$

**Example 7.12** *continued*

This is quite a bit lower than 1 mA, the value we are aiming for. It is easy to see from the above equation that a simple way to restore  $I_E$  to its nominal value would be to reduce  $R_E$  from 3.3 k $\Omega$  by the magnitude of the second term in the denominator (0.267 k $\Omega$ ). Thus a more suitable value for  $R_E$  in this case would be  $R_E = 3$  k $\Omega$ , which results in  $I_E = 1.01$  mA  $\simeq 1$  mA.<sup>10</sup>

It should be noted that if we are willing to draw a higher current from the power supply and to accept a lower input resistance for the amplifier, then we may use a voltage-divider current equal, say, to  $I_E$  (i.e., 1 mA), resulting in  $R_1 = 8$  k $\Omega$  and  $R_2 = 4$  k $\Omega$ . We shall refer to the circuit using these latter values as design 2, for which the actual value of  $I_E$  using the initial value of  $R_E$  of 3.3 k $\Omega$  will be

$$I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99 \simeq 1 \text{ mA}$$

In this case, design 2, we need not change the value of  $R_E$ .

Finally, the value of  $R_C$  can be determined from

$$R_C = \frac{12 - V_C}{I_C}$$

Substituting  $I_C = \alpha I_E = 0.99 \times 1 = 0.99$  mA  $\simeq 1$  mA results, for both designs, in

$$R_C = \frac{12 - 8}{1} = 4 \text{ k}\Omega$$

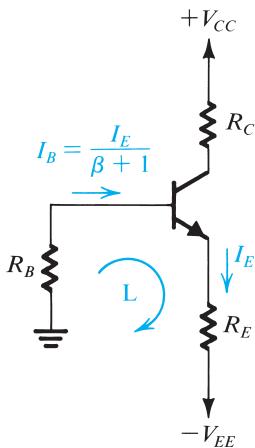
**EXERCISE**

- 7.34** For design 1 in Example 7.12, calculate the expected range of  $I_E$  if the transistor used has  $\beta$  in the range of 50 to 150. Express the range of  $I_E$  as a percentage of the nominal value ( $I_E \simeq 1$  mA) obtained for  $\beta = 100$ . Repeat for design 2.

**Ans.** For design 1: 0.94 mA to 1.04 mA, a 10% range; for design 2: 0.984 mA to 0.995 mA, a 1.1% range.

**A Two-Power-Supply Version of the Classical Bias Arrangement** A somewhat simpler bias arrangement is possible if two power supplies are available, as shown in Fig. 7.53.

<sup>10</sup>Although reducing  $R_E$  restores  $I_E$  to the design value of 1 mA, it does not solve the problem of the dependence of the value of  $I_E$  on  $\beta$ . See Exercise 7.34.



**Figure 7.53** Biasing the BJT using two power supplies. Resistor  $R_B$  is needed only if the signal is to be capacitively coupled to the base. Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total  $\beta$ -independence of the bias current.

Writing a loop equation for the loop labeled L gives

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)} \quad (7.146)$$

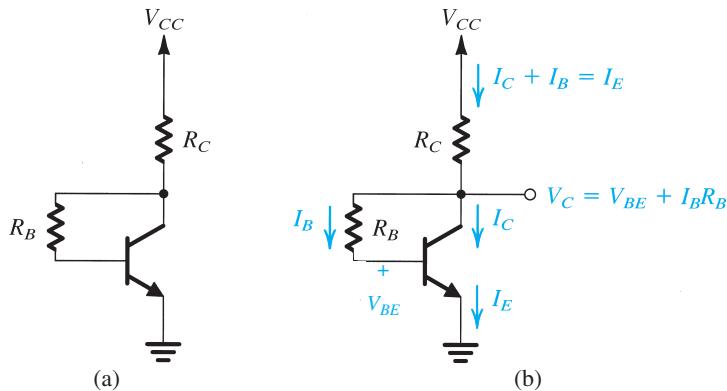
This equation is identical to Eq. (7.143) except for  $V_{EE}$  replacing  $V_{BB}$ . Thus the two constraints of Eqs. (7.144) and (7.145) apply here as well. Note that if the transistor is to be used with the base grounded (i.e., in the common-base configuration), then  $R_B$  can be eliminated altogether. On the other hand, if the input signal is to be coupled to the base, then  $R_B$  is needed. We shall study complete circuits of the various BJT amplifier configurations in Section 7.5. Finally, observe that the circuit in Fig. 7.53 is the counterpart of the MOS circuit in Fig. 7.48(e).

### EXERCISE

- D7.35** The bias arrangement of Fig. 7.53 is to be used for a common-base amplifier. Design the circuit to establish a dc emitter current of 1 mA and provide the highest possible voltage gain while allowing for a signal swing at the collector of  $\pm 2$  V. Use +10-V and -5-V power supplies.

**Ans.**  $R_B = 0$ ;  $R_E = 4.3 \text{ k}\Omega$ ;  $R_C = 8.4 \text{ k}\Omega$

**Biasing Using a Collector-to-Base Feedback Resistor** In the BJT case, there is a counterpart to the MOSFET circuit of Fig. 7.50. Figure 7.54(a) shows such a simple but effective biasing arrangement that is suitable for common-emitter amplifiers. The circuit employs a resistor  $R_B$  connected between the collector and the base. Resistor  $R_B$  provides negative feedback, which helps to stabilize the bias point of the BJT.



**Figure 7.54** (a) A common-emitter transistor amplifier biased by a feedback resistor  $R_B$ . (b) Analysis of the circuit in (a).

Analysis of the circuit is shown in Fig. 7.54(b), from which we can write

$$\begin{aligned}V_{CC} &= I_E R_C + I_B R_B + V_{BE} \\&= I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE}\end{aligned}$$

Thus the emitter bias current is given by

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B / (\beta + 1)} \quad (7.147)$$

It is interesting to note that this equation is identical to Eq. (7.143), which governs the operation of the traditional bias circuit, except that  $V_{CC}$  replaces  $V_{BB}$  and  $R_C$  replaces  $R_E$ . It follows that to obtain a value of  $I_E$  that is insensitive to variation of  $\beta$ , we select  $R_B / (\beta + 1) \ll R_C$ . Note, however, that the value of  $R_B$  determines the allowable negative signal swing at the collector since

$$V_{CB} = I_B R_B = I_E \frac{R_B}{\beta + 1} \quad (7.148)$$

### EXERCISE

**D7.36** Design the circuit of Fig. 7.54 to obtain a dc emitter current of 1 mA, maximum gain, and a  $\pm 2$ -V signal swing at the collector; that is, design for  $V_{CE} = +2.3$  V. Let  $V_{CC} = 10$  V and  $\beta = 100$ .

**Ans.**  $R_B = 162$  k $\Omega$ ;  $R_C = 7.7$  k $\Omega$ . Note that if standard 5% resistor values are used (Appendix J), we select  $R_B = 160$  k $\Omega$  and  $R_C = 7.5$  k $\Omega$ . This results in  $I_E = 1.02$  mA and  $V_C = +2.3$  V.

## 7.5 Discrete-Circuit Amplifiers

With our study of transistor amplifier basics complete, we now put everything together by presenting practical circuits for discrete-circuit amplifiers. These circuits, which utilize the amplifier configurations studied in Section 7.3 and the biasing methods of Section 7.4, can be assembled using off-the-shelf discrete transistors, resistors, and capacitors. Though practical and carefully selected to illustrate some important points, the circuits presented in this section should be regarded as examples of discrete-circuit transistor amplifiers. Indeed, there is a great variety of such circuits, a number of which are explored in the end-of-chapter problems.

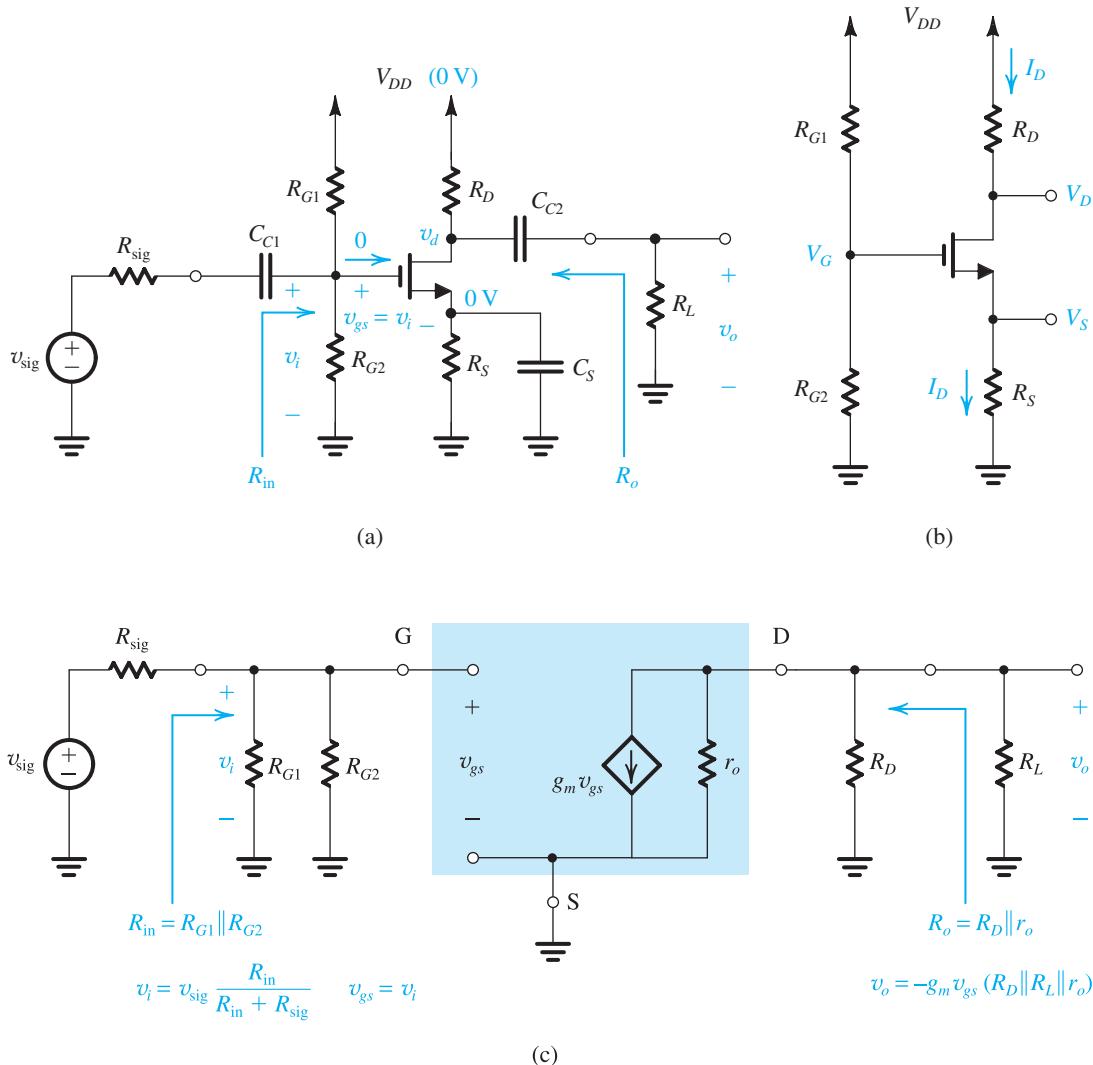
As mentioned earlier, the vast majority of discrete-circuit amplifiers utilize BJTs. This is reflected in this section where all the circuits presented except for one utilize BJTs. Of course, if desired, one can utilize MOSFETs in the same amplifier configurations presented here. Also, the MOSFET is the device of choice in the design of integrated-circuit (IC) amplifiers. We begin our study of IC amplifiers in Chapter 8.

As will be seen shortly, the circuits presented in this section utilize large capacitors (in the  $\mu\text{F}$  range) to couple the signal source to the input of the amplifier, and to couple the amplifier output signal to a load resistance or to the input of another amplifier stage. As well, a large capacitor is employed to establish a signal ground at the desired terminal of the transistor (e.g., at the emitter of a CE amplifier). The use of capacitors for these purposes simplifies the design considerably: Since capacitors block dc, one is able to first carry out the dc bias design and then connect the signal source and load to the amplifier without disturbing the dc design. These amplifiers are therefore known as **capacitively coupled amplifiers**.

### 7.5.1 A Common-Source (CS) Amplifier

As mentioned in Section 7.3, the common-source (CS) configuration is the most widely used of all MOSFET amplifier circuits. A common-source amplifier realized using the bias circuit of Fig. 7.48(c) is shown in Fig. 7.55(a). Observe that to establish a **signal ground**, or an **ac ground** as it is sometimes called, at the source, we have connected a large capacitor,  $C_s$ , between the source and ground. This capacitor, usually in the microfarad range, is required to provide a very small impedance (ideally, zero impedance—i.e., in effect, a short circuit) at all signal frequencies of interest. In this way, the signal current passes through  $C_s$  to ground and thus *bypasses* the resistance  $R_s$ ; hence,  $C_s$  is called a **bypass capacitor**. Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 10.1. For our purposes here we shall assume that  $C_s$  is acting as a perfect short circuit and thus is establishing a zero signal voltage at the MOSFET source.

To prevent disturbances to the dc bias current and voltages, the signal to be amplified, shown as voltage source  $v_{\text{sig}}$  with an internal resistance  $R_{\text{sig}}$ , is connected to the gate through a large capacitor  $C_{C1}$ . Capacitor  $C_{C1}$ , known as a **coupling capacitor**, is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc. Here again, we note that as the signal frequency is lowered, the impedance of  $C_{C1}$  (i.e.,  $1/j\omega C_{C1}$ ) will increase and its effectiveness as a coupling capacitor will be correspondingly reduced. This problem, too, will be considered in Section 10.1 in connection with the dependence of the amplifier



**Figure 7.55** (a) A common-source amplifier using the classical biasing arrangement of Fig. 7.48(c). (b) Circuit for determining the bias point. (c) Equivalent circuit and analysis.

operation on frequency. For our purposes here we shall assume that  $C_{C1}$  is acting as a perfect short circuit as far as the signal is concerned.

The voltage signal resulting at the drain is coupled to the load resistance  $R_L$  via another coupling capacitor  $C_{C2}$ . We shall assume that  $C_{C2}$  acts as a perfect short circuit at all signal frequencies of interest and thus that the output voltage  $v_o = v_d$ . Note that  $R_L$  can be either an actual load resistor, to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of another amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 9).

Since a capacitor behaves as an open circuit at dc, the circuit for performing the dc bias design and analysis is obtained by open-circuiting all capacitors. The resulting circuit is shown in Fig. 7.55(b) and can be designed as discussed in Section 7.4.1.

To determine the terminal characteristics of the CS amplifier of Fig. 7.55(a)—that is, its input resistance, voltage gain, and output resistance—we replace the MOSFET with its hybrid- $\pi$  small-signal model, replace  $V_{DD}$  with a signal ground, and replace all coupling and bypass capacitors with short circuits. The result is the circuit in Fig. 7.55(c). Analysis is straightforward and is shown on the figure, thus

$$R_{in} = R_{G1} \parallel R_{G2} \quad (7.149)$$

which shows that to keep  $R_{in}$  high, large values should be used for  $R_{G1}$  and  $R_{G2}$ , usually in the megohm range. The overall voltage gain  $G_v$  is

$$G_v = -\frac{R_{in}}{R_{in} + R_{sig}} g_m (R_D \parallel R_L \parallel r_o) \quad (7.150)$$

Observe that we have taken  $r_o$  into account, simply because it is easy to do so. Its effect, however, is usually small (this is not the case for IC amplifiers, as will be explained in Chapter 8). Finally, to encourage the reader to do the small-signal analysis directly on the original circuit diagram, with the MOSFET model used implicitly, we show some of the analysis on the circuit of Fig. 7.55(a).

### EXERCISES

- D7.37** Design the bias circuit in Fig. 7.55(b) for the CS amplifier of Fig. 7.55(a). Assume the MOSFET is specified to have  $V_t = 1$  V,  $k_n = 4$  mA/V<sup>2</sup>, and  $V_A = 100$  V. Neglecting the Early effect, design for  $I_D = 0.5$  mA,  $V_s = 3.5$  V, and  $V_D = 6$  V using a power-supply  $V_{DD} = 15$  V. Specify the values of  $R_s$  and  $R_D$ . If a current of 2  $\mu$ A is used in the voltage divider, specify the values of  $R_{G1}$  and  $R_{G2}$ . Give the values of the MOSFET parameters  $g_m$  and  $r_o$  at the bias point.

**Ans.**  $R_s = 7$  k $\Omega$ ;  $R_D = 18$  k $\Omega$ ;  $R_{G1} = 5$  M $\Omega$ ;  $R_{G2} = 2.5$  M $\Omega$ ;  $g_m = 2$  mA/V;  $r_o = 200$  k $\Omega$

- 7.38** For the CS amplifier of Fig. 7.55(a) use the design obtained in Exercise 7.37 to determine  $R_{in}$ ,  $R_o$ , and the overall voltage gain  $G_v$  when  $R_{sig} = 100$  k $\Omega$  and  $R_L = 20$  k $\Omega$ .

**Ans.** 1.67 M $\Omega$ ; 16.5 k $\Omega$ ; -17.1 V/V

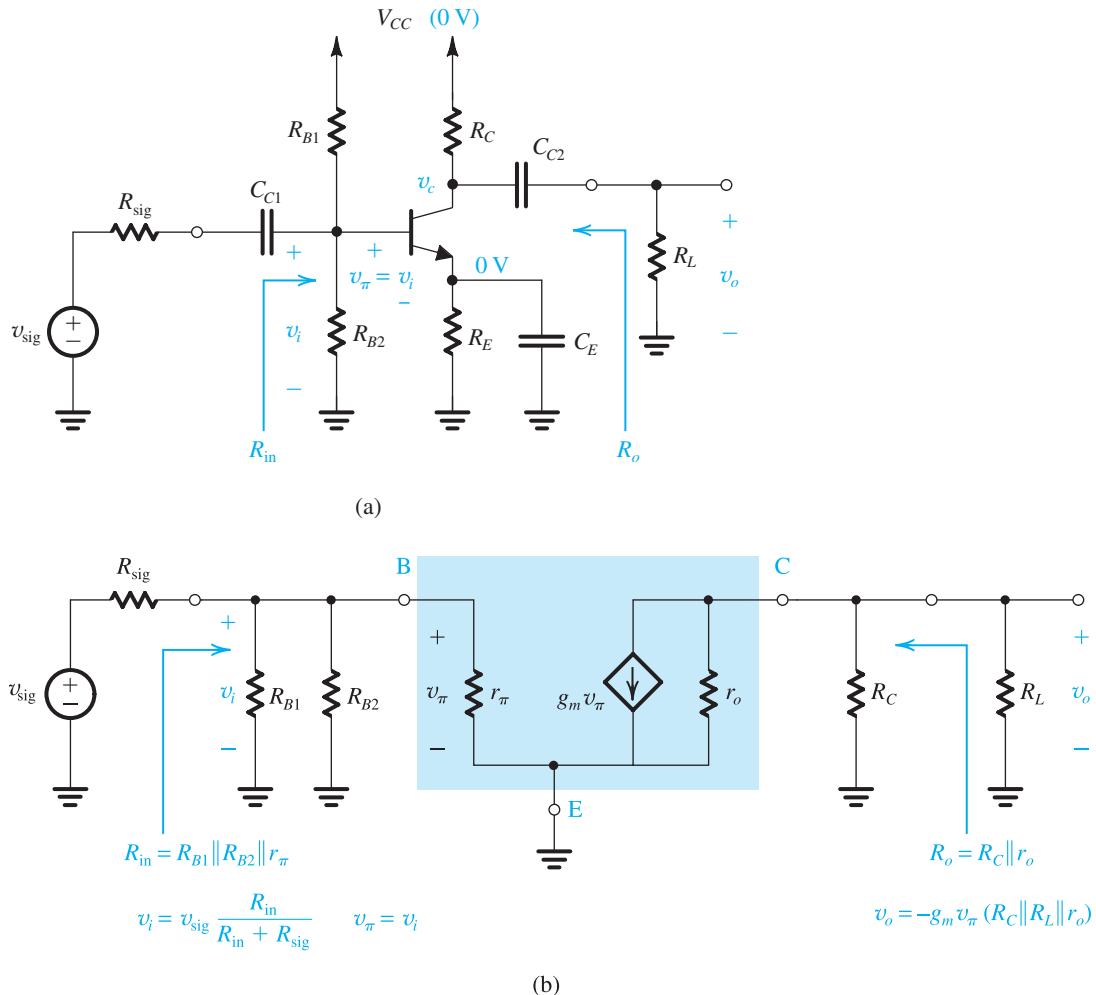
- D7.39** As discussed in Section 7.3, beneficial effects can be realized by having an unbypassed resistance  $R_s$  in the source lead of the CS amplifier. This can be implemented in the circuit of Fig. 7.55(a) by splitting the resistance  $R_s$  into two resistances:  $R_s$ , which is left unbypassed, and  $(R_s - R_s)$ , across which the bypass capacitor  $C_s$  is connected. Now, if in order to improve linearity of the amplifier in Exercises 7.37 and 7.38,  $v_{gs}$  is to be reduced to half its value, what value should  $R_s$  have? What would the amplifier gain  $G_v$  become? Recall that when  $R_s$  is included it becomes difficult to include  $r_o$  in the analysis, so neglect it.

**Ans.**  $R_s = 500$   $\Omega$ ;  $G_v = -8.9$  V/V

### 7.5.2 A Common-Emitter Amplifier

The common-emitter (CE) amplifier is the most widely used of all BJT amplifier configurations. Figure 7.56(a) shows a CE amplifier utilizing the classical biasing arrangement of Fig. 7.48(c), the design of which was considered in Section 7.4. The CE circuit in Fig. 7.54(a) is the BJT counterpart of the CS amplifier of Fig. 7.55(a). It utilizes coupling capacitors  $C_{C1}$  and  $C_{C2}$  and bypass capacitor  $C_E$ . Here we assume that these capacitors, while blocking dc, behave as perfect short circuits at all signal frequencies of interest.

To determine the characteristic parameters of the CE amplifier, we replace the BJT with its hybrid- $\pi$  model, replace  $V_{CC}$  with a short circuit to ground, and replace the coupling and bypass capacitor with short circuits. The resulting small-signal equivalent circuit of the CE amplifier is shown in Fig. 7.56(b). The analysis is straightforward and is given in the



**Figure 7.56** (a) A common-emitter amplifier using the classical biasing arrangement of Fig. 7.52(a). (b) Equivalent circuit and analysis.

figure, thus

$$R_{\text{in}} = R_{B1} \parallel R_{B2} \parallel r_{\pi} \quad (7.151)$$

which indicates that to keep  $R_{\text{in}}$  relatively high,  $R_{B1}$  and  $R_{B2}$  should be selected large (typically in the range of tens or hundreds of kilohms). This requirement conflicts with the need to keep  $R_{B1}$  and  $R_{B2}$  low so as to minimize the dependence of the dc current  $I_C$  on the transistor  $\beta$ . We discussed this design trade-off in Section 7.4.

The voltage gain  $G_v$  is given by

$$G_v = -\frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} g_m (R_C \parallel R_L \parallel r_o) \quad (7.152)$$

Note that we have taken  $r_o$  into account because it is easy to do so. However, as already mentioned, the effect of this parameter on discrete-circuit amplifier performance is usually small.

### EXERCISES

- D7.40** Design the bias circuit of the CE amplifier of Fig. 7.56(a) to obtain  $I_E = 0.5$  mA and  $V_C = +6$  V. Design for a dc voltage at the base of 5 V and a current through  $R_{B2}$  of 50  $\mu$ A. Let  $V_{CC} = +15$  V,  $\beta = 100$ , and  $V_{BE} \approx 0.7$  V. Specify the values of  $R_{B1}$ ,  $R_{B2}$ ,  $R_E$ , and  $R_C$ . Also give the values of the BJT small-signal parameters  $g_m$ ,  $r_{\pi}$ , and  $r_o$  at the bias point. (For the calculation of  $r_o$ , let  $V_A = 100$  V.)

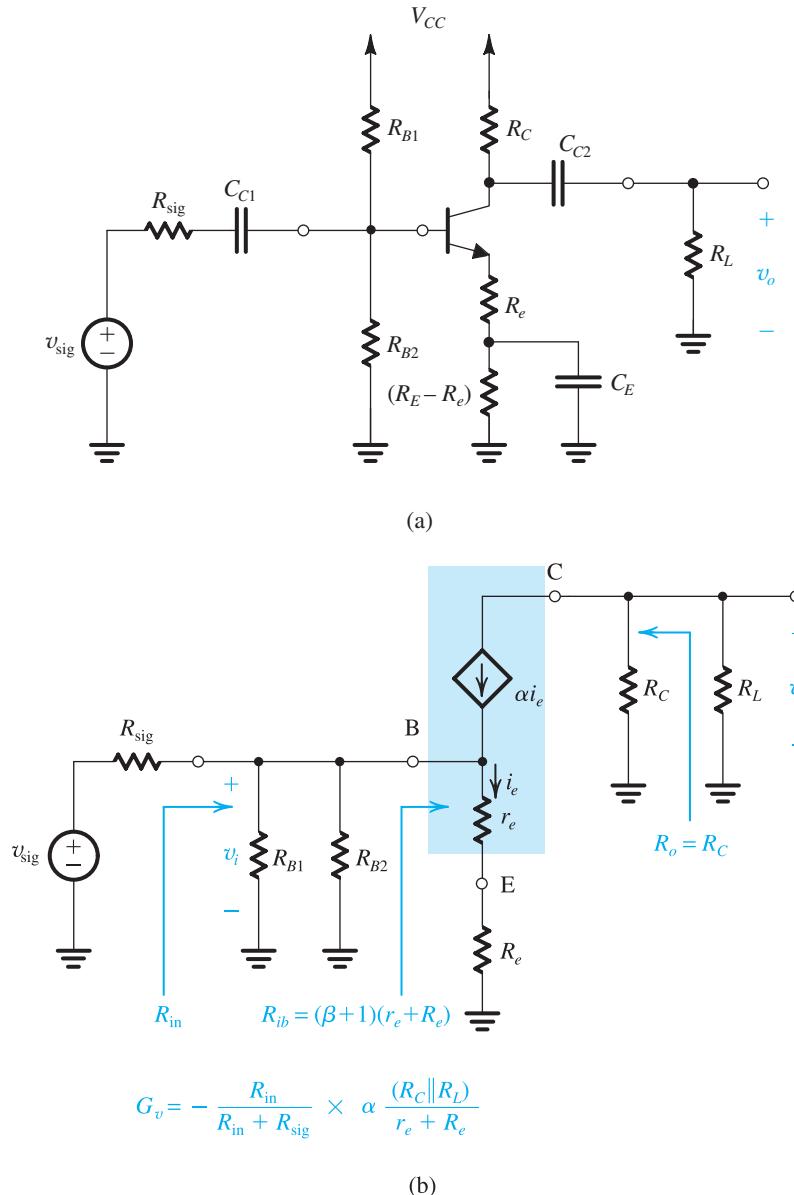
**Ans.**  $R_{B1} = 182$  k $\Omega$ ;  $R_{B2} = 100$  k $\Omega$ ;  $R_E = 8.6$  k $\Omega$ ;  $R_C = 18$  k $\Omega$ ;  $g_m = 20$  mA/V,  $r_{\pi} = 5$  k $\Omega$ ,  $r_o = 200$  k $\Omega$

- 7.41** For the amplifier designed in Exercise 7.40, find  $R_{\text{in}}$ ,  $R_o$ , and  $G_v$  when  $R_{\text{sig}} = 10$  k $\Omega$  and  $R_L = 20$  k $\Omega$ .

**Ans.**  $R_{\text{in}} = 4.64$  k $\Omega$ ;  $R_o = 16.51$  k $\Omega$ ;  $G_v = -57.3$  V/V

### 7.5.3 A Common-Emitter Amplifier with an Emitter Resistance $R_e$

As discussed in Section 7.3.4, it is beneficial to include a small resistance in the transistor emitter lead. This can be implemented in the circuit of Fig. 7.56(a) by splitting the emitter bias resistance  $R_E$  into two components: an unbypassed resistance  $R_e$ , and a resistance  $(R_E - R_e)$  across which the bypass capacitor  $C_E$  is connected. The resulting circuit is shown in Fig. 7.57(a) and its small-signal model is shown in Fig. 7.57(b). In the latter we utilize the T model of the BJT because it results in much simpler analysis (recall that this is always the case when a resistance is connected in series with the emitter). Also note that we have not included  $r_o$ , for doing so would complicate the analysis significantly. This burden would not be justified given that  $r_o$  has little effect on the performance of discrete-circuit amplifiers.



**Figure 7.57** (a) A common-emitter amplifier with an unbiased emitter resistance  $R_e$ . (b) The amplifier small-signal model and analysis.

Analysis of the circuit in Fig. 7.57(b) is straightforward and is shown in the figure. Thus,

$$\begin{aligned} R_{\text{in}} &= R_{B1} \parallel R_{B2} \parallel (\beta + 1)(r_e + R_e) \\ &= R_{B1} \parallel R_{B2} \parallel [r_\pi + (\beta + 1)R_e] \end{aligned} \quad (7.153)$$

from which we note that including  $R_e$  increases  $R_{in}$  because it increases the input resistance looking into the base by adding a component  $(\beta + 1)R_e$  to  $r_\pi$ . The overall voltage gain  $G_v$  is

$$\begin{aligned} G_v &= -\frac{R_{in}}{R_{in} + R_{sig}} \times \alpha \frac{\text{Total resistance in collector}}{\text{Total resistance in emitter}} \\ &= -\alpha \frac{R_{in}}{R_{in} + R_{sig}} \frac{R_C \parallel R_L}{r_e + R_e} \end{aligned} \quad (7.154)$$

### EXERCISE

- 7.42** For the amplifier designed in Exercise 7.40 and analyzed in Exercise 7.41, let it be required to raise  $R_{in}$  to 10 kΩ. What is the required value of  $R_e$ , and what does the overall voltage gain  $G_v$  become?

**Ans.**  $R_e = 67.7 \Omega$ ;  $G_v = -39.8 \text{ V/V}$

### 7.5.4 A Common-Base (CB) Amplifier

Figure 7.58(a) shows a CB amplifier designed using the biasing arrangement of Fig. 7.53. Note that the availability of two power supplies,  $V_{CC}$  and  $-V_{EE}$ , enables us to connect the base directly to ground, obviating the need for a large bypass capacitor to establish a signal ground at the base.

The small-signal equivalent circuit of the CB amplifier is shown in Fig. 7.58(b). As expected, we have utilized the T model of the BJT and have not included  $r_o$ . Including  $r_o$  would complicate the analysis significantly without making much difference to the results in the case of discrete-circuit amplifiers. From the circuit in Fig. 7.58(b) we find

$$R_{in} = r_e \parallel R_E \simeq r_e \simeq 1/g_m$$

which as expected can be very small, causing  $v_i$  to be a small fraction of  $v_{sig}$ ,

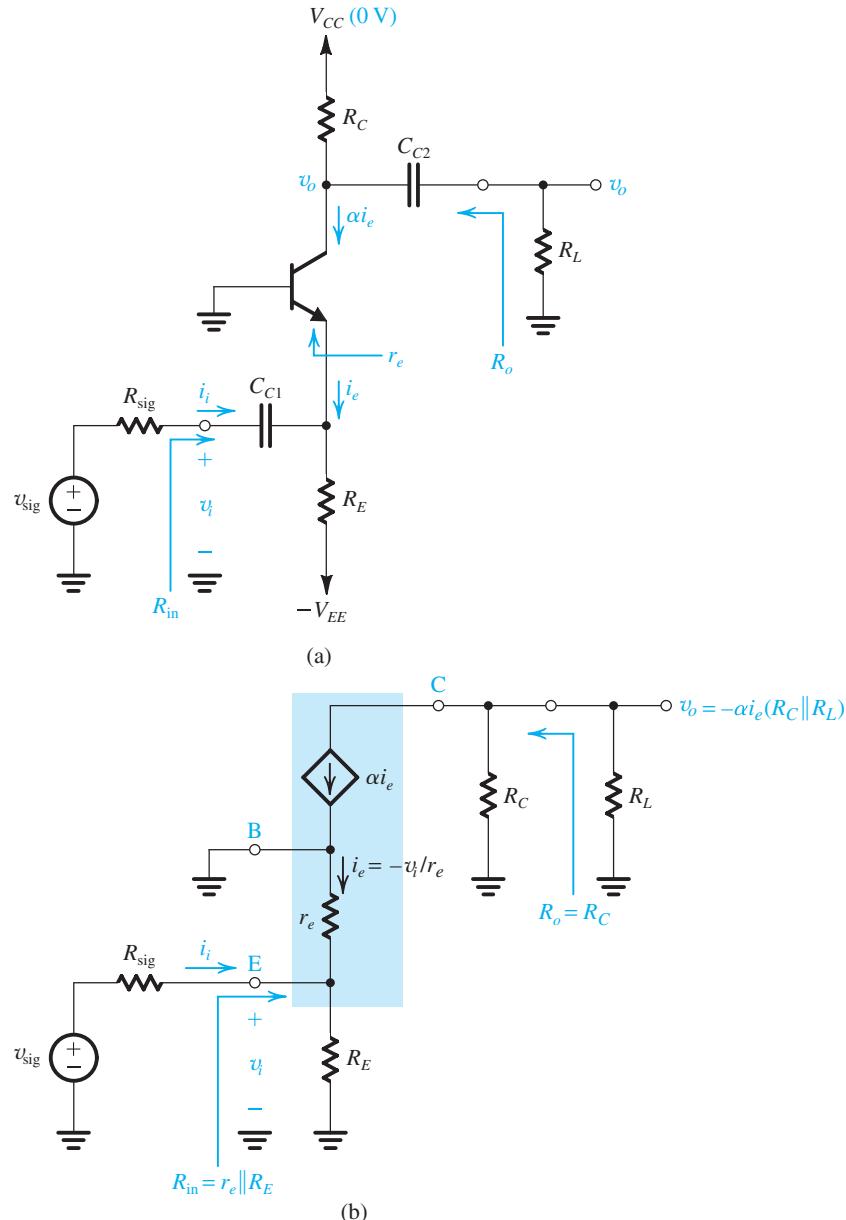
$$v_i = v_{sig} \frac{R_{in}}{R_{in} + R_{sig}}$$

Now,

$$i_e = -\frac{v_i}{r_e}$$

and

$$v_o = -\alpha i_e (R_C \parallel R_L)$$



**Figure 7.58** (a) A common-base amplifier using the structure of Fig. 7.53 with  $R_B$  omitted (since the base is grounded). (b) Equivalent circuit obtained by replacing the transistor with its T model.

Thus, the overall voltage gain is given by

$$G_v = \alpha \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \frac{R_C \parallel R_L}{r_e} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} g_m (R_C \parallel R_L) \quad (7.155)$$

**EXERCISE**

**D7.43** Design the CB amplifier of Fig. 7.58(a) to provide an input resistance  $R_{in}$  that matches the source resistance of a cable with a characteristic resistance of  $50 \Omega$ . Assume that  $R_E \gg r_e$ . The available power supplies are  $\pm 5$  V and  $R_L = 8 \text{ k}\Omega$ . Design for a dc collector voltage  $V_C = +1$  V. Specify the values of  $R_C$  and  $R_E$ . What overall voltage gain is obtained? If  $v_{sig}$  is a sine wave with a peak amplitude of 10 mV, what is the peak amplitude of the output voltage? Let  $\alpha \simeq 1$ .

**Ans.**  $R_C = 8 \text{ k}\Omega$ ;  $R_E = 8.6 \text{ k}\Omega$ ; 40 V/V; 0.4 V

### 7.5.5 An Emitter Follower

Figure 7.59(a) shows an emitter follower designed using the bias arrangement of Fig. 7.53 and two power supplies,  $V_{CC}$  and  $-V_{EE}$ . The bias resistance  $R_B$  affects the input resistance of the follower and should be chosen as large as possible while limiting the dc voltage drop across it to a small fraction of  $V_{EE}$ ; otherwise the dependence of the bias current  $I_C$  on  $\beta$  can become unacceptably large.

Figure 7.59(b) shows the small-signal equivalent circuit of the emitter follower. Here, as expected, we have replaced the BJT with its T model and included  $r_o$  (since this can be done very simply). The input resistance of the emitter follower can be seen to be

$$R_{in} = R_B \parallel R_{ib} \quad (7.156)$$

where  $R_{ib}$ , the input resistance looking into the base, can be obtained by using the resistance-reflection rule. Toward that end, note that  $r_o$  appears in parallel with  $R_E$  and  $R_L$  (which is why it can be easily taken into account). Thus,

$$R_{ib} = (\beta + 1)[r_e + (R_E \parallel r_o \parallel R_L)] \quad (7.157)$$

The overall voltage gain can be determined by tracking the signal transmission from source to load,

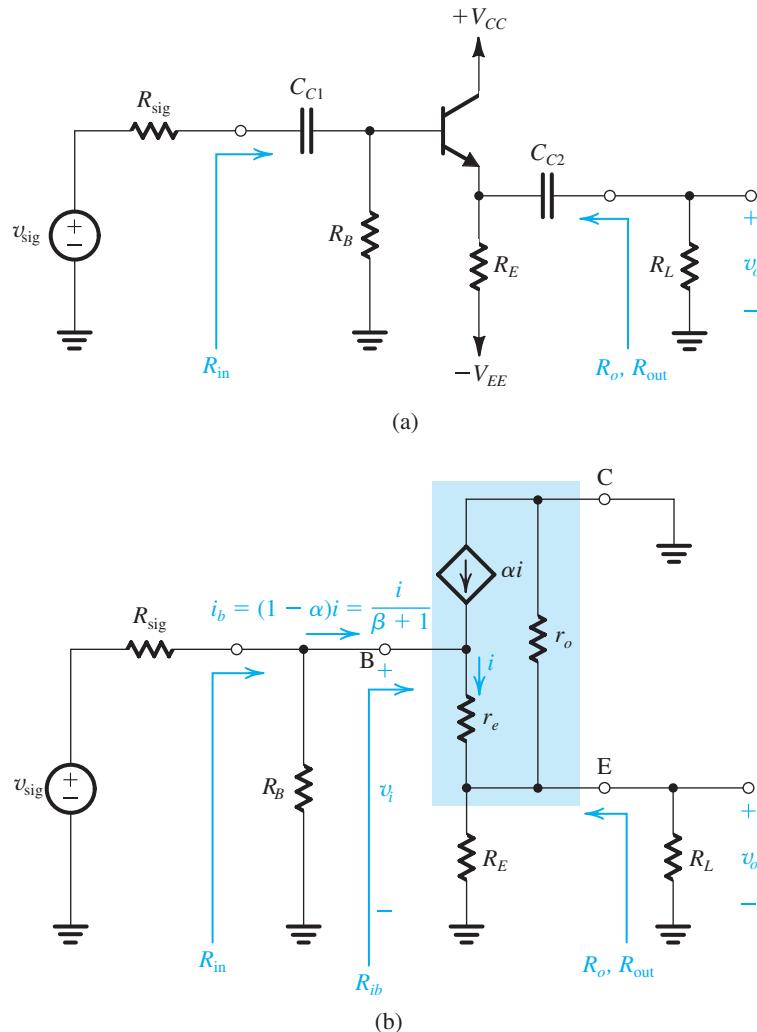
$$v_i = v_{sig} \frac{R_{in}}{R_{in} + R_{sig}} \quad (7.158)$$

and

$$v_o = v_i \frac{R_E \parallel r_o \parallel R_L}{r_e + (R_E \parallel r_o \parallel R_L)} \quad (7.159)$$

Thus,

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} \frac{(R_E \parallel r_o \parallel R_L)}{r_e + (R_E \parallel r_o \parallel R_L)} \quad (7.160)$$



**Figure 7.59** (a) An emitter-follower circuit. (b) Small-signal equivalent circuit of the emitter follower with the transistor replaced by its T model. Note that  $r_o$  is included because it is easy to do so. Normally, its effect on performance is small.

Finally, the output resistance  $R_{\text{out}}$  can be obtained by short-circuiting  $v_{\text{sig}}$  and looking back into the output terminal, excluding  $R_L$ , as

$$R_{\text{out}} = r_o \parallel R_E \parallel \left[ r_e + \frac{R_B \parallel R_{\text{sig}}}{\beta + 1} \right] \quad (7.161)$$

Note that we have used the inverse resistance-reflection rule, namely, dividing the total resistance in the base,  $(R_B \parallel R_{\text{sig}})$ , by  $(\beta + 1)$ .

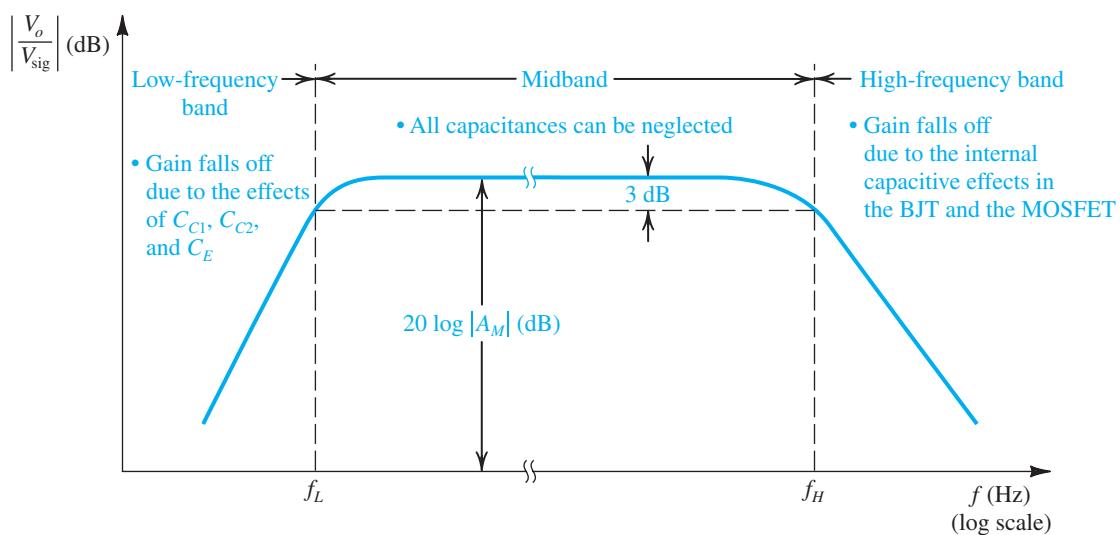
**EXERCISE**

**D7.44** Design the emitter follower of Fig. 7.59(a) to operate at a dc emitter current  $I_E = 1$  mA. Allow a dc voltage drop across  $R_B$  of 1 V. The available power supplies are  $\pm 5$  V,  $\beta = 100$ ,  $V_{BE} = 0.7$  V, and  $V_A = 100$  V. Specify the values required for  $R_B$  and  $R_E$ . Now if  $R_{\text{sig}} = 50$  k $\Omega$  and  $R_L = 1$  k $\Omega$ , find  $R_{\text{in}}$ ,  $v_i/v_{\text{sig}}$ ,  $v_o/v_i$ ,  $G_v$ , and  $R_{\text{out}}$ . (Note: In performing the bias design, neglect the Early effect.)

**Ans.**  $R_B = 100$  k $\Omega$ ;  $R_E = 3.3$  k $\Omega$ ; 44.3 k $\Omega$ ; 0.469 V/V; 0.968 V/V; 0.454 V/V; 320  $\Omega$

## 7.5.6 The Amplifier Frequency Response

Thus far, we have assumed that the gain of transistor amplifiers is constant independent of the frequency of the input signal. This would imply that transistor amplifiers have infinite bandwidth, which of course is not true. To illustrate, we show in Fig. 7.60 a sketch of the magnitude of the gain of a common-emitter or a CS amplifier such as those shown in Figs. 7.56 and 7.55, respectively, versus frequency. Observe that there is indeed a wide frequency range over which the gain remains almost constant. This obviously is the useful frequency range of



**Figure 7.60** Sketch of the magnitude of the gain of a CE (Fig. 7.56) or CS (Fig. 7.55) amplifier versus frequency. The graph delineates the three frequency bands relevant to frequency-response determination.

operation for the particular amplifier. Thus far, we have been assuming that our amplifiers are operating in this frequency band, called the **midband**.

Figure 7.60 indicates that at lower frequencies, the magnitude of amplifier gain falls off. This is because the coupling and bypass capacitors no longer have low impedances. Recall that we assumed that their impedances were small enough to act as short circuits. Although this can be true at midband frequencies, as the frequency of the input signal is lowered, the reactance  $1/j\omega C$  of each of these capacitors becomes significant, and it can be shown that this results in the overall voltage gain of the amplifier decreasing.

Figure 7.60 indicates also that the gain of the amplifier falls off at the high-frequency end. This is due to the internal capacitive effects in the BJT and the MOSFET. In Chapter 10 we shall study the internal capacitive effects of both transistor types and will augment their hybrid- $\pi$  models with capacitances that model these effects.

We will undertake a detailed study of the frequency response of transistor amplifiers in Chapter 10. For the time being, however, it is important for the reader to realize that for every transistor amplifier, there is a finite band over which the gain is almost constant. The boundaries of this useful frequency band, or midband, are the two frequencies  $f_L$  and  $f_H$  at which the gain drops by a certain number of decibels (usually 3 dB) below its value at midband. As indicated in Fig. 7.60, the amplifier **bandwidth**, or 3-dB bandwidth, is defined as the difference between the lower ( $f_L$ ) and upper or higher ( $f_H$ ) 3-dB frequencies:

$$BW = f_H - f_L$$

and since usually  $f_L \ll f_H$ ,

$$BW \simeq f_H$$

A figure of merit for the amplifier is its **gain-bandwidth product**, defined as

➤  $GB = |A_M|BW$

where  $|A_M|$  is the magnitude of the amplifier gain in the midband. It will be seen in Chapter 10 that in amplifier design it is usually possible to trade off gain for bandwidth. One way to accomplish this, for instance, is by including resistance  $R_e$  in the emitter of the CE amplifier.

## Summary

- The essence of the use of the MOSFET (the BJT) as an amplifier is that when the transistor is operated in the active region,  $v_{GS}$  controls  $i_D$  ( $v_{BE}$  controls  $i_C$ ) in the manner of a voltage-controlled current source. When the device is dc biased in the active region, and the signal  $v_{gs}$  ( $v_{be}$ ) is kept small, the operation becomes almost linear, with  $i_d = g_m v_{gs}$  ( $i_c = g_m v_{be}$ ).
- The most fundamental parameter in characterizing the small-signal linear operation of a transistor is the transconductance  $g_m$ . For a MOSFET,  $g_m = \mu_n C_{ox} (W/L) V_{ov} = \sqrt{2\mu_n C_{ox} (W/L)} I_D = 2I_D/V_{ov}$ ; and for the BJT,  $g_m = I_C/V_T$ .
- A systematic procedure for the analysis of a transistor amplifier circuit is presented in Table 7.1. Tables 7.2 and 7.3 present the small-signal models for the MOSFET and the BJT, respectively.
- When a resistance is connected in series with the source (or emitter), the T model is the most convenient to use.
- The three basic configurations of MOS and BJT amplifiers are presented in Fig. 7.33. Their characteristic parameter values are provided in Table 7.4 (for the MOS case) and in Table 7.5 (for the BJT case).
- The CS amplifier, which has (ideally) infinite input resistance and a reasonably high gain but a rather high output resistance and a limited high-frequency response (more on the latter point in Chapter 10), is used to obtain most of the gain in a cascade amplifier. Similar remarks apply to the CE amplifier, except that it has a relatively low input resistance ( $r_\pi = \beta/g_m$ ) arising from the finite base current of the BJT (finite  $\beta$ ). Its voltage gain, however, can be larger than that of the CS amplifier because of the higher values of  $g_m$  obtained with BJTs.
- Adding a resistance  $R_s$  in the source of a CS amplifier (a resistance  $R_e$  in the emitter of a CE amplifier) can lead to beneficial effects including the following: raising the input resistance of the CE amplifier, increasing linearity, and extending the useful amplifier bandwidth, at the expense of reducing the gain, all by a factor equal to  $(1 + g_m R_s)$  [ $(1 + g_m R_e)$  for the BJT case].
- The CG(CB) amplifier has a low input resistance and thus, used alone, it has limited and specialized applications. However, its excellent high-frequency response makes it attractive in combination with the CS(CE) amplifier (Chapters 8 and 10).
- The source follower has (ideally) infinite input resistance, a voltage gain lower than but close to unity, and a low output resistance. It is employed as a voltage buffer and as the output stage of a multistage amplifier. Similar remarks apply to the emitter follower except that its input resistance, though large, is finite. Specifically, the emitter follower multiplies the total resistance in the emitter by  $(\beta + 1)$  before presenting it to the signal source.
- The resistance-reflection rule is a powerful tool in the analysis of BJT amplifier circuits: All resistances in the emitter circuit including the emitter resistance  $r_e$  can be reflected to the base side by multiplying them by  $(\beta + 1)$ . Conversely, we can reflect all resistances in the base circuit to the emitter side by dividing them by  $(\beta + 1)$ .
- In the analysis and design of discrete-circuit amplifiers, it is rarely necessary to take the transistor output resistance  $r_o$  into account. In some situations, however,  $r_o$  can be easily taken into account; specifically in the CS(CE) amplifier and in the source(emitter) follower. In IC amplifiers,  $r_o$  must always be taken into account.
- A key step in the design of transistor amplifiers is to bias the transistor to operate at an appropriate point in the active region. A good bias design ensures that the parameters of the operating point ( $I_D$ ,  $V_{ov}$ , and  $V_{ds}$  for the MOSFET;  $I_C$  and  $V_{ce}$  for the BJT) are predictable and stable and do not vary by large amounts when the transistor is replaced by another of the same type. The bias methods studied in this chapter are suited for discrete-circuit amplifiers only because they utilize large coupling and bypass capacitors.
- Discrete-circuit amplifiers predominantly employ BJTs. The opposite is true for IC amplifiers, where the device of choice is the MOSFET.

# PROBLEMS

## Computer Simulation Problems

**SIM** Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

## Section 7.1: Basic Principles

**7.1** For the MOS amplifier of Fig. 7.2(a) with  $V_{DD} = 5$  V,  $V_t = 0.5$  V,  $k_n = 10 \text{ mA/V}^2$ , and  $R_D = 20 \text{ k}\Omega$ , determine the coordinates of the active-region segment (AB) of the VTC [Fig. 7.2(b)].

**D 7.2** For the MOS amplifier of Fig. 7.2(a) with  $V_{DD} = 5$  V and  $k_n = 5 \text{ mA/V}^2$ , it is required to have the end point of the VTC, point B, at  $V_{DS} = 0.5$  V. What value of  $R_D$  is required? If the transistor is replaced with another having twice the value of the transconductance parameter  $k_n$ , what new value of  $R_D$  is needed?

**D 7.3** It is required to bias the MOS amplifier of Fig. 7.3 at point Q for which  $V_{OV} = 0.2$  V and  $V_{DS} = 1$  V. Find the required value of  $R_D$  when  $V_{DD} = 5$  V,  $V_t = 0.5$  V, and  $k_n = 10 \text{ mA/V}^2$ . Also specify the coordinates of the VTC end point B. What is the small-signal voltage gain of this amplifier? Assuming linear operation, what is the maximum allowable negative signal swing at the output? What is the corresponding peak input signal?

**7.4** The MOS amplifier of Fig. 7.4(a), when operated with  $V_{DD} = 2$  V, is found to have a maximum small-signal voltage gain magnitude of 14 V/V. Find  $V_{OV}$  and  $V_{DS}$  for bias point Q at which a voltage gain of  $-12$  V/V is obtained.

**7.5** Consider the amplifier of Fig. 7.4(a) for the case  $V_{DD} = 5$  V,  $R_D = 24 \text{ k}\Omega$ ,  $k'_n(W/L) = 1 \text{ mA/V}^2$ , and  $V_t = 1$  V.

- Find the coordinates of the two end points of the saturation-region segment of the amplifier transfer characteristic, that is, points A and B on the sketch of Fig. 7.4(b).
- If the amplifier is biased to operate with an overdrive voltage  $V_{OV}$  of 0.5 V, find the coordinates of the bias point

Q on the transfer characteristic. Also, find the value of  $I_D$  and of the incremental gain  $A_v$  at the bias point.

- For the situation in (b), and disregarding the distortion caused by the MOSFET's square-law characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input while the transistor remains in saturation? What is the amplitude of the output voltage signal that results? What gain value does the combination of these amplitudes imply? By what percentage is this gain value different from the incremental gain value calculated above? Why is there a difference?

**7.6** Various measurements are made on an NMOS amplifier for which the drain resistor  $R_D$  is  $20 \text{ k}\Omega$ . First, dc measurements show the voltage across the drain resistor,  $V_{RD}$ , to be 1.5 V and the gate-to-source bias voltage to be 0.7 V. Then, ac measurements with small signals show the voltage gain to be  $-10$  V/V. What is the value of  $V_t$  for this transistor? If the process transconductance parameter  $k'_n$  is  $200 \mu\text{A/V}^2$ , what is the MOSFET's  $W/L$ ?

**\*7.7** The expression for the incremental voltage gain  $A_v$  given in Eq. (7.16) can be written as

$$A_v = -\frac{2(V_{DD} - V_{DS})}{V_{OV}}$$

where  $V_{DS}$  is the bias voltage at the drain. This expression indicates that for given values of  $V_{DD}$  and  $V_{OV}$ , the gain magnitude can be increased by biasing the transistor at a lower  $V_{DS}$ . This, however, reduces the allowable output signal swing in the negative direction. Assuming linear operation around the bias point, show that the largest possible negative output signal peak  $\hat{v}_o$  that is achievable while the transistor remains saturated is

$$\hat{v}_o = (V_{DS} - V_{OV}) / \left( 1 + \frac{1}{|A_v|} \right)$$

For  $V_{DD} = 5$  V and  $V_{OV} = 0.5$  V, provide a table of values for  $A_v$ ,  $\hat{v}_o$ , and the corresponding  $\hat{v}_i$  for  $V_{DS} = 1$  V, 1.5 V, 2 V, and 2.5 V. If  $k'_n(W/L) = 1 \text{ mA/V}^2$ , find  $I_D$  and  $R_D$  for the design for which  $V_{DS} = 1$  V.

**D \*7.8** Design the MOS amplifier of Fig. 7.4(a) to obtain maximum gain while allowing for an output voltage swing of at least  $\pm 0.5$  V. Let  $V_{DD} = 5$  V, and utilize an overdrive

voltage of approximately 0.2 V.

- Specify  $V_{DS}$  at the bias point.
- What is the gain achieved? What is the signal amplitude  $\hat{v}_{gs}$  that results in the 0.5-V signal amplitude at the output?
- If the dc bias current in the drain is to be 100  $\mu$ A, what value of  $R_D$  is needed?
- If  $k'_n = 200 \mu\text{A/V}^2$ , what  $W/L$  ratio is required for the MOSFET?

**\*7.9** Figure P7.9 shows an amplifier in which the load resistor  $R_D$  has been replaced with another NMOS transistor  $Q_2$  connected as a two-terminal device. Note that because  $v_{DG}$  of  $Q_2$  is zero, it will be operating in saturation at all times, even when  $v_t = 0$  and  $i_{D2} = i_{D1} = 0$ . Note also that the two transistors conduct equal drain currents. Using  $i_{D1} = i_{D2}$ , show that for the range of  $v_t$  over which  $Q_1$  is operating in saturation, that is, for

$$V_{t1} \leq v_t \leq v_o + V_{t1}$$

the output voltage will be given by

$$v_o = V_{DD} - V_t + \sqrt{\frac{(W/L)_1}{(W/L)_2}} V_t - \sqrt{\frac{(W/L)_1}{(W/L)_2}} v_t$$

where we have assumed  $V_{t1} = V_{t2} = V_t$ . Thus the circuit functions as a linear amplifier, even for large input signals. For  $(W/L)_1 = (50 \mu\text{m}/0.5 \mu\text{m})$  and  $(W/L)_2 = (5 \mu\text{m}/0.5 \mu\text{m})$ , find the voltage gain.

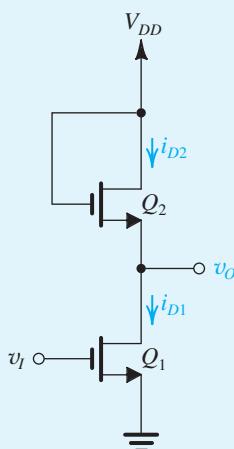


Figure P7.9

**7.10** A BJT amplifier circuit such as that in Fig. 7.6 is operated with  $V_{CC} = +5$  V and is biased at  $V_{CE} = +1$  V. Find the voltage gain, the maximum allowed output negative swing without the transistor entering saturation, and the corresponding maximum input signal permitted.

**7.11** For the amplifier circuit in Fig. 7.6 with  $V_{CC} = +5$  V and  $R_C = 1 \text{k}\Omega$ , find  $V_{CE}$  and the voltage gain at the following dc collector bias currents: 0.5 mA, 1 mA, 2.5 mA, 4 mA, and 4.5 mA. For each, give the maximum possible positive- and negative-output signal swing as determined by the need to keep the transistor in the active region. Present your results in a table.

**D 7.12** Consider the CE amplifier circuit of Fig. 7.6 when operated with a dc supply  $V_{CC} = +5$  V. It is required to find the point at which the transistor should be biased; that is, find the value of  $V_{CE}$  so that the output sine-wave signal  $v_{ce}$  resulting from an input sine-wave signal  $v_{be}$  of 5-mV peak amplitude has the maximum possible magnitude. What is the peak amplitude of the output sine wave and the value of the gain obtained? Assume linear operation around the bias point. (Hint: To obtain the maximum possible output amplitude for a given input, you need to bias the transistor as close to the edge of saturation as possible without entering saturation at any time, that is, without  $v_{CE}$  decreasing below 0.3 V.)

**7.13** A designer considers a number of low-voltage BJT amplifier designs utilizing power supplies with voltage  $V_{CC}$  of 1.0, 1.5, 2.0, or 3.0 V. For transistors that saturate at  $V_{CE} = 0.3$  V, what is the largest possible voltage gain achievable with each of these supply voltages? If in each case biasing is adjusted so that  $V_{CE} = V_{CC}/2$ , what gains are achieved? If a negative-going output signal swing of 0.4 V is required, at what  $V_{CE}$  should the transistor be biased to obtain maximum gain? What is the gain achieved with each of the supply voltages? (Notice that all of these gains are independent of the value of  $I_C$  chosen!)

**D \*7.14** A BJT amplifier such as that in Fig. 7.6 is to be designed to support relatively undistorted sine-wave output signals of peak amplitudes  $P$  volt without the BJT entering saturation or cutoff and to have the largest possible voltage gain, denoted  $A_v$  V/V. Show that the minimum supply voltage  $V_{CC}$  needed is given by

$$V_{CC} = V_{CESat} + P + |A_v|V_T$$

Also, find  $V_{CC}$ , specified to the nearest 0.5 V, for the following situations:

- (a)  $A_v = -20 \text{ V/V}, P = 0.2 \text{ V}$
- (b)  $A_v = -50 \text{ V/V}, P = 0.5 \text{ V}$
- (c)  $A_v = -100 \text{ V/V}, P = 0.5 \text{ V}$
- (d)  $A_v = -100 \text{ V/V}, P = 1.0 \text{ V}$
- (e)  $A_v = -200 \text{ V/V}, P = 1.0 \text{ V}$
- (f)  $A_v = -500 \text{ V/V}, P = 1.0 \text{ V}$
- (g)  $A_v = -500 \text{ V/V}, P = 2.0 \text{ V}$

**7.15** The transistor in the circuit of Fig. P7.15 is biased at a dc collector current of 0.3 mA. What is the voltage gain? (Hint: Use Thévenin's theorem to convert the circuit to the form in Fig. 7.6.)

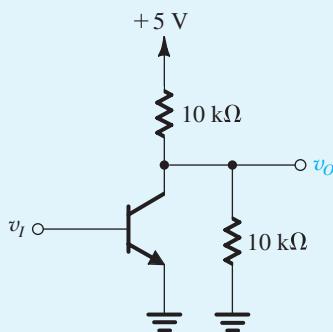


Figure P7.15

**7.16** Sketch and label the voltage-transfer characteristics of the *pnp* amplifiers shown in Fig. P7.16.

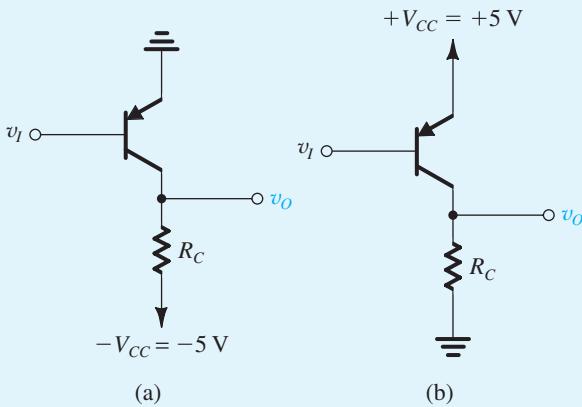


Figure P7.16

**\*7.17** In deriving the expression for small-signal voltage gain  $A_v$  in Eq. (7.21) we neglected the Early effect. Derive this expression including the Early effect by substituting

$$i_C = I_s e^{v_{BE}/V_T} \left( 1 + \frac{v_{CE}}{V_A} \right)$$

in Eq. (7.4) and including the factor  $(1 + V_{CE}/V_A)$  in Eq. (7.11). Show that the gain expression changes to

$$A_v = \frac{-I_C R_C / V_T}{\left[ 1 + \frac{I_C R_C}{V_A + V_{CE}} \right]} = -\frac{(V_{CC} - V_{CE}) / V_T}{\left[ 1 + \frac{V_{CC} - V_{CE}}{V_A + V_{CE}} \right]}$$

For the case  $V_{CC} = 5 \text{ V}$  and  $V_{CE} = 3 \text{ V}$ , what is the gain without and with the Early effect taken into account? Let  $V_A = 100 \text{ V}$ .

**7.18** When the amplifier circuit of Fig. 7.6 is biased with a certain  $V_{BE}$ , the dc voltage at the collector is found to be +2 V. For  $V_{CC} = +5 \text{ V}$  and  $R_C = 1 \text{ k}\Omega$ , find  $I_C$  and the small-signal voltage gain. For a change  $\Delta v_{BE} = +5 \text{ mV}$ , calculate the resulting  $\Delta v_O$ . Calculate it two ways: by using the transistor exponential characteristic  $\Delta i_C$ , and approximately, using the small-signal voltage gain. Repeat for  $\Delta v_{BE} = -5 \text{ mV}$ . Summarize your results in a table.

**\*7.19** Consider the amplifier circuit of Fig. 7.6 when operated with a supply voltage  $V_{CC} = +3 \text{ V}$ .

- (a) What is the theoretical maximum voltage gain that this amplifier can provide?
- (b) What value of  $V_{CE}$  must this amplifier be biased at to provide a voltage gain of  $-60 \text{ V/V}$ ?
- (c) If the dc collector current  $I_C$  at the bias point in (b) is to be 0.5 mA, what value of  $R_C$  should be used?
- (d) What is the value of  $V_{BE}$  required to provide the bias point mentioned above? Assume that the BJT has  $I_s = 10^{-15} \text{ A}$ .
- (e) If a sine-wave signal  $v_{be}$  having a 5-mV peak amplitude is superimposed on  $V_{BE}$ , find the corresponding output voltage signal  $v_{ce}$  that will be superimposed on  $V_{CE}$  assuming linear operation around the bias point.
- (f) Characterize the signal current  $i_c$  that will be superimposed on the dc bias current  $I_C$ .

- (g) What is the value of the dc base current  $I_B$  at the bias point? Assume  $\beta = 100$ . Characterize the signal current  $i_b$  that will be superimposed on the base current  $I_B$ .
- (h) Dividing the amplitude of  $v_{be}$  by the amplitude of  $i_b$ , evaluate the incremental (or small-signal) input resistance of the amplifier.
- (i) Sketch and clearly label correlated graphs for  $v_{BE}$ ,  $v_{CE}$ ,  $i_c$ , and  $i_b$  versus time. Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

**7.20** The essence of transistor operation is that a change in  $v_{BE}$ ,  $\Delta v_{BE}$ , produces a change in  $i_c$ ,  $\Delta i_c$ . By keeping  $\Delta v_{BE}$  small,  $\Delta i_c$  is approximately linearly related to  $\Delta v_{BE}$ ,  $\Delta i_c = g_m \Delta v_{BE}$ , where  $g_m$  is known as the transistor transconductance. By passing  $\Delta i_c$  through  $R_C$ , an output voltage signal  $\Delta v_o$  is obtained. Use the expression for the small-signal voltage gain in Eq. (7.20) to derive an expression for  $g_m$ . Find the value of  $g_m$  for a transistor biased at  $I_c = 0.5$  mA.

**7.21** The purpose of this problem is to illustrate the application of graphical analysis to the circuit shown in Fig. P7.21. Sketch  $i_c - v_{CE}$  characteristic curves for the BJT for  $i_b = 10$   $\mu$ A, 20  $\mu$ A, 30  $\mu$ A, and 40  $\mu$ A. Assume the lines to be horizontal (i.e., neglect the Early effect), and let  $\beta = 100$ . For  $V_{CC} = 5$  V and  $R_C = 1$  k $\Omega$ , sketch the load line. What peak-to-peak collector voltage swing will result for  $i_b$  varying

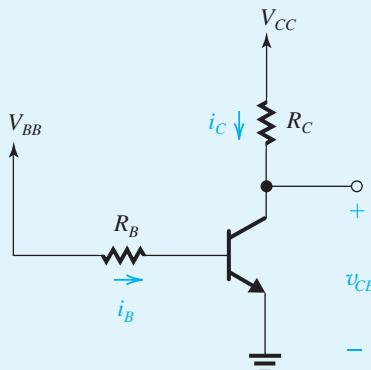


Figure P7.21

over the range 10  $\mu$ A to 40  $\mu$ A? If the BJT is biased at  $V_{CE} = \frac{1}{2}V_{CC}$ , find the value of  $I_C$  and  $I_B$ . If at this current  $V_{BE} = 0.7$  V and if  $R_B = 100$  k $\Omega$ , find the required value of  $V_{BB}$ .

**\*7.22** Sketch the  $i_c - v_{CE}$  characteristics of an *n*p*n* transistor having  $\beta = 100$  and  $V_A = 100$  V. Sketch characteristic curves for  $i_b = 20$   $\mu$ A, 50  $\mu$ A, 80  $\mu$ A, and 100  $\mu$ A. For the purpose of this sketch, assume that  $i_c = \beta i_b$  at  $v_{CE} = 0$ . Also, sketch the load line obtained for  $V_{CC} = 10$  V and  $R_C = 1$  k $\Omega$ . If the dc bias current into the base is 50  $\mu$ A, write the equation for the corresponding  $i_c - v_{CE}$  curve. Also, write the equation for the load line, and solve the two equations to obtain  $V_{CE}$  and  $I_c$ . If the input signal causes a sinusoidal signal of 30- $\mu$ A peak amplitude to be superimposed on  $I_b$ , find the corresponding signal components of  $i_c$  and  $v_{CE}$ .

## Section 7.2: Small-Signal Operation and Models

**\*7.23** This problem investigates the nonlinear distortion introduced by a MOSFET amplifier. Let the signal  $v_{gs}$  be a sine wave with amplitude  $V_{gs}$ , and substitute  $v_{gs} = V_{gs} \sin \omega t$  in Eq. (7.28). Using the trigonometric identity  $\sin^2 \theta = \frac{1}{2} - \frac{1}{2} \cos 2\theta$ , show that the ratio of the signal at frequency  $2\omega$  to that at frequency  $\omega$ , expressed as a percentage (known as the second-harmonic distortion) is

$$\text{Second-harmonic distortion} = \frac{1}{4} \frac{V_{gs}}{V_{ov}} \times 100$$

If in a particular application  $V_{gs}$  is 10 mV, find the minimum overdrive voltage at which the transistor should be operated so that the second-harmonic distortion is kept to less than 1%.

**7.24** Consider an NMOS transistor having  $k_n = 10$  mA/V<sup>2</sup>. Let the transistor be biased at  $V_{ov} = 0.2$  V. For operation in saturation, what dc bias current  $I_D$  results? If a 0.02-V signal is superimposed on  $V_{GS}$ , find the corresponding increment in collector current by evaluating the total collector current  $i_D$  and subtracting the dc bias current  $I_D$ . Repeat for a -0.02-V signal. Use these results to estimate  $g_m$  of the FET at this bias point. Compare with the value of  $g_m$  obtained using Eq. (7.33).

**7.25** Consider the FET amplifier of Fig. 7.10 for the case  $V_t = 0.4$  V,  $k_n = 5$  mA/V<sup>2</sup>,  $V_{GS} = 0.6$  V,  $V_{DD} = 1.8$  V, and  $R_D = 10$  kΩ.

- (a) Find the dc quantities  $I_D$  and  $V_{DS}$ .
- (b) Calculate the value of  $g_m$  at the bias point.
- (c) Calculate the value of the voltage gain.
- (d) If the MOSFET has  $\lambda = 0.1$  V<sup>-1</sup>, find  $r_o$  at the bias point and calculate the voltage gain.

**D \*7.26** An NMOS amplifier is to be designed to provide a 0.20-V peak output signal across a 20-kΩ load that can be used as a drain resistor. If a gain of at least 10 V/V is needed, what  $g_m$  is required? Using a dc supply of 1.8 V, what values of  $I_D$  and  $V_{OV}$  would you choose? What  $W/L$  ratio is required if  $\mu_n C_{ox} = 200$  μA/V<sup>2</sup>? If  $V_t = 0.4$  V, find  $V_{GS}$ .

**D \*7.27** In this problem we investigate an optimum design of the CS amplifier circuit of Fig. 7.10. First, use the voltage gain expression  $A_v = -g_m R_D$  together with Eq. (7.42) for  $g_m$  to show that

$$A_v = -\frac{2I_D R_D}{V_{OV}} = -\frac{2(V_{DD} - V_{DS})}{V_{OV}}$$

Next, let the maximum positive input signal be  $\hat{v}_i$ . To keep the second-harmonic distortion to an acceptable level, we bias the MOSFET to operate at an overdrive voltage  $V_{OV} \gg \hat{v}_i$ . Let  $V_{OV} = m\hat{v}_i$ . Now, to maximize the voltage gain  $|A_v|$ , we design for the lowest possible  $V_{DS}$ . Show that the minimum  $V_{DS}$  that is consistent with allowing a negative signal voltage swing at the drain of  $|A_v| \hat{v}_i$  while maintaining saturation-mode operation is given by

$$V_{DS} = \frac{V_{OV} + \hat{v}_i + 2V_{DD}(\hat{v}_i/V_{OV})}{1 + 2(\hat{v}_i/V_{OV})}$$

Now, find  $V_{OV}$ ,  $V_{DS}$ ,  $A_v$ , and  $\hat{v}_o$  for the case  $V_{DD} = 2.5$  V,  $\hat{v}_i = 20$  mV, and  $m = 15$ . If it is desired to operate this transistor at  $I_D = 200$  μA, find the values of  $R_D$  and  $W/L$ , assuming that for this process technology  $k'_n = 100$  μA/V<sup>2</sup>.

**7.28** In the table below, for MOS transistors operating under a variety of conditions, complete as many entries as possible. Although some data is not available, it is always possible to calculate  $g_m$  using one of Eqs. (7.40), (7.41), or (7.42). Assume  $\mu_n = 500$  cm<sup>2</sup>/V·s,  $\mu_p = 250$  cm<sup>2</sup>/V·s, and  $C_{ox} = 0.4$  fF/μm<sup>2</sup>.

Case	Type	Voltages (V)			Dimensions (μm)					
		$I_D$ (mA)	$ V_{GS} $	$ V_t $	$V_{OV}$	$W$	$L$	$W/L$	$K'(W/L)$	$g_m$ (mA/V)
a	N	1	3	2			1			
b	N	1		0.7	0.5					
c	N	10			2	50				
d	N	0.5			0.5					
e	N	0.1								
f	N		1.8	0.8		10	2			
g	P	0.5				40	4			
h	P		3	1					25	0.5
i	P	10				4000	2			
j	P	10			4					
k	P				1	30	3			
l	P				5					0.08

**7.29** An NMOS technology has  $\mu_n C_{ox} = 250 \mu\text{A/V}^2$  and  $V_t = 0.5 \text{ V}$ . For a transistor with  $L = 0.5 \mu\text{m}$ , find the value of  $W$  that results in  $g_m = 2 \text{ mA/V}$  at  $I_D = 0.25 \text{ mA}$ . Also, find the required  $V_{GS}$ .

**7.30** For the NMOS amplifier in Fig. P7.30, replace the transistor with its T equivalent circuit, assuming  $\lambda = 0$ . Derive expressions for the voltage gains  $v_s/v_i$  and  $v_d/v_i$ .

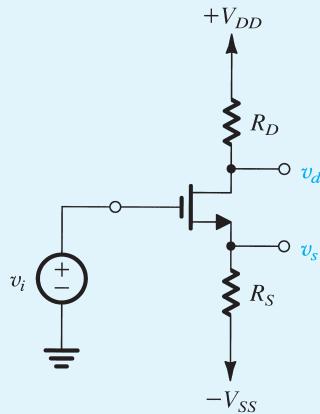


Figure P7.30

**SIM 7.31** In the circuit of Fig. P7.31, the NMOS transistor has  $|V_t| = 0.5 \text{ V}$  and  $V_A = 50 \text{ V}$  and operates with  $V_D = 1 \text{ V}$ . What is the voltage gain  $v_o/v_i$ ? What do  $V_D$  and the gain become for  $I$  increased to  $1 \text{ mA}$ ?

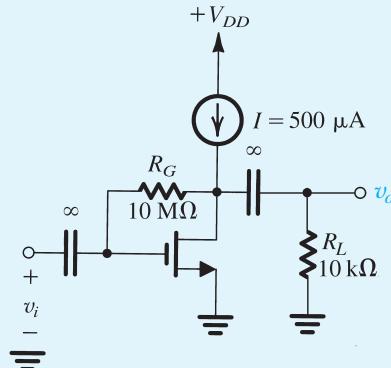


Figure P7.31

**7.32** For a  $0.18\text{-}\mu\text{m}$  CMOS fabrication process:  $V_m = 0.5 \text{ V}$ ,  $V_{tp} = -0.5 \text{ V}$ ,  $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ ,  $\mu_p C_{ox} = 100 \mu\text{A/V}^2$ ,  $C_{ox} = 8.6 \text{ fF}/\mu\text{m}^2$ ,  $V_A$  ( $n$ -channel devices) =  $5L$  ( $\mu\text{m}$ ), and  $|V_A|$  ( $p$ -channel devices) =  $6L$  ( $\mu\text{m}$ ). Find the small-signal model parameters ( $g_m$  and  $r_o$ ) for both an NMOS and a PMOS transistor having  $W/L = 10 \mu\text{m}/0.5 \mu\text{m}$  and operating at  $I_D = 100 \mu\text{A}$ . Also, find the overdrive voltage at which each device must be operating.

**\*7.33** Figure P7.33 shows a discrete-circuit amplifier. The input signal  $v_{sig}$  is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite). All capacitors behave as short circuits for signals and as open circuits for dc.

- If the transistor has  $V_t = 1 \text{ V}$ , and  $k_h = 4 \text{ mA/V}^2$ , verify that the bias circuit establishes  $V_{GS} = 1.5 \text{ V}$ ,  $I_D = 0.5 \text{ mA}$ , and  $V_D = +7.0 \text{ V}$ . That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
- Find  $g_m$  and  $r_o$  if  $V_A = 100 \text{ V}$ .
- Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.
- Find  $R_{in}$ ,  $v_{gs}/v_{sig}$ ,  $v_o/v_{gs}$ , and  $v_o/v_{sig}$ .

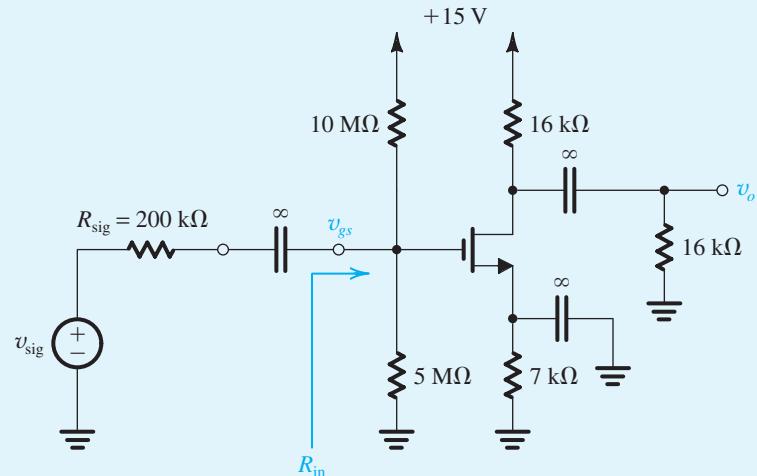


Figure P7.33

**7.34** Consider a transistor biased to operate in the active mode at a dc collector current  $I_C$ . Calculate the collector signal current as a fraction of  $I_C$  (i.e.,  $i_c/I_C$ ) for input signals  $v_{be}$  of  $+1\text{ mV}$ ,  $-1\text{ mV}$ ,  $+2\text{ mV}$ ,  $-2\text{ mV}$ ,  $+5\text{ mV}$ ,  $-5\text{ mV}$ ,  $+8\text{ mV}$ ,  $-8\text{ mV}$ ,  $+10\text{ mV}$ ,  $-10\text{ mV}$ ,  $+12\text{ mV}$ , and  $-12\text{ mV}$ . In each case do the calculation two ways:

- (a) using the exponential characteristic, and
- (b) using the small-signal approximation.

Present your results in the form of a table that includes a column for the error introduced by the small-signal approximation. Comment on the range of validity of the small-signal approximation.

**7.35** An *npn* BJT with grounded emitter is operated with  $V_{BE} = 0.700\text{ V}$ , at which the collector current is  $0.5\text{ mA}$ . A  $5\text{-k}\Omega$  resistor connects the collector to a  $+5\text{-V}$  supply. What is the resulting collector voltage  $V_C$ ? Now, if a signal applied to the base raises  $v_{BE}$  to  $705\text{ mV}$ , find the resulting total collector current  $i_c$  and total collector voltage  $v_c$  using the exponential  $i_c-v_{BE}$  relationship. For this situation, what are  $v_{be}$  and  $v_c$ ? Calculate the voltage gain  $v_c/v_{be}$ . Compare with the value obtained using the small-signal approximation, that is,  $-g_m R_c$ .

**7.36** A transistor with  $\beta = 100$  is biased to operate at a dc collector current of  $0.5\text{ mA}$ . Find the values of  $g_m$ ,  $r_\pi$ , and  $r_e$ . Repeat for a bias current of  $50\text{ }\mu\text{A}$ .

**7.37** A *pnp* BJT is biased to operate at  $I_C = 1.0\text{ mA}$ . What is the associated value of  $g_m$ ? If  $\beta = 100$ , what is the value of the small-signal resistance seen looking into the emitter ( $r_e$ )? Into the base ( $r_\pi$ )? If the collector is connected to a  $5\text{-k}\Omega$  load, with a signal of  $5\text{-mV}$  peak applied between base and emitter, what output signal voltage results?

**D 7.38** A designer wishes to create a BJT amplifier with a  $g_m$  of  $30\text{ mA/V}$  and a base input resistance of  $3000\text{ }\Omega$  or more.

What collector-bias current should he choose? What is the minimum  $\beta$  he can tolerate for the transistor used?

**7.39** A transistor operating with nominal  $g_m$  of  $40\text{ mA/V}$  has a  $\beta$  that ranges from  $50$  to  $150$ . Also, the bias circuit, being less than ideal, allows a  $\pm 20\%$  variation in  $I_C$ . What are the extreme values found of the resistance looking into the base?

**7.40** In the circuit of Fig. 7.20,  $V_{BE}$  is adjusted so that  $V_C = 1\text{ V}$ . If  $V_{CC} = 3\text{ V}$ ,  $R_C = 2\text{ k}\Omega$ , and a signal  $v_{be} = 0.005 \sin \omega t$  volts is applied, find expressions for the total instantaneous quantities  $i_c(t)$ ,  $v_c(t)$ , and  $i_B(t)$ . The transistor has  $\beta = 100$ . What is the voltage gain?

**D \*7.41** We wish to design the amplifier circuit of Fig. 7.20 under the constraint that  $V_{CC}$  is fixed. Let the input signal  $v_{be} = \hat{V}_{be} \sin \omega t$ , where  $\hat{V}_{be}$  is the maximum value for acceptable linearity. For the design that results in the largest signal at the collector, without the BJT leaving the active region, show that

$$R_C I_C = (V_{CC} - 0.3) / \left( 1 + \frac{\hat{V}_{be}}{V_T} \right)$$

and find an expression for the voltage gain obtained. For  $V_{CC} = 3\text{ V}$  and  $\hat{V}_{be} = 5\text{ mV}$ , find the dc voltage at the collector, the amplitude of the output voltage signal, and the voltage gain.

**7.42** The table below summarizes some of the basic attributes of a number of BJTs of different types, operating as amplifiers under various conditions. Provide the missing entries. (Note: Isn't it remarkable how much two parameters can reveal?)

**7.43** A BJT is biased to operate in the active mode at a dc collector current of  $1\text{ mA}$ . It has a  $\beta$  of  $100$  and  $V_A$  of  $100\text{ V}$ . Give the four small-signal models (Figs. 7.25 and 7.27) of the BJT complete with the values of their parameters.

Transistor	a	b	c	d	e	f	g
$\alpha$	1.000					0.90	
$\beta$		100				5	
$I_C$ (mA)	1.00		1.00				
$I_E$ (mA)		1.00					
$I_B$ (mA)			0.020				
$g_m$ (mA/V)							1.10
$r_e$ ( $\Omega$ )					100		700
$r_\pi$ ( $\Omega$ )					10.1 k $\Omega$		

**7.44** Using the T model of Fig. 7.26(a), show that the input resistance between base and emitter, looking into the base, is equal to  $r_\pi$ .

**7.45** Show that the collector current provided by the model of Fig. 7.26(b) is equal to that provided by the model in Fig. 7.26(a).

**7.46** Show that the hybrid- $\pi$  model of Fig. 7.24(b) is the incremental version of the large-signal model of Fig. 6.5(d).

**7.47** Show that the T model of Fig. 7.26(b) is the incremental version of the large-signal model of Fig. 6.5(b).

**7.48** The transistor amplifier in Fig. P7.48 is biased with a current source  $I$  and has a very high  $\beta$ . Find the dc voltage at the collector,  $V_C$ . Also, find the value of  $r_e$ . Replace the transistor with the T model of Fig. 7.26(b) (note that the dc current source  $I$  should be replaced with an open circuit). Hence find the voltage gain  $v_c/v_i$ .

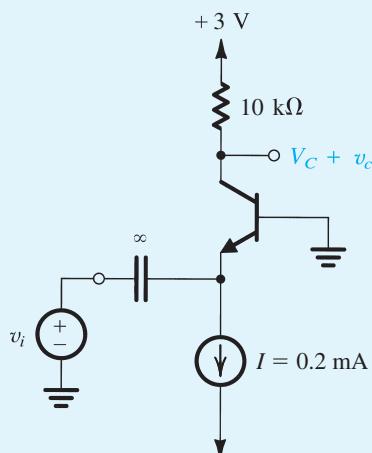


Figure P7.48

**7.49** For the conceptual circuit shown in Fig. 7.23,  $R_C = 2 \text{ k}\Omega$ ,  $g_m = 50 \text{ mA/V}$ , and  $\beta = 100$ . If a peak-to-peak output voltage of 1 V is measured at the collector, what are the peak-to-peak values of  $v_{be}$  and  $i_b$ ?

**7.50** Figure P7.50 shows the circuit of an amplifier fed with a signal source  $v_{\text{sig}}$  with a source resistance  $R_{\text{sig}}$ . The bias circuitry is not shown. Replace the BJT with its hybrid- $\pi$  equivalent circuit of Fig. 7.24(a). Find the input resistance  $R_{\text{in}} \equiv v_\pi/i_b$ , the voltage transmission from source to amplifier

input,  $v_\pi/v_{\text{sig}}$ , and the voltage gain from base to collector,  $v_o/v_\pi$ . Use these to show that the overall voltage gain  $v_o/v_{\text{sig}}$  is given by

$$\frac{v_o}{v_{\text{sig}}} = -\frac{\beta R_C}{r_\pi + R_{\text{sig}}}$$

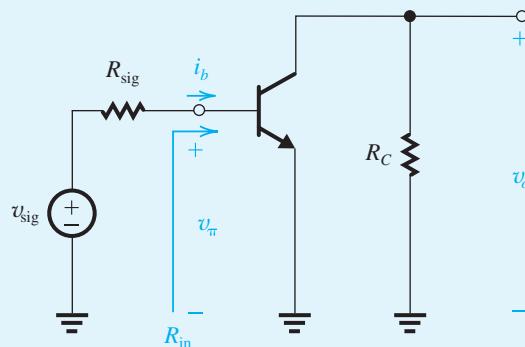


Figure P7.50

**7.51** Figure P7.51 shows a transistor with the collector connected to the base. The bias arrangement is not shown. Since a zero  $v_{BC}$  implies operation in the active mode, the BJT can be replaced by one of the small-signal models of Figs. 7.24 and 7.26. Use the model of Fig. 7.26(b) and show that the resulting two-terminal device, known as a diode-connected transistor, has a small-signal resistance  $r$  equal to  $r_e$ .

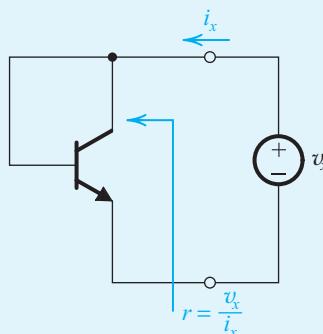


Figure P7.51

**7.52** Figure P7.52 shows a particular configuration of BJT amplifiers known as “emitter follower.” The bias arrangement is not shown. Replace the BJT with its T equivalent-circuit

model of Fig. 7.26(b). Show that

$$R_{in} \equiv \frac{v_i}{i_b} = (\beta + 1)(r_e + R_e)$$

$$\frac{v_o}{v_i} = \frac{R_e}{R_e + r_e}$$

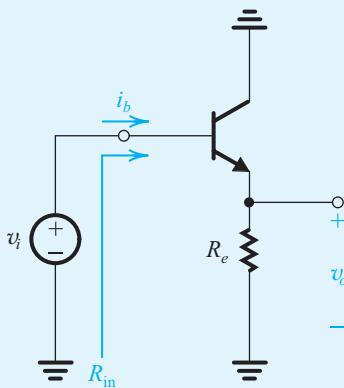


Figure P7.52

**7.53** For the circuit shown in Fig. P7.53, draw a complete small-signal equivalent circuit utilizing an appropriate T model for the BJT (use  $\alpha = 0.99$ ). Your circuit should show the values of all components, including the model parameters. What is the input resistance  $R_{in}$ ? Calculate the overall voltage gain ( $v_o/v_{sig}$ ).

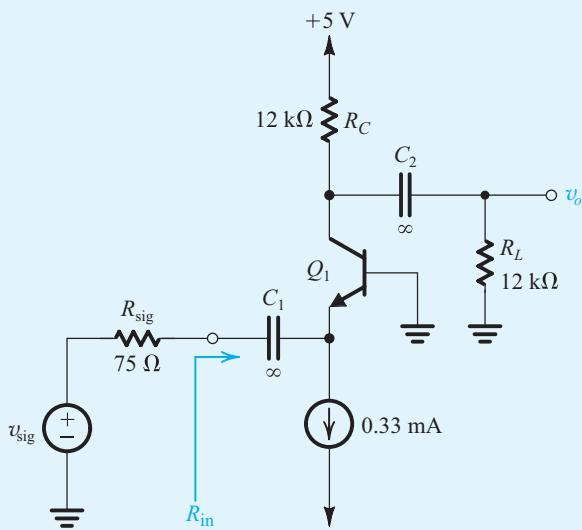


Figure P7.53

**7.54** In the circuit shown in Fig. P7.54, the transistor has a  $\beta$  of 200. What is the dc voltage at the collector? Replacing the BJT with one of the hybrid- $\pi$  models (neglecting  $r_o$ ), draw the equivalent circuit of the amplifier. Find the input resistances  $R_{ib}$  and  $R_{in}$  and the overall voltage gain ( $v_o/v_{sig}$ ). For an output signal of  $\pm 0.4$  V, what values of  $v_{sig}$  and  $v_b$  are required?

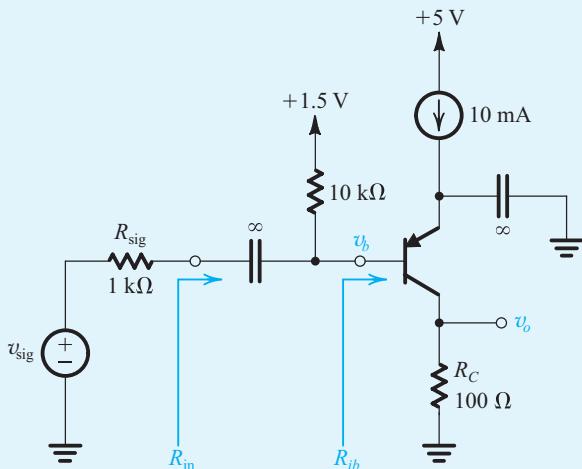


Figure P7.54

**7.55** Consider the augmented hybrid- $\pi$  model shown in Fig. 7.25(a). Disregarding how biasing is to be done, what is the largest possible voltage gain available for a signal source connected directly to the base and a very-high-resistance load? Calculate the value of the maximum possible gain for  $V_A = 25$  V and  $V_T = 125$  V.

**D 7.56** Redesign the circuit of Fig. 7.30(a) by raising the resistor values by a factor  $n$  to increase the resistance seen by the input  $v_i$  to  $75 \Omega$ . What value of voltage gain results? Grounded-base circuits of this kind are used in systems such as cable TV, in which, for highest-quality signaling, load resistances need to be “matched” to the equivalent resistances of the interconnecting cables.

**D \*7.57** Design an amplifier using the configuration of Fig. 7.30(a). The power supplies available are  $\pm 5$  V. The input signal source has a resistance of  $50 \Omega$ , and it is required that the amplifier input resistance match this value. (Note that  $R_{in} = r_e \parallel R_E \simeq r_e$ .) The amplifier is to have the greatest possible voltage gain and the largest possible output signal but retain small-signal linear operation (i.e., the signal component across the base-emitter junction should be limited to no more

than 10 mV). Find appropriate values for  $R_E$  and  $R_C$ . What is the value of voltage gain realized from signal source to output?

**\*7.58** The transistor in the circuit shown in Fig. P7.58 is biased to operate in the active mode. Assuming that  $\beta$  is very large, find the collector bias current  $I_C$ . Replace the transistor with the small-signal equivalent-circuit model of Fig. 7.26(b) (remember to replace the dc power supply with a short circuit). Analyze the resulting amplifier equivalent circuit to show that

$$\frac{v_{o1}}{v_i} = \frac{R_E}{R_E + r_e}$$

$$\frac{v_{o2}}{v_i} = \frac{-\alpha R_C}{R_E + r_e}$$

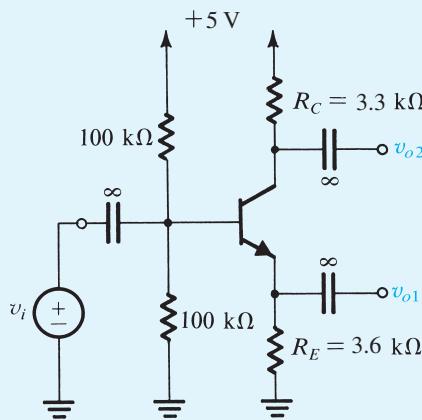


Figure P7.58

Find the values of these voltage gains (for  $\alpha \simeq 1$ ). Now, if the terminal labeled  $v_{o1}$  is connected to ground, what does the voltage gain  $v_{o2}/v_i$  become?

### Section 7.3: Basic Configurations

**7.59** An amplifier with an input resistance of  $100 \text{ k}\Omega$ , an open-circuit voltage gain of  $100 \text{ V/V}$ , and an output resistance of  $100 \Omega$  is connected between a  $20\text{-k}\Omega$  signal source and a  $2\text{-k}\Omega$  load. Find the overall voltage gain  $G_v$ . Also find the current gain, defined as the ratio of the load current to the current drawn from the signal source.

**D 7.60** Specify the parameters  $R_{in}$ ,  $A_{vo}$ , and  $R_o$  of an amplifier that is to be connected between a  $100\text{-k}\Omega$  source and a  $2\text{-k}\Omega$  load and is required to meet the following specifications:

- No more than 5% of the signal strength is lost in the connection to the amplifier input;
- If the load resistance changes from the nominal value of  $2\text{k}\Omega$  to a low value of  $1\text{k}\Omega$ , the change in output voltage is limited to 5% of nominal value; and
- The nominal overall voltage gain is  $10 \text{ V/V}$ .

**7.61** Figure P7.61 shows an alternative equivalent-circuit representation of an amplifier. If this circuit is to be equivalent to that in Fig. 7.34(b) show that  $G_m = A_{vo} R_o$ . Also convince yourself that the transconductance  $G_m$  is defined as

$$G_m = \left. \frac{i_o}{v_i} \right|_{R_L=0}$$

and hence is known as the short-circuit transconductance. Now, if the amplifier is fed with a signal source ( $v_{sig}$ ,  $R_{sig}$ ) and is connected to a load resistance  $R_L$  show that the gain of the amplifier proper  $A_v$  is given by  $A_v = G_m (R_o \parallel R_L)$  and the overall voltage gain  $G_v$  is given by

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} G_m (R_o \parallel R_L)$$

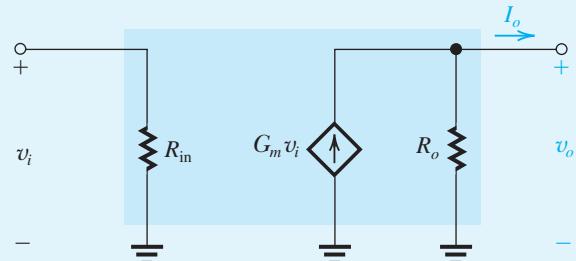


Figure P7.61

**7.62** An alternative equivalent circuit of an amplifier fed with a signal source ( $v_{sig}$ ,  $R_{sig}$ ) and connected to a load  $R_L$  is shown in Fig. P7.62. Here  $G_{vo}$  is the open-circuit overall voltage gain,

$$G_{vo} = \left. \frac{v_o}{v_{sig}} \right|_{R_L=\infty}$$

and  $R_{\text{out}}$  is the output resistance with  $v_{\text{sig}}$  set to zero. This is different than  $R_o$ . Show that

$$G_{vo} = \frac{R_f}{R_i + R_{\text{sig}}} A_{vo}$$

where  $R_i = R_{\text{in}}|_{R_L=\infty}$ .

Also show that the overall voltage gain is

$$G_v = G_{vo} \frac{R_L}{R_L + R_{\text{out}}}$$

**\*\*7.63** Most practical amplifiers have internal feedback that make them non-unilateral. In such a case,  $R_{\text{in}}$  depends on  $R_L$ . To illustrate this point we show in Fig. P7.63 the equivalent circuit of an amplifier where a feedback resistance  $R_f$  models the internal feedback mechanism that is present in this amplifier. It is  $R_f$  that makes the amplifier non-unilateral. Show that

$$R_{\text{in}} = R_1 \parallel \left[ \frac{R_f + (R_2 \parallel R_L)}{1 + g_m(R_2 \parallel R_L)} \right]$$

$$A_{vo} = -g_m R_2 \frac{1 - 1/(g_m R_f)}{1 + (R_2/R_f)}$$

$$R_o = R_2 \parallel R_f$$

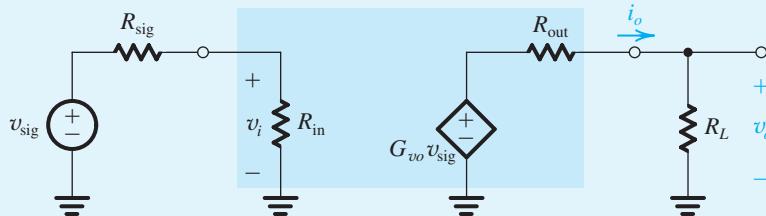


Figure P7.62

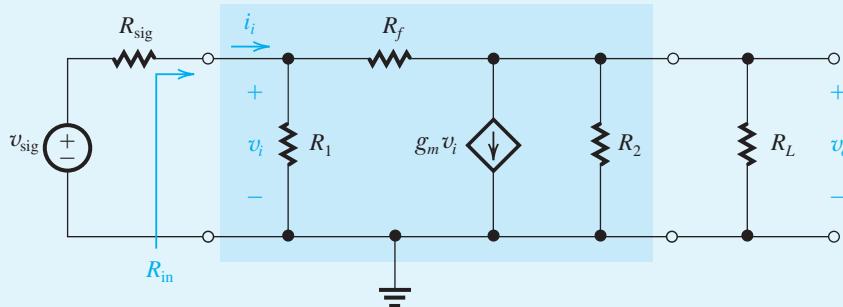


Figure P7.63

Evaluate  $R_{\text{in}}$ ,  $A_{vo}$ , and  $R_o$  for the case  $R_1 = 100 \text{ k}\Omega$ ,  $R_f = 1 \text{ M}\Omega$ ,  $g_m = 100 \text{ mA/V}$ ,  $R_2 = 100 \Omega$ , and  $R_L = 1 \text{ k}\Omega$ . Which of the amplifier characteristic parameters is most affected by  $R_f$  (that is, relative to the case with  $R_f = \infty$ )? For  $R_{\text{sig}} = 100 \text{ k}\Omega$  determine the overall voltage gain,  $G_v$ , with and without  $R_f$  present.

**7.64** Calculate the overall voltage gain of a CS amplifier fed with a  $1-\text{M}\Omega$  source and connected to a  $10-\text{k}\Omega$  load. The MOSFET has  $g_m = 2 \text{ mA/V}$ , and a drain resistance  $R_D = 10 \text{ k}\Omega$  is utilized.

**7.65** A CS amplifier utilizes a MOSFET with  $\mu_n C_{ox} = 400 \text{ }\mu\text{A/V}^2$  and  $W/L = 10$ . It is biased at  $I_D = 320 \text{ }\mu\text{A}$  and uses  $R_D = 10 \text{ k}\Omega$ . Find  $R_{\text{in}}$ ,  $A_{vo}$ , and  $R_o$ . Also, if a load resistance of  $10 \text{ k}\Omega$  is connected to the output, what overall voltage gain  $G_v$  is realized? Now, if a 0.2-V peak sine-wave signal is required at the output, what must the peak amplitude of  $v_{\text{sig}}$  be?

**7.66** A common-source amplifier utilizes a MOSFET operated at  $V_{OV} = 0.25 \text{ V}$ . The amplifier feeds a load resistance  $R_L = 15 \text{ k}\Omega$ . The designer selects  $R_D = 2R_L$ . If it is required to realize an overall voltage gain  $G_v$  of  $-10 \text{ V/V}$  what  $g_m$  is needed? Also specify the bias current  $I_D$ . If, to increase the output signal swing,  $R_D$  is reduced to  $R_D = R_L$ , what does  $G_v$  become?

**7.67** Two identical CS amplifiers are connected in cascade. The first stage is fed with a source  $v_{\text{sig}}$  having a resistance  $R_{\text{sig}} = 200 \text{ k}\Omega$ . A load resistance  $R_L = 10 \text{ k}\Omega$  is connected to the drain of the second stage. Each MOSFET is biased at  $I_D = 0.3 \text{ mA}$  and operates with  $V_{OV} = 0.2 \text{ V}$ . Each stage utilizes a drain resistance  $R_D = 10 \text{ k}\Omega$ .

- (a) Sketch the equivalent circuit of the two-stage amplifier.
- (b) Calculate the overall voltage gain  $G_v$ .

**7.68** A CE amplifier utilizes a BJT with  $\beta = 100$  biased at  $I_C = 0.5 \text{ mA}$ ; it has a collector resistance  $R_C = 10 \text{ k}\Omega$ . Find  $R_{\text{in}}$ ,  $R_o$ , and  $A_{vo}$ . If the amplifier is fed with a signal source having a resistance of  $10 \text{ k}\Omega$ , and a load resistance  $R_L = 10 \text{ k}\Omega$  is connected to the output terminal, find the resulting  $A_v$  and  $G_v$ . If the peak voltage of the sine wave appearing between base and emitter is to be limited to  $5 \text{ mV}$ , what  $\hat{v}_{\text{sig}}$  is allowed, and what output voltage signal appears across the load?

**D \*7.69** In this problem we investigate the effect of the inevitable variability of  $\beta$  on the realized gain of the CE amplifier. For this purpose, use the overall gain expression in Eq. (7.114).

$$|G_v| = \frac{R'_L}{(R_{\text{sig}}/\beta) + (1/g_m)}$$

where  $R'_L = R_L \parallel R_C$ .

Consider the case  $R'_L = 10 \text{ k}\Omega$  and  $R_{\text{sig}} = 10 \text{ k}\Omega$ , and let the BJT be biased at  $I_C = 1 \text{ mA}$ . The BJT has a nominal  $\beta$  of 100.

- (a) What is the nominal value of  $|G_v|$ ?
- (b) If  $\beta$  can be anywhere between 50 and 150, what is the corresponding range of  $|G_v|$ ?
- (c) If in a particular design, it is required to maintain  $|G_v|$  within  $\pm 20\%$  of its nominal value, what is the maximum allowable range of  $\beta$ ?
- (d) If it is not possible to restrict  $\beta$  to the range found in (c), and the designer has to contend with  $\beta$  in the range 50 to 150, what value of bias current  $I_C$  would result in  $|G_v|$  falling in a range of  $\pm 20\%$  of a new nominal value? What is the nominal value of  $|G_v|$  in this case?

**7.70** Two identical CE amplifiers are connected in cascade. The first stage is fed with a source  $v_{\text{sig}}$  having a resistance  $R_{\text{sig}} = 10 \text{ k}\Omega$ . A load resistance  $R_L = 10 \text{ k}\Omega$  is connected to the collector of the second stage. Each BJT is biased at  $I_C = 0.25 \text{ mA}$  and has  $\beta = 100$ . Each stage utilizes a collector resistance  $R_C = 10 \text{ k}\Omega$ .

- (a) Sketch the equivalent circuit of the two-stage amplifier.
- (b) Find the overall voltage gain,  $v_{o2}/v_{\text{sig}}$ .

**7.71** A MOSFET connected in the CS configuration has a transconductance  $g_m = 5 \text{ mA/V}$ . When a resistance  $R_s$  is connected in the source lead, the effective transconductance is reduced to  $2 \text{ mA/V}$ . What do you estimate the value of  $R_s$  to be?

**7.72** A CS amplifier using an NMOS transistor with  $g_m = 2 \text{ mA/V}$  is found to have an overall voltage gain of  $-10 \text{ V/V}$ . What value should a resistance  $R_s$  inserted in the source lead have to reduce the overall voltage gain to  $-5 \text{ V/V}$ ?

**7.73** The overall voltage gain of a CS amplifier with a resistance  $R_s = 0.5 \text{ k}\Omega$  in the source lead was measured and found to be  $-10 \text{ V/V}$ . When  $R_s$  was shorted, but the circuit operation remained linear, the gain doubled. What must  $g_m$  be? What value of  $R_s$  is needed to obtain an overall voltage gain of  $-16 \text{ V/V}$ ?

**7.74** A CE amplifier utilizes a BJT with  $\beta = 100$  biased at  $I_C = 0.5 \text{ mA}$  and has a collector resistance  $R_C = 12 \text{ k}\Omega$  and a resistance  $R_e = 250\Omega$  connected in the emitter. Find  $R_{\text{in}}$ ,  $A_{vo}$ , and  $R_o$ . If the amplifier is fed with a signal source having a resistance of  $10 \text{ k}\Omega$ , and a load resistance  $R_L = 12 \text{ k}\Omega$  is connected to the output terminal, find the resulting  $A_v$  and  $G_v$ . If the peak voltage of the sine wave appearing between base and emitter is to be limited to  $5 \text{ mV}$ , what  $\hat{v}_{\text{sig}}$  is allowed, and what output voltage signal appears across the load?

**D 7.75** Design a CE amplifier with a resistance  $R_e$  in the emitter to meet the following specifications:

- (i) Input resistance  $R_{\text{in}} = 15 \text{ k}\Omega$ .
- (ii) When fed from a signal source with a peak amplitude of  $0.15 \text{ V}$  and a source resistance of  $30 \text{ k}\Omega$ , the peak amplitude of  $v_\pi$  is  $5 \text{ mV}$ .

Specify  $R_e$  and the bias current  $I_C$ . The BJT has  $\beta = 74$ . If the total resistance in the collector is  $6 \text{ k}\Omega$ , find the overall voltage gain  $G_v$  and the peak amplitude of the output signal  $v_o$ .

**SIM D 7.76** Inclusion of an emitter resistance  $R_e$  reduces the variability of the gain  $G_v$  due to the inevitable wide variance in the value of  $\beta$ . Consider a CE amplifier operating between a signal source with  $R_{\text{sig}} = 10 \text{ k}\Omega$  and a total collector resistance  $R_C \parallel R_L$  of  $10 \text{ k}\Omega$ . The BJT is biased at  $I_C = 1 \text{ mA}$  and its  $\beta$  is specified to be nominally 100 but can lie in the range of 50 to 150. First determine the nominal value and the range of

$|G_v|$  without resistance  $R_e$ . Then select a value for  $R_e$  that will ensure that  $|G_v|$  be within  $\pm 20\%$  of its new nominal value. Specify the value of  $R_e$ , the new nominal value of  $|G_v|$ , and the expected range of  $|G_v|$ .

**7.77** A CG amplifier using an NMOS transistor for which  $g_m = 2 \text{ mA/V}$  has a  $5\text{-k}\Omega$  drain resistance  $R_D$  and a  $5\text{-k}\Omega$  load resistance  $R_L$ . The amplifier is driven by a voltage source having a  $750\text{-}\Omega$  resistance. What is the input resistance of the amplifier? What is the overall voltage gain  $G_v$ ? By what factor must the bias current  $I_D$  of the MOSFET be changed so that  $R_{in}$  matches  $R_{sig}$ ?

**7.78** A CG amplifier when fed with a signal source having  $R_{sig} = 100 \Omega$  is found to have an overall voltage gain of  $12 \text{ V/V}$ . When a  $100\text{-}\Omega$  resistance was added in series with the signal generator the overall voltage gain decreased to  $10 \text{ V/V}$ . What must  $g_m$  of the MOSFET be? If the MOSFET is biased at  $I_D = 0.25 \text{ mA}$ , at what overdrive voltage must it be operating?

**D 7.79** A CB amplifier is operating with  $R_L = 10 \text{ k}\Omega$ ,  $R_C = 10 \text{ k}\Omega$ , and  $R_{sig} = 50 \Omega$ . At what current  $I_C$  should the transistor be biased for the input resistance  $R_{in}$  to equal that of the signal source? What is the resulting overall voltage gain? Assume  $\alpha \approx 1$ .

**7.80** For the circuit in Fig. P7.80, let  $R_{sig} \gg r_e$  and  $\alpha \approx 1$ . Find  $v_o$ .

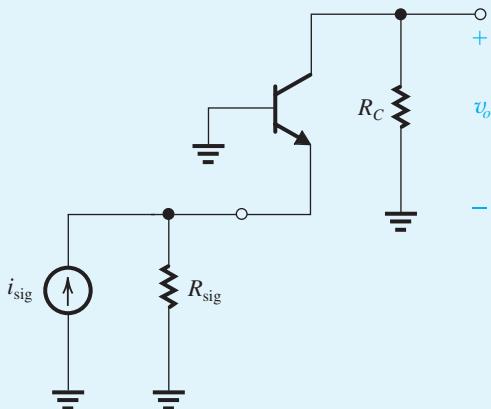


Figure P7.80

**7.81** A CB amplifier is biased at  $I_E = 0.2 \text{ mA}$  with  $R_C = R_L = 10 \text{ k}\Omega$  and is driven by a signal source with  $R_{sig} = 0.5 \text{ k}\Omega$ . Find the overall voltage gain  $G_v$ . If the maximum signal amplitude of the voltage between base and emitter is limited to  $10 \text{ mV}$ ,

what are the corresponding amplitudes of  $v_{sig}$  and  $v_o$ ? Assume  $\alpha \approx 1$ .

**7.82** A source follower is required to connect a high-resistance source to a load whose resistance is nominally  $2 \text{ k}\Omega$  but can be as low as  $1.5 \text{ k}\Omega$  and as high as  $5 \text{ k}\Omega$ . What is the maximum output resistance that the source follower must have if the output voltage is to remain within  $\pm 10\%$  of nominal value? If the MOSFET has  $k_n = 2.5 \text{ mA/V}^2$ , at what current  $I_D$  must it be biased? At what overdrive voltage is the MOSFET operating?

**D 7.83** A source follower is required to deliver a  $0.5\text{-V}$  peak sinusoid to a  $2\text{-k}\Omega$  load. If the peak amplitude of  $v_{gs}$  is to be limited to  $50 \text{ mV}$ , and the MOSFET transconductance parameter  $k_n$  is  $5 \text{ mA/V}^2$ , what is the lowest value of  $I_D$  at which the MOSFET can be biased? At this bias current, what are the maximum and minimum currents that the MOSFET will be conducting (at the positive and negative peaks of the output sine wave)? What must the peak amplitude of  $v_{sig}$  be?

**D 7.84** An emitter follower is required to deliver a  $0.5\text{-V}$  peak sinusoid to a  $2\text{-k}\Omega$  load. If the peak amplitude of  $v_{be}$  is to be limited to  $5 \text{ mV}$ , what is the lowest value of  $I_E$  at which the BJT can be biased? At this bias current, what are the maximum and minimum currents that the BJT will be conducting (at the positive and negative peaks of the output sine wave)? If the resistance of the signal source is  $200 \text{ k}\Omega$ , what value of  $G_v$  is obtained? Thus determine the required amplitude of  $v_{sig}$ . Assume  $\beta = 100$ .

**7.85** An emitter follower with a BJT biased at  $I_C = 2 \text{ mA}$  and having  $\beta = 100$  is connected between a source with  $R_{sig} = 10 \text{ k}\Omega$  and a load  $R_L = 0.5 \text{ k}\Omega$ .

- Find  $R_{in}$ ,  $v_b/v_{sig}$ , and  $v_o/v_{sig}$ .
- If the signal amplitude across the base-emitter junction is to be limited to  $10 \text{ mV}$ , what is the corresponding amplitude of  $v_{sig}$  and  $v_o$ ?
- Find the open-circuit voltage gain  $G_{vo}$  and the output resistance  $R_{out}$ . Use these values first to verify the value of  $G_v$  obtained in (a), then to find the value of  $G_v$  obtained with  $R_L$  reduced to  $250 \Omega$ .

**7.86** An emitter follower is operating at a collector bias current of  $0.5 \text{ mA}$  and is used to connect a  $10\text{-k}\Omega$  source to a  $1\text{-k}\Omega$  load. If the nominal value of  $\beta$  is  $100$ , what output resistance  $R_{out}$  and overall voltage gain  $G_v$  result? Now if

transistor  $\beta$  is specified to lie in the range 50 to 150, find the corresponding range of  $R_{\text{out}}$  and  $G_v$ .

**7.87** An emitter follower, when driven from a 5-k $\Omega$  source, was found to have an output resistance  $R_{\text{out}}$  of 150  $\Omega$ . The output resistance increased to 250  $\Omega$  when the source resistance was increased to 10 k $\Omega$ . Find the overall voltage gain when the follower is driven by a 10-k $\Omega$  source and loaded by a 1-k $\Omega$  resistor.

**7.88** For the general amplifier circuit shown in Fig. P7.88 neglect the Early effect.

- (a) Find expressions for  $v_c/v_{\text{sig}}$  and  $v_e/v_{\text{sig}}$ .
- (b) If  $v_{\text{sig}}$  is disconnected from node X, node X is grounded, and node Y is disconnected from ground and connected to  $v_{\text{sig}}$ , find the new expression for  $v_c/v_{\text{sig}}$ .

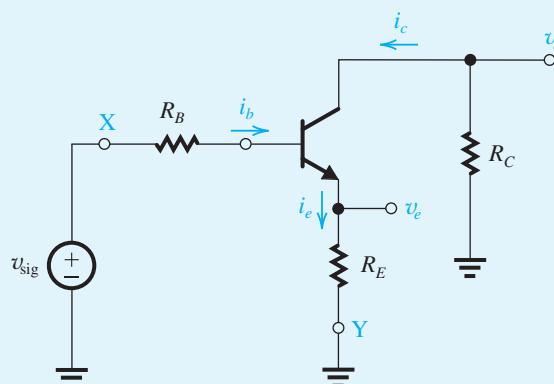


Figure P7.88

**7.89** When the Early effect is neglected, the overall voltage gain of a CE amplifier with a collector resistance  $R_C = 10$  k $\Omega$  is calculated to be  $-100$  V/V. If the BJT is biased at  $I_C = 1$  mA and the Early voltage is 100 V, provide a better estimate of the voltage gain  $G_v$ .

**\*7.90** Show that when  $r_o$  is taken into account, the voltage gain of the source follower becomes

$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = \frac{R_L \parallel r_o}{(R_L \parallel r_o) + \frac{1}{g_m}}$$

Now, with  $R_L$  removed, the voltage gain is carefully measured and found to be 0.98. Then, when  $R_L$  is connected and its value is varied, it is found that the gain is halved at  $R_L = 500$   $\Omega$ . If the amplifier remained linear throughout this measurement, what must the values of  $g_m$  and  $r_o$  be?

**D 7.91** In this problem, we investigate the effect of changing the bias current  $I_C$  on the overall voltage gain  $G_v$  of a CE amplifier. Consider the situation of a CE amplifier operating with a signal source having  $R_{\text{sig}} = 10$  k $\Omega$  and having  $R_C \parallel R_L = 10$  k $\Omega$ . The BJT is specified to have  $\beta = 100$  and  $V_A = 25$  V. Use Eq. (7.114) (with  $r_o$  included in parallel with  $R_C$  and  $R_L$  in the numerator) to find  $|G_v|$  at  $I_C = 0.1$  mA, 0.2 mA, 0.5 mA, 1.0 mA, and 1.25 mA. Observe the effect of  $r_o$  on limiting  $|G_v|$  as  $I_C$  is increased. Find the value of  $I_C$  that results in  $|G_v| = 50$  V/V.

## Section 7.4: Biasing

**D 7.92** Consider the classical biasing scheme shown in Fig. 7.48(c), using a 9-V supply. For the MOSFET,  $V_t = 1$  V,  $\lambda = 0$ , and  $k_n = 2$  mA/V<sup>2</sup>. Arrange that the drain current is 1 mA, with about one-third of the supply voltage across each of  $R_S$  and  $R_D$ . Use 22 M $\Omega$  for the larger of  $R_{G1}$  and  $R_{G2}$ . What are the values of  $R_{G1}$ ,  $R_{G2}$ ,  $R_S$ , and  $R_D$  that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?

**D 7.93** Using the circuit topology displayed in Fig. 7.48(e), arrange to bias the NMOS transistor at  $I_D = 0.5$  mA with  $V_D$  midway between cutoff and the beginning of triode operation. The available supplies are  $\pm 5$  V. For the NMOS transistor,  $V_t = 1.0$  V,  $\lambda = 0$ , and  $k_n = 1$  mA/V<sup>2</sup>. Use a gate-bias resistor of 10 M $\Omega$ . Specify  $R_S$  and  $R_D$  to two significant digits.

**D \*7.94** In an electronic instrument using the biasing scheme shown in Fig. 7.48(c), a manufacturing error reduces  $R_S$  to zero. Let  $V_{DD} = 15$  V,  $R_{G1} = 10$  M $\Omega$ , and  $R_{G2} = 5.1$  M $\Omega$ . What is the value of  $V_G$  created? If supplier specifications allow  $k_n$  to vary from 0.2 to 0.3 mA/V<sup>2</sup> and  $V_t$  to vary from 1.0 V to 1.5 V, what are the extreme values of  $I_D$  that may result? What value of  $R_S$  should have been installed to limit the maximum value of  $I_D$  to 1.5 mA? Choose an appropriate standard 5% resistor value (refer to Appendix J). What extreme values of current now result?

**7.95** An NMOS transistor is connected in the bias circuit of Fig. 7.48(c), with  $V_G = 5$  V and  $R_S = 3$  k $\Omega$ . The transistor has  $V_t = 1$  V and  $k_n = 2$  mA/V<sup>2</sup>. What bias current results? If a transistor for which  $k_n$  is 50% higher is used, what is the resulting percentage increase in  $I_D$ ?

**SIM 7.96** The bias circuit of Fig. 7.48(c) is used in a design with  $V_G = 5$  V and  $R_S = 2$  k $\Omega$ . For a MOSFET with

$k_n = 2 \text{ mA/V}^2$ , the source voltage was measured and found to be 2 V. What must  $V_t$  be for this device? If a device for which  $V_t$  is 0.5 V less is used, what does  $V_s$  become? What bias current results?

**D 7.97** Design the circuit of Fig. 7.48(e) for a MOSFET having  $V_t = 1 \text{ V}$  and  $k'_p W/L = 4 \text{ mA/V}^2$ . Let  $V_{DD} = V_{SS} = 5 \text{ V}$ . Design for a dc bias current of 0.5 mA and for the largest possible voltage gain (and thus the largest possible  $R_D$ ) consistent with allowing a 2-V peak-to-peak voltage swing at the drain. Assume that the signal voltage on the source terminal of the FET is zero.

**SIM D 7.98** Design the circuit in Fig. P7.98 so that the transistor operates in saturation with  $V_D$  biased 1 V from the edge of the triode region, with  $I_D = 1 \text{ mA}$  and  $V_D = 3 \text{ V}$ , for each of the following two devices (use a 10- $\mu\text{A}$  current in the voltage divider):

- (a)  $|V_t| = 1 \text{ V}$  and  $k'_p W/L = 0.5 \text{ mA/V}^2$
- (b)  $|V_t| = 2 \text{ V}$  and  $k'_p W/L = 1.25 \text{ mA/V}^2$

For each case, specify the values of  $V_G$ ,  $V_D$ ,  $V_S$ ,  $R_1$ ,  $R_2$ ,  $R_S$ , and  $R_D$ .

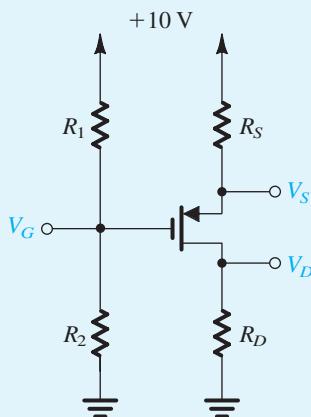


Figure P7.98

**D \*\*7.99** A very useful way to characterize the stability of the bias current  $I_D$  is to evaluate the sensitivity of  $I_D$  relative to a particular transistor parameter whose variability might be large. The sensitivity of  $I_D$  relative to the MOSFET parameter  $K \equiv \frac{1}{2} k' (W/L)$  is defined as

$$S_K^{I_D} \equiv \frac{\partial I_D / I_D}{\partial K / K} = \frac{\partial I_D}{\partial K} \frac{K}{I_D}$$

and its value, when multiplied by the variability (or tolerance) of  $K$ , provides the corresponding expected variability of  $I_D$ ,

$$\frac{\Delta I_D}{I_D} = S_K^{I_D} \left( \frac{\Delta K}{K} \right)$$

The purpose of this problem is to investigate the use of the sensitivity function in the design of the bias circuit of Fig. 7.48(e).

(a) Show that for  $V_t$  constant,

$$S_K^{I_D} = 1 / \left( 1 + 2\sqrt{KI_D}R_S \right)$$

- (b) For a MOSFET having  $K = 100 \mu\text{A/V}^2$  with a variability of  $\pm 10\%$  and  $V_t = 1 \text{ V}$ , find the value of  $R_S$  that would result in  $I_D = 100 \mu\text{A}$  with a variability of  $\pm 1\%$ . Also, find  $V_{GS}$  and the required value of  $V_{SS}$ .
- (c) If the available supply  $V_{SS} = 5 \text{ V}$ , find the value of  $R_S$  for  $I_D = 100 \mu\text{A}$ . Evaluate the sensitivity function, and give the expected variability of  $I_D$  in this case.

**D \*\*7.100** The variability ( $\Delta I_D / I_D$ ) in the bias current  $I_D$  due to the variability ( $\Delta V_t / V_t$ ) in the threshold voltage  $V_t$  can be evaluated from

$$\frac{\Delta I_D}{I_D} = S_{V_t}^{I_D} \left( \frac{\Delta V_t}{V_t} \right)$$

where  $S_{V_t}^{I_D}$ , the sensitivity of  $I_D$  relative to  $V_t$ , is defined as

$$S_{V_t}^{I_D} = \frac{\partial I_D}{\partial V_t} \frac{V_t}{I_D}$$

- (a) For the case of a MOSFET biased with a fixed  $V_{GS}$ , show that

$$S_{V_t}^{I_D} = - \frac{2V_t}{V_{ov}}$$

and find the variability in  $I_D$  for  $V_t = 0.5 \text{ V}$  and  $\Delta V_t / V_t = \pm 5\%$ . Let the MOSFET be biased at  $V_{ov} = 0.25 \text{ V}$ .

- (b) For the case of a MOSFET biased with a fixed gate voltage  $V_G$  and a resistance  $R_S$  included in the source lead, show that

$$S_{V_t}^{I_D} = - \frac{2V_t}{V_{ov} + 2I_D R_S}$$

For the same parameters given in (a), find the required value of  $(I_D R_S)$  and  $V_G$  to limit  $\Delta I_D / I_D$  to  $\pm 5\%$ . What value of  $R_S$  is needed if  $I_D$  is  $100 \mu\text{A}$ ?

**SIM 7.101** In the circuit of Fig. 7.50, let  $R_G = 10 \text{ M}\Omega$ ,  $R_D = 10 \text{ k}\Omega$ , and  $V_{DD} = 10 \text{ V}$ . For each of the following two transistors, find the voltages  $V_D$  and  $V_G$ .

- (a)  $V_t = 1 \text{ V}$  and  $k_n = 0.5 \text{ mA/V}^2$
- (b)  $V_t = 2 \text{ V}$  and  $k_n = 1.25 \text{ mA/V}^2$

**D 7.102** Using the feedback bias arrangement shown in Fig. 7.50 with a 5-V supply and an NMOS device for which  $V_t = 1 \text{ V}$  and  $k_n = 10 \text{ mA/V}^2$ , find  $R_D$  to establish a drain current of 0.2 mA.

**D 7.103** Figure P7.103 shows a variation of the feedback-bias circuit of Fig. 7.50. Using a 5-V supply with an NMOS transistor for which  $V_t = 0.8 \text{ V}$ ,  $k_n = 8 \text{ mA/V}^2$ , and  $\lambda = 0$ , provide a design that biases the transistor at  $I_D = 1 \text{ mA}$ , with  $V_{DS}$  large enough to allow saturation operation for a 2-V negative signal swing at the drain. Use  $22 \text{ M}\Omega$  as the largest resistor in the feedback-bias network. What values of  $R_D$ ,  $R_{G1}$ , and  $R_{G2}$  have you chosen? Specify all resistors to two significant digits.

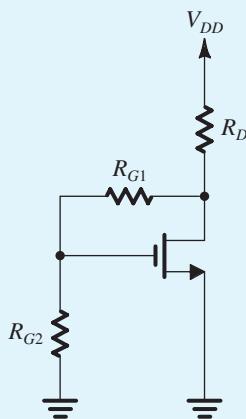


Figure P7.103

**D 7.104** For the circuit in Fig. 7.51(a), neglect the base current  $I_B$  in comparison with the current in the voltage divider. It is required to bias the transistor at  $I_C = 1 \text{ mA}$ , which requires selecting  $R_{B1}$  and  $R_{B2}$  so that  $V_{BE} = 0.710 \text{ V}$ . If  $V_{CC} = 3 \text{ V}$ , what must the ratio  $R_{B1}/R_{B2}$  be? Now, if  $R_{B1}$  and  $R_{B2}$  are 1% resistors, that is, each can be in the range of 0.99 to 1.01 of its nominal value, what is the range obtained for  $V_{BE}$ ? What is the corresponding range of  $I_C$ ? If  $R_C = 2 \text{ k}\Omega$ , what is

the range obtained for  $V_{CE}$ ? Comment on the efficacy of this biasing arrangement.

**D 7.105** It is required to bias the transistor in the circuit of Fig. 7.51(b) at  $I_C = 1 \text{ mA}$ . The transistor  $\beta$  is specified to be nominally 100, but it can fall in the range of 50 to 150. For  $V_{CC} = +3 \text{ V}$  and  $R_C = 2 \text{ k}\Omega$ , find the required value of  $R_B$  to achieve  $I_C = 1 \text{ mA}$  for the “nominal” transistor. What is the expected range for  $I_C$  and  $V_{CE}$ ? Comment on the efficacy of this bias design.

**D 7.106** Consider the single-supply bias network shown in Fig. 7.52(a). Provide a design using a 9-V supply in which the supply voltage is equally split between  $R_C$ ,  $V_{CE}$ , and  $R_E$  with a collector current of 0.6 mA. The transistor  $\beta$  is specified to have a minimum value of 90. Use a voltage-divider current of  $I_E/10$ , or slightly higher. Since a reasonable design should operate for the best transistors for which  $\beta$  is very high, do your initial design with  $\beta = \infty$ . Then choose suitable 5% resistors (see Appendix J), making the choice in a way that will result in a  $V_{BB}$  that is slightly higher than the ideal value. Specify the values you have chosen for  $R_E$ ,  $R_C$ ,  $R_1$ , and  $R_2$ . Now, find  $V_B$ ,  $V_E$ ,  $V_C$ , and  $I_C$  for your final design using  $\beta = 90$ .

**D 7.107** Repeat Problem 7.106, but use a voltage-divider current that is  $I_E/2$ . Check your design at  $\beta = 90$ . If you have the data available, find how low  $\beta$  can be while the value of  $I_C$  does not fall below that obtained with the design of Problem 7.106 for  $\beta = 90$ .

**D \*7.108** It is required to design the bias circuit of Fig. 7.52 for a BJT whose nominal  $\beta = 100$ .

- (a) Find the largest ratio ( $R_B/R_E$ ) that will guarantee  $I_E$  remains within  $\pm 5\%$  of its nominal value for  $\beta$  as low as 50 and as high as 150.
- (b) If the resistance ratio found in (a) is used, find an expression for the voltage  $V_{BB} \equiv V_{CC}R_2/(R_1 + R_2)$  that will result in a voltage drop of  $V_{CC}/3$  across  $R_E$ .
- (c) For  $V_{CC} = 5 \text{ V}$ , find the required values of  $R_1$ ,  $R_2$ , and  $R_E$  to obtain  $I_E = 0.5 \text{ mA}$  and to satisfy the requirement for stability of  $I_E$  in (a).
- (d) Find  $R_C$  so that  $V_{CE} = 1.0 \text{ V}$  for  $\beta$  equal to its nominal value.

Check your design by evaluating the resulting range of  $I_E$ .

**D \*7.109** Consider the two-supply bias arrangement shown in Fig. 7.53 using  $\pm 5$ -V supplies. It is required to design the circuit so that  $I_C = 0.5$  mA and  $V_C$  is placed 2 V above  $V_E$ .

- For  $\beta = \infty$ , what values of  $R_E$  and  $R_C$  are required?
- If the BJT is specified to have a minimum  $\beta$  of 50, find the largest value for  $R_B$  consistent with the need to limit the voltage drop across it to one-tenth the voltage drop across  $R_E$ .
- What standard 5% resistor values (see Appendix J) would you use for  $R_B$ ,  $R_E$ , and  $R_C$ ? In making your selection, use somewhat lower values in order to compensate for the low- $\beta$  effects.
- For the values you selected in (c), find  $I_C$ ,  $V_B$ ,  $V_E$ , and  $V_C$  for  $\beta = \infty$  and for  $\beta = 50$ .

**D \*7.110** Utilizing  $\pm 3$ -V power supplies, it is required to design a version of the circuit in Fig. 7.53 in which the signal will be coupled to the emitter and thus  $R_B$  can be set to zero. Find values for  $R_E$  and  $R_C$  so that a dc emitter current of 0.4 mA is obtained and so that the gain is maximized while allowing  $\pm 1$  V of signal swing at the collector. If temperature increases from the nominal value of  $25^\circ\text{C}$  to  $125^\circ\text{C}$ , estimate the percentage change in collector bias current. In addition to the  $-2\text{ mV}/^\circ\text{C}$  change in  $V_{BE}$ , assume that the transistor  $\beta$  changes over this temperature range from 50 to 150.

**SIM D 7.111** Using a 3-V power supply, design a version of the circuit of Fig. 7.54 to provide a dc emitter current of 0.5 mA and to allow a  $\pm 1$ -V signal swing at the collector. The BJT has a nominal  $\beta = 100$ . Use standard 5% resistor values (see Appendix J). If the actual BJT used has  $\beta = 50$ , what emitter current is obtained? Also, what is the allowable signal swing at the collector? Repeat for  $\beta = 150$ .

- D \*7.112** (a) Using a 3-V power supply, design the feedback bias circuit of Fig. 7.54 to provide  $I_C = 1$  mA and  $V_C = V_{CC}/2$  for  $\beta = 100$ .  
 (b) Select standard 5% resistor values, and reevaluate  $V_C$  and  $I_C$  for  $\beta = 100$ .  
 (c) Find  $V_C$  and  $I_C$  for  $\beta = \infty$ .  
 (d) To improve the situation that obtains when high- $\beta$  transistors are used, we have to arrange for an additional current to flow through  $R_B$ . This can be achieved by connecting a resistor between base and emitter, as shown in Fig. P7.112.

Design this circuit for  $\beta = 100$ . Use a current through  $R_{B2}$  equal to the base current. Now, what values of  $V_C$  and  $I_C$  result with  $\beta = \infty$ ?

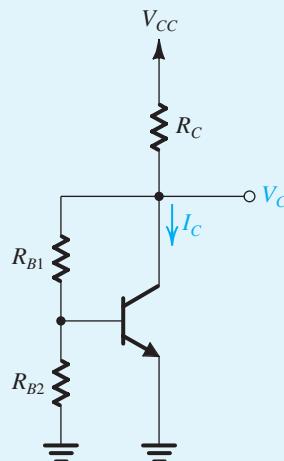


Figure P7.112

**D 7.113** A circuit that can provide a very large voltage gain for a high-resistance load is shown in Fig. P7.113. Find the values of  $I$  and  $R_B$  to bias the BJT at  $I_C = 1$  mA and  $V_C = 1.5$  V. Let  $\beta = 100$ .

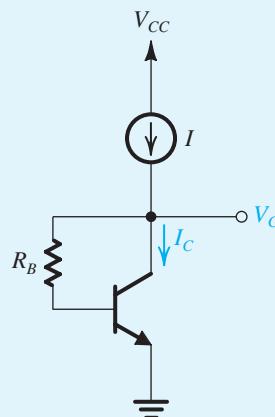


Figure P7.113

**7.114** The circuit in Fig. P7.114 provides a constant current  $I_O$  as long as the circuit to which the collector is

connected maintains the BJT in the active mode. Show that

$$I_o = \alpha \frac{V_{CC} [R_2 / (R_1 + R_2)] - V_{BE}}{R_E + (R_1 \parallel R_2) / (\beta + 1)}$$

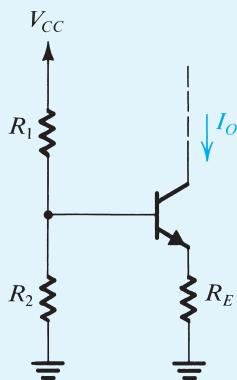


Figure P7.114

**SIM D \*7.115** For the circuit in Fig. P7.115, assuming all transistors to be identical with  $\beta$  infinite, derive an expression for the output current  $I_o$ , and show that by selecting

$$R_1 = R_2$$

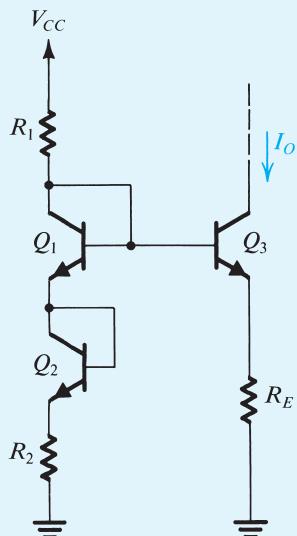


Figure P7.115

and keeping the current in each junction the same, the current  $I_o$  will be

$$I_o = \frac{V_{CC}}{2R_E}$$

which is independent of  $V_{BE}$ . What must the relationship of  $R_E$  to  $R_1$  and  $R_2$  be? For  $V_{CC} = 10$  V and  $V_{BE} = 0.7$  V, design the circuit to obtain an output current of 0.5 mA. What is the lowest voltage that can be applied to the collector of  $Q_3$ ?

**D 7.116** For the circuit in Fig. P7.116 find the value of  $R$  that will result in  $I_o \simeq 0.5$  mA. What is the largest voltage that can be applied to the collector? Assume  $|V_{BE}| = 0.7$  V.

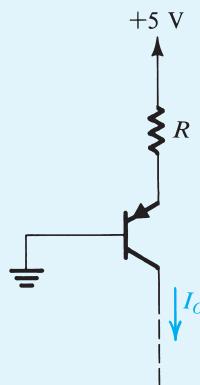


Figure P7.116

## Section 7.5: Discrete-Circuit Amplifiers

**7.117** Calculate the overall voltage gain  $G_v$  of a common-source amplifier for which  $g_m = 3$  mA/V,  $r_o = 100$  k $\Omega$ ,  $R_D = 10$  k $\Omega$ , and  $R_G = 10$  M $\Omega$ . The amplifier is fed from a signal source with a Thévenin resistance of 1 M $\Omega$ , and the amplifier output is coupled to a load resistance of 20 k $\Omega$ .

**SIM 7.118** The NMOS transistor in the CS amplifier shown in Fig. P7.118 has  $V_t = 0.7$  V and  $V_A = 50$  V.

- Neglecting the Early effect, verify that the MOSFET is operating in saturation with  $I_D = 0.5$  mA and  $V_{ov} = 0.3$  V. What must the MOSFET's  $k_n$  be? What is the dc voltage at the drain?
- Find  $R_{in}$  and  $G_v$ .
- If  $v_{sig}$  is a sinusoid with a peak amplitude  $\hat{v}_{sig}$ , find the maximum allowable value of  $\hat{v}_{sig}$  for which the transistor remains in saturation. What is the corresponding amplitude of the output voltage?

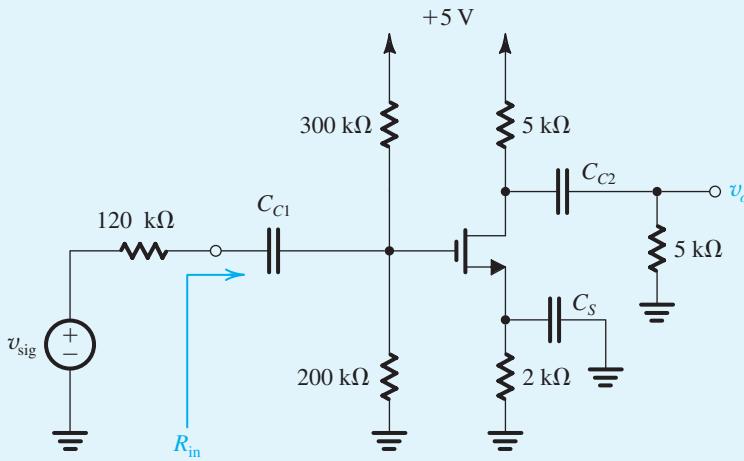


Figure P7.118

- (d) What is the value of resistance  $R_s$  that needs to be inserted in series with capacitor  $C_S$  in order to allow us to double the input signal  $\hat{v}_{\text{sig}}$ ? What output voltage now results?

**SIM D #7.119** The PMOS transistor in the CS amplifier of Fig. P7.119 has  $V_{tp} = -0.7$  V and a very large  $|V_A|$ .

- (a) Select a value for  $R_s$  to bias the transistor at  $I_D = 0.3$  mA and  $|V_{ov}| = 0.3$  V. Assume  $v_{\text{sig}}$  to have a zero dc component.  
(b) Select a value for  $R_D$  that results in  $G_v = -10$  V/V.

- (c) Find the largest sinusoid  $\hat{v}_{\text{sig}}$  that the amplifier can handle while remaining in the saturation region. What is the corresponding signal at the output?

- (d) If to obtain reasonably linear operation,  $\hat{v}_{\text{sig}}$  is limited to 50 mV, what value can  $R_D$  be increased to while maintaining saturation-region operation? What is the new value of  $G_v$ ?

**7.120** Figure P7.120 shows a scheme for coupling and amplifying a high-frequency pulse signal. The circuit utilizes

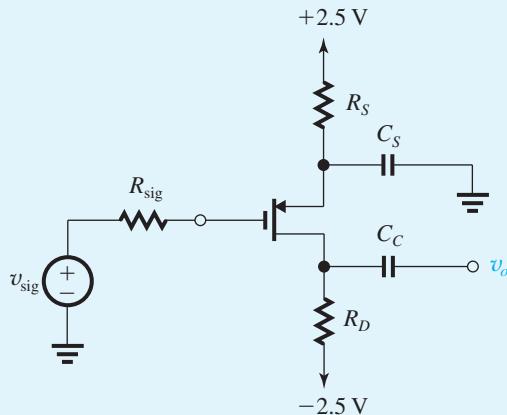


Figure P7.119

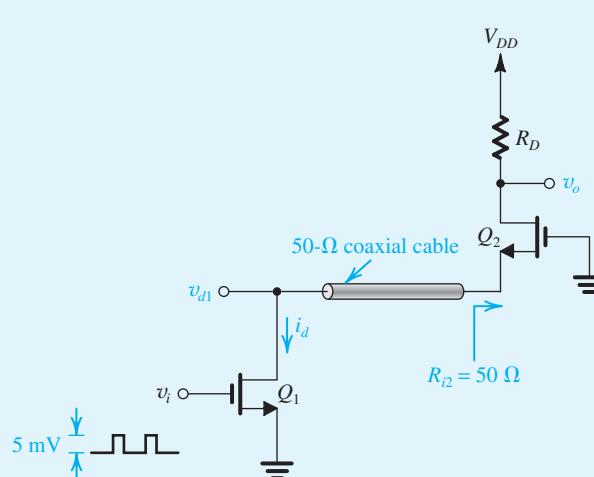


Figure P7.120

two MOSFETs whose bias details are not shown and a  $50\text{-}\Omega$  coaxial cable. Transistor  $Q_1$  operates as a CS amplifier and  $Q_2$  as a CG amplifier. For proper operation, transistor  $Q_2$  is required to present a  $50\text{-}\Omega$  resistance to the cable. This situation is known as “proper termination” of the cable and ensures that there will be no signal reflection coming back on the cable. When the cable is properly terminated, its input resistance is  $50\ \Omega$ . What must  $g_{m2}$  be? If  $Q_1$  is biased at the same point as  $Q_2$ , what is the amplitude of the current pulses in the drain of  $Q_1$ ? What is the amplitude of the voltage pulses at the drain of  $Q_1$ ? What value of  $R_D$  is required to provide 1-V pulses at the drain of  $Q_2$ ?

**D \*7.121** The MOSFET in the circuit of Fig. P7.121 has  $V_t = 0.8\text{ V}$ ,  $k_n = 5\text{ mA/V}^2$ , and  $V_A = 40\text{ V}$ .

- Find the values of  $R_s$ ,  $R_D$ , and  $R_G$  so that  $I_D = 0.4\text{ mA}$ , the largest possible value for  $R_D$  is used while a maximum signal swing at the drain of  $\pm 0.8\text{ V}$  is possible, and the input resistance at the gate is  $10\text{ M}\Omega$ . Neglect the Early effect.
- Find the values of  $g_m$  and  $r_o$  at the bias point.
- If terminal Z is grounded, terminal X is connected to a signal source having a resistance of  $1\text{ M}\Omega$ , and terminal Y is connected to a load resistance of  $10\text{ k}\Omega$ , find the voltage gain from signal source to load.
- If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower?

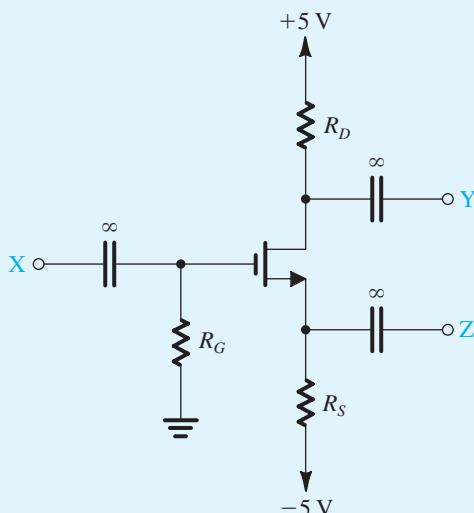
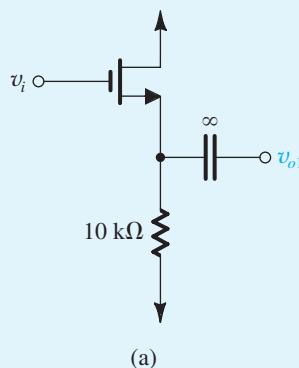


Figure P7.121

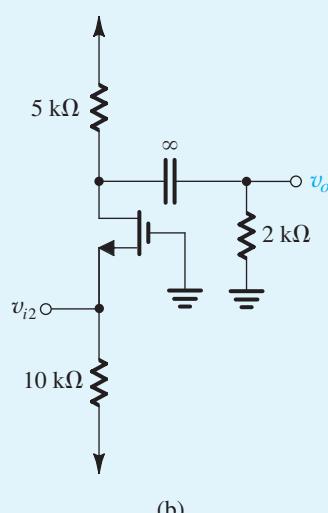
- If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of  $50\text{ }\mu\text{A}$  and having a resistance of  $100\text{ k}\Omega$ , find the voltage signal that can be measured at Y. For simplicity, neglect the effect of  $r_o$ .

#### \*7.122

- The NMOS transistor in the source-follower circuit of Fig. P7.122(a) has  $g_m = 10\text{ mA/V}$  and a large  $r_o$ . Find the open-circuit voltage gain and the output resistance.
- The NMOS transistor in the common-gate amplifier of Fig. P7.122(b) has  $g_m = 10\text{ mA/V}$  and a large  $r_o$ . Find the input resistance and the voltage gain.
- If the output of the source follower in (a) is connected to the input of the common-gate amplifier in (b), use the results of (a) and (b) to obtain the overall voltage gain  $v_o/v_i$ .



(a)



(b)

Figure P7.122

**D \*\*7.123** The MOSFET in the amplifier circuit of Fig. P7.123 has  $V_t = 0.6$  V,  $k_n = 5 \text{ mA/V}^2$ , and  $V_A = 60$  V. The signal  $v_{\text{sig}}$  has a zero average.

- It is required to bias the transistor to operate at an overdrive voltage  $V_{ov} = 0.2$  V. What must the dc voltage at the drain be? Calculate the dc drain current  $I_D$  taking into account  $V_A$ . Now, what value must the drain resistance  $R_D$  have?
- Calculate the values of  $g_m$  and  $r_o$  at the bias point established in (a).
- Using the small-signal equivalent circuit of the amplifier, show that the voltage gain is given by

$$\frac{v_o}{v_{\text{sig}}} = -\frac{R_2/R_1}{1 + \frac{1 + R_2/R_1}{g_m(R_D \parallel r_o \parallel R_2)(1 - 1/g_m R_2)}}$$

and find the value of the gain.

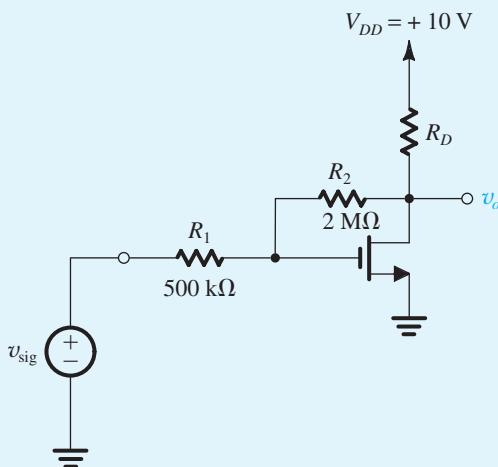


Figure P7.123

P.S. This feedback amplifier and the gain expression should remind you of an op amp utilized in the inverting configuration. We shall study feedback formally in Chapter 11.

**D \*\*7.124** The MOSFET in the amplifier circuit of Fig. P7.124 has  $V_t = 0.6$  V and  $k_n = 5 \text{ mA/V}^2$ . We shall assume that  $V_A$  is sufficiently large so that we can ignore the Early effect. The input signal  $v_{\text{sig}}$  has a zero average.

- It is required to bias the transistor to operate at an overdrive voltage  $V_{ov} = 0.2$  V. What must the dc voltage at the drain be? Calculate the dc drain current  $I_D$ . What value must  $R_D$  have?
- Calculate the value of  $g_m$  at the bias point.
- Use the small-signal equivalent circuit of the amplifier to show that

$$\frac{v_o}{v_{\text{sig}}} = \frac{1 + (R_2/R_1)}{1 + \frac{(1 + R_2/R_1)}{g_m R'_D}}$$

and

$$R_{\text{in}} = \frac{1}{g_m} (1 + g_m R'_D \frac{R_1}{R_1 + R_2})$$

where

$$R'_D = R_D \parallel (R_1 + R_2)$$

- Evaluate  $v_o/v_{\text{sig}}$  and  $R_{\text{in}}$ .

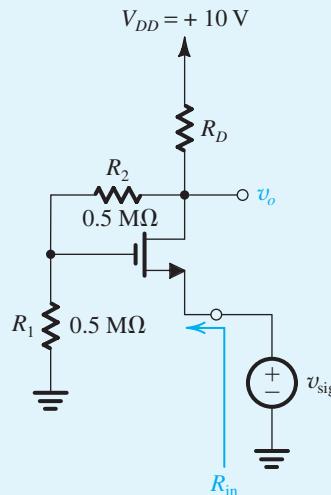


Figure P7.124

P.S. This feedback amplifier circuit and the gain formula should remind you of an op amp connected in the noninverting configuration. We shall study feedback formally in Chapter 11.

**D 7.125** For the common-emitter amplifier shown in Fig. P7.125, let  $V_{CC} = 15$  V,  $R_1 = 27$  k $\Omega$ ,  $R_2 = 15$  k $\Omega$ ,  $R_E = 2.4$  k $\Omega$ , and  $R_C = 3.9$  k $\Omega$ . The transistor has  $\beta = 100$ . Calculate the dc bias current  $I_C$ . If the amplifier operates between a source for which  $R_{sig} = 2$  k $\Omega$  and a load of 2 k $\Omega$ , replace the transistor with its hybrid- $\pi$  model, and find the values of  $R_{in}$ , and the overall voltage gain  $v_o/v_{sig}$ .

**D 7.126** Using the topology of Fig. P7.125, design an amplifier to operate between a 2-k $\Omega$  source and a 2-k $\Omega$  load with a gain  $v_o/v_{sig}$  of  $-40$  V/V. The power supply available is 15 V. Use an emitter current of approximately 2 mA and a current of about one-tenth of that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has  $\beta = 100$ . Use standard 5% resistors (see Appendix J).

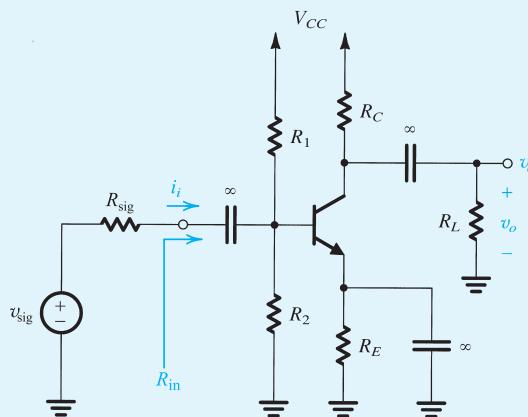


Figure P7.125

**D 7.127** A designer, having examined the situation described in Problem 7.125 and estimating the available gain to be approximately  $-36.3$  V/V, wants to explore the possibility of improvement by reducing the loading

of the source by the amplifier input. As an experiment, the designer varies the resistance levels by a factor of approximately 3:  $R_1$  to 82 k $\Omega$ ,  $R_2$  to 47 k $\Omega$ ,  $R_E$  to 7.2 k $\Omega$ , and  $R_C$  to 12 k $\Omega$  (standard values of 5%-tolerance resistors). With  $V_{CC} = 15$  V,  $R_{sig} = 2$  k $\Omega$ ,  $R_L = 2$  k $\Omega$ , and  $\beta = 100$ , what does the gain become? Comment.

**D 7.128** The CE amplifier circuit of Fig. P7.128 is biased with a constant-current source  $I$ . It is required to design the circuit (i.e., find values for  $I$ ,  $R_B$ , and  $R_C$ ) to meet the following specifications:

- (a)  $R_{in} \simeq 10$  k $\Omega$ .
- (b) The dc voltage drop across  $R_B$  is approximately 0.2 V.
- (c) The open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never fall by more than approximately 0.4 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that  $v_{sig}$  is a sinusoidal source, the available supply  $V_{CC} = 5$  V, and the transistor has  $\beta = 100$ . Use standard 5% resistance values, and specify the value of  $I$  to one significant digit. What base-to-collector open-circuit voltage gain does your design provide? If  $R_{sig} = R_L = 20$  k $\Omega$ , what is the overall voltage gain?

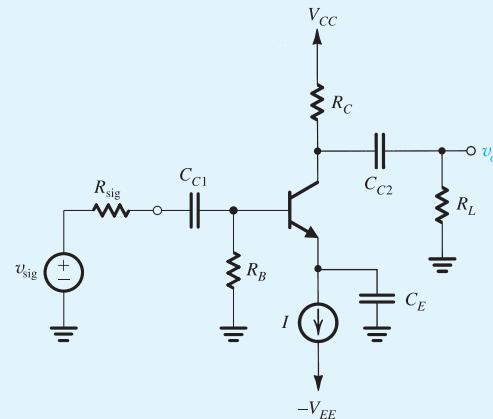


Figure P7.128

**D 7.129** In the circuit of Fig. P7.129,  $v_{\text{sig}}$  is a small sine-wave signal with zero average. The transistor  $\beta$  is 100.

- (a) Find the value of  $R_E$  to establish a dc emitter current of about 0.5 mA.

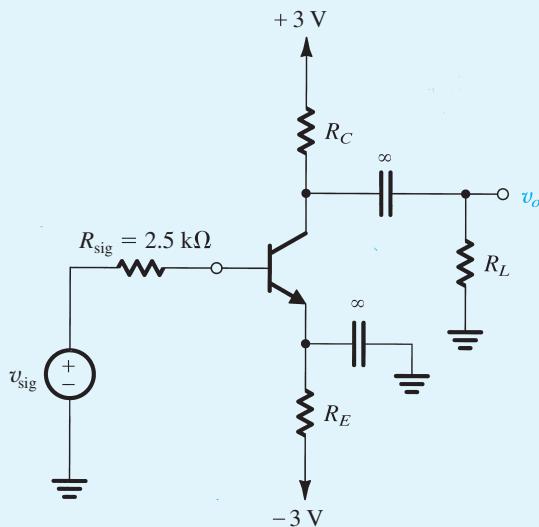


Figure P7.129

- (b) Find  $R_C$  to establish a dc collector voltage of about +0.5 V.

- (c) For  $R_L = 10 \text{ k}\Omega$ , draw the small-signal equivalent circuit of the amplifier and determine its overall voltage gain.

**\*7.130** The amplifier of Fig. P7.130 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage,  $R_{\text{in}2}$ , constitutes the load resistance of the first stage.

- (a) For  $V_{CC} = 15 \text{ V}$ ,  $R_1 = 100 \text{ k}\Omega$ ,  $R_2 = 47 \text{ k}\Omega$ ,  $R_E = 3.9 \text{ k}\Omega$ ,  $R_C = 6.8 \text{ k}\Omega$ , and  $\beta = 100$ , determine the dc collector current and dc collector voltage of each transistor.  
 (b) Draw the small-signal equivalent circuit of the entire amplifier and give the values of all its components.  
 (c) Find  $R_{\text{in}1}$  and  $v_{b1}/v_{\text{sig}}$  for  $R_{\text{sig}} = 5 \text{ k}\Omega$ .  
 (d) Find  $R_{\text{in}2}$  and  $v_{b2}/v_{b1}$ .  
 (e) For  $R_L = 2 \text{ k}\Omega$ , find  $v_o/v_{b2}$ .  
 (f) Find the overall voltage gain  $v_o/v_{\text{sig}}$ .

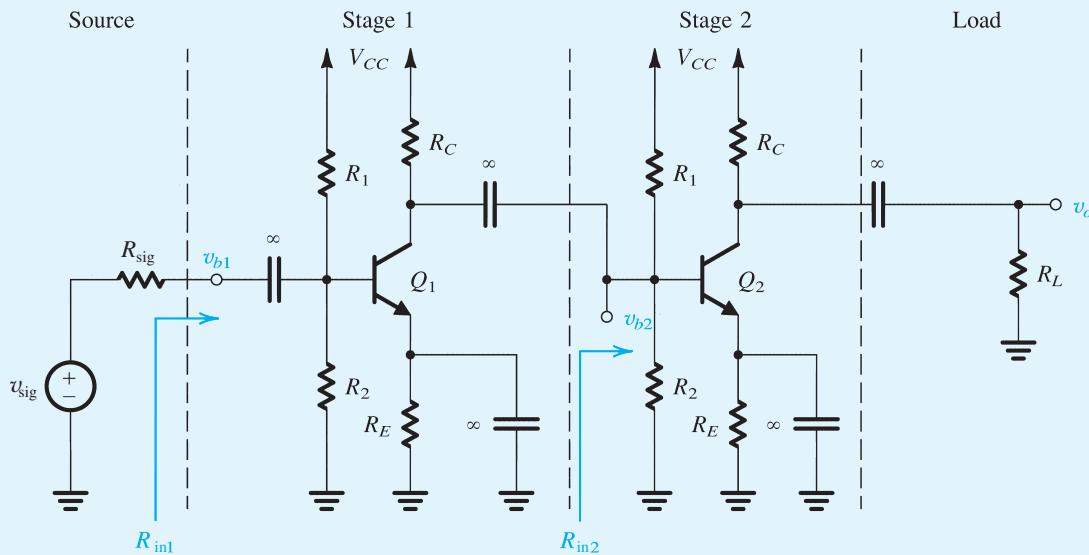


Figure P7.130

- 7.131** In the circuit of Fig. P7.131, the BJT is biased with a constant-current source, and  $v_{\text{sig}}$  is a small sine-wave signal. Find  $R_{\text{in}}$  and the gain  $v_o/v_{\text{sig}}$ . Assume  $\beta = 100$ . If the amplitude of the signal  $v_{be}$  is to be limited to 5 mV, what is the largest signal at the input? What is the corresponding signal at the output?

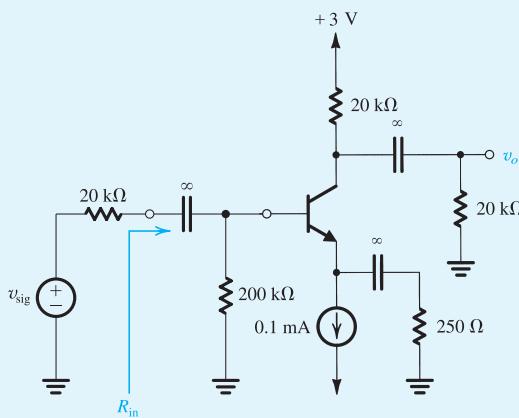


Figure P7.131

- \***7.132** The BJT in the circuit of Fig. P7.132 has  $\beta = 100$ .

- Find the dc collector current and the dc voltage at the collector.
- Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain  $v_o/v_i$ .

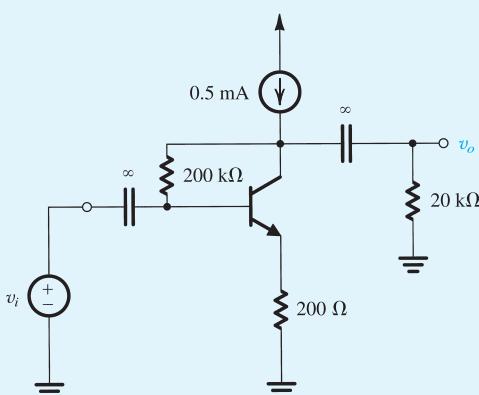


Figure P7.132

- 7.133** For the circuit in Fig. P7.133, find the input resistance  $R_{\text{in}}$  and the voltage gain  $v_o/v_{\text{sig}}$ . Assume that the source provides a small signal  $v_{\text{sig}}$  and that  $\beta = 100$ .

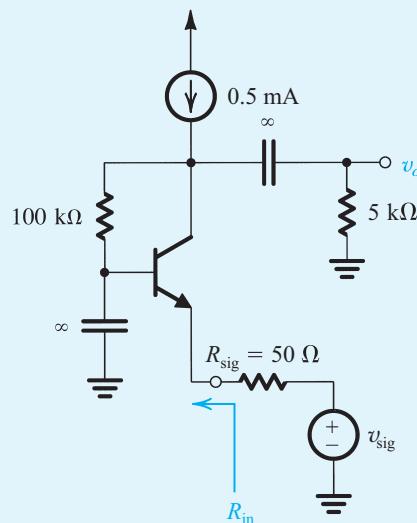


Figure P7.133

- 7.134** For the emitter-follower circuit shown in Fig. P7.134, the BJT used is specified to have  $\beta$  values in the range of 50 to 200 (a distressing situation for the circuit designer).

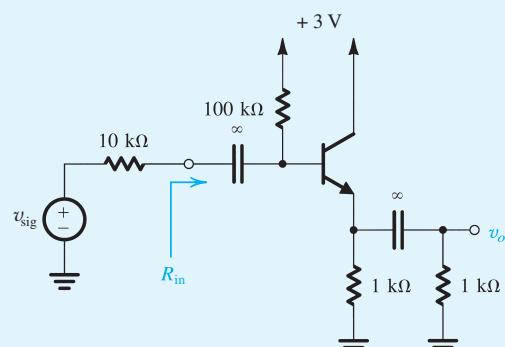


Figure P7.134

## 504 Chapter 7 Transistor Amplifiers

For the two extreme values of  $\beta$  ( $\beta=50$  and  $\beta=200$ ), find:

- $I_E$ ,  $V_E$ , and  $V_B$
- the input resistance  $R_{in}$
- the voltage gain  $v_o/v_{sig}$

**7.135** For the emitter follower in Fig. P7.135, the signal source is directly coupled to the transistor base. If the dc component of  $v_{sig}$  is zero, find the dc emitter current. Assume  $\beta=100$ . Neglecting  $r_o$ , find  $R_{in}$ , the voltage gain  $v_o/v_{sig}$ , the current gain  $i_o/i_i$ , and the output resistance  $R_{out}$ .

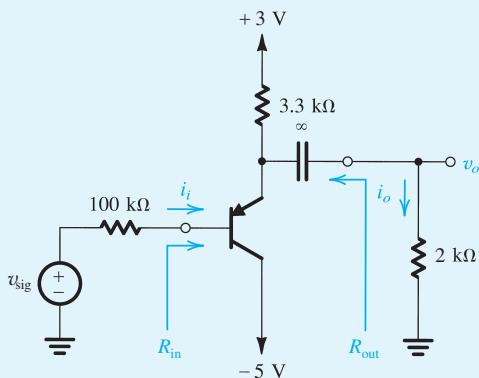


Figure P7.135

**\*\*7.136** For the circuit in Fig. P7.136, called a **bootstrapped follower**:

- Find the dc emitter current and  $g_m$ ,  $r_e$ , and  $r_\pi$ . Use  $\beta=100$ .
- Replace the BJT with its T model (neglecting  $r_o$ ), and analyze the circuit to determine the input resistance  $R_{in}$  and the voltage gain  $v_o/v_{sig}$ .
- Repeat (b) for the case when capacitor  $C_B$  is open-circuited. Compare the results with those obtained in (b) to find the advantages of bootstrapping.

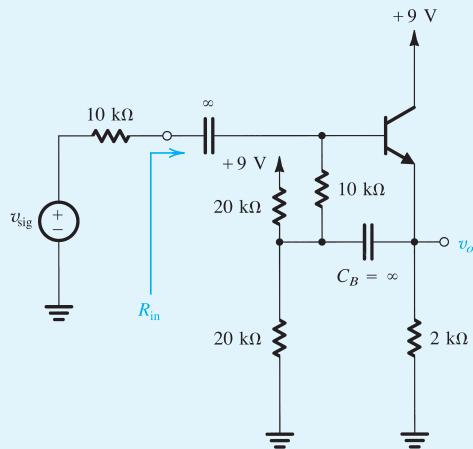


Figure P7.136

**\*\*7.137** For the follower circuit in Fig. P7.137, let transistor  $Q_1$  have  $\beta=50$  and transistor  $Q_2$  have  $\beta=100$ , and neglect the effect of  $r_o$ . Use  $V_{BE}=0.7\text{ V}$ .

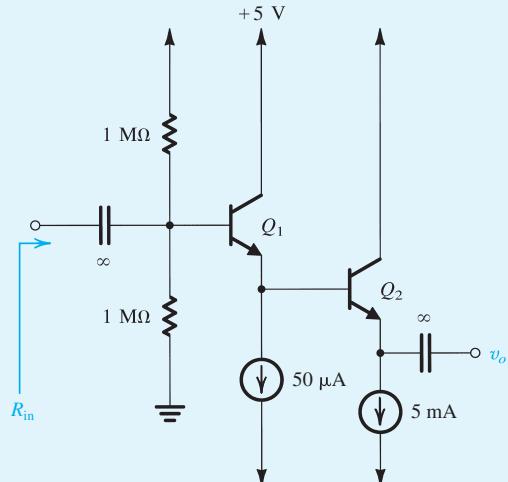


Figure P7.137

- (a) Find the dc emitter currents of  $Q_1$  and  $Q_2$ . Also, find the dc voltages  $V_{B1}$  and  $V_{B2}$ .
- (b) If a load resistance  $R_L = 1 \text{ k}\Omega$  is connected to the output terminal, find the voltage gain from the base to the emitter of  $Q_2$ ,  $v_o/v_{b2}$ , and find the input resistance  $R_{ib2}$  looking into the base of  $Q_2$ . (*Hint:* Consider  $Q_2$  as an emitter follower fed by a voltage  $v_{b2}$  at its base.)
- (c) Replacing  $Q_2$  with its input resistance  $R_{ib2}$  found in (b), analyze the circuit of emitter follower  $Q_1$  to determine its input resistance  $R_{in}$ , and the gain from its base to its emitter,  $v_{e1}/v_{b1}$ .
- (d) If the circuit is fed with a source having a  $100\text{-k}\Omega$  resistance, find the transmission to the base of  $Q_1$ ,  $v_{b1}/v_{sig}$ .
- (e) Find the overall voltage gain  $v_o/v_{sig}$ .

**D 7.138** A CE amplifier has a midband voltage gain of  $|A_M| = 100 \text{ V/V}$ , a lower 3-dB frequency of  $f_L = 100 \text{ Hz}$ , and a higher 3-dB frequency  $f_H = 500 \text{ kHz}$ . In Chapter 10 we will learn that connecting a resistance  $R_e$  in the emitter of the BJT results in lowering  $f_L$  and raising  $f_H$  by the factor  $(1 + g_m R_e)$ . If the BJT is biased at  $I_C = 1 \text{ mA}$ , find  $R_e$  that will result in  $f_H$  at least equal to  $2 \text{ MHz}$ . What will the new values of  $f_L$  and  $A_M$  be?

## APPENDIX L

# ANSWERS TO SELECTED PROBLEMS

### CHAPTER 1

- 1.1** (a) 5 mA; (b) 5 k $\Omega$ ; (c) 1 V; (d) 10 mA
- 1.3** (a) 5 V, 25 mW; (b) 5 k $\Omega$ , 5 mW; (c) 10 mA, 1 k $\Omega$ ; (d) 10 V, 100 k $\Omega$ ; (e) 31.6 mA, 31.6 V
- 1.5** 990 k $\Omega$ , 190 k $\Omega$ , 90 k $\Omega$ , 10 k $\Omega$ ; 9.9 k $\Omega$  (1% reduction), 9.09 k $\Omega$  (9.1% reduction), 5 k $\Omega$  (50% reduction)
- 1.7** 2 V, 1.2 k $\Omega$ ; 1.88 V to 2.12 V; 1.26 k $\Omega$  to 1.14 k $\Omega$
- 1.9** 4.80 V, Shunt the 10-k $\Omega$  resistor with 157 k $\Omega$ ; Add a series resistance of 200  $\Omega$ .
- 1.11** 10 k $\Omega$ , 5 k $\Omega$
- 1.15** 0.77 V, 12.31 k $\Omega$ , 0.05 mA
- 1.16** 0.75 mA, 0.5 mA, 1.25 mA, 2.5 V
- 1.20** (a)  $10^{-7}$  s,  $10^7$  Hz,  $6.28 \times 10^7$  rad/s; (f)  $10^3$  rad/s,  $1.59 \times 10^2$  Hz,  $6.28 \times 10^{-3}$  s
- 1.22** (a)  $(1-j 1.59)$  k $\Omega$ ; (b)  $(247.3-j 1553)$   $\Omega$ ; (c)  $(71.72-j 45.04)$  k $\Omega$ ; (d)  $(100+j 628)$   $\Omega$
- 1.24** 60 mV, 1.2  $\mu$ A, 50 k $\Omega$
- 1.25** 5 k $\Omega$
- 1.29** (a) 165 V; (b) 24 V
- 1.32** 14 kHz, 441 mV (peak); 312 mV; 693 mV, 71.4  $\mu$ s
- 1.34** 0, 110, 1011, 11100, 111011
- 1.36** (c) 12, 1.2 mV, 0.6 mV
- 1.38**  $7.056 \times 10^5$  bits/second.
- 1.40** 11 V/V or 20.8 dB; 22 A/A or 26.8 dB; 242 W/W or 23.8 dB; 120 mW, 95.8 mW, 20.2%
- 1.43** (a) 82.6 V/V or 38.3 dB
- 1.46** 0.69 V; 0.69 V/V or  $-3.2$  dB; 8280 A/A or 78.4 dB; 5713 W/W or 37.6 dB.
- 1.48** S-A-B-L is preferred as it provides higher voltage gain.
- 1.51** (a) 400 V/V; (b) 40 k $\Omega$ ,  $2 \times 10^4$  A/A,  $8 \times 10^6$  W/W; (c) 500  $\Omega$ ; (d) 750 V/V; (e) 100 k $\Omega$ , 100  $\Omega$ , 484 V/V
- 1.56** 38.1 V/V

- 1.59** Voltage amplifier,  $R_i = 1 \times 10^5 \Omega$ ,  $R_o = 1 \times 10^2 \Omega$ ,  $A_{vo} = 121 \text{ V/V}$
- 1.64** 1025 V/V or 60.2 dB, 2500 A/A or 68 dB,  $2.63 \times 10^6 \text{ W/W}$  or 64.2 dB
- 1.68** 4 MHz
- 1.70** 64 nF
- 1.73**  $0.51/CR$
- 1.75**  $0.8 \text{ k}\Omega$ ,  $8.65 \text{ k}\Omega$ , connect 2 nF to node B.
- 1.78** 159 kHz; 14.5 Hz;  $\simeq 159 \text{ kHz}$
- 1.81** 10 Hz, 10 kHz, 0.04 dB, 0.04 dB, 10 Hz, 10 kHz

## CHAPTER 2

- 2.2** 4004 V/V
- 2.5** 40,000 V/V
- 2.7** 0.1%
- 2.8** In all cases,  $-5 \text{ V/V}$ ,  $20 \text{ k}\Omega$
- 2.11** (a)  $-1 \text{ V/V}$ ; (c)  $-0.1 \text{ V/V}$ ; (e)  $-10 \text{ V/V}$
- 2.13**  $10 \text{ k}\Omega$ ,  $100 \text{ k}\Omega$
- 2.15** Average =  $+5 \text{ V}$ , highest =  $+10 \text{ V}$ , lowest =  $0 \text{ V}$
- 2.17**  $\pm 2x\%$ ;  $-98$  to  $-102 \text{ V/V}$
- 2.19**  $1.8 \text{ k}\Omega$ ;  $18 \text{ k}\Omega$
- 2.21**  $\pm 2 \text{ mV}$
- 2.24**  $1000 \left(1 + \frac{R_2}{R_1}\right)$ ,  $100 \left(1 + \frac{R_2}{R_1}\right)$ ,  $10 \left(1 + \frac{R_2}{R_1}\right)$ ;  $1000 R_1$ ,  $100 R_1$ ,  $10 R_1$
- 2.26** (b)  $1 \text{ k}\Omega$ ,  $100 \text{ k}\Omega$ ,  $909 \text{ V/V}$
- 2.28** (a)  $10.2 \text{ k}\Omega$
- 2.32** (a)  $0.1 \text{ mA}$ ,  $0.1 \text{ mA}$ ,  $10 \text{ mA}$ ,  $10.1 \text{ mA}$ ,  $-1 \text{ V}$ ; (b)  $1.19 \text{ k}\Omega$ ; (c)  $-11.1 \text{ V}$  to  $-2.01 \text{ V}$
- 2.34** (a)  $1 \text{ k}\Omega$ ; (b)  $0, \infty$ ; (c)  $-0.57 \text{ mA}$  to  $+0.57 \text{ mA}$  (d)  $2.2 \text{ mA}$
- 2.36**  $v_o = -(10 v_i + 5 v_2); -5 \text{ V}$
- 2.43**  $12.8 \text{ k}\Omega$
- 2.44** (a)  $\infty$ ; 0; (b)  $10 \text{ k}\Omega$ ,  $10 \text{ k}\Omega$ ; (d)  $10 \text{ k}\Omega$ ,  $990 \text{ k}\Omega$
- 2.46**  $100 \text{ k}\Omega$ ; no
- 2.50**  $2 \sin (2\pi \times 1000t)$
- 2.51**  $1/x$ ; 1 to  $\infty$ ; add 1-k $\Omega$  resistor between the left end of the pot and ground.

**2.53** (a) 10 mV, 10  $\mu$ A, 10  $\mu$ A; (b) 10 V, 10 mA, 0; from the power supply of the op amp

**2.58** (a)  $-0.83$  V/V, 17%; (c)  $-0.98$  V/V, 2%; (e)  $-9$  V/V, 10%

**2.60** 20 V/V, 10 k $\Omega$ , 0.0095 V/V, 66.4 dB

**2.64**  $R_1 = R_3, R_2 = R_4$

**2.65**  $0.02x$  V/V; 0.002 V/V, 54 dB; 0.02 V/V, 34 dB; 0.1 V/V, 20 dB

**2.67** 1 k $\Omega$ , 1 M $\Omega$ , 1 k $\Omega$ , 1 M $\Omega$ ; 1% tolerances

**2.69**  $R = 1$  M $\Omega$ ,  $R_5 = 756$   $\Omega$ ,  $R_6 = 6.8$  k $\Omega$

**2.73** (a)  $-0.12$  V to  $+0.12$  V; (b)  $-12$  V to  $+12$  V

**2.75** Ideal: 21 V/V, 0,  $\infty$ ;  $\pm 1\%$  resistors:  $A_d = 21 \pm 4\%$ ,  $|A_{cm}| = 0.02$ , CMRR = 60.4 dB

**2.77** (a)  $v_B/v_A = 3$  V/V,  $v_C/v_A = -3$  V/V; (b) 6 V/V; (c) 56 V pp, 19.8 V rms

**2.79** (a) 1591 Hz; (b) leads by  $90^\circ$ ; (c) increases by a factor of 10; (d) the same as in (b)

**2.81** 1 MHz; 0.159  $\mu$ s

**2.83**  $R = 10$  k $\Omega$ ,  $C = 159$  pF;  $R_f = 1$  M $\Omega$ , 1 kHz; (a)  $v_o$  decreases linearly to  $-6.3$  V, (b)  $v_o$  decreases exponentially,  $v_o(t) = -100(1 - e^{-t/159})$ , reaching  $-6.1$  V at the end of the pulse.

**2.86**  $R_1 = 10$  k $\Omega$ ,  $R_2 = 1$  M $\Omega$ ,  $C = 0.16$  nF; 100 kHz

**2.88** 15.9 kHz,  $v_o = -5 \sin(10^6 t + 90^\circ)$  V

**2.90** Square wave of the same frequency, 8 V peak amplitude, average is 0 V; 30 k $\Omega$

**2.92**  $R_1 = 1$  k $\Omega$ ,  $R_2 = 100$  k $\Omega$ ,  $C = 79$  nF; 20 Hz

**2.94** 4 mV

**2.96** 9 mV; 12 mV

**2.98** (a) 0.53  $\mu$ A, into the input terminals; (b)  $-3$  mV; (c)  $-60$  nA

**2.100**  $R_1 = 1.01$  k $\Omega$ ,  $R_2 = R_3 = 100$  k $\Omega$ ,  $C_1 = 1.58$   $\mu$ F,  $C_2 = 0.16$   $\mu$ F

**2.102** 6 V; 3 V; 9 mV

**2.104** (a) 0.2 V; (b) 0.4 V; (c) 10 k $\Omega$ , 20 mV; (d) 0.22 V

**2.106** (a) 9.9 k $\Omega$ ; (b) 0.222 V

**2.108** 80,000 V/V, 125 Hz, 10 MHz

**2.111** 19.61 kHz, 49.75 V/V, 4.975 V/V

**2.113** (a) 5.1 MHz; (c) 10 MHz; (e) 10.1 MHz; (g) 2 MHz

**2.116** 36.6 MHz

**2.118** 500 MHz; 3; 7 MHz; 3.6 MHz

**2.121** 100 mV

**2.125** 1 MHz, 3.18 V

## CHAPTER 3

- 3.1**  $-55^{\circ}\text{C}$ :  $2.68 \times 10^6 \text{ cm}^{-3}$ , one out of every  $1.9 \times 10^{16}$  silicon atoms;  $+75^{\circ}\text{C}$ :  $3.70 \times 10^{11} \text{ cm}^{-3}$ ,  $N/n_i = 1.4 \times 10^{11}$
- 3.3**  $5 \times 10^{18} \text{ cm}^{-3}$ ;  $45 \text{ cm}^{-3}$ ;
- 3.5** At  $27^{\circ}\text{C}$ :  $n_n = 10^{17}/\text{cm}^3$ ,  $p_n = 2.25 \times 10^3 \text{ cm}^3$ ;  
At  $125^{\circ}\text{C}$ :  $n_n = 10^{17}/\text{cm}^3$ ,  $p_n = 2.23 \times 10^8 \text{ cm}^3$
- 3.7**  $v_{p-\text{drift}} = 1.44 \times 10^6 \text{ cm/s}$ ,  $v_{n-\text{drift}} = 4.05 \times 10^6 \text{ cm/s}$
- 3.9**  $9.26 \times 10^{17}/\text{cm}^3$
- 3.12**  $778 \text{ mV}$ ;  $0.2 \mu\text{m}$ ,  $0.1 \mu\text{m}$ ,  $0.1 \mu\text{m}$ ;  $1.6 \times 10^{-14}\text{C}$
- 3.14**  $1.6 \text{ pC}$
- 3.16**  $59.6 \text{ mV}$
- 3.20**  $7.85 \times 10^{-17} \text{ A}$ ;  $0.3 \text{ mA}$
- 3.22**  $3.6 \times 10^{-16} \text{ A}$ ;  $0.742 \text{ V}$
- 3.24**  $31.6 \text{ fF}$ ;  $14.16 \text{ fF}$
- 3.27**  $0.5 \text{ pF}$ ;  $129.5 \text{ ps}$

## CHAPTER 4

- 4.2** (a)  $-3 \text{ V}$ ,  $0.6 \text{ mA}$ ; (b)  $+3 \text{ V}$ ,  $0 \text{ mA}$
- 4.3** (a)  $V = 2 \text{ V}$ ,  $I = 2.5 \text{ mA}$ ; (b)  $I = 1 \text{ mA}$ ,  $V = 1 \text{ V}$
- 4.6**  $X = AB$ ;  $Y = A + B$ ;  $X$  and  $Y$  are the same for  $A = B$ ;  $X$  and  $Y$  are opposite if  $A \# B$ .
- 4.9** (a)  $I = 0$ ,  $V = 1 \text{ V}$ ; (b)  $I = 0.25 \text{ mA}$ ,  $V = 0 \text{ V}$
- 4.11**  $R \geq 4.2 \text{ k}\Omega$ ,  $169.7 \text{ V}$
- 4.13**  $2.5 \text{ V}$ ;  $1.25 \text{ V}$ ;  $25 \text{ mA}$ ;  $12.5 \text{ mA}$ ;  $2.5 \text{ V}$
- 4.15**  $34 \text{ V}$ ;  $8.3 \Omega$ ;  $0.6 \text{ A}$ ;  $29 \text{ V}$ ;  $34 \text{ V}$ ,  $8 \Omega$ ;  $25\%$ ;  $103 \text{ mA}$ ;  $0.625 \text{ A}$ ;  $29 \text{ V}$
- 4.17** At  $-55^{\circ}\text{C}$ ,  $V_T = 18.8 \text{ mV}$ ; At  $+55^{\circ}\text{C}$ ,  $V_T = 28.3 \text{ mV}$ ;  $V_T = 25 \text{ mV}$  at  $17^{\circ}\text{C}$ .
- 4.19**  $0.335 \mu\text{A}$
- 4.21** (a)  $6.91 \times 10^{-13} \text{ A}$ ,  $0.64 \text{ V}$ ; (c)  $5.11 \times 10^{-17} \text{ A}$ ,  $0.59 \text{ V}$
- 4.23**  $3.9 \text{ mA}$ ;  $-22 \text{ mV}$
- 4.26**  $A_4 = 2A_3 = 4A_2 = 8A_1 = 1.5 \text{ mA}$
- 4.28**  $42 \Omega$
- 4.31**  $50^{\circ}\text{C}$ ;  $6 \text{ W}$ ;  $8.33^{\circ}\text{C/W}$
- 4.33**  $230 \text{ mV}$ ; independent of temperature

**4.35** 0.6635 V, 0.3365 mA**4.37**  $R = 582 \Omega$ **4.41** (a) -2.3 V, 0.53 mA; (b) +3 V, 0 mA**4.43** (a)  $I = 0$ ,  $V = -1.23$  V; (b)  $I = 0.133$  mA,  $V = 0$  V**4.45**  $R \geq 4.23$  k $\Omega$ , 169.7 V; essentially the same.**4.48** 0.24 mV, 2.0 mV, 9.6 mV; 25  $\mu$ A**4.53**  $V_o/V_i = 1/(1+j\omega Cr_d)$ ;  $-\tan^{-1}(\omega C V_T/I)$ ; 157  $\mu$ A  $-84.3^\circ$  to  $-5.71^\circ$ **4.56**  $R = 417 \Omega$ ; 7.39 mA; 6.8 mV; -3.4 mV; -6.8 mV; -13.6 mV**4.59** (a)  $r_z = 8 \Omega$ , 1.04 W; (b)  $V_{Z0} = 8.8$  V, 188 mW**4.61** 88.9 mV**4.63** 167  $\Omega$ ; 7.65 V; 7.35 V; 7.78 V; 707  $\Omega$ ; 7.2 V**4.66** (a) 9.825 V; (b) 207  $\Omega$ ; (c) 33 mV/V,  $\pm 1.65\%$ ; (d) -6.77 V/A, -1.35%; (e) 70.9 mA, 732 mW**4.69** 0.324 V**4.71** 13.44 V; 48.4%; 8.3 V; 8.3 mA**4.73** (a) 10.1:1; (b) 1.072:1**4.75** 45 V**4.77** (a) 12.77 V, 13.37 V; (b) 7.1%, 2.24%; (c) 192 mA, 607 mA; (d) 371 mA; 1.2 A**4.80** (a) 9.7 V; (b) 542  $\mu$ F; (c) 25.7 V, 38.5 V; (d) 739 mA; (e) 1.42 A**4.83** 10.74 V; 23.5  $\mu$ s; 4.913 A; 4.913 A**4.85** (a) +1 V, +2 V, +2.7 V; (b) +3 V, +6 V, +6.7 V; (c) 0 V, 0 V, 0 V, -13 V; (d) 0 V, 0 V, -13 V.**4.96** -7.07 V

## CHAPTER 5

**5.1** 580 to 2900  $\mu\text{m}^2$ ; 24 to 54  $\mu\text{m}$ **5.4** (a) 0.5; (b) 0.5; (c) 1.0; (d) 0.5**5.7** 0.35  $\mu\text{m}$ **5.9** 0.5 V; 0.5 mA**5.11** (a) -1.1 V; (b) -0.4 V; (c) 0.05 mA; 0.5 mA**5.13** 116.3  $\Omega$ , 116.3 mV; 50**5.17** 2.8 V; 500  $\Omega$ , 100  $\Omega$

- 5.19**  $5 \text{ mA/V}^2$ ; 0.6 V
- 5.21** 0.5 V; 20;  $145 \mu\text{A}$ ; 1.5 V, 1.125 mA
- 5.23**  $2.5 \text{ k}\Omega$  to  $125 \Omega$ ; (a)  $5 \text{ k}\Omega$  to  $250 \Omega$ ; (b)  $1.25 \text{ k}\Omega$  to  $62.5 \Omega$ ; (c)  $2.5 \text{ k}\Omega$  to  $125 \Omega$ .
- 5.29** (a) 3%; (b) 5%
- 5.31**  $200 \text{ k}\Omega$ ,  $20 \text{ k}\Omega$ ; 5%, 5%
- 5.33**  $104 \mu\text{A}$ ; 4%; double  $L$  to  $3 \mu\text{m}$
- 5.35** Increases by a factor of 16.
- 5.38**  $350 \mu\text{A}$ ;  $750 \mu\text{A}$ ;  $864 \mu\text{A}$ ;  $880 \mu\text{A}$ ;  $960 \mu\text{A}$
- 5.41** At 3.0 V, transistor is cut off; at 2.5 V, transistor enters saturation region; at 0.5 V, transistor enters triode region.
- 5.43** 1 V, 0 V, 1 V, 0.25 V;  $5 \text{ k}\Omega$ ,  $5 \text{ k}\Omega$ ,  $5 \text{ k}\Omega$ ,  $5 \text{ k}\Omega$ ;  $10 \text{ k}\Omega$ , 2 V;  $10 \text{ k}\Omega$ ,  $-1 \text{ V}$ ;  $10 \text{ k}\Omega$ , 2 V;  $10 \text{ k}\Omega$ ,  $-0.75 \text{ V}$
- 5.45** 0.08 mA;  $10 \text{ k}\Omega$ ,  $5 \text{ k}\Omega$ ;  $17.5 \text{ k}\Omega$
- 5.48**  $4 \text{ k}\Omega$
- 5.50**  $4 \mu\text{m}$ ,  $11.1 \mu\text{m}$ ;  $1.4 \text{ k}\Omega$
- 5.52** 0.45 mA,  $+7.3 \text{ V}$ ; quite tolerant.
- 5.54** 44.4;  $1.25 \text{ k}\Omega$
- 5.56**  $-1 \text{ V}$ ,  $-1.43 \text{ V}$ ,  $-2.8 \text{ V}$ ,  $1 \text{ V}$ ,  $2.8 \text{ V}$ ,  $+1 \text{ V}$ ,  $2.8 \text{ V}$ ,  $-1 \text{ V}$
- 5.59**  $I_1 = 405 \mu\text{A}$ ,  $V_2 = 1.5 \text{ V}$ ;  $I_3 = 217 \mu\text{A}$ ,  $V_4 = 1.232 \text{ V}$ ;  $V_5 = 1.5 \text{ V}$ ,  $I_6 = 405 \mu\text{A}$
- 5.61** (a) 0.5 V, 0.5 V,  $-0.983 \text{ V}$ ; (b) 0.1 V, 0.9 V,  $-1.01 \text{ V}$
- 5.63**  $-1.24 \text{ V}$
- 5.65** triode, 0.59 mA; triode, 5 mA; saturation, 9 mA; saturation, 9 mA

## CHAPTER 6

- 6.2**  $4.7 \times 10^{-17} \text{ A}$ ,  $1.87 \times 10^{-16} \text{ A}$ ;  $A_2/A_1 = 4$
- 6.4** 0.31 V
- 6.6** Old: 0.673 V; New: 0.846 V
- 6.8** 80; 0.988
- 6.10** 0.5; 0.67; 0.91; 0.95; 0.98; 0.99; 0.995; 0.998; 0.999
- 6.12**  $I_C = 0.5 \text{ mA} \rightarrow 3 \text{ mA}$ ;  $I_E = 0.51 \text{ mA} \rightarrow 3.01 \text{ mA}$ ;  $30 \text{ mW}$
- 6.14**  $990 \mu\text{A}$ , 99, 0.99;  $980 \mu\text{A}$ , 49, 0.98;  $950 \mu\text{A}$ , 19, 0.95
- 6.17**  $-0.668 \text{ V}$ ;  $1.04 \text{ V}$ ; 0.02 mA

- 6.19** EBJ: 0.691 V; CBJ: 0.576 V; EBJ: 0.49  $\mu$ A; CBJ: 48.5  $\mu$ A
- 6.23** 0.758 V; 0.815 V
- 6.25** 238 mA;  $6 \times 10^{-14}$  A; 87
- 6.28** (a) 2 mA, -0.7 V; (b) -2 V; (c) 2 V, 0.5 mA; (d) 1.6 mA, -4.5 V
- 6.30** 8.3 k $\Omega$ ; 20; 100; 200
- 6.32**  $R_C = 4$  k $\Omega$ ;  $R_E = 3.64$  k $\Omega$ ;  $R_{C\max} = 5.86$  k $\Omega$
- 6.34**  $R_E = 3.66$  k $\Omega$ ;  $R_C = 5$  k $\Omega$
- 6.36** 10.24  $\mu$ A
- 6.38** 0.75 V; 0.55 V
- 6.40** 3.35  $\mu$ A; 3000
- 6.43** 125 k $\Omega$ ; 125 V; 12.5 k $\Omega$
- 6.45** 1 mA; 10 V; 50 V; 50 k $\Omega$
- 6.47**  $\beta = 100$ ;  $\beta_{ac} = 80$ ;  $\Delta i_C = 0.18$  mA,  $i_C = 1.18$  mA
- 6.50**  $\beta_{\text{forced}} = 11.2$ ;  $V_C = 4.8$  V;  $R_B = 45.7$  k $\Omega$
- 6.52** 2.05 V, 2.38 V
- 6.55**  $R_1 = 18$  k $\Omega$ ,  $R_2 = 12$  k $\Omega$ ; 0.46 mA, 2.54 V
- 6.58** +0.41 V, +1.11 V, -1.15 V; +1.2 V, +1.9 V, -1.9 V; 204
- 6.61** (a) -0.7 V, +1.2 V; (b) +1.2 V, 0.5 mA; (c) -0.7 V, 0 V, +1.2 V; (d) +1.45 V, -0.5 V; (e) +0.75 V, +1.45 V, -0.5 V
- 6.63**  $R_E = 4$  k $\Omega$ ,  $R_B = 50$  k $\Omega$ ,  $R_C = 4$  k $\Omega$ ,  $I_C = 0.85$  mA to 0.98 mA,  $V_C = -1.6$  V to -1.1 V
- 6.66** (a) 0 V, +0.7 V, -0.725 V, -1.425 V, +1.1 V; (b) +0.23 V +0.93 V, -1 V, -1.7 V, +1.47 V
- 6.68** 0 V, 0 V; +1.8 V, +1.1 V; -2.2 V, -1.5 V; -3 V, -2.3 V

## CHAPTER 7

- 7.2** A: (0.5 V, 5 V); B: (0.72 V, 0.22 V)
- 7.3** 20 k $\Omega$ ; (0.72 V, 0.22 V); -40 V/V; 0.78 V; 19.5 mV
- 7.6** 0.4 V; 8.33
- 7.8** (a) 0.712 V; (b) -42.7 V/V, 11.7 mV; (c) 42.88 k $\Omega$ ; 24.9
- 7.10** -160 V/V; 0.7 V; 4.4 mV
- 7.12** 1.08 V; 0.78 V; -156.7 V/V
- 7.15** -60 V/V

- 7.18** 3 mA;  $-120 \text{ V/V}$ ;  $+5 \text{ mV}$ : exp.  $\rightarrow -660 \text{ mV}$ , linear  $\rightarrow -600 \text{ mV}$ ;  
 $-5 \text{ mV}$ : exp.  $\rightarrow +540 \text{ mV}$ , linear  $\rightarrow +600 \text{ mV}$ .
- 7.25** (a) 0.1 mA, 0.8 V; (b) 1 mA/V; (c)  $-10 \text{ V/V}$ ; (d)  $100 \text{ k}\Omega$ ,  $-9.1 \text{ V/V}$
- 7.26** 0.5 mA/V; 0.067 mA, 0.27 V; 9.14; 0.67 V
- 7.29**  $16 \mu\text{m}$ ; 0.75 V
- 7.31**  $-18.2 \text{ V/V}$ ; 1.207 V,  $-23.6 \text{ V/V}$
- 7.33** (b) 2 mA/V,  $200 \text{ k}\Omega$ ; (d)  $3.33 \text{ M}\Omega$ ,  $0.94 \text{ V/V}$ ,  $-15.38 \text{ V/V}$ ,  $-14.5 \text{ V/V}$
- 7.35** 2.5 V; 0.611 mA, 1.95 V; 5 mV;  $-0.55 \text{ V}$ ;  $-110 \text{ V/V}$ ;  $-100 \text{ V/V}$
- 7.37** 40 mA/V;  $25 \Omega$ ;  $2.5 \text{ k}\Omega$ ; 1 V
- 7.39** 1.04 k $\Omega$  to 4.7 k $\Omega$
- 7.42** (a) 1.000,  $\infty$ , 1.00 mA, 1.00 mA, 0 mA, 40 mA/V,  $25 \Omega$ ,  $\infty \Omega$ ; (c) 0.980, 50, 1.00 mA,  
 1.02 mA, 0.02 mA, 40 mA/V,  $24.5 \Omega$ ,  $1.25 \text{ k}\Omega$ ; (e) 0.990, 100, 0.248 mA, 0.25 mA,  
 0.002 mA, 9.92 mA/V,  $100 \Omega$ ,  $10.1 \text{ k}\Omega$
- 7.48** 1 V;  $125 \Omega$ ; 80 V/V
- 7.53**  $R_{\text{in}} = 75 \Omega$ ;  $v_o/v_{\text{sig}} = 39.6 \text{ V/V}$
- 7.55**  $-1000 \text{ V/V}$ ;  $-5000 \text{ V/V}$
- 7.57**  $8.6 \text{ k}\Omega$ ,  $7.7 \text{ k}\Omega$ ; 77 V/V
- 7.59** 79.4 V/V; 4762 A/A
- 7.64**  $-10 \text{ V/V}$
- 7.66** 1 mA/V;  $125 \mu\text{A}$ ;  $-7.5 \text{ V/V}$
- 7.68**  $5 \text{ k}\Omega$ ,  $10 \text{ k}\Omega$ ,  $-200 \text{ V/V}$ ;  $-100 \text{ V/V}$ ,  $-33.3 \text{ V/V}$ ; 15 mV, 0.5 V
- 7.70** (b) 1250 V/V
- 7.72**  $0.5 \text{ k}\Omega$
- 7.74**  $30.3 \text{ k}\Omega$ ,  $-40 \text{ V/V}$ ,  $12 \text{ k}\Omega$ ;  $-20 \text{ V/V}$ ,  $-15 \text{ V/V}$ ; 6.65 mV, 100 mV
- 7.76** 80 V/V, 44.4 V/V to 109.1 V/V;  $R_e = 275 \Omega$ , 25 V/V, 20 V/V to 27.3 V/V
- 7.78** 2.5 mA/V; 0.2 V
- 7.80**  $i_{\text{sig}}R_C$
- 7.82** 0.357 k $\Omega$ ; 1.6 mA; 1.13 V
- 7.84** 1.25 mA; 1.5 mA, 1.0 mA; 0.5 V/V; 1 V
- 7.86**  $149 \Omega$ ,  $0.87 \text{ V/V}$ ;  $116 \Omega$  to  $246 \Omega$ ;  $0.80 \text{ V/V}$  to  $0.90 \text{ V/V}$
- 7.89**  $-91 \text{ V/V}$
- 7.91** 27.5 V/V, 41.2 V/V, 55.6 V/V, 57.1 V/V, 55.6 V/V; 0.325 mA
- 7.92** 18 M $\Omega$ , 22 M $\Omega$ , 3 k $\Omega$ , 3 k $\Omega$ ; 2 V
- 7.94** 5.07 V, 1.27 mA to 2.48 mA;  $620 \Omega$ ; 0.91 mA to 1.5 mA

- 7.96** 2 V; 2.4 V; 1.2 mA
- 7.101** (a) 2.7 V, 2.2 V; (b) 3.05 V, 3.05 V
- 7.103** 2.5 k $\Omega$ , 22 M $\Omega$ , 20 M $\Omega$
- 7.105** (a) 230 k $\Omega$ ; 0.5 mA to 1.5 mA; 1 V to 0 V (saturated transistor), design very intolerant of  $\beta$  variation.
- 7.108** (a) 5.73; (b)  $V_{BB} = V_{BE} + 0.352 V_{CC}$ ; (c) 38.8 k $\Omega$ , 37.5 k $\Omega$ , 3.33 k $\Omega$ ; (d) 8.1 k $\Omega$ ; 0.475 mA to 0.509 mA with a nominal value of 0.5 mA
- 7.110** 5.75 k $\Omega$ , 6.2 k $\Omega$ ; 10.8%
- 7.112** (a)  $R_C = 1.5 \text{ k}\Omega$ ,  $R_B = 80 \text{ k}\Omega$ ; (b)  $R_C = 1.5 \text{ k}\Omega$ ,  $R_B = 82 \text{ k}\Omega$ ; 1.52 V, 0.98 mA; (c) 0.7 V, 1.53 mA; (d)  $R_{B1} = 40 \text{ k}\Omega$ ,  $R_{B2} = 70 \text{ k}\Omega$ ,  $R_C = 1.47 \text{ k}\Omega$ , 1.1 V, 1.28 mA
- 7.116** 8.6 k $\Omega$ , +0.4 V
- 7.118** (a)  $V_D = 2.5 \text{ V}$ ,  $k_n = 11.1 \text{ mA/V}^2$ ; (b) 120 k $\Omega$ , -4.1 V/V; (c) 0.264 V, 1.08 V; (d) 300  $\Omega$ , 1.08 V
- 7.120** 20 mA/V; 0.1 mA; 5 mV; 10 k $\Omega$
- 7.122** (a) 0.99 V/V, 99  $\Omega$ ; (b) 99  $\Omega$ , 14.3 V/V; (c) 7.15 V/V
- 7.124** (a) 1.6 V, 0.1 mA, 82.4 k $\Omega$ ; (b) 1 mA/V; (d) 1.95 V/V, 39.1 k $\Omega$
- 7.126**  $R_1 = 47 \text{ k}\Omega$ ,  $R_2 = 24 \text{ k}\Omega$ ,  $R_E = 2.2 \text{ k}\Omega$ ,  $R_C$  either 4.7 k $\Omega$  or 5.1 k $\Omega$
- 7.128**  $R_B = 91 \text{ k}\Omega$ ,  $R_C = 22 \text{ k}\Omega$ ,  $I = 0.2 \text{ mA}$ ; -176 V/V; -29.7 V/V
- 7.130** (a) 1 mA, 8.2 V; (c) 2.32 k $\Omega$ , 0.32 V/V; (d) 2.32 k $\Omega$ , -69.2 V/V; (e) -61.8 V/V; (f) 1368.5 V/V
- 7.132** (a) 0.495 mA, 1.18 V; -71.9 V/V
- 7.134**  $\beta = 50$ : (a) 0.78 mA, 0.78 V, 1.48 V; (b) 21.3 k $\Omega$ ; (c) 0.64 V/V;  $\beta = 200$ : (a) 1.54 mA, 1.54 V, 2.24 V; (b) 50.9 k $\Omega$ ; (c) 0.81 V/V
- 7.136** (a) 1.73 mA, 68.4 mA/V, 14.5  $\Omega$ , 1.4645 k $\Omega$ ; (b) 148.3 k $\Omega$ , 0.93 V/V; (c) 18.21 k $\Omega$ , 0.64 V/V
- 7.138** 75  $\Omega$ ; 25 Hz; 25 V/V

## CHAPTER 8

- 8.1** 12 k $\Omega$ ; 0.2 V; 25 k $\Omega$ ; 20  $\mu$ A
- 8.3** 50; 8.75 k $\Omega$
- 8.6** 5  $\mu$ m, 25  $\mu$ m, 10  $\mu$ m, 2.5  $\mu$ m, 5  $\mu$ m; 15 k $\Omega$ ; 25 k $\Omega$ , 31.25 k $\Omega$
- 8.8** (a) 0.691 V to 0.863 V, 10  $\mu$ A to 10 mA; (b) 9.62  $\mu$ A, 0.098 mA, 0.98 mA, 9.62 mA
- 8.11** 0.1 mA, 10%

- 8.14** Both cases:  $-0.7 \text{ V}$ ,  $+2 \text{ V}$ ,  $+0.7 \text{ V}$ ,  $-0.7 \text{ V}$ ,  $-1.7 \text{ V}$ ; (a)  $I = 0.4 \text{ mA}$ ; (b)  $I = 0.04 \text{ mA}$
- 8.17**  $700 \Omega$ ,  $5 \text{ A/A}$ ,  $10 \text{ k}\Omega$ .
- 8.19**  $v_o = g_{m1}v_i (W_3/W_2)R_L$ ;  $g_{m1}R_L (W_3/W_2)$ ;  $1/g_{m2}$ ;  $-g_{m1}/g_{m2}$
- 8.21** (a)  $1.6 \text{ k}\Omega$ ; (b)  $250 \Omega$
- 8.25**  $I = 10 \mu\text{A}$ :  $0.4 \text{ mA/V}$ ,  $250 \text{ k}\Omega$ ,  $1 \text{ M}\Omega$ ,  $400 \text{ V/V}$ ;  $I = 100 \mu\text{A}$ :  $4 \text{ mA/V}$ ,  $25 \text{ k}\Omega$ ,  $100 \text{ k}\Omega$ ,  $400 \text{ V/V}$ ;  $I = 1 \text{ mA}$ :  $40 \text{ mA/V}$ ,  $2.5 \text{ k}\Omega$ ,  $10 \text{ k}\Omega$ ,  $400 \text{ V/V}$
- 8.27**  $50 \text{ V/V}$ ;  $0.2 \text{ mA}$ ;  $12.5 \mu\text{m}$
- 8.29**  $0.4 \mu\text{m}$ ;  $25$ ;  $0.2 \text{ mA}$
- 8.31**  $0.5 \text{ mA}$ ;  $4 \text{ mA/V}$
- 8.33**  $1 \text{ mA/V}$ ;  $15 \text{ k}\Omega$ ;  $15 \text{ V/V}$ ;  $3.9 \mu\text{m}$
- 8.35**  $0.144 \text{ mA}$
- 8.37** (a)  $80 \mu\text{A/V}$ ,  $0.18 \text{ M}\Omega$ ,  $14.4 \text{ V/V}$ ; (b)  $0.79 \text{ V}$ ,  $0.253 \text{ mA/V}$ ,  $18 \text{ k}\Omega$ ,  $4.55 \text{ V/V}$ ; (c)  $0.8 \text{ mA/V}$ ,  $18 \text{ k}\Omega$ ,  $14.4 \text{ V}$ ; (d)  $0.08 \text{ V}$ ,  $0.253 \text{ mA/V}$ ,  $180 \text{ k}\Omega$ ,  $45.5 \text{ V/V}$ ; (e) lowest  $A_0$ : first design when operated at  $I_D = 100 \mu\text{A}$ ,  $A_0 = 4.55 \text{ V/V}$ , highest  $A_0$ : second design when operated at  $I_D = 10 \mu\text{A}$ ,  $A_0 = 45.5 \text{ V/V}$ ; gain increases by a factor 10.
- 8.39**  $0.5 \mu\text{m}$ ;  $12.5$
- 8.41**  $1.05 \text{ V}$ ;  $2 \mu\text{m}$ ;  $8$ ;  $32$
- 8.43** (a)  $0.95 \text{ V}$ ,  $0.475 \mu\text{A}$ ,  $2.375 \text{ V}$ ; (b)  $-86.5 \text{ V/V}$ ,  $1.9 \text{ V}$ ,  $22 \text{ mV}$ ; (c)  $33.7 \text{ k}\Omega$
- 8.45**  $0.913 \text{ V}$ ;  $1.07 \text{ V}$
- 8.47** (a)  $25 \mu\text{A}$ ; (b)  $0.33 \text{ V}$  and  $2.98 \text{ V}$ ; (c)  $-189.3 \text{ V/V}$ ; (d)  $-195.8 \text{ V/V}$ ; (e)  $-210.6 \text{ V/V}$
- 8.49** (a)  $0.25 \text{ mA}$ ; (b)  $120 \text{ k}\Omega$ ,  $120 \text{ k}\Omega$ ,  $60 \text{ k}\Omega$ ; (c)  $5 \text{ k}\Omega$ ,  $10 \text{ mA/V}$ ; (d)  $5 \text{ k}\Omega$ ,  $-600 \text{ V/V}$ ,  $60 \text{ k}\Omega$
- 8.51**  $980 \Omega$ ;  $61 \text{ k}\Omega$ ;  $10.1 \text{ V/V}$
- 8.53**  $2 \text{ k}\Omega$ ;  $1.1 \text{ V}$
- 8.55** (a)  $100 \mu\text{A}$ ,  $1.03 \text{ V}$ ; (b)  $0.9 \text{ mA/V}$ ,  $200 \text{ k}\Omega$ ; (c)  $2.2 \text{ k}\Omega$ ; (d)  $209 \text{ k}\Omega$ ; (e)  $90.9 \text{ V/V}$ ,  $89 \text{ V/V}$ ; (f)  $32 \text{ mV}$
- 8.57**  $r_o$
- 8.59**  $0.99$  (or more exactly,  $0.975$ );  $14.8 \text{ M}\Omega$
- 8.61** (a)  $208 \Omega$ ; (b)  $500 \Omega$ ; (c)  $4.8 \text{ k}\Omega$ ;  $101$  with  $R_e = \infty$
- 8.63** (a)  $50$ ,  $1.6 \text{ M}\Omega$ ; (b)  $250$ ,  $320 \text{ k}\Omega$
- 8.65**  $0.5 \mu\text{m}$ ;  $20$ ;  $1 \text{ V}$ ;  $0.25 \text{ mA}$ ;  $0.5 \text{ V}$
- 8.67**  $0.6 \mu\text{m}$ ;  $0.125 \text{ mA}$ ;  $(W/L)_{1,2} = 10$ ;  $(W/L)_{3,4} = 40$
- 8.69**  $g_{m2}r_{o2}$

- 8.71** 0.2 V; 0.5 V to 0.8 V
- 8.74** 1.2 V; 1.0 V; 0.8 V; 100;  $6.91 \text{ M}\Omega$
- 8.76**  $1 \text{ M}\Omega$
- 8.79**  $-10^5 \text{ V/V}$
- 8.81** (a)  $1.41 \text{ mA/V}$ ,  $822.3 \text{ k}\Omega$ ,  $-1159 \text{ V/V}$ ; (b)  $1.41 \text{ mA/V}$ ,  $457 \text{ k}\Omega$ ,  $-644 \text{ V/V}$
- 8.83**  $(g_{m3}r_{o3})(g_{m2}r_{o2})r_{o1}$
- 8.85** (a)  $I_{O1} = I_{O2} = \frac{1}{2}I_{\text{REF}}/(1 + 2/\beta^2)$ ; (b) Use  $I_{\text{REF}} = 0.7 \text{ mA}$  and 3 transistors  $Q_3$ ,  $Q_4$  and  $Q_5$  whose EBJ areas are in the ratio 1:2:4; currents realized are  $0.0999 \text{ mA}$ ,  $0.1999 \text{ mA}$  and  $0.3997 \text{ mA}$ .
- 8.88** (a) 0.3 V, 0.8 V; (b)  $8 \mu\text{A}$ ,  $172 \mu\text{A}$ ; (c)  $180 \mu\text{A}$ ; (d) 1.1 V; (e)  $12 \text{ M}\Omega$ ; (f)  $0.08 \mu\text{A}$ , 0.04%
- 8.90** (a)  $R_E = 2.88 \text{ k}\Omega$ ; (b)  $8.2 \text{ M}\Omega$ ,  $0.7 \mu\text{A}$
- 8.92** (a)  $58.5 \text{ k}\Omega$ ; (b)  $79.9 \text{ M}\Omega$ ,
- 8.95**  $360 \mu\text{A}$ ;  $2.4 \text{ mA/V}$ ;  $0.48 \text{ mA/V}$ ;  $27.8 \text{ k}\Omega$ ;  $0.81 \text{ V/V}$ ;  $339 \Omega$ ;  $0.7 \text{ V/V}$
- 8.97** (b)  $g_{m1} = 0.632 \text{ mA/V}$ ,  $g_{m2} = 40 \text{ mA/V}$ ,  $r_{\pi2} = 5 \text{ k}\Omega$ ; (c)  $-19.5 \text{ V/V}$ ; (d)  $487 \text{ k}\Omega$ ,  $-9.6 \text{ V/V}$ ; (e)  $10 \text{ M}\Omega$ ,  $-18.6 \text{ V/V}$
- 8.99**  $50.2 \text{ V/V}$

## CHAPTER 9

- 9.1** (a) 0.2 V, 0.6 V; (b)  $-0.6 \text{ V}$ ,  $0.08 \text{ mA}$ ,  $0.08 \text{ mA}$ ,  $+0.6 \text{ V}$ ,  $+0.6 \text{ V}$ ; (c)  $-0.2 \text{ V}$ ,  $0.08 \text{ mA}$ ,  $0.08 \text{ mA}$ ,  $+0.6 \text{ V}$ ,  $+0.6 \text{ V}$ ; (d)  $-0.7 \text{ V}$ ,  $0.08 \text{ mA}$ ,  $0.08 \text{ mA}$ ,  $+0.6 \text{ V}$ ,  $+0.6 \text{ V}$ ; (e)  $1.0 \text{ V}$ ; (f)  $-0.8 \text{ V}$ ,  $-0.2 \text{ V}$
- 9.3** (a) 0 V,  $-0.6 \text{ V}$ ,  $0.6 \text{ V}$ ,  $0.6 \text{ V}$ , 0 V; (b)  $0.104 \text{ V}$ ,  $-0.541 \text{ V}$ ,  $0.4 \text{ V}$ ,  $0.8 \text{ V}$ ,  $0.4 \text{ V}$ ; (c)  $0.283 \text{ V}$ ,  $-0.4 \text{ V}$ ,  $+0.2 \text{ V}$ ,  $1 \text{ V}$ ,  $0.8 \text{ V}$ ; (d)  $-0.104 \text{ V}$ ,  $-0.645 \text{ V}$ ,  $+0.8 \text{ V}$ ,  $+0.4 \text{ V}$ ,  $-0.4 \text{ V}$ ; (e)  $-0.283 \text{ V}$ ,  $-0.683 \text{ V}$ ,  $+1 \text{ V}$ ,  $+0.2 \text{ V}$ ,  $-0.8 \text{ V}$
- 9.5**  $0.587 \text{ V}$ ;  $-0.587 \text{ V}$ ;  $0.612 \text{ V}$ ;  $0.025 \text{ V}$ ;  $0.10 \text{ V}$ ,  $4 \text{ V/V}$ ;  $-0.025 \text{ V}$
- 9.7**  $0.35 \text{ V}$ ;  $16.3$ ;  $1.14 \text{ mA/V}$
- 9.9**  $0.212 \text{ V}$ ;  $554.5 \mu\text{A}$
- 9.11** (a)  $0.1 V_{OV}$ ; (b)  $0$ ,  $0.338 V_{OV}$ ,  $0.05 V_{OV}$ ,  $0.005 V_{OV}$ ,  $1.072 V_{OV}$
- 9.13**  $0.25 \text{ V}$ ;  $0.5 \text{ mA}$ ;  $5 \text{ k}\Omega$ ;  $40$
- 9.15**  $0.5 \text{ mA}$ ;  $3.6 \text{ k}\Omega$ ;  $38.6$
- 9.17**  $I = 2I_D$ ;  $P_{\text{diff}} = 2P_{\text{CS}}$
- 9.19** (a)  $g_{m1,2} \left[ \frac{1}{g_{m3,4}} \| r_{o3,4} \| r_{o1,2} \right]$ ; (b)  $\sqrt{[\mu_n(W/L)_{1,2}]/[\mu_p(W/L)_{3,4}]}$ ; (c) 25

- 9.23**  $8 \text{ k}\Omega$ ;  $W/L, I_D$  (mA) and  $|V_{GS}|$  (V) are:  $Q_1(50, 0.1, 0.7)$ ,  $Q_2(50, 0.1, 0.7)$ ,  $Q_3(100, 0.2, 0.7)$ ,  $Q_4(20, 0.1, 0.7)$ ,  $Q_5(20, 0.1, 0.7)$ ,  $Q_6(100, 0.2, 0.7)$ ,  $Q_7(40, 0.2, 0.7)$
- 9.25**  $0.632 \mu\text{m}$ ;  $0.28 \text{ mA}$
- 9.27**  $v_{B1} = +0.5 \text{ V}$ :  $-0.177 \text{ V}$ ,  $+0.52 \text{ V}$ ,  $2.5 \text{ V}$ ;  $v_{B1} = -0.5 \text{ V}$ :  $-0.677 \text{ V}$ ,  $+2.5 \text{ V}$ ,  $+0.52 \text{ V}$
- 9.30** (a)  $-0.574 \text{ V}$ ,  $0.4 \text{ V}$ ,  $0.4 \text{ V}$ ; (b)  $-0.326 \text{ V}$  to  $0.674 \text{ V}$ ; (c)  $5 \text{ mV}$
- 9.32** (a)  $V_{CC} - (I/2)R_C$ ; (b)  $2 \text{ V}$ ; (c)  $0.4 \text{ mA}$ ,  $5 \text{ k}\Omega$
- 9.34**  $R_C = 5.05 \text{ k}\Omega$ ,  $+1.6 \text{ V}$
- 9.36**  $0.5 \text{ mA}$ ,  $1.0 \text{ mA}$ ;  $17.3 \text{ mV}$
- 9.38**  $8 \text{ mA/V}$ ;  $40 \text{ k}\Omega$
- 9.40**  $5 \text{ mV}$ ;  $250 \text{ }\Omega$ ;  $-40 \text{ V/V}$ ;  $200 \text{ mV}$ ;  $400 \text{ mV}$
- 9.42** Each emitter has a resistance  $R_e = 450 \text{ }\Omega$ ,  $R_C = 10 \text{ k}\Omega$ ;  $I = 1 \text{ mA}$ ; Possible value of  $V_{CC} = 10 \text{ V}$
- 9.49**  $12 \text{ V/V}$
- 9.51**  $16 \text{ V/V}$
- 9.53**  $25 \text{ V/V}$ ;  $101 \text{ k}\Omega$
- 9.55**  $7.7 \text{ V/V}$ ;  $5 \times 10^{-4} \text{ V/V}$ ;  $1.54 \times 10^4$  or  $83.8 \text{ dB}$
- 9.57** (a)  $2.332 \text{ V}$ ; (b)  $5.06 \text{ k}\Omega$ ; (c)  $2.47 \text{ V}$ ; (d)  $-1.92 \text{ V/V}$ ; (e)  $0.287 \text{ V}$
- 9.59**  $4 \mu\text{m}$
- 9.61** (a)  $20 \text{ V/V}$ ; (b)  $0.23 \text{ V/V}$ ; (c)  $86.5$  or  $38.7 \text{ dB}$ ; (d)  $-0.023 \sin 2\pi \times 60t + 0.2 \sin 2\pi \times 1000t$ , volts
- 9.63** (a)  $100 \text{ V/V}$ ; (b)  $50 \text{ k}\Omega$ ; (c)  $2.5 \times 10^{-4} \text{ V/V}$ ; (d)  $4 \times 10^5$  or  $112 \text{ dB}$ ; (e)  $25 \text{ M}\Omega$
- 9.65** (a)  $50 \text{ V/V}$ ; (b)  $2.5 \times 10^{-3} \text{ V/V}$ ,  $2 \times 10^4$  or  $86 \text{ dB}$ ; (c)  $5 \times 10^{-5} \text{ V/V}$ ,  $10^6$  or  $120 \text{ dB}$
- 9.67** (a) Two emitter resistances and a single bias-current source  $I$ ;  $R_e = 25 \text{ }\Omega$ ;  $R_C = 10 \text{ k}\Omega$ ;  $V_{CC} = +15 \text{ V}$ ;  $R_{EE} = 50 \text{ k}\Omega$ ;  $V_A = 100 \text{ V}$ ;  $2.4 \text{ M}\Omega$
- 9.69**  $2/3$  in one transistor and  $1/3$  in the other;  $0.008 \text{ V/V}$
- 9.72**  $11 \text{ mV}$ ; variability of  $V_t$ ;  $7.33\%$
- 9.74**  $2.5 \text{ mV}$
- 9.77**  $-0.25 \text{ mV}$
- 9.79**  $1.25 \text{ mV}$
- 9.81** (a)  $x = 0.3 \text{ k}\Omega$ ; (b)  $x = 0.225 \text{ k}\Omega$
- 9.83**  $2\alpha I/3$  and  $\alpha I/3$ ;  $\alpha I R_C/3$ ;  $18.75 \text{ mV}$ ;  $17.3 \text{ mV}$
- 9.85**  $20 \text{ k}\Omega$ ;  $40 \text{ V/V}$
- 9.87**  $1.4 \text{ mA/V}$ ;  $25 \text{ k}\Omega$ ;  $25 \text{ k}\Omega$ ;  $17.5 \text{ V/V}$

**9.89** 3 V**9.92** 1 mA/V; 75 k $\Omega$ ; 75 V/V; 75 k $\Omega$ **9.94** 20 k $\Omega$ ; 20 k $\Omega$ ; 10 mA/V; 200 V/V; 100 V/V**9.96**  $-2V_T/\beta_P^2$ ;  $-20 \mu\text{V}$ **9.98**  $2.67 \times 10^4$  V/V**9.100**  $\frac{I/2}{\beta+1} / \left( \frac{\beta}{2} \right)$ , a reduction by a factor of  $(\beta/2)$ ;  $R_{id}$  increases by a factor  $(\beta/3)$ **9.102** 1.13 mA/V; 75 k $\Omega$ ; 85 V/V**9.105** 1 mA/V; 25 k $\Omega$ ; 25 V/V; 25 k $\Omega$ , 0.02 mA/V; 0.98 k $\Omega$ ; 0.98 A/A; 50 k $\Omega$ ; 2600 k $\Omega$ ;  $-0.0196$  V/V; 1274 or 62.1 dB**9.107** 0.1**9.110** 8 mA/V; 100 k $\Omega$ ; 800 V/V; 37.5 k $\Omega$ ; 100 k $\Omega$ ;  $-0.013$  V/V; 60,000 or 96 dB; 444.4 V/V**9.112** (a) 83.3 k $\Omega$ ; (b) 1200 V/V; (c)  $21 \times 10^6$  or 146 dB**9.114** (a)  $W/L$ : 12.5, 12.5, 50, 50, 25, 100, 25, 25, 0 V; (b)  $-0.1$  V to  $+0.7$  V; (c)  $-0.7$  V to  $+0.7$  V; (d) 900 V/V**9.116** 108  $\mu\text{A}$ ; 909 mV; 0.86 mV**9.118** (a)  $W/L$ : 32.9, 32.9, 178, 178, 65.8, 356, 65.8, 32.9; (b) 0.65 V to 1.05 V; (c) 0.15 V to 1.05 V; 144 V/V**9.120** 25 V/V; 20 k $\Omega$ ; 5000 A/A**9.122**  $R_s$ ; 7.37 k $\Omega$ ; reduced to about half its original value; change  $R_4$  to 1.085 k $\Omega$ , this will slightly reduce  $A_2$ .**9.124** (a) 0.52 mA, 1.04 mA, 2.1 mA, 0 V; (b) 4 k $\Omega$ , 65.5  $\Omega$ ; (e) 8770 V/V

## CHAPTER 10

**10.1** 20 nf**10.3** 10  $\mu\text{F}$ ; 88.4 Hz; 8.84 Hz**10.5** (a) 10 k $\Omega$ ; (b) 3.53  $\mu\text{F}$ ; (c) 10 Hz; (d) 100 Hz; (e) dc gain = 2, makes perfect sense since  $C_s$  behaves as an open-circuit at dc.**10.7** 5  $\mu\text{F}$ ; 0.5  $\mu\text{F}$ ; 0.5  $\mu\text{F}$ ; 92.2 Hz; 6  $\mu\text{F}$ **10.10** 141.4**10.13**  $g_m = 1.3$  mA/V;  $g_{mb} = 0.25$  mA/V;  $r_o = 100$  k $\Omega$ ;  $C_{gs} = 61.6$  fF;  $C_{gd} = 4.3$  fF;  $C_{sb} = 12.8$  fF;  $C_{db} = 9.4$  fF;  $f_T = 3.1$  GHz**10.17**  $L = L_{\min}$ : 6.5 V/V, 113 GHz;  $2L_{\min}$ : 13 V/V, 28.3 GHz;  $3L_{\min}$ : 19.5 V/V, 12.6 GHz;  $4L_{\min}$ : 26 V/V, 7.1 GHz;  $5L_{\min}$ : 32.5 V/V, 4.5 GHz

- 10.19** 265.3 MHz
- 10.21** 500 MHz; 600 MHz; 252 ps; 0.43 pF
- 10.23** 50 MHz; 10 MHz
- 10.25** 5 pF;  $< 31.8 \text{ k}\Omega$
- 10.28** 200.2 pF;  $-1000/[1 + sC_{\text{in}}R_{\text{sig}}]$ ; 795 kHz; 795 MHz
- 10.31** 870 kHz;  $-6.1 \text{ V/V}$ ;  $R_{\text{in}} = 33.3 \text{ k}\Omega \rightarrow 3.1 \text{ V/V}$ ;  $R_L = 1.24 \text{ k}\Omega \rightarrow 1.6 \text{ V/V}$
- 10.33**  $-9.2 \text{ V/V}$ ; 525 kHz
- 10.35** 61 pF; 522 kHz
- 10.37**  $-33 \text{ V/V}$ ; 873 kHz; 28.8 MHz;  $f_H$  increases by a factor of 1.16 and voltage gain decreases by the same factor while GB remains nearly constant. Power dissipation increases by a factor of 2.
- 10.39**  $-32.8 \text{ V/V}$ ; 572 kHz
- 10.41** (a) 1001 pF, 1.001 pF; (c) 20 pF, 20 pF; (e)  $-90 \text{ pF}$ , 9 pF; +90 pF
- 10.44** (a) 0.54 mA; (b) 21.6, A/V, 4.63 k $\Omega$ ; (c)  $-10.8 \text{ V/V}$ ; (d) 4 k $\Omega$ , 2.14 k $\Omega$ ; (e)  $-7.4 \text{ V/V}$ ; (f) 14.37 pF; (g) 16.3 MHz
- 10.46**  $-80 \text{ V/V}$ ; 3.8 MHz; 6.4 GHz; 304 MHz
- 10.48**  $-81.4 \text{ V/V}$ ; 21.4 MHz; 11.2 GHz
- 10.50** (a) 99.2 MHz; (b) 227.6 MHz
- 10.53** (a) 4.26; (b) 49.3
- 10.55**  $5.67 \times 10^7 \text{ rad/s}$
- 10.57**  $-40.6 \text{ V/V}$ ;  $\tau_{gs} = 243.8 \text{ ns}$ ;  $\tau_{gd} = 3112.8 \text{ ns}$ ;  $\tau_{CL} = 300 \text{ ns}$ ; 43.5 MHz
- 10.59**  $-80 \text{ V/V}$ ; 10.1 pF; 788 kHz; 652 kHz; the latter as it takes into account  $C_L$ .
- 10.61** 41.6 fF
- 10.63**  $-138.9 \text{ V/V}$ ; 2.98 MHz; 2.28 MHz, the latter as it takes into account  $C_L$ .
- 10.66** 8.3 V/V; 239 MHz; 7.23 MHz; 7.23 MHz
- 10.69** 11.1 fF
- 10.71**  $-913 \text{ V/V}$ ; 6.28 MHz
- 10.73** 0.2 V; 0.2 mA; 289.4 MHz; 57.9 kHz,  $-100 \text{ V/V}$  (40 dB)
- 10.76**  $-26.5 \text{ V/V}$ ; 5.7 MHz
- 10.78**  $-100,000 \text{ V/V}$ ; 31.8 kHz, 31.8 kHz; 3.18 GHz
- 10.79** 0.91 V/V;  $200 \Omega$ ; 398 MHz; 33.4 MHz, 90.7 MHz; 31.6 MHz
- 10.82**  $0.8/[s^2 + 8.886 \times 10^6 \text{ s} + 39.48 \times 10^{12}]$
- 10.84** 0.96 V/V; 2 GHz; 676 MHz, 4.6 GHz; 676 MHz
- 10.86** 1.59 MHz

- 10.88** 4 MHz; decreases by a factor of 4 to 1 MHz
- 10.90** (b)  $-49.8 \text{ V/V}$ ; (c)  $53.2 \text{ pF}$ ,  $598 \text{ kHz}$ ,  $29.8 \text{ MHz}$
- 10.92**  $50 \text{ V/V}$ ;  $15.9 \text{ MHz}$ ;  $1.59 \text{ GHz}$ ;  $3.18 \text{ GHz}$
- 10.96** (a)  $-100 \text{ V/V}$ ,  $603 \text{ kHz}$ ,  $60.3 \text{ MHz}$ ; (b)  $-50 \text{ V/V}$ ,  $1.02 \text{ MHz}$ ,  $51.2 \text{ MHz}$
- 10.101** (a)  $2.5 \text{ M}\Omega$ ,  $-4000 \text{ V/V}$ ; (b)  $107.6 \text{ kHz}$ ; two dominant capacitances:  $C_L$  (most significant) and  $C_{\mu 2}$
- 10.103**  $66.7 \text{ V/V}$ ;  $2 \text{ MHz}$
- 10.106** (a)  $10,000 \text{ V/V}$ ; (b)  $11.1 \text{ MHz}$

## CHAPTER 11

- 11.1**  $4.9 \times 10^{-3}$ ;  $169.5$ ;  $-15.3\%$
- 11.3**  $1$ ;  $0.999 \text{ V/V}$ ;  $60 \text{ dB}$ ;  $0.999 \text{ V}$ ,  $0.001 \text{ V}$ ;  $-0.011\%$
- 11.5** (b) (i)  $1000$ ; (ii)  $100$ ; (iii)  $20$
- 11.7**  $2500 \text{ V/V}$ ;  $0.0196 \text{ V/V}$ ;  $49$ ;  $50 \text{ V/V}$ ;  $34 \text{ dB}$
- 11.10**  $99$ ;  $4$
- 11.12**  $1000 \text{ V/V}$ ;  $0.099 \text{ V/V}$
- 11.14**  $416.6 \text{ V/V}$ ;  $9.33 \times 10^{-3} \text{ V/V}$ ;  $5016.8 \text{ V/V}$ ,  $9.95 \times 10^{-3} \text{ V/V}$ ;  $41.66 \text{ V/V}$ ,  $9.33 \times 10^{-2} \text{ V/V}$ ;  $501.68 \text{ V/V}$ ,  $9.95 \times 10^{-2} \text{ V/V}$
- 11.16**  $500 \text{ V/V}$ ;  $0.098 \text{ V/V}$ ;  $653.4 \text{ V/V}$
- 11.19**  $1 \text{ MHz}$ ,  $1 \text{ Hz}$
- 11.21** Three stages; each with a closed-loop gain of  $10 \text{ V/V}$ , an amount of feedback of  $100$ , and  $\beta = 0.099 \text{ V/V}$ .
- 11.23**  $50 \text{ V/V}$ ;  $0.008 \text{ V/V}$ ;  $16 \text{ Hz}$
- 11.25**  $0.089$ ; for  $|v_s| \leq 0.9 \text{ V}$ ,  $v_o/v_s = 11.1 \text{ V/V}$ , for  $0.9 \text{ V} \leq |v_s| \leq 1.4 \text{ V}$ ,  $v_o/v_s = 10.1 \text{ V/V}$ , and for  $|v_s| \geq 1.4 \text{ V}$ ,  $v_o = \pm 15 \text{ V}$
- 11.27** (a)  $90 \text{ k}\Omega$ ; (b)  $43.11$ ,  $9.77 \text{ V/V}$ ; (c)  $2.343$
- 11.29** (a)  $1 + \frac{R_2}{R_1} = 11 \text{ V/V}$ ; (b)  $0.1 \text{ mA}$ ,  $0.3 \text{ mA}$ ,  $+7.7 \text{ V}$ ; (c)  $23.2$ ; (d)  $10.5 \text{ V/V}$
- 11.31** (a)  $0.9 \text{ k}\Omega$ ; (b)  $31.33$ ,  $9.7 \text{ V/V}$ ,  $-3\%$ , change  $R_F$  to  $933 \Omega$
- 11.33** (a)  $47.62 \beta$ ,  $47.62 \text{ V/V}$ ; (b)  $821 \text{ k}\Omega$ ,  $179 \text{ k}\Omega$
- 11.35** Lower;  $199$ ;  $20 \text{ k}\Omega$
- 11.37**  $100 \text{ V/V}$ ;  $1.001 \text{ M}\Omega$
- 11.39** (a)  $1 + (R_2/R_1) = 11 \text{ V/V}$ ; (b)  $0.1 \text{ mA}$ ,  $0.3 \text{ mA}$ ,  $+7.7 \text{ V}$ ; (c)  $255.3 \text{ V/V}$ ,  $0.359 \text{ k}\Omega$ ,  $0.917 \text{ k}\Omega$ ; (d)  $1/11$ ; (e)  $10.5 \text{ V/V}$ ,  $8.59 \text{ k}\Omega$ ,  $39.4 \Omega$ ,  $4.5\%$

11.41 (b) 10 V/V; (c) 0.2 V, 1.1 V, 0.2 V, 0.9 V; (d)  $-35.3 \text{ V/V}$ ,  $-50 \text{ V/V}$ ,  $0.935 \text{ V/V}$ ,  $1650 \text{ V/V}$ ; (e) 0.1 V/V; (f)  $9.94 \text{ V/V}$ ,  $-0.6\%$ ; (g)  $5.6 \Omega$

11.44 (c)  $1.2 \text{ k}\Omega$ ; (d)  $1.42 \text{ k}\Omega$ ,  $628 \Omega$ ; (e)  $23.8 \text{ V/V}$ ; (f)  $145 \text{ k}\Omega$ ,  $0.53 \Omega$

11.46  $100 \Omega$ ;  $9.94 \text{ mA/V}$

11.48 (c)  $-0.999 \text{ k}\Omega$

11.50 (a)  $0.135 \text{ V/V}$ ; (b)  $7.4 \text{ V/V}$ ; (c)  $0.14 \Omega$

11.53 (a)  $200 \Omega$ ; (b)  $1418.4 \text{ mA/V}$ ; (c)  $283.7$ ,  $284.7$ ; (d)  $4.982 \text{ mA/V}$ , very close; (e)  $28.2 \text{ k}\Omega$ ,  $8 \text{ M}\Omega$

11.56  $9.56 \text{ mA/V}$ ;  $503.4 \text{ k}\Omega$

11.58 (a)  $0 \text{ V}$ ,  $+0.6 \text{ V}$ ,  $+0.6 \text{ V}$ ; (b)  $0.1 \text{ mA/V}$ ; (c)  $0.099 \text{ mA/V}$ ; (d)  $203 \text{ M}\Omega$ ; (e)  $0.99 \text{ V/V}$ ;  $1.25 \Omega$

11.60  $-9.88 \text{ k}\Omega$ ,  $11.1 \Omega$ ,  $1.1 \Omega$  compared to  $-9.99 \text{ k}\Omega$ ,  $1.11 \Omega$ ,  $0.11 \Omega$ .

11.62 3.23;  $-0.1 \text{ mA/V}$ ;  $-32.3 \text{ k}\Omega$ ;  $-7.63 \text{ k}\Omega$ ; due to the approximation used in the systematic analysis method.

11.64 (a)  $-R_F/R_s$ ,  $20 \text{ k}\Omega$ ; (b)  $-9.88 \text{ V/V}$ ,  $21.7 \Omega$ ,  $22.1 \Omega$ ; (c)  $82.18 \text{ kHz}$

11.66 159, larger by about 2.5%, a result of the approximations involved in the general method. The more accurate value is the one obtained here.

11.68  $10 \text{ k}\Omega$ ;  $-9.52 \text{ k}\Omega$ ;  $11.9 \Omega$ ;  $244 \Omega$

11.70 (b)  $-98.8 \text{ V/V}$ ;  $7.2 \Omega$ ;  $10.3 \Omega$

11.72  $0.53 \text{ k}\Omega$ ;  $10.5 \Omega$ ;  $526 \Omega$

11.74 (d)  $-99.8 \text{ A/A}$ ,  $-0.1 \text{ A/A}$ ,  $9.98$ ,  $-9.1 \text{ A/A}$ ,  $0.2 \text{ k}\Omega$ ,  $18.2 \Omega$ ; (e)  $328.4 \text{ k}\Omega$

11.76 970.9,  $-9709 \text{ A/A}$ ,  $-9.99 \text{ A/A}$ ;  $A\beta$  and  $A$  differ slightly from the results in Example 11.10; however,  $A_f$  is identical.

11.81  $I_{C1} = 0.1 \text{ mA}$ ,  $I_{C2} = 10 \text{ mA}$ ;  $V_o/V_s = 3.62 \text{ V/V}$ ;  $R_{in} = 176.7 \Omega$

11.83  $20 \text{ krad/s}$ ;  $4 \times 10^{-3} \text{ V/V}$ ;  $250 \text{ V/V}$

11.85  $8 \times 10^{-4}$

11.87  $10 \text{ V/V}$ ;  $10^5 \text{ Hz}$ ;  $1 \text{ MHz}$ ; by the amount-of-feedback  $\simeq 10^4$ .

11.89 (a)  $2.025 \times 10^{-4}$ ,  $5.5 \times 10^4 \text{ Hz}$ ; (b)  $3306 \text{ V/V}$ ,  $1653 \text{ V/V}$ ; (c) 0.5; (d)  $(-5.5 \pm j 13.25) \times 10^4 \text{ Hz}$ ,  $1.325$

11.91 0.1; 0.686; 2.1

11.93 2;  $173.2 \text{ kHz}$

11.95  $3.085 \times 10^3 \text{ Hz}$ ;  $18.15^\circ$ ;  $10^{-3}$

11.97  $3.16 \times 10^{-4}$ ;  $2.4 \times 10^3 \text{ V/V}$  or  $67.6 \text{ dB}$ .

11.99  $2.4 \times 10^4 \text{ V/V}$  or  $87.6 \text{ dB}$ ;  $9.09 \times 10^3 \text{ V/V}$  or  $79.2 \text{ dB}$ .

11.101 2 kHz; 500

**11.104** 10 Hz; 15.9 nF

**11.106** (b)  $3.16 \times 10^4$  Hz,  $1.8^\circ$ ; (c) zero:  $-10^3$  rad/s, poles:  $(-0.505 \pm j 31.62) \times 10^3$  rad/s, the response is very peaky with a peak of 1000 at 31.62 krad/s.

## CHAPTER 12

**12.1**  $-9.3$  V to  $+9.7$  V;  $-8.6$  V to  $+10.4$  V;  $-4.65$  V to  $+9.7$  V;  $-3.95$  V to  $+10.4$  V;  
 $-9.7$  V to  $+9.7$  V;  $-9$  V to  $+10.4$  V

**12.3**  $2.7$  k $\Omega$ ;  $24$  mW

**12.6**  $V_{CC}I$  (in all cases)

**12.8**  $\hat{V}$ ;  $\hat{V}/R_L$ ;  $25\%$

**12.11**  $4.5$  V;  $6.4\%$ ;  $625$   $\Omega$

**12.13**  $10$  V;  $6.37$  V;  $6.85$   $\Omega$ ,  $7.3$  W;  $9.62$   $\Omega$ ,  $1.3$  W

**12.17**  $1.266$  V;  $12.5$   $\Omega$ ;  $0.889$  V/V;  $0.998$  V/V

**12.19**  $2.15$  mA

**12.22**  $1$  mA;  $-1.06$  V;  $+4$  V;  $-6$  V

**12.24**  $0.98$  mA;  $+5.1$  V;  $-10$  V;  $99$ ;  $1.96$  mA;  $1.92$  mA

**12.28**  $20.7$  mA;  $788$  mW;  $7.9^\circ\text{C}$ ;  $I_Q$  becomes  $37.6$  mA, etc., etc.

**12.30** (a)  $1.365$  k $\Omega$ ,  $1.365$  k $\Omega$ ,  $1.365$  V; (b)  $1.420$ ; (c)  $1.512$  V; (d)  $1.641$  V

**12.32** (a) For  $R_L = \infty$ : at  $v_l = 0$ ,  $I_1 = 0$ ; at  $v_l = +10$  V,  $I_1 = 20$   $\mu$ A, at  $v_l = -10$  V,  $I_1 = -20$   $\mu$ A; (b)  $R_L = 100$   $\Omega$ ; at  $v_l = 0$ ,  $I_1 = 0$ , at  $v_l = +10$  V,  $I_1 = 22.5$   $\mu$ A, at  $v_l = -10$  V,  $I_1 = -22.5$   $\mu$ A.

**12.34**  $215$   $\Omega$ ,  $215$   $\Omega$ ,  $0.75$   $\Omega$ ,  $0.75$   $\Omega$ ;  $0.7$   $\Omega$ ;  $0.704$  V

**12.37** (a)  $0.0164$  mA,  $1.64$  mA; (b)  $32.8$   $v_i$ ,  $-66.2$  V/V; (c)  $27.2$  k $\Omega$

**12.39**  $R_1 = 300$  k $\Omega$ ,  $R_2 = 632$  k $\Omega$ ;  $9.484$  V and  $-10.644$  V

**12.41**  $3.84$   $\Omega$ ;  $384$  mV;  $0.94$   $\mu$ A

**12.43**  $6.5$   $\Omega$ ;  $487.5$  mV;  $2.9$   $\mu$ A

**12.45** (b)  $1.25$  V,  $1.56$  mA

**12.47** (a)  $Q_1 : 35.6$ ,  $Q_2 : 88.9$ ,  $Q_N : 356$ ,  $Q_P : 889$ ; (b)  $-0.6$  V; (c)  $1.38$  V

**12.49**  $\pm 2.05$  V

**12.51** (b)  $0.15$  V

**12.53** (a)  $533.3$ ,  $1333.3$ ; (b)  $10$  V/V; (c)  $-5\%$ ; (d)  $1.85$  V and  $-1.85$  V; (e)  $0.3$  V and  $-0.3$  V; (f)  $-1.77$  V to  $+1.77$  V

**12.55**  $R_2$  and  $R_3$ ;  $R_3$ ;  $R_2$ ;  $R_2 = 33.3$  k $\Omega$  and  $R_3 = 1.33$  k $\Omega$

- 12.57** 16 V; 2.7 W; 13 V  $p - p$
- 12.59** 30 k $\Omega$ , 40 k $\Omega$
- 12.62** +3 V; -3 V
- 12.64** (c) 8  $\Omega$ , 5 A, 50 W; (d) 6  $\Omega$ , 5 A, 37.5 W; (e) 3  $\Omega$ , 5 A, 18.75 W
- 12.66** 12.5°C/W; 8 W; 112.5°C
- 12.68** (a) 37.5°C/W; (b) 1.33 W; (c) 62.5°C
- 12.70** 72°C; 1.5°C/W; 4 cm

## CHAPTER 13

- 13.1** -0.8 V to +1.2 V; -0.8 V to +0.8 V
- 13.3** 0.15 V
- 13.5** 0.45  $\mu$ m; 2000 V/V
- 13.7** (a) 10,000 V/V; (b)  $10^8$  rad/s and  $10^7$  rad/s; (c)  $10^9$  rad/s, 4 pF,  $25 \times 10^3$  rad/s,  $5 \times 10^8$  rad/s
- 13.9** (a) 1.59 pF; (b)  $f_{P1} = f_t/A_0$ ,  $f_{P2} = 318$  MHz,  $f_Z = 200$  MHz; (c) 46°; (d)  $500 \Omega$ , 72.5°; (e) 722  $\Omega$
- 13.11** 125.6 V/ $\mu$ s; 0.8 pF
- 13.13** (a) 2 pF; (b) 1.51 pF
- 13.15** (a) 0.16 V; (b) 2 pF; (c) 78.1
- 13.17** (b) 0.45  $\mu$ m
- 13.19** 250  $\mu$ A; 400  $\mu$ A; 200  $\mu$ A; 50  $\mu$ A
- 13.21** 25, 25, 25, 25, 6.25, 6.25, 6.25, 6.25, 125, 125, 50
- 13.23** 100  $\mu$ A; 150  $\mu$ A; 15.92 MHz; 54.7°; 6.58 MHz;  $C_L = 24.2$  pF; 4.13 V/ $\mu$ s
- 13.25** 0.12 V;  $I_B = I = 150 \mu$ A; 15 V/ $\mu$ s;  $W/L : 26, 26, 65, 65, 26, 26, 26, 26, 130, 130, 52$
- 13.28** (a) -0.25 V to +1.3 V; (b) -1.3 V to +0.25 V; (c) -0.25 V to +0.25 V; (d) -1.3 V to +1.3 V
- 13.30**  $C_p = 0.176 C_L$
- 13.33**  $V_{EB} = 625$  mV; A device: 7.3 mA/V, 137  $\Omega$ , 6.85 k $\Omega$ , 278 k $\Omega$ ; B device: 21.9 mA/V, 46  $\Omega$ , 2.28 k $\Omega$ , 90.9 k $\Omega$
- 13.35**  $I_3 = I_1 \left\{ \left[ \frac{1}{\sqrt{k_1}} + \frac{1}{\sqrt{k_2}} \right] \middle/ \left[ \frac{1}{\sqrt{k_3}} + \frac{1}{\sqrt{k_4}} \right] \right\}^2 ; 0.1$  mA
- 13.37** 603 mV; 518 mV; 8.5 k $\Omega$
- 13.39** 4.75  $\mu$ A;  $R_4 = 1.94$  k $\Omega$

- 13.41**  $14 \mu\text{A}$
- 13.43**  $53.3 \text{ nA}; 20.1 \text{ nA}$
- 13.45**  $-3 \text{ V to } +4.8 \text{ V}$
- 13.47**  $6.4 \text{ k}\Omega; 270 \mu\text{A}$
- 13.49**  $1.68 \text{ mA}; 50.4 \text{ mW}$
- 13.51**  $4.63 \text{ k}\Omega$
- 13.53**  $10 \text{ mV}$
- 13.55**  $0.691 \mu\text{A}; 3.6 \text{ mV}$
- 13.57**  $R = 18.2 \text{ k}\Omega; 15.55 \text{ M}\Omega$
- 13.60**  $3.1 \text{ M}\Omega, 9.38 \text{ mA/V}$
- 13.62**  $-3.6 \text{ V to } +4.2 \text{ V}$
- 13.64**  $14.4 \Omega$
- 13.66**  $20.2 \text{ mA}; \text{double the value of } R_7$
- 13.68**  $5.67 \text{ MHz}$
- 13.70**  $180 \text{ Hz}; 0.7 \text{ pF}$
- 13.73**  $159.2 \text{ kHz}; 10^8 \text{ rad/s or } 15.9 \text{ MHz}$
- 13.75** (a)  $0.05 \text{ mA}, 0.05 \text{ mA}, 0.05 \text{ mA}, 0.05 \text{ mA}, 1 \text{ mA}, 1 \text{ mA}, 1 \text{ mA};$  (b)  $100 \text{ k}\Omega;$   
(c)  $5 \times 10^4 \text{ V/V or } 94 \text{ dB};$  (d)  $63.7 \text{ pF}$
- 13.77**  $Q_5: Q_1 = 1; Q_6: Q_1 = 4; 3.47 \text{ k}\Omega; 3 \text{ M}\Omega \text{ and } 7 \text{ M}\Omega$
- 13.79** (a)  $0.1 \text{ V to } 2.2 \text{ V};$  (b)  $0.8 \text{ V to } 2.9 \text{ V}$
- 13.81**  $12.5 \text{ k}\Omega; 0.8 \text{ V to } 3.35 \text{ V}; 100 \text{ k}\Omega; 10 \mu\text{A}, 50 \text{ k}\Omega$
- 13.83**  $36.9/I; 1240 \text{ V/V}; 1240(IR_L)/(IR_L + 36.9); 5.1 \mu\text{A}, 11.8 \mu\text{A}$
- 13.85** (a)  $0.1 \text{ V to } 2.9 \text{ V};$  (b)  $20 \text{ k}\Omega;$  (c)  $0.2 \Omega;$  (d)  $12.3 \text{ mA}, 0.3 \text{ mA}, 1.6 \text{ k}\Omega;$  (e)  $0.3 \text{ mA}, 12.3 \text{ mA}, 2.4 \text{ k}\Omega$
- 13.88**  $10.6 \mu\text{A}; 0.3 \text{ mA}$

## CHAPTER 14

- 14.1** (a)  $2.18 \text{ k}\Omega;$  (b)  $5.40 \text{ k}\Omega;$  (c)  $3.71$
- 14.2** (a)  $6;$  (b)  $1.67 \text{ k}\Omega$
- 14.16**  $0.6 \text{ V}; 0.7 \text{ V}$
- 14.18**  $NM_H = 0.2 V_{DD}; NM_L = 0.3 V_{DD}; 0.2 V_{DD}; 2 \text{ V}$
- 14.20** (a)  $0.12 \text{ V}, 2.5 \text{ V}, 1.5 \text{ V}, 0.68 \text{ V};$  (b)  $V_{OH} = 2.5 - 0.4N, NM_H = 1.5 - 0.4N, N = 2;$   
(c) (i)  $3 \text{ mW},$  (ii)  $1 \text{ mW}$

- 14.22**  $V_{IL} = 0.776$  V,  $V_{IH} = 0.816$  V;  $NM_H = 1.184$  V;  $NM_L = 0.776$  V;  $-50$  V/V
- 14.24**  $V_{DD} = 1.2$  V,  $R_D = 38.3$  k $\Omega$ ,  $W/L = 1.5$ ; 0 W, 36  $\mu$ W
- 14.26**  $V_{DD} = 1.2$  V,  $R_D = 23$  k $\Omega$ ,  $W/L = 2.5$ ; 0.435 V, 0.6 V, 0.7 V, 0.385 V, 0.5 V
- 14.29** 6.84
- 14.31** (a) 244 nm, 22,181 nm<sup>2</sup>; (b) 1 V, 0 V, 0.5375 V, 0.4625 V, 0.4625 V, 0.4625 V  
(c) both equal; 2.18 k $\Omega$
- 14.33** 1.82
- 14.35** 40.1
- 14.37** (a) 0.78  $\mu$ m, 0.127  $\mu$ m<sup>2</sup>; (b) 1.3 V, 0 V, 0.7125 V, 0.5875 V, 0.59 V, 0.59 V, 0.0625 V, 1.24 V, 0.53 V, 0.53 V; (c) 1.48 k $\Omega$ , 1.48 k $\Omega$ ; (d)  $-5.8$  V/V, 0.762 V, 0.538 V, 0.224 V; (e) 0.57 V,  $-0.08$  V, 60%; (f) 0.61 V,  $-0.04$  V, 40%
- 14.39** (a)  $v_o(t) = 10 e^{-t/\tau}$ ; (b) 69 ns, 220 ns
- 14.41** 69 ps, 35 ps, 52 ps
- 14.43** (a) 1.2 ns, 0.6 ns; (b) 1 pF; (c)  $C_{out} = 0.6$  pF,  $C_{load} = 0.4$  pF
- 14.45** 30 ps, 60 ps, 45 ps
- 14.47** 57.5 ps, 69 ps, 63.3 ps
- 14.49**  $(W/L)_n \geq 1.725$ ,  $(W/L)_p \geq 4.14$
- 14.51** 34.4 ps, 42.6 ps, 38.5 ps; 13 GHz
- 14.53** 36.3 ps, 36.3 ps, 36.3 ps; 9.35 fF
- 14.55** (c)  $14.66 \times 10^3 (2C_n + C_w)$ ; (d)  $8.625 \times 10^3 (3.4C_n + C_w)$  (e) (i) In both cases,  $t_p = 29.32 \times 10^3 C_n$ , thus when  $C$  is entirely intrinsic, scaling does not affect  $t_p$ ; (ii) For  $W_p = W_n$ ,  $t_p = 14.66 \times 10^3 C_w$ , and for  $W_p = 2.4W_n$ ,  $t_p = 8.625 \times 10^3 C_w$ , thus using a matched design reduces  $t_p$  only when  $C$  is dominated by external capacitance.
- 14.60** (a) 2.65 V; (b) 2.24 V
- 14.63** 32.4 fJ; 64.8 W; 36 A
- 14.65** 0.36 pF
- 14.67** 32 pJ
- 14.69** (a)  $t_p$  and the maximum operating frequency remain unchanged, PDP is reduced by a factor of 0.52; (b)  $t_p$  increases by a factor (1/0.72) and the maximum operating frequency is reduced by the factor of 0.72. The PDP decreases by a factor of 0.72.

## CHAPTER 15

- 15.1**  $4.88 \times 10^8$  or 488 million transistors
- 15.3** 260 cm<sup>2</sup>/Vs, 144.4 cm<sup>2</sup>/Vs;  $E_{cr}(\text{NMOS}) = 3.85 \times 10^4$  V/cm;  $E_{cr}(\text{PMOS}) = 6.92 \times 10^4$  V/cm

- 15.5** (b) 0.62
- 15.7** (b) 2.75
- 15.9** (a) 207 pA; (b) 207 mA, 207 mW
- 15.11** (a)  $270\ \Omega$ ; (b) 0.1 pF; (c) 93.2 ps
- 15.13** 1.3 V; 0.095 V;  $40.5\ \mu\text{A}$ ;  $52.7\ \mu\text{W}$
- 15.15** 167 ps; 36.9 ps; 102 ps
- 15.17** 2.1; 0.5 V; 0.5 V, 0.47 V, 0.44 V
- 15.19** 1.69; 0.58 V;  $152\ \mu\text{W}$
- 15.23** 1.26
- 15.26** 0.834 V
- 15.28** 25.8 ps
- 15.30** 2.07 V, 0 V;  $10.4\ \mu\text{A}$ ; 0.9 ns; 0.5 ns
- 15.34**  $13.5\ \mu\text{A}$ ;  $351.6\ \mu\text{A}$ ;  $182.6\ \mu\text{A}$ ; 0.18 ns
- 15.36** (a) 1.2 V, 0 V; (b)  $240\ \mu\text{A}$ ,  $60\ \mu\text{A}$ ,  $7.8\ \mu\text{A}$ ,  $56.25\ \mu\text{A}$ , 49.4 ps; (c)  $240\ \mu\text{A}$ ,  $60\ \mu\text{A}$ ,  $225\ \mu\text{A}$ ,  $1.9\ \mu\text{A}$ , 34.2 ps, 0.466 V; 41.8 ps
- 15.39**  $8.3\ \text{k}\Omega$ ; 83 ps
- 15.45** 0.188 ns
- 15.47** 0.188 ns; 0.077 ns
- 15.49** (d) 0.35 V, 0.6 V
- 15.51** 2 GHz
- 15.53**  $-1.453\ \text{V}$ ,  $-1.205\ \text{V}$ ,  $-1.73\ \text{V}$ ,  $-0.88\ \text{V}$ ;  $0.230\ \text{V}$ ,  $0.325\ \text{V}$ ,  $0.345\ \text{V}$
- 15.55** 22.45 mW
- 15.57** 1 V; +5 V;  $(A+B).(C+D)$
- 15.59** 2.6 V; 8.18 mA

## CHAPTER 16

- 16.1** A(0 V, 0 V), B(2.5 V, 2.5 V), C(5 V, 5 V); 25 V/V; 0.2 V
- 16.4**  $(W/L)_{1,3} = 0.13\ \mu\text{m}/0.13\ \mu\text{m}$ ,  $(W/L)_{2,4} = 0.52\ \mu\text{m}/0.13\ \mu\text{m}$ ,  $(W/L)_{5,8} = 0.26\ \mu\text{m}/0.13\ \mu\text{m}$
- 16.6**  $(W/L)_{5,6} = 3.83$ , higher than the values without velocity saturation to compensate for the current reduction resulting from velocity saturation.
- 16.7**  $0.4\ \mu\text{m}/0.13\ \mu\text{m}$ ; 65 ps
- 16.11** 4,294,967,296

**16.13** 16

**16.15** 57%

**16.17**  $(W/L)_a \leq 4.5$

**16.19** 4.5; (i) 0.23 V, 121.8  $\mu\text{A}$ ; (ii) 0.34 V, 158.7  $\mu\text{A}$ ; (iii) 0.4 V, 180  $\mu\text{A}$

**16.22** 1.75, greater than the value without velocity saturation because of the current reduction due to velocity saturation.

**16.24** (a) 3; (b) 4.93 ns; (c) 3.33 ns

**16.26** 3

**16.29**  $L = 0.13 \mu\text{m}$ ,  $(W/L)_n = (W/L)_p = (W/L)_a = 1$

**16.31** 128 Mbits

**16.33** 0.5 pA

**16.35** 0.4 mA/V; 353 mV; 130 mV; 100% (doubling); 4 ns

**16.37**  $(W/L)_n = 3.33$ ,  $(W/L)_p = 13.32$ ; 1.44 ns; 2 ns

**16.39** (a) 0.4 V; (b) 0.1 V, 0.3 V; (c) 132  $\mu\text{A}$ ; (d)  $(W/L)_{1,2} = 26.4$ ,  $(W/L)_{3,4} = 6.6$ ,  $(W/L)_5 = 52.8$

**16.41** 10; 1024; 10,240; 1024; 12,288

**16.43** 40 MHz, 48%

**16.45** 4

**16.48** (a) 2.4 ns; (b) 22 ns, 3.16 V; (c) 1.9 ns

## CHAPTER 17

**17.2** (a) 0.995 V,  $-5.7^\circ$ ; (b) 0.707 V,  $-45^\circ$ ; (c) 0.1 V,  $-84.3^\circ$ ; (d) 0.01 V,  $-89.4^\circ$

**17.4** 1 V/V; 0.977 V/V; 0.001 V/V

**17.6** 0.97 dB; 14.15 dB

**17.10** (a) LP:  $T(s) = 10^{20}/(s + 10^4)(s^2 + 0.618 \times 10^4 s + 10^8)(s^2 + 1.618 \times 10^4 s + 10^8)$   
 (b) HP:  $T(s) = s^5/(s + 10^4)(s^2 + 0.618 \times 10^4 s + 10^8)(s^2 + 1.618 \times 10^4 s + 10^8)$ ;

**17.12**  $T(s) = 0.2656(s^2 + 4)/(s^2 + 0.5s + 1.0625)$ ; 0.2656

**17.14**  $1/(s^3 + 2s^2 + 3s + 2)$ ;  $-1, -0.5 \pm j1.323$

**17.17** 35.7 dB

**17.19**  $N = 4$ ;  $2\pi \times 10^4(-0.383 \pm j0.924)$ ,  $2\pi \times 10^4 (-0.924 \pm j0.383)$ ;  $\omega_0^4/(s^2 + 0.765 \omega_0 s + \omega_0^2) \times (s^2 + 1.848 \omega_0 s + \omega_0^2)$  where  $\omega_0 = 2\pi \times 10^4 \text{ rad/s}$ ; 38.2 dB

**17.22** 0.975 rad/s, 0.782 rad/s, 0.434 rad/s, 0 rad/s; 1 rad/s, 0.901 rad/s, 0.623 rad/s, 0.223 rad/s;  $-64.9 \text{ dB}$ ; 42 dB/octave

**17.24** (a)  $N = 10$ , 4 dB; (b) Normalized to  $\omega_p = 2\pi \times 3.4 \times 10^4$  rad/s, the poles are:  
 $-0.0224 \pm j0.9978$ ;  $-0.0651 \pm j0.9001$ ;  $-0.1013 \pm j0.7143$ ;  $-0.1277 \pm j0.4586$ ;  $-0.1415 \pm j0.1580$ ,  $T(s) = 7.60 \times 10^4 / (s^2 + s 0.0448 \omega_p + 0.9961 \omega_p^2)$   
 $(s^2 + 0.1302 \omega_p + 0.8144 \omega_p^2)(s^2 + s 0.2026 \omega_p + 0.5205 \omega_p^2)(s^2 + 0.2554 \omega_p + 0.2266 \omega_p^2)(s^2 + s 0.2830 \omega_p + 0.0450 \omega_p^2)$

**17.26**  $R_1 = 120 \text{ k}\Omega$ ;  $C = 6.63 \text{ nF}$ ;  $R_2 = 120 \text{ k}\Omega$

**17.28**  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $C_1 = 0.16 \mu\text{F}$ ,  $C_2 = 1.6 \text{ nF}$ ; High-frequency gain = 40 dB

**17.30**  $T(s) = -(s - \omega_0)/(s + \omega_0)$  where  $\omega_0 = 1/CR$ ;  $T(j\omega) = \left(1 - j\frac{\omega}{\omega_0}\right) / \left(1 + j\frac{\omega}{\omega_0}\right)$ ;  
 $-2 \tan^{-1}(\omega/\omega_0)$ ; 5.36 kΩ, 11.55 kΩ, 20 kΩ, 34.60 kΩ, 74.63 kΩ.

**17.33**  $T(s) = 10^8 / (s^2 + 5000 s + 10^8)$ ; 9.354 krad/s, 2.066

**17.35**  $T(s) = s^2 / (s^2 + \sqrt{2}s + 1)$ ; Zeros: two at  $s = 0$ ; Poles:  $-0.707 \pm j0.707$

**17.37**  $T(s) = \pi \times 10^4 s / [s^2 + \pi \times 10^3 s + (2\pi \times 10^4)^2]$ ; Zeros:  $s = 0$  and  $s = \infty$ ;  
Poles:  $1.57 \times 10^3 \times (-1 \pm j39.988)$

**17.39**  $[s^2 + (2\pi \times 60)^2] / [s^2 + s(2\pi \times 60) + (2\pi \times 60)^2]$

**17.42**  $T(s) = (1/LC) / [s^2 + s/CR + (1/LC)]$

**17.44** (a) -0.5%; (b) -0.5%; (c) no change

**17.46**  $s^2 / \left( s^2 + \frac{1}{CR} + \frac{1}{LC} \right)$

**17.49**  $V_o = \left[ s^2 V_y + s \left( \frac{\omega_0}{Q} \right) V_z + \omega_0^2 V_x \right] / \left[ s^2 + s \left( \frac{\omega_0}{Q} \right) + \omega_0^2 \right]$

**17.51**  $R_1 = R_2 = R_3 = 10 \text{ k}\Omega$ ; (a)  $C_4 = 0.15 \mu\text{F}$ ; (b)  $C_4 = 15 \text{ nF}$ ; (c)  $C_4 = 1.5 \text{ nF}$

**17.55** First-order section (Fig. 17.13a):  $R_1 = R_2 = 100 \text{ k}\Omega$ ,  $C = 10 \text{ nF}$ ; Second-order section (Fig. 17.22a):  $C_4 = C_6 = 10 \text{ nF}$ ,  $R_1 = R_2 = R_3 = R_5 = 100 \text{ k}\Omega$ ,  $R_6 = 161.8 \text{ k}\Omega$ ,  $K = 1$ ;  
Second-order section (Fig. 17.22a):  $C_4 = C_6 = 10 \text{ nF}$ ,  $R_1 = R_2 = R_3 = R_5 = 100 \text{ k}\Omega$ ,  $R_6 = 61.8 \text{ k}\Omega$ ,  $K = 1$

**17.57**  $C_4 = C_6 = 1 \text{ nF}$ ,  $R_1 = R_2 = R_3 = R_5 = 79.6 \text{ k}\Omega$ ,  $R_6 = 159.2 \text{ k}\Omega$ ,  $r_1 = r_2 = 10 \text{ k}\Omega$

**17.60** (b) First-order section:  $C = 1 \text{ nF}$ ,  $R_1 = R_2 = 13.71 \text{ k}\Omega$ , Second-order LPN section:  
 $R_1 = R_2 = R_3 = R_5 = 9.76 \text{ k}\Omega$ ,  $C_{61} = 618 \text{ pF}$ ,  $C_{62} = 382 \text{ pF}$ ,  $R_6 = 35.9 \text{ k}\Omega$ ,  $K = 1$

**17.62** (b)  $C = 1 \text{ nF}$ ,  $R = 10 \text{ k}\Omega$ ,  $R_1 = 10 \text{ k}\Omega$ ,  $R_f = 10 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $R_3 = 70 \text{ k}\Omega$ ,  
 $R_L = R_H = 10 \text{ k}\Omega$ ,  $R_B = 40 \text{ k}\Omega$ ,  $R_F = 57.1 \text{ k}\Omega$

**17.64** 1%

**17.67** (b) First-order section:  $C = 1 \text{ nF}$ ,  $R_1 = R_2 = 13.71 \text{ k}\Omega$ , Second-order LPN section:  
 $C = 1 \text{ nF}$ ,  $R = 9.76 \text{ k}\Omega$ ,  $R_d = 35.9 \text{ k}\Omega$ ,  $r = 10 \text{ k}\Omega$ ,  $C_1 = 618 \text{ pF}$ ,  $R_1 = R_3 = \infty$ ,  
 $R_2 = 9.76 \text{ k}\Omega$

**17.71**  $\omega_0 = 6/CR$ ,  $Q = 3$ , Center-frequency gain = -18 V/V.

**17.73** (a)  $Q^2$ ; (b)  $2Q^2$

**17.75 (b)** Second-order section [Fig. 17.34(c)]:  $R_1 = R_2 = 10 \text{ k}\Omega$ ,  $C_3 = 492 \text{ pF}$ ,  $C_4 = 5.15 \text{ nF}$ ; Second-order section [Fig. 17.34(c)]:  $R_1 = R_2 = 10 \text{ k}\Omega$ ,  $C_3 = 1.29 \text{ nF}$ ,  $C_4 = 1.97 \text{ nF}$ ; First-order section (Fig. 17.13a):  $R_1 = R_2 = 10 \text{ k}\Omega$ ,  $C = 1.59 \text{ nF}$

**17.77**  $S_L^{\omega_0} = -\frac{1}{2}$ ,  $S_C^{\omega_0} = -\frac{1}{2}$ ,  $S_R^{\omega_0} = 0$ ;  $S_L^Q = -\frac{1}{2}$ ,  $S_C^Q = \frac{1}{2}$ ,  $S_R^Q = 1$

**17.79**  $S_A^{\omega_0} = 0$ ,  $S_A^Q = 2Q^2/A$

**17.81**  $S_{C_4}^{\omega_0} = S_{C_6}^{\omega_0} = S_{R_1}^{\omega_0} = S_{R_3}^{\omega_0} = S_{R_5}^{\omega_0} = -\frac{1}{2}$ ,  $S_{R_2}^{\omega_0} = +\frac{1}{2}$ ,  $S_{R_6}^{\omega_0} = +1$ ,  $S_{C_6}^Q = S_{R_2}^Q = +\frac{1}{2}$ ,  
 $S_{C_4}^Q = S_{R_1, R_2, R_3}^Q = -\frac{1}{2}$ ,

**17.83** 1 mA/V; 0.99 kΩ

**17.85** 0.314 mA/V

**17.87**  $G_{m1} = 2.51 \text{ mA/V}$ ;  $G_{m2} = 0.251 \text{ mA/V}$

**17.90**  $C_1 = Q^2 C$ ;  $G_m = \omega_0 Q C$

**17.92**  $G_m = 0.785 \text{ mA/V}$ ;  $G_{m2} = 0.785 \text{ mA/V}$ ;  $G_{m3} = 0.157 \text{ mA/V}$ ;  $G_{m4} = 0.785 \text{ mA/V}$

**17.94** 1 pC; 0.1 μA; 0.1 V; 100 cycles;  $10^4 \text{ V/s}$

**17.96**  $C_3 = C_4 = 6.283 \text{ pF}$ ;  $C_5 = 0.126 \text{ pF}$ ;  $C_6 = 0.126 \text{ pF}$

**17.98** 80.3 rad/s; 83; 967 kHz; 66.7 V/V

**17.100** 838.8 kHz; 47.4

**17.103**  $A$  (dB): 7, 8.5, 9.3, 9.8, 10.1;  $W/B$ : 31.6, 8.6, 5.9, 4.9, 4.5

## CHAPTER 18

**18.1**  $\omega_0$ ;  $AK = 1$

**18.3 (a)** 1; **(b)** 2

**18.5** 0.6 mA/V; 15.92 MHz

**18.7**  $120^\circ$ ;  $\omega_0 = \sqrt{3}/CR$ ;  $2/R$

**18.11**  $\omega_0 = 1/CR$ ;  $Q = 1/3$ ; Gain = 1/3

**18.13**  $\omega_0 = 1/CR$ ;  $Q = 1/\left(2 - \frac{R_2}{R_1}\right)$

**18.15**  $\omega_0 = 1/CR$ ;  $R_2/R_1 \geq 2$

**18.17** 7.88 V

**18.19**  $f_0 = 406 \text{ Hz}$ ;  $R_f = 290 \text{ k}\Omega$

**18.22** 9.95 kΩ; 3.6 V; add a diode in series with each of the limiter diodes.

**18.24**  $\omega_0 = 1/\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}$ ; simplified condition:  $g_m R_L > \frac{C_2}{C_1}$

18.26  $\omega_0 = 1/\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}$ ;  $g_m R'_L > \frac{C_1}{C_2}$

18.28 (b)  $\omega_0 = 1/\sqrt{LC}$ ;  $IR_C > 0.1$  V, (c)  $(4/\pi)$  V

18.30 2.0165 MHz to 2.0173 MHz, a range of 800 Hz.

18.32 (a)  $V_{TH} = \left(\frac{L_+}{R_2} + \frac{V}{R_3}\right)(R_1 \| R_2 \| R_3)$ ;  $V_{TL} = \left(\frac{L_-}{R_2} + \frac{V}{R_3}\right)(R_1 \| R_2 \| R_3)$ ;  
 (b)  $R_2 = 656.7$  k $\Omega$ ,  $R_3 = 19.7$  k $\Omega$

18.36 (a) Output will be either +12 V or -12 V; (b) The output is a symmetric square wave ( $\pm 12$  V) of frequency  $f$  and it lags the sine wave by an angle of  $65.4^\circ$ ; 0.1 V.

18.38 1989 Hz

18.40  $V_Z = 3.6$  V;  $R_1 = R = 25$  k $\Omega$ ;  $R_3 = 5.83$  k $\Omega$ ;  $C = 0.01$   $\mu$ F;  $R = 25$  k $\Omega$

18.42 96  $\mu$ s

18.44  $C_1 = 1$  nF,  $C_2 = 0.1$  nF,  $R_1 = R_2 = 100$  k $\Omega$ ,  $R_3 = 134.1$  k $\Omega$ ,  $R_4 = 470$  k $\Omega$ ; 5.8 V; 61.8  $\mu$ s

18.46 (a) 18.2 k $\Omega$ ; (b) 10.67 V

18.48 (b) 100.6 kHz, 75%; (c) 15.6  $\mu$ s, 55.2 kHz, 86.2%; 3.90  $\mu$ s, 156 kHz, 61%

18.50 1.85 V