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Final Exam

Honor Code

0 points possible (ungraded)

On this exam, I will not cheat, use unfair means, join intentionally or unintentionally any online or offline group in which exam answers are posted or discussed, or engage in any behavior that would commonly be deemed academically unethical. I acknowledge that I may be suspended or expelled from Brac University if I am found to have engaged in any academically unethical behavior. I further recognize that non-compliance with the above may lead to further disciplinary actions which I accept without complaint.

Do you agree with the statement?

☒ I agree with the statement



Submit

You have used 1 of 1 attempt

Answers are displayed within the problem

Question 1

10.0/10.0 points (graded)

Consider below code sequence:

```
i. Subi $2, $1, 3
ii. and $12, $2, $5
iii. or $13, $6, $7
iv. lw $1, 24($13)
v. beq $14, $1, IF
vi. sw $14, 100($16)
```

What should be the value of the RegDST, ALUSrc, MemToReg and MemWrite for instruction vi? Write a 4-bit binary expression where each digit corresponds to the value of each of the mentioned control signals. For example, if the values are 0,0,x,0 respectively then you will write 00x0. Use 'x' for don't care

✓ Answer: x1x1

How many clock cycles would you need if you only used the Stalling method to remove the hazard?

✓ Answer: 16

What would be the CPI if you only used the Stalling method to remove the hazard? Write only 2 digits after the decimal without rounding

✓ Answer: 2.66

How many clock cycles would you need if you only use Stalling and Forwarding method to remove the hazard?

✓ Answer: 11

What would be the CPI if you only used the Stalling and Forwarding method to remove the hazard? Write only 2 digits after the decimal without rounding

✓ Answer: 1.83

Submit

You have used 1 of 2 attempts

❗ Answers are displayed within the problem

Question 2

6.0/10.0 points (graded)

Suppose a direct-mapped cache can store 32 KiB of data. Each block contains 2048 words and the address length is 106 bit. Now answer the following questions:

How many blocks are there in the cache?

✓ Answer: 4

How many data bits are required for the cache?

✓ Answer: 15

How many tag bits are required for the cache?

✓ Answer: 91

What is the actual cache size in KiB? (including the valid and tag bit)

Write your answer in KiB up to 2 decimal places. Do not write a unit.

32.777

✗ Answer: 32.04

32.777

To what block number does byte address 27652 map?

✗ Answer: 3.0

Submit

You have used 1 of 2 attempts

i Answers are displayed within the problem

Question 3

2.0/10.0 points (graded)

Suppose it takes 492 ns to perform a set of tasks where it takes 195 ns to perform parallel tasks. Now if we use 24 processors, how much time is reduced?

Write your answer up to 2 decimal places rounded off without any unit

182.625

✗ Answer: 186.88

182.625

If 225 tasks are serial and 1836 are parallel, what should be the speedup if we use 174 processors compared to if we use 59 processors?

Write your answer up to 2 decimal places rounded off without any unit

1.087

✓ Answer: 1.09

1.087

If we have 259 serial tasks and 261 parallel tasks, what should be the speedup if we use 54 processors compared to a single processor?

Write your answer up to 2 decimal places rounded off without any unit

✖ Answer: 1.97

What should be the percentage of potential based on the previous question information and answer?

Write your answer up to 2 decimal places rounded off without any unit

✖ Answer: 3.65

How many processors would be needed to make the task in the previous question 2 times faster compared to a single processor?

✖ Answer: 261.0

Submit

You have used 1 of 2 attempts

i Answers are displayed within the problem

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