Questions

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Question

1.0/1.0 point (graded)

While faculties taking your online classes via Google Meet, which kind of communication does take place?

- [x] Synchronous
- [ ] Asynchronous

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Question

1.0/1.0 point (graded)

Which communication protocol is less memory efficient?

- [ ] Synchronous
- [x] Asynchronous

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Question

1.0/1.0 point (graded)

When any of you post on Google Classroom or Slack platform for any issue, then which communication does take place?

- [ ] Synchronous
- [x] Asynchronous

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Question

2.0/2.0 points (graded)

Asynchronous communication is slower because:

- [ ] It is limitted to carry 8 bits only
- [x] It has extra overhead of bit synchronization
- [x] It has to add and remove extra bits, which is complex and time consuming.
- [ ] No it is as same speed as synchronous

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Question

1.0/1.0 point (graded)

How can Master or slave check that the reciver has successfully received the transmitted data in SPI?

- [ ] SPI sends data to unique addressed Slave
- [ ] There is ACK/NACK bits
- [ ] There is stop condition and "syn" character indicating successful transmission of data.
- [x] No mechanism in SPI to acknowledge successful transmission

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Question

1.0/1.0 point (graded)

We know, In SPI, slave sends data to master along with the pre-generated clock signal of master. How can master know how many bits of data the slave want to transfer?

- [ ] Master sends random number of clock pulses
- [ ] Slave informs master about how many bits it wants to transfer
- [x] Master generates clock pulses depends on the maximum number of bits the data bus can tranfer on those devices.
- [ ] There is a fixed amount of clock pulses that master generates all the time in all devices

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Question

1.0/1.0 point (graded)

SPI can check error using parity bit. Is this statement true or false?

False

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Question

1.0/1.0 point (graded)

When there is no data flow through asynchronous line then the line is held at

- [x] High voltage level
- [ ] Low voltage level
- [ ] Neutral level (No voltage transfer)

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Question

1.0/1.0 point (graded)

When the sending UART drives the data transmission line from a low voltage to a high voltage, it indicates

- [ ] Start condition
- [ ] Stop condition
- [ ] Parity checking
- [ ] Total transmission of whole data is finished
- [x] Also needs to check Clock line to determine the condition.

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Question

1.0/1.0 point (graded)

If we want to connect a MPU, a MCU as master with some peripheral devices as slaves, then how can data transfer will take place through UART?

- [ ] By using TX-RX lines from both the masters
- [ ] Using unique addressing to each master and slave devices
- [ ] Can implement daisy chain configuration
- [x] It is limited to single master configuration

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Question

1.0/1.0 point (graded)

A communication protocol which is limited to carry 8 bits, and synchronous, does not have any data bit error checking mechanism. What is it?

- [ ] SPI
- [ ] UART
- [x] I2C

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Question

1.0/1.0 point (graded)

If you want to transfer continous stream of data, at a faster speed then which one is preferred?

- [x] SPI
- [ ] UART
- [ ] I2C

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Question

1.0/1.0 point (graded)

In data transmission, if you need less faulty or less error data, which protocol is preferred from the following?

- [ ] SPI
- [x] UART
- [ ] I2C

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Question

1.0/1.0 point (graded)

If your project needs at least two or more devices that can control clocking or selection of slaves, also needs perfect transmit and receive acknowledgment, but can sacrifice speed of transmission, then which protocol is preferred?

- [ ] SPI
- [ ] UART
- [x] I2C

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Question

1.0/1.0 point (graded)

In I2C, suppose two master devices want to transfer data at the same time. Master 2 finds that SDA line is high, and then it pulls the SDA line low, then which of the following statements are true?

- [ ] Master 2 finds that data line is being used by master 1.
- [x] Master 1 finds that data line is being used by master 2.
- [ ] Master 1 can tranfer data when Master 2 will pull the SDA line low at the end of transmission.
- [x] Master 1 can tranfer data when Master 2 will pull the SDA line high at the end of transmission.
- [ ] This situation can be handled down easily if we use SPI protocol instead of I2C.

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Question

1.0/1.0 point (graded)

If we want to add multiple slaves with different functionality, then which protocol is most suitable in case of adding slaves easily?

- [ ] SPI
- [ ] UART
- [x] I2C

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Question

1.0/1.0 point (graded)

In which protocol you think both of the devices has same priority. No master slave relation is required?

- [ ] SPI
- [x] UART
- [ ] I2C

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Question

1.0/1.0 point (graded)

Transmission and receiving end can use different transmission protocol.

- [ ] True
- [x] False

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Question

1.0/1.0 point (graded)

Which of the following statement(s) is/are true?

- [ ] SPI require acknowledgement but I2C use parity bit for secure data transmission
- [x] UART use separate wires for data transmission and receiving but I2C use single wire
- [ ] UART can address different slaves by using different Slave select (SS) lines

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