QEMU implementation of NXP S32K3X8EVB board

Group 10

Project Report

Master degree in Computer Engineering: Embedded Systems

Referents:
Prof. Stefano Di Carlo
Prof. Carpegna Alessio
Prof. Carpegna Alessio
Prof. Eftekhari Moghadam Vahid
Prof. Magliano Enrico

Authors:
Francesco Mignone
Leonardo Gallina
Andrea Baraldi
Silvia Bonenti
Lorenzo Parata

Abstract

This document provides a comprehensive overview of the design and development of a DLX micropro-
cessor, a project undertaken by Group 02 as part of the Microelectronic Systems course at Politecnico
di Torino. The project aims to enhance understanding of microprocessor design stack: starting from
a RTL VHDL description to the Physical Design process. The report details the structure and the
process that lead to the implementation. To allow the reader to understand the design choices, the
report is structured as follows:

- **Chapter 1: Introduction** - Introduces the DLX microprocessor architecture, its instruction
  set, and the project objectives.

- **Chapter 2: DLX Structure** - Discusses the design process, including the control unit, Data-
  path, and functional units.

- **Chapter 3: Synthesis** - Describes the testing methodologies used to validate the design and
  ensure correctness.

- **Chapter 4: Physical Design** - Covers the synthesis process and the physical design steps
  taken to prepare the microprocessor for fabrication.

- **Chapter 5: Tools and Scripts** - Lists the tools and technologies used throughout the project,
  including VHDL, ModelSim/QuestaSim, Innovus, Docker and custom scripts.

- **Chapter 6: Conclusions** - Summarizes the project outcomes, challenges faced, and lessons
  learned.

- **Appendices** - Provides additional resources, including VHDL code, user scripts, and TCL
  templates used in the project.

Prior knowledge of VHDL and digital design principles is assumed, as the report focuses on the imple-
mentation details and design choices made during the project. Also a general knowledge of computer
architectures is recommended, mostly in RISC principles pipelined architectures. The document serves
as a valuable resource for understanding the complexities of microprocessor design and the practical
application of theoretical concepts in a real-world project.

Contents

APPENDIX A

QEMU Code

A.1   Control unit