

---

# **Analog Design Techniques**

**Jan Genoe (jan.genoe@kuleuven.be)**

**Feb 28, 2023**



## CONTENTS

<b>I</b>	<b>Chip Design</b>	<b>3</b>
1	Differential Amplifiers	5
2	Folded cascode stage	11
<b>II</b>	<b>Capita Selecta</b>	<b>15</b>
3	Capacitive voltage conversion	17
<b>III</b>	<b>References</b>	<b>25</b>
4	References	27
<b>IV</b>	<b>Overzicht</b>	<b>29</b>



by **Jan Genoe**

This [Jupyter Book](#) comprises notebooks used in the lectures of [Analog Design Techniques](#) of the [KU Leuven](#), campus Diepenbeek.

---

**Note:** This is currently still work in progress. Please refer to Toledo as the key source of information. This book is only added as support.

---

## Table of Contents

- Chip Design
  - *Differential Amplifiers*
  - *Folded cascode stage*
- Capita Selecta
  - *Capacitive voltage conversion*
- References
  - *References*
- Overzicht
  - [Lijst cursussen](#)
  - [Auteur Jan Genoe](#)

## Licenties

The content is licensed under a [Creative Commons Attribution 4.0 International License](#) The code is licensed under the [MIT license](#)



# **Part I**

## **Chip Design**





## DIFFERENTIAL AMPLIFIERS

 reveal.js slides  open in JupyterLab  JupyterDeck slides

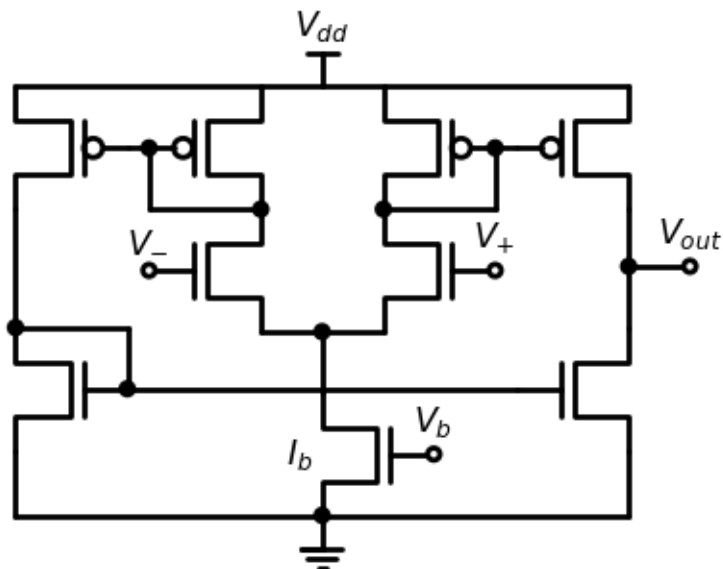


Fig. 1.1: Differential amplifier configuration



Fig. 1.2: Differential applifier configuration



Fig. 1.3: Differential applifier configuration



Fig. 1.4: Differential applifier configuration



Fig. 1.5: Differential applifier configuration



Fig. 1.6: Differential amplifier configuration



Fig. 1.7: Differential applifier configuration



Fig. 1.8: Differential applifier configuration

## FOLDED CASCODE STAGE

 reveal.js  slides  open in JupyterLab  JupyterDeck  slides

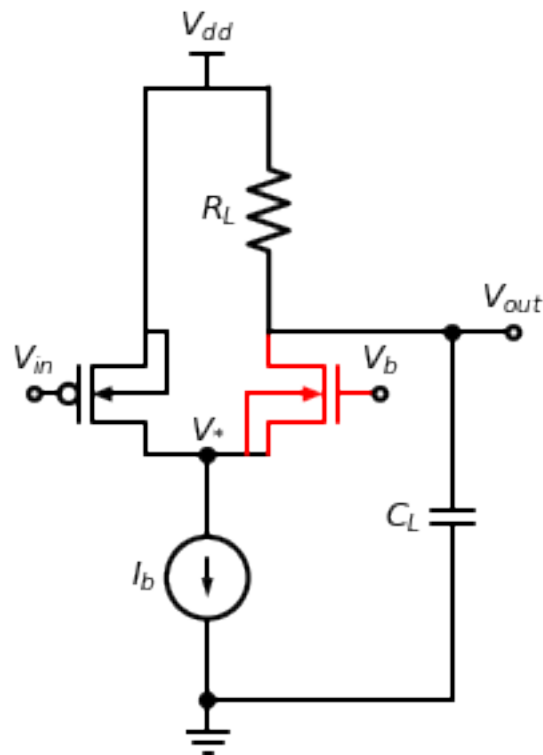


Fig. 2.1: Theoretical folded cascode configuration

In Fig. 2.1 we also add a cascode transistor (in red) between the input transistor and the output node. This corresponds as a consequence to a classical cascode stage. However, there is one major difference: the cascode transistor is of the opposite polarity when compared to the input transistors. In Fig. 2.1 the input transistor is a pMOS transistor and the cascode transistor is an nMOS transistor. Obviously, this also alters the current flow, and in order to maintain the current flow between power ( $V_{dd}$ ) and ground, an additional current source ( $I_b$ ) needs to be added.

For the practical implementation of this folded cascode, we replace the current source ( $I_b$ ) with the transistor  $T_3$ , as can be seen in Fig. 2.2.

The amplification of this simple folded cascode amplifier stage is defined by:

- the  $g_m$  of the input transistor  $T_1$
- the conductance of the load resistor  $g_L$
- the output conductance of the folded cascode stage  $g_{casc}$
- the capacitive load  $C_L$

$$A = \frac{g_{m1}}{g_L + g_{casc} + j\omega C_L}$$

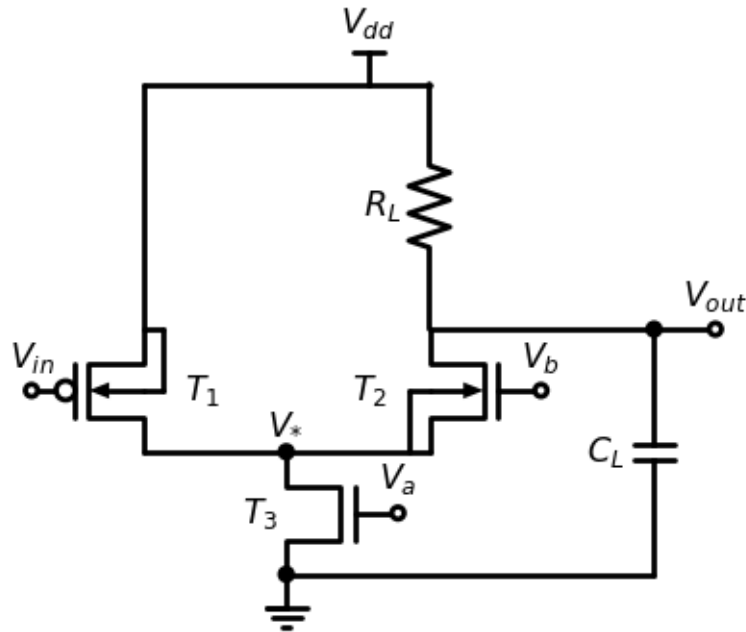


Fig. 2.2: Practical folded cascode amplifier stage configuration

The important next step is obviously the determination for  $g_{casc}$ . We use Fig. 2.3 for elaborating this output impedance.





Fig. 2.3: Circuit block under consideration for measuring the folded cascode output impedance



**Part II**

**Capita Selecta**



## CAPACITIVE VOLTAGE CONVERSION

 reveal.js slides  open in JupyterLab  JupyterDeck slides

Classical power conversion makes use of inductors and transformers to deliver power at different voltage levels. However, these components typically transform these power converters into bulky and heavy components. However, there are several applications where we only need a voltage and a rather limited current sourced. Moreover, for power converters on silicon chips, efficient inductors are not possible and capacitive power converters are needed. In this chapter we discuss those power converters.

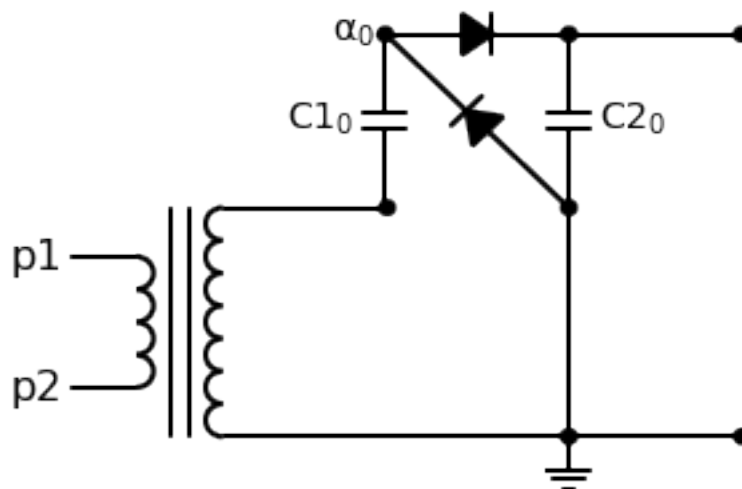


Fig. 3.1: Voltage doubler schematic with large  $C2$  without resistive load



Fig. 3.2: Voltage doubler with large C2 node voltages without resistive load



Fig. 3.3: Voltage doubler with large C2 node voltages with resistive load



Fig. 3.4: Voltage doubler with large C2 in the presence of resistive load



Fig. 3.5: Voltage doubler with equal capacitances





Fig. 3.6: Voltage doubler with equal capacitances node voltages and a resistive load



Fig. 3.7: Capacitive Voltage upconverter schematic comprising 7 stages



Fig. 3.8: Node voltages of a capacitive Voltage upconverter comprising 7 stages



## **Part III**

# **References**



**REFERENCES**





## **Part IV**

# **Overzicht**

