# Analog Design Techniques

**Jan Genoe (jan.genoe@kuleuven.be)**

**Feb 16, 2026**

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**by Jan Genoe**

This Jupyter Book comprises notebooks used in the lectures of Analog Design Techniques of the KU Leuven, campus Diepenbeek.

> **Note**
>
> This is currently still work in progress. Please refer to Toledo as the key source of information. This book is only added as support.

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  - Auteur Jan Genoe


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# Part I

# Chip Design

CHAPTER

# ONE

# DIFFERENTIAL AMPLIFIERS

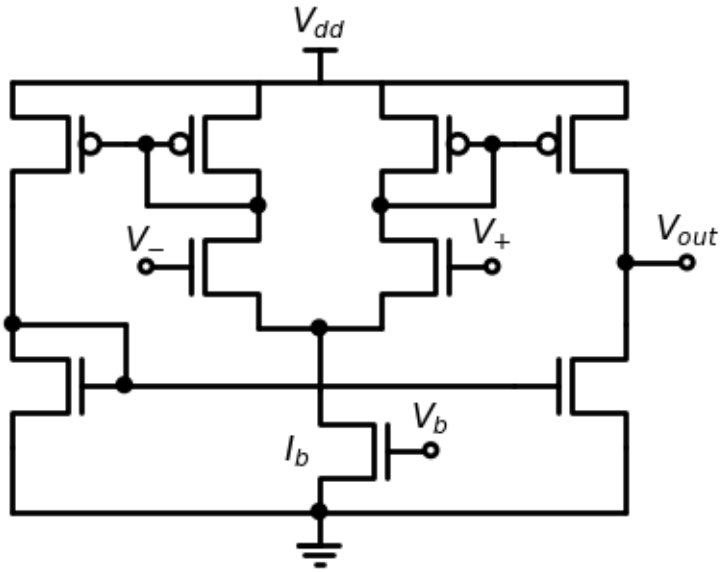



Fig. 1.1: Differential applifier configuration

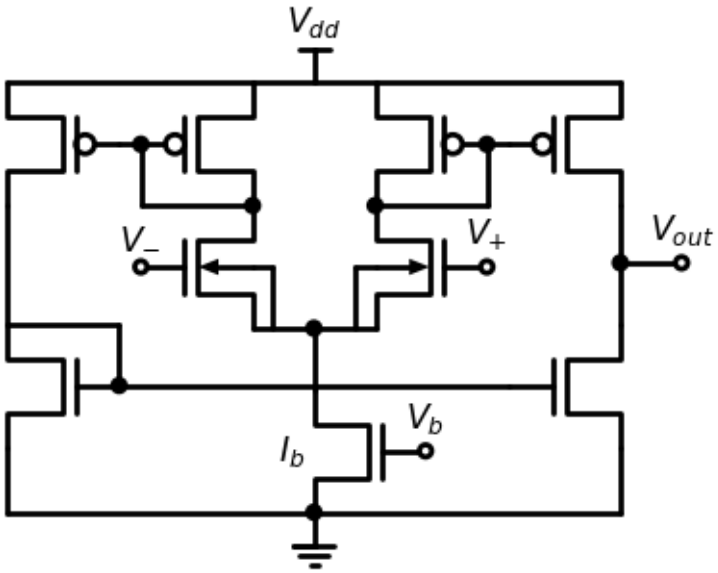



Fig. 1.2: Differential applifier configuration

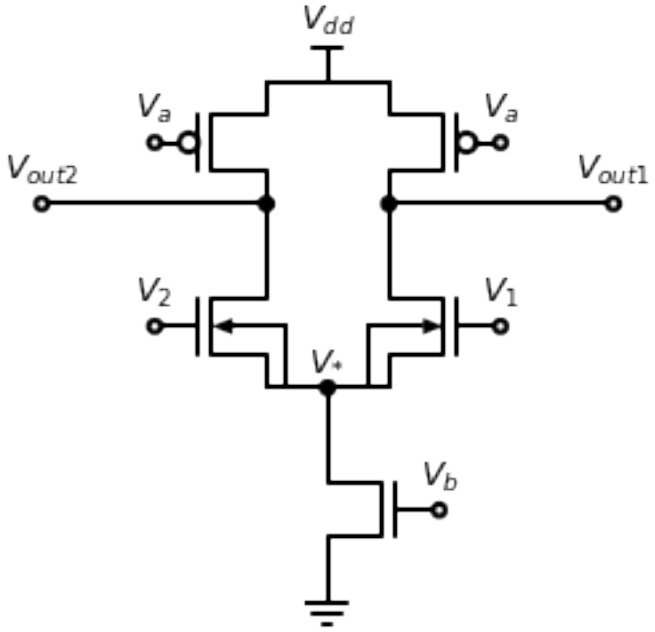



Fig. 1.3: Differential applifier configuration

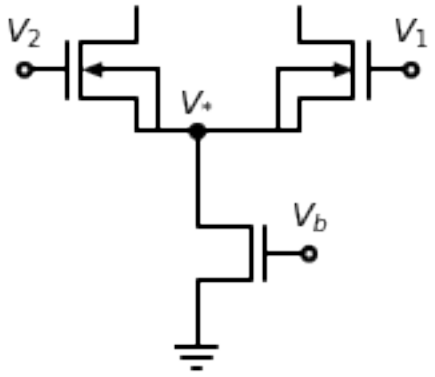



Fig. 1.4: Differential applifier configuration

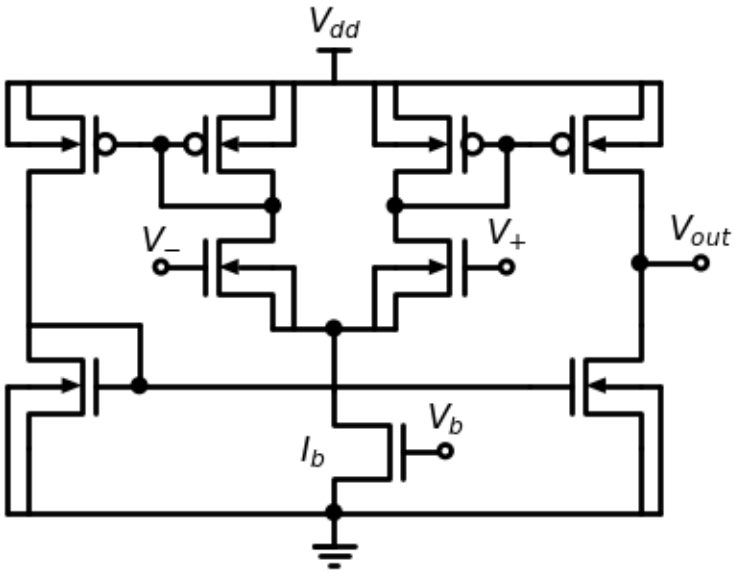



Fig. 1.5: Differential applifier configuration

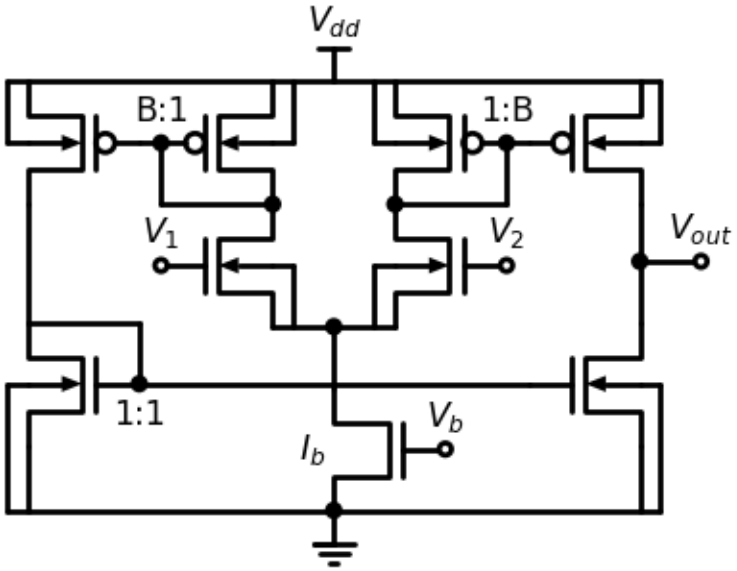



Fig. 1.6: Differential applifier configuration

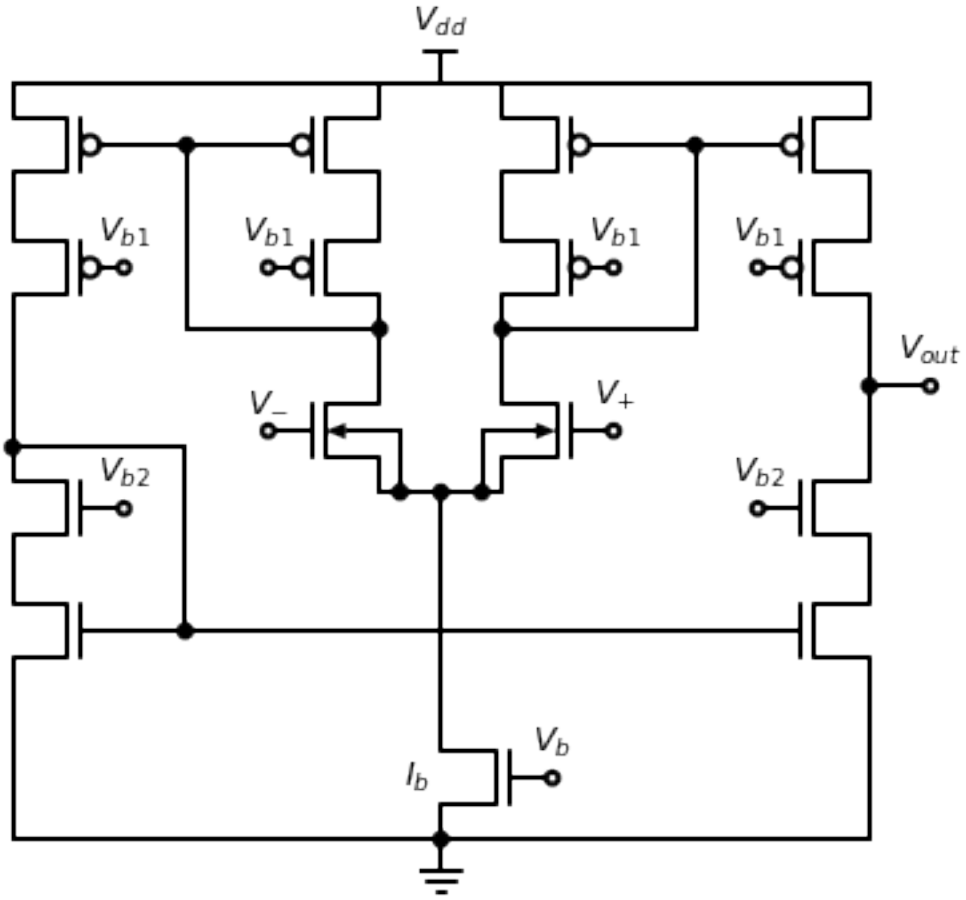



Fig. 1.7: Differential applifier configuration

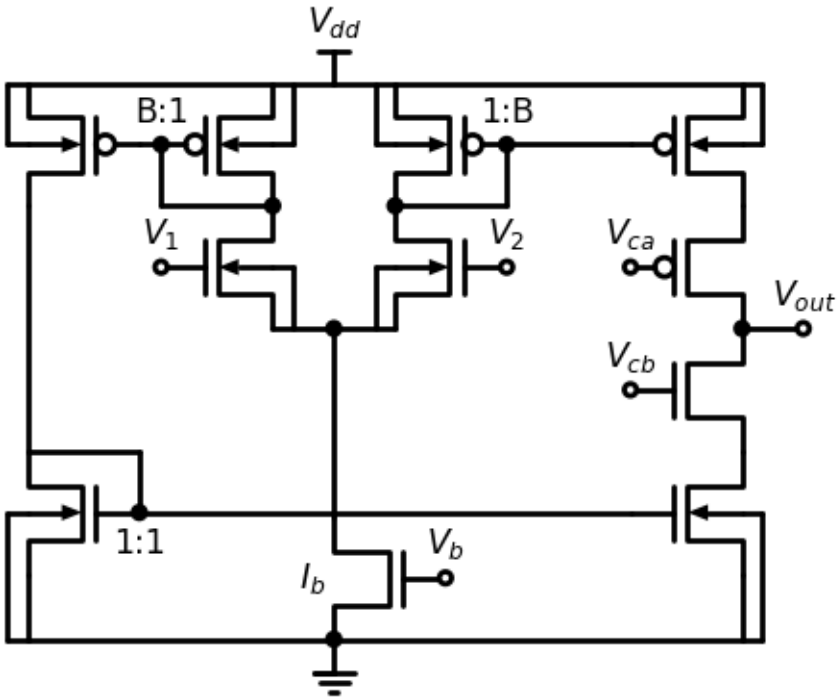



Fig. 1.8: Differential applifier configuration

CHAPTER

# TWO

# FOLDED CASCODE STAGE

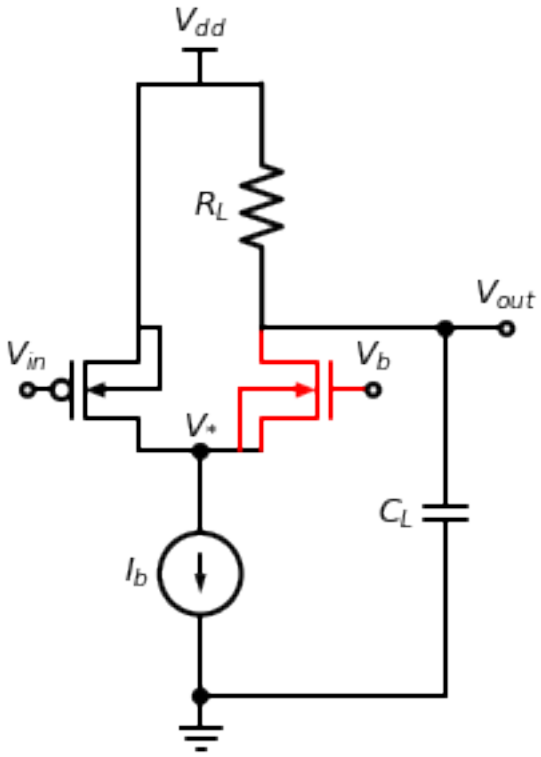



Fig. 2.1: Theoretical folded cascode configuration

In Fig. 2.1 we also add a cascode transistor (in red) between the input transistor and the output node. This corresponds as a consequence to a classical cascode stage. However, there is one major difference: the cascode transistor is of the opposite polarity when compared to the input transistors. In Fig. 2.1 the input transistor is a pMOS transistor and the cascode transistor is an nMOS transistor. Obviously, this also alters the current flow, and in order to maintain the current flow between power ($V_{dd}$) and ground, an addition current source ($I_b$) needs to be added.

For the practical implementation of this folded cascode, we replace the current source ($I_b$) with the transistor $T_3$, as can be seen in Fig. 2.2.

The amplification of this simple folded cascode amplifier stage is defined by:

- the $g_m$ of the input transistor $T_1$

- the conductance of the load resistor $g_L$
- the output conductance of the folded cascode stage $g_{casc}$
- the capacitive load $C_L$

$$A = \frac{g_{m1}}{g_L + g_{casc} + j\omega C_L}$$

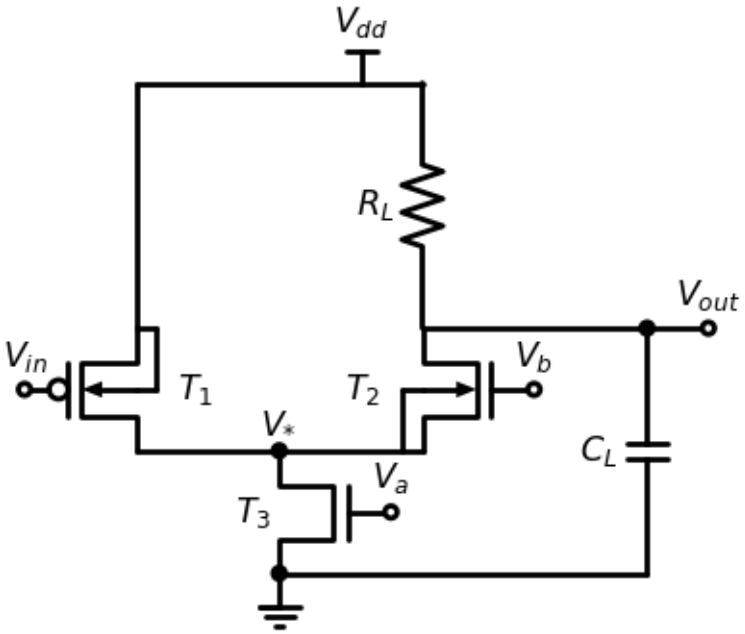



Fig. 2.2: Practical folded cascode amplifier stage configuration

The important next step is obviously the determination fo $g_{casc}$. We use Fig. 2.3 for elaborating this output impedance.

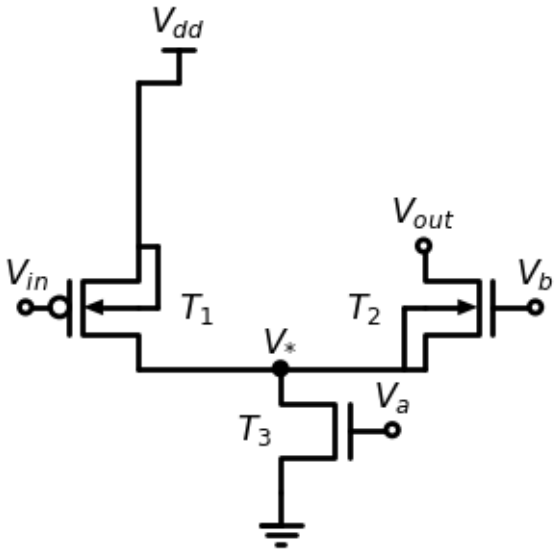



Fig. 2.3: Circuit block under consideration for measuring the folded cascode output impedance

# Part II

# Capita Selecta

CHAPTER

THREE

# CAPACITIVE VOLTAGE CONVERSION

Classical power conversion makes use of inductors and transformers to deliver power at different voltage levels. However, these components typically transform these power converters into bulky and heavy components. However, there are several applications where we only need a voltage and a rather limited current sourced. Moreover, for power converters on silicon chips, efficient inductors are not possible and capacitive power converters are needed. In this chapter we discuss those power converters.

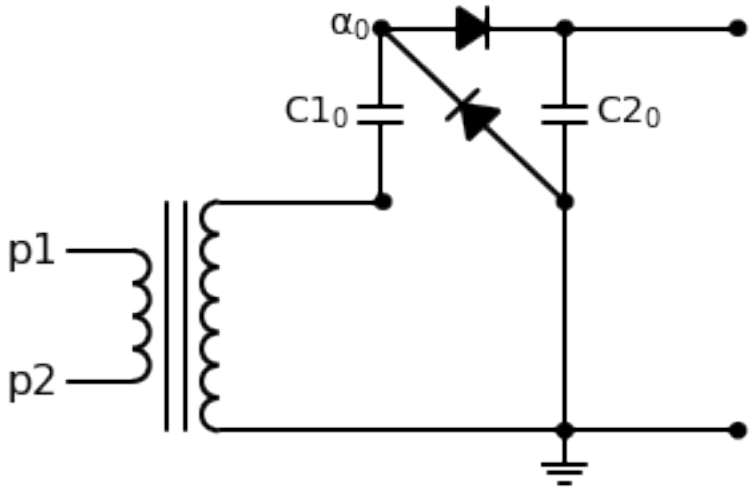



Fig. 3.1: Voltage doubler schematic with large C2 without resistive load

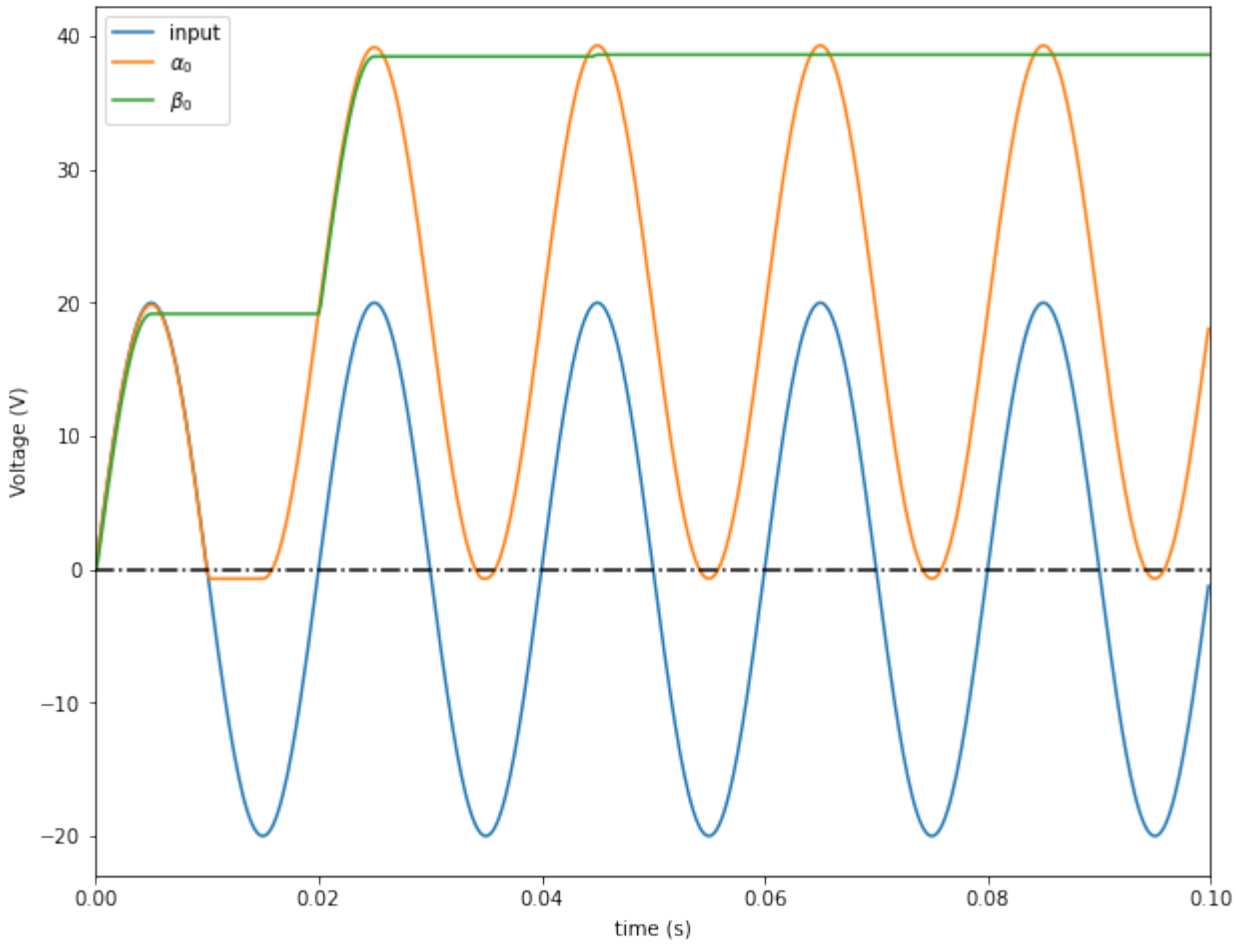



Fig. 3.2: Voltage doubler with large C2 node voltages without resistive load

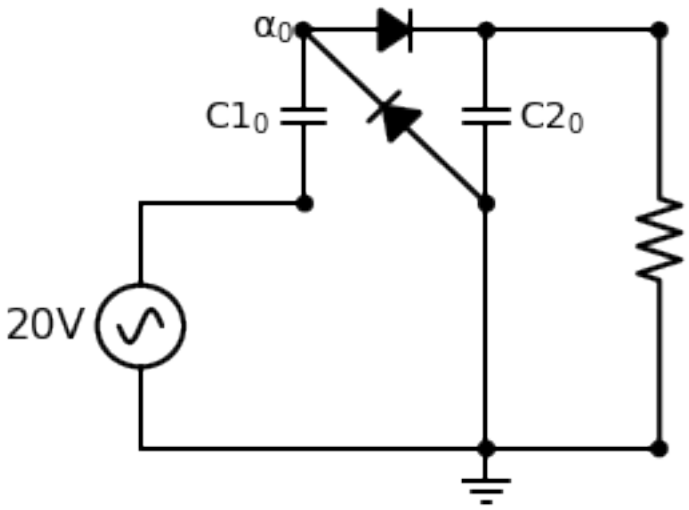



Fig. 3.3: Voltage doubler with large C2 node voltages with resistive load

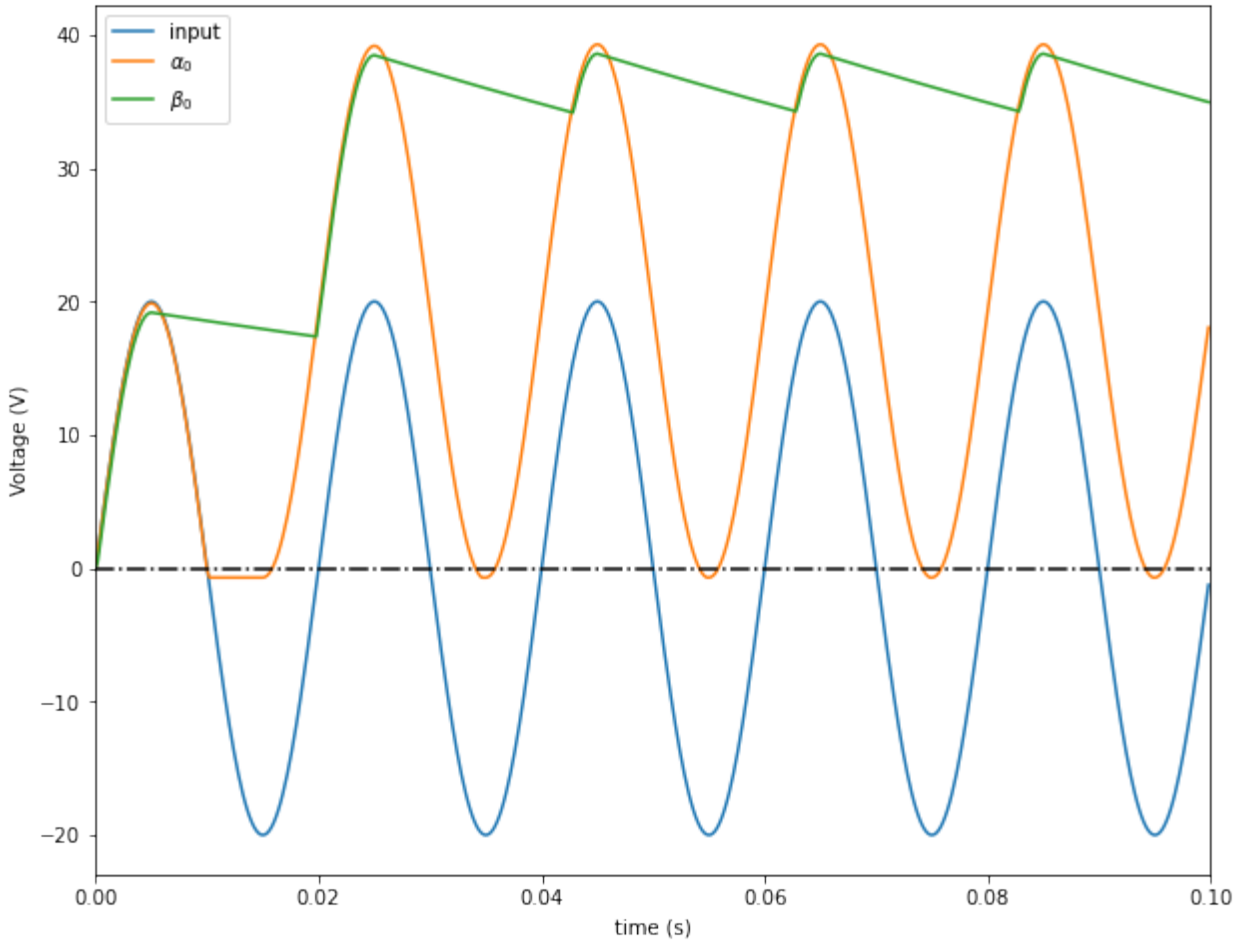



Fig. 3.4: Voltage doubler with large C2 in the presence of resistive load

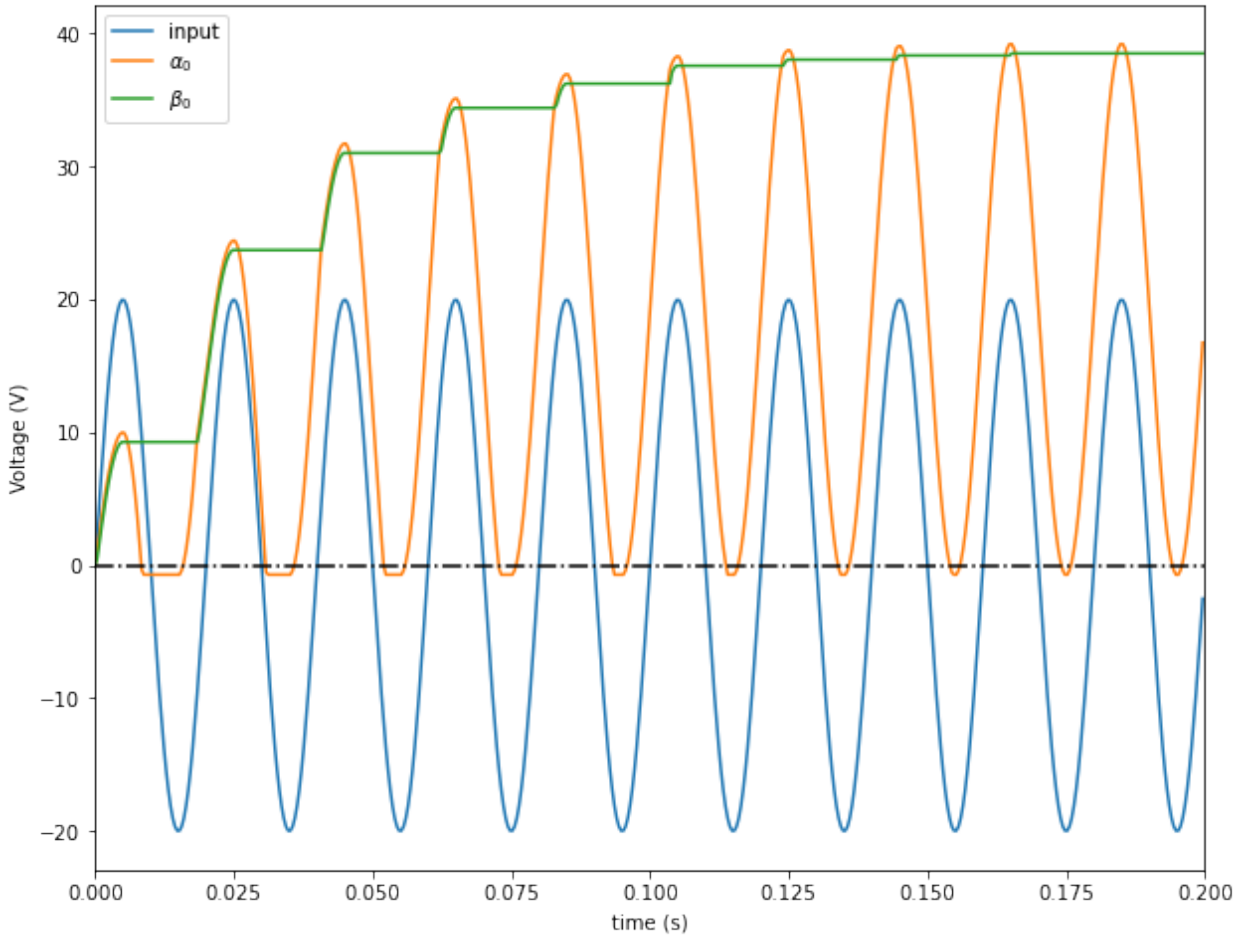



Fig. 3.5: Voltage doubler with equal capacitances

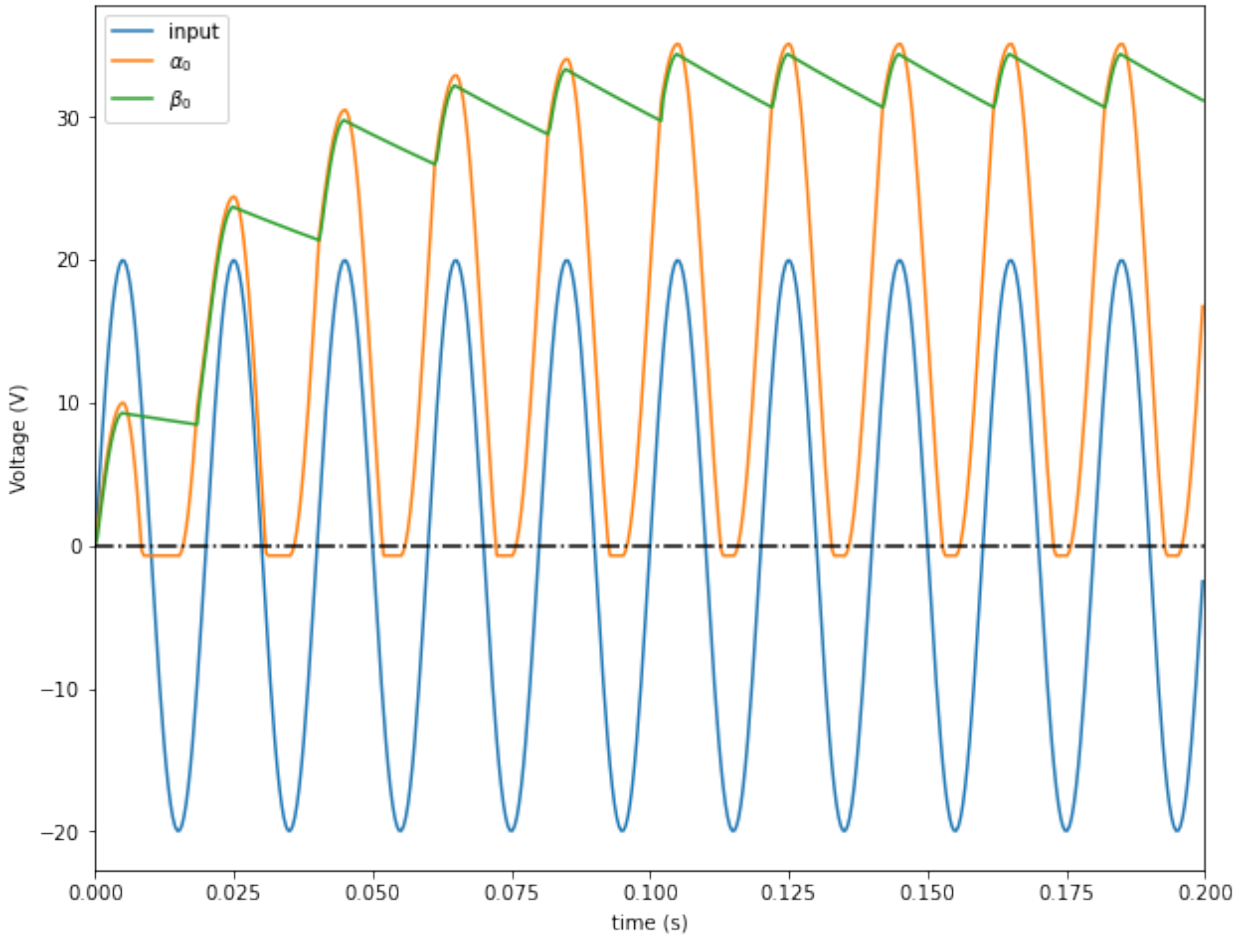



Fig. 3.6: Voltage doubler with equal capacitances node voltages and a resistive load

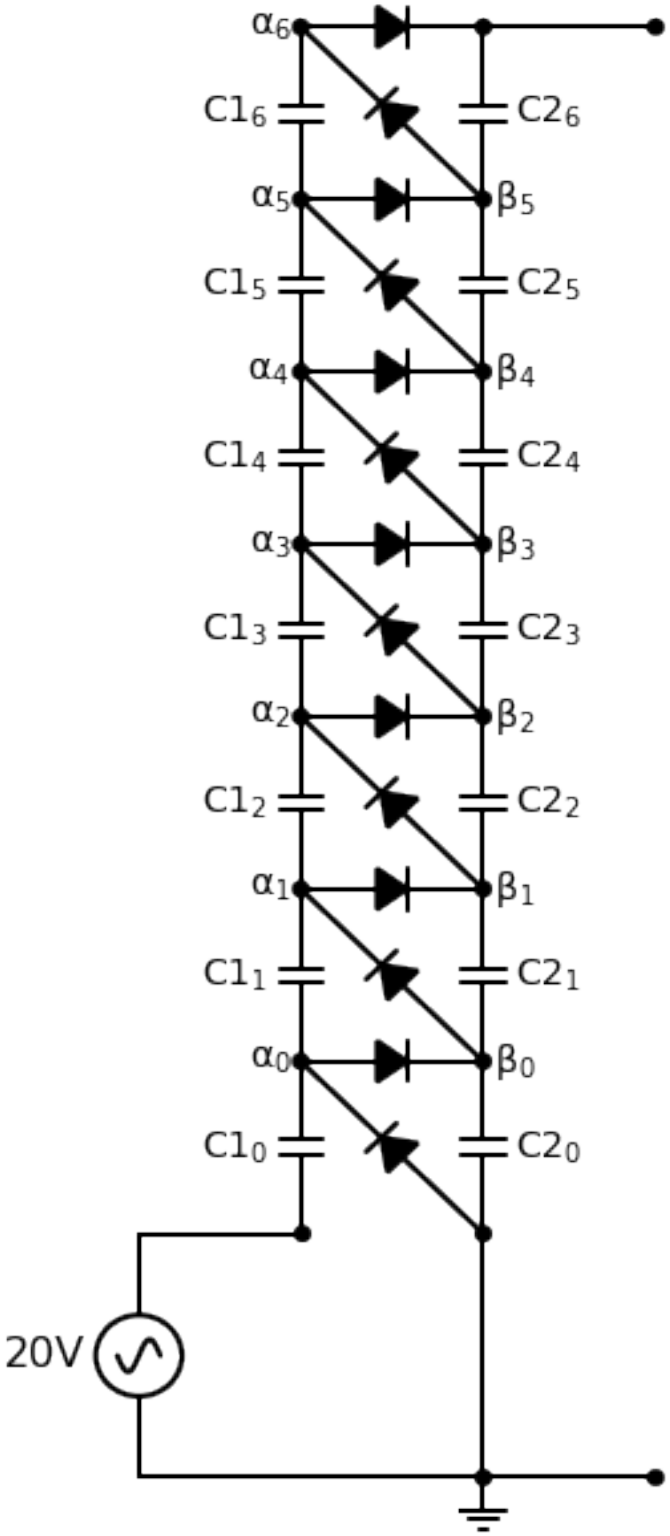



Fig. 3.7: Capacitive Voltage upconvertor schematic comprising 7 stages

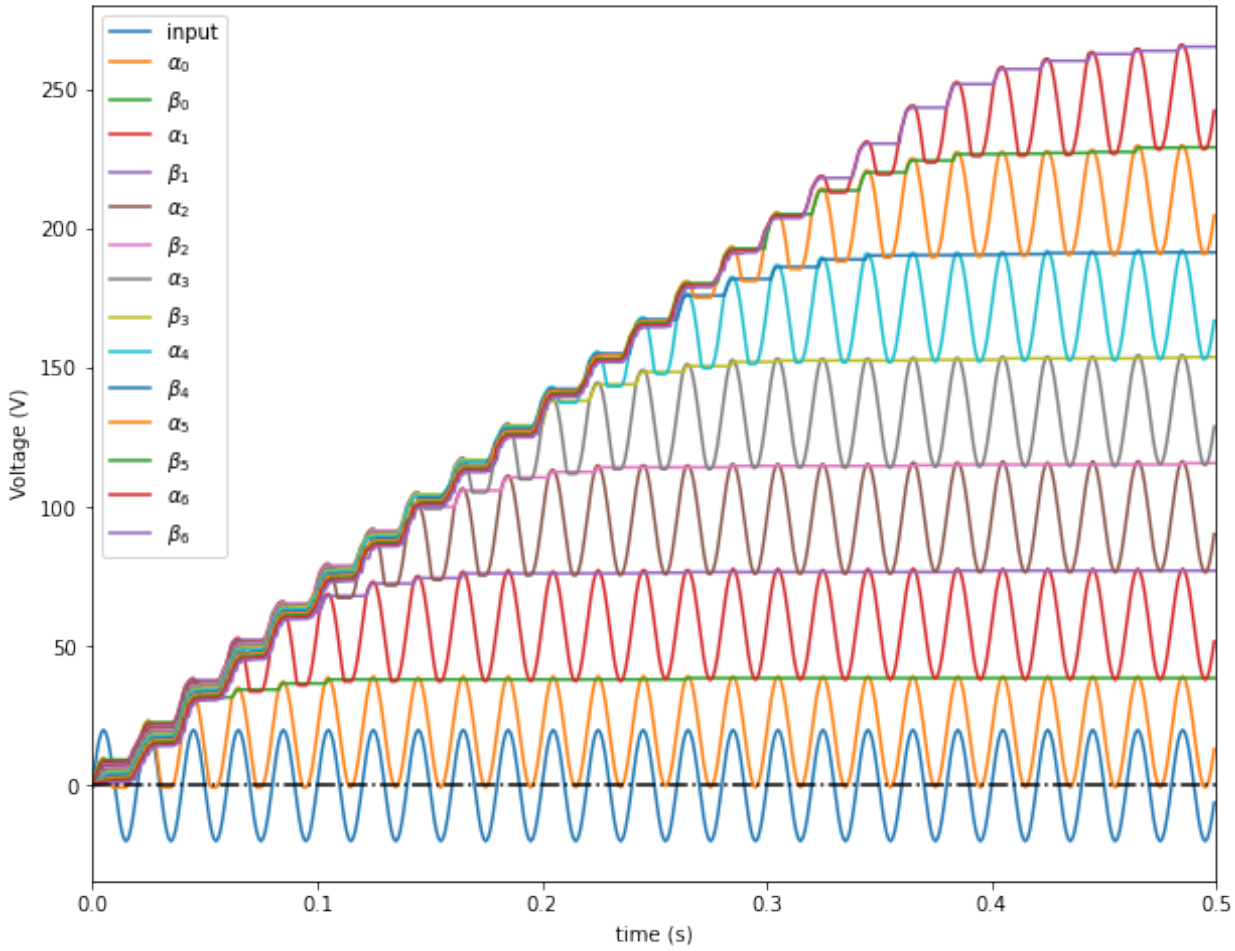


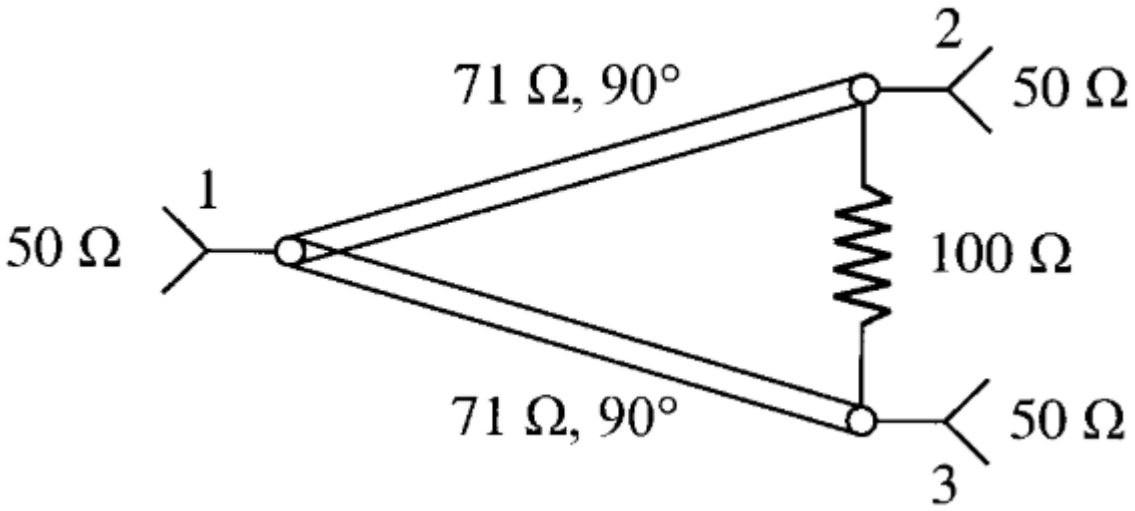

Fig. 3.8: Node voltages of a capacitive Voltage upconvertor comprising 7 stages

CHAPTER

FOUR

# WILKINSON POWER DIVIDER

In this notebook we create a Wilkinson power divider, which splits an input signal into two equals phase output signals. Theoretical results about this circuit are exposed in reference [1]. Here we will reproduce the ideal circuit illustrated below and discussed in reference [2]. In this example, the circuit is designed to operate at 1 GHz.




- [1] P. Hallbjörner, Microw. Opt. Technol. Lett. 38, 99 (2003).
- [2] Microwaves 101: "Wilkinson Power Splitters"

The circuit setup can be checked by visualizing the circuit graph (this requires the python package `networkx` to be available).

Let's look to the scattering parameters of the circuit:

## 4.1 Currents and Voltages

Is is possible to calculate currents and voltages at the Circuit's internals ports. However, if you try with this specific example, one obtains:

This situation is "normal", in the sense that the voltages and currents calculation methods does not support the case of more than 2 ports are connected together, which is the case in this example, as we have defined the connection list:

```
connections = [
            [(port1, 0), (branch1, 0), (branch2, 0)],
```

(continues on next page)

(continued from previous page)

```
            [(port2, 0), (branch1, 1), (resistor, 0)],
            [(port3, 0), (branch2, 1), (resistor, 1)]
        ]
```

However, note that the voltages and currents calculations at external ports works:

But there is hope! It is possible to calculate the internal voltages and currents of the circuit using intermediate splitting Networks. In our case, one needs three “T” Networks and to make only pair of connections:

The resulting graph is a bit more stuffed:

But the results are the same:

And this time one can calculate internal voltages and currents:

You will find more details on voltages and currents calculation on the dedicated example.

# Part III

# References

CHAPTER

FIVE

# REFERENCES

# Part IV

# Overzicht