Hardware Memo 2A

Paging Device Signal Names

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DEFINITIONS OF SIGNAL NAMES IN THE PAGING DEVICE

A 17-25 - Outputs of the sixteen register A-memory. These nine bits are the extended page number (for a 19-bit address) for the virtual page matched by the associative memory.

ACCØ, ACC1 - the two condition code bits for the page matched by the A memory. These determine the permissible access types (ØØ- no access, Ø1 - read only, 1Ø - read write first, 11 - Read/Write).

ACCOK - This signal is high when the protection bits for the page matched in the A-memory, or Associative memory, indicate theat the current reference is legal.

ACF - This level indicates that the current memory reference is in an execute relocated instruction and the MA is addressing locations zero through 17. The location to be referenced is pointed to by the AC pointer (ACP).

ACF RQ - This signal is a pulse which sets the request cycle flip-flop during ACF memory references. It is delayed from the normal time for setting the MC RQ FF to allow time for the adder output to develop.

ACK - This signal is a pulse coincident with the memory acknowledge pulse on the memory buss.

ACP 17 through 35 - This register contains the address where the 16-word block of AC's is to be referenced during execute-relocate instruction.

AD 17 through 35 - This is the output of the adder which produces the address to reference the page table during a page word reload cycle, produces the address of the block of AC's during execute-relocate instruction, and also produces the address of the block of eight words that the status information of the paging device is read from or stored into.

ADR NG - This level indicates that the page mapping information is not contained in either the A or B or C associative memories.

AFND - This indicates that the current address is contained in one of the sixteen associative registers of the A memory.

AKM - indicates that neither the B or C memory keys match and the reloaded page word should be put in the A memory.

AMX 1Ø through 35 - This is an output of a four-way mulitplexer which selects among one of the three DBR's or the AC pointer to be fed into the adder.

ARØM-AR15M - This signal is low (ground) for the associative register in the A memory that matches the current virtual page. It is used to develop the X-Y select information.

ARØCLR-AR15CLR - pulse which loads the match portion of the associative register (Ø-15) with the address on the VMA lines. Occurs during reload of a single associative register with page table information. Also occurs during a rest SW instruction (LPM or SPW with AC11 a one) and changes all the Fill bits to a zero.

ASEL - This level indicates that the address mixer is to be gated from the output of the A memory.

ASELX - This is the same signal as the ASEL but separately buffered and drives boards one through five.

AT6 - This is a time pulse from the processor which is used to indicate that during an execute relocate instruction that references after this time pulse are to be relocated. It occurs at the end of the processor's effective address cycle.

AXØ-AX3 - outputs of the select drivers for the memory portion of the A memory. Any one of these lines high indicates that an A memory natch has been made (only one should be high).

B17-25, BCCØ, BCC1 - outputs of the B memory, corresponding to real MA bits 17-25 and condition bits Ø, 1.

BCCOK - This is similar to the ACCOK and indicates that the B memory protection bits are OK for the current memory cycle.

BIT Ø through 35 - This is the output of the A input multiplexer which is used to select each of the 8 words in the state block which is stored into memory during the store state word instruction.

BK 7 to BK 11 - These are the bits which are the key for the B memory which identify the area in virtual memory that the B memory obtains page entries for.

BKM - This indicates that the B key is matched with the current address.

BMT - This indicates that the associative register in the B meory currently addressed is not empty.

BSEL - This indicates that the MA mixer gates from the output of the B memory.

BSELX - This is the same as BSEL but buffered and drives the boards 1 through five.

BVMA 18 through 35 - These are the MA lines from the processor which are buffered and in general are used to drive less speed-critical logic.

C 17-25, CCCØ, CCC1 - outputs of the C memory corresponding to B memory.

CC0, CC1 - outputs of three input multiplexers that reflect the condition bits Ø, 1 of the currently active memory (A, B, or C).

CCCOK - This indicates that the protection bits of the C memory are OK for the current memory reference.

CK 12 through 16 - These bits are the key for the C memory which indicate which location in virtual memory the C memory associates for. CK 12 is a one for user pages and CK 13-16 determine the 16K block.

CKM - This indicates that the C key matches the current address.

CLRAM, CLRBM, CLRCM - a pulse occurring during the initial part of the page word fetch(APR ACC) that clears the old entry in corresponding 16-word memory.

CLRBC - This level is high during a reset SW (AC11=1) instruction and is used to set the BMT and CMT bits. The select lines of the B, C memory are driven during LPM instructions to select a pair of locations during each of the eight fetches the instruction generates.

CMB - This level clears the memory buffer in the paging device.

CMT - This level indicates that the C memory associative register currently addressed is not empty.

COUNT - This is the input pulse to the quantum counter which is a one megahertz pulse train gated by Not PI Hold and Not State Word instruction.

CPB - This indicates that the parity buffer in the processor is to be cleared and is generated at the beginning of every memory cycle that the paging device initiates.

CSEL - This indicates that the MA mixer is to select the output of the C memory.

CSELX - This has the same logical significance as CSEL.

CYCCLR - This signal is the OR of memory acknowledge and MR CLR and is used in general to clear flipflops that are active at the beginning of memory cycles.

DBR1, 17-35 - These are the output bits of the first DBR register.

DBR2, 17-35 - These are the output bits of the second DBR register.

DBR3, 17-35 - The outputs of the third DBR register which points to the location in real memory where the page table associated with that DBR register starts.

DBRL1, D-16 - is associated with the first DBR register and contains the length of the page table.

DBRL2, 1Ø-16 - is associated with the second DBR.

DBRL3, B1Ø-B16 - is associated with the third DBR register.

DSW - This is true during a Store page memory (SPM) instruction. This is used to assert Memory Write requests.

ETØ - This is a time pulse for the processor which is used to initiate the timing chain in the paging device associated with the Execute relocated and State Word instruction.

EX REL A - This is a level from the processor which indicates that the current memory reference is to be relocated. This, combined with the Execute relocated and EXEC references to address above 400,000, is used for the condition to page the current address.

EX TRAP COND - This signal is a signal fron the processor which indicates that the processor is executing a priority interrupt or a UUO.

EX USER - This is a signal from the processor which indicates that the user flipflop is true. This is used to determine whether or not the Execute relocated and the Store State and Load State Word instructions are legal.

EXR - This is one of the status bits of the paging device and indicates whether EXEC references to locations above 400,000 are to be paged or not. It is cleared by the Reset key on the console.

FA Ø9-17 - is the fault address register and contains the page referenced when the last fault occurred. The high order bit is a one for faults to user pages (DBR 1, 2) and zero for EXEC page faults(DBR 3).

FMA MAEN - This is a signal from the processor which indicates that the memory reference is to an AC addressed as memory, i.e., the address is below location 2Ø octal. It is used to inhibit memory references to be started from the paging kludge.

FSTR - This is the fault strobe signal generated whenever an illegal page reference occurs and is used to strobe error conditions into the fault status flipflops and also to initiate the MC Illegal A & R pulse in the processor which abandons the current instruction.

HIGH - a signal which appears on each of the eleven boards separately, tying all the unused inputs on gates to a logical one signal. It is derived from a resistor divider accross +5. If highly confusing failures are occurring it often pays to check to insure that this line hasn't been accidnetally grounded.

IEND - This indicates the end of an instruction (actually the fetch of the next instruction) which is used to terminate the Execute relocated condition.

IFA 1Ø-17 - This is the output of a two-input multiplexer which selects either the memory buffer of the current page address and is loaded into the fault status flipflops and also to initiate the MC address register either during a Load State Word instruction or during a fault.

IMB 1-35 - This is the input to the paging device memory buffer register and comes from DEC to TTL level converters on the memory buss.

IOPC 18-35 - These are the outputs of a two-input multiplexer which is driven from either the memory buffer or the IVMA lines and is used to load the OPC register during a Load State Word instruction, or when the program counter in the processor is being changed (to preserve the state of the old program counter).

IPCF Ø-12 - This is the output of a two-input multiplexer which selects either the input PC flags or the memory buffer and is used to either load the PC flags register from the miscellaneous program counter bits in the left half or from the momory buffer during a Load State Word instruction.

IR 3-12 - These are signals originating in the processor which are the outputs of the instruction register and are used to decode the Execute relocated and the State Word instruction.

IR 1ØX - This indicates that the instruction register contains the instruction somewhere between instruction 1ØØ and 1Ø7.

IR 1XX - This indicates that the instruction register contains instructions somewhere between 1ØØ and 177.

IRSW - This is the decoded State Word instruction (LPM, SPM) which is op code 1Ø2.

IRXCTR - This is the decoded Execute relocated instruction (XCTR) which is op code 1Ø3 .

IUSER - This indicates that the memory reference is a user reference and is true if EX RELA is asserted or during XCTR instruction.

IVMA 17-35 - This is the MA originating from the processor and is generally used to drive things which are speed-sensitive.

JPC 18-35 - This register is Jump Program counter and is loaded from the old program counter when transfers are made and indicates the location of the last transfer. It is only loaded while in user mode.

LDFA, LD JPC)
LDPCF, LDOPC)
LDMAR)
LD QT, LD ST)
LD DBR1)
LD DBR2)
LD DBR3)
LD ACP) - Are pulses generated after the RD RS from memory is received for the appropriate word during an LPM instruction.

LDP - occurs after the read restart pulse after a sufficient length of time has passed for the memory buffer register to have settled.

LD PCFA, B - generated during LPM for word 1 (OPC) and at ITØ and IT1.

LDPW - occurs when the memory restart comes from the memory during a reference that was to load a page table entry into the associative memory.

LDSW - This pulse is true when the read restart comes from the memory during a Load State Word instruction and is used to generate the other load pulses.

MA 18-31=Ø - This signal is derived from the processor and indicates that the processor is addressing one of the accumulator registers Ø-17.

MA 17-35 - is the output of the memory address multiplexer and is the memory address generated by the paging device which is put on the memory buss.

MAI ACK - is the acknowledge pulse from the memory buss.

MAI RD RS - is the read restart pulse from the memory buss.

MAR 15-35 - is the MAR register which is compared against the address and if the MAR conditions is true then an interrupt is generated on the processr. MAR 15 specifies a USER address and MAR 16, 17 specify (ØØ) Always (Ø;) PC fetches (1Ø) WRITE cycles (11) any reference.

MARC - is the pulse which indicates that the current memory cycle met the MAR interrupt conditions.

MBEN - is a level which indicates that the memory cycle currently in progress is for the paging device and is not to affect the registers in the processor.

MBS - is a pulse which indicates that the address acknowledge has been received from the memory during a Write cycle for the paging device and the data should be strobed onto the memory buss. It is sent to the processor to initiate the parity timing chain which eventually sends out MCWR RS on the buss.

MC RD, MC WR - are signals from the processor which are sent on to the memory during actual processor memory references to control the mode of the requested memory cycle. They are also used to check for paging reference violations such as Read Only.

MC RQ PULSE - a pulse from the processor which initiates a memory cycle. May occur during references to Fast meory in which case FMA MA EN is true.

MPX ENB - line which ties the ENB inputs of all the eight-input multiplexers to ground.

MR CLR - a signal occurring at the beginning of every instruction. Initializes the state of many flipflops in the paging device.

MR RST - a signal that occurs when Key Reset is pushed. Resets all other mode-controlling flipflops into a predefined state.

MXØ, 4 -
MYØ, 4 - outputs of the comparator that are high if the inputs are identical. MXØ, MYØ are the high order inputs used to generate MARC.

NSK - is a flipflop which is set at the beginning of instructions and cleared when the program counter is incremented and indicates that a skip is necessary during the abort phase of an Execute relocated instruction to allow the processor to begin execution at the instruction after the Execute relocated.

OPC 18-35 - is the old program counter register.

PA 17-25 - are the outputs of a two-input multiplexer which selects either the left or right half of the memory buss and drives the inputs to the associative registers during a page word memory cycle. It selects either the left or right halfword of the page table depending upon the evenness of oddness of the referenced page.

PC AOS - a signal from the processor which indicates that the program counter has been incremented.

PC RT FM MA - a signal which indicates that an address is being jammed into the right half of the PC and this is used to strobe the JPC register from the OPC register.

PCCØ, PCC1 - the bits corresponding to PA 17-35 which are the outputs of the multiplexer either the left or right half of the page word entry and loaded into the associative register condition code Ø and 1.

PCD - the pure code indication which indicates the processor is referencing a paged address for an instruction is to reference Read Only pages.

PCF - this is the PC fetch flipflop and is set at the beginning of an instruction and cleared after the first memory reference. It indicates that the memory reference is fetching an instruction pointed to by the program counter.

PCF 5-17 - the outputs of register which stores the assorted flags in the left half of the PC word.

PFMEN - a signal developed by the paging box during XCTR instructions. Directs all references for location Ø-17 to memory relocated by the ACP.

PG CLR PB - a pulse sent to the processor to clear the parity buffer at the beginning of every memory cycle.

PG FAC INH - a signal developed by the page IR decoder sent to the processor to assert FAC INH.

PG PC AOS - a signal sent to the processor to increment the PC (see NSK).

PG RD - the output paging device which is given to the memory to indicate a read request is desired.

PG SAC INH - driven from the instruction decoders and indicates that store AC cycles are to be inhibited.

PG ST INH - also driven from the instruction decoders and inhibits the store time cycle of the processor.

PG WR - the signal driven from the paging device which indicates that the memory reference is to be a write cycle.

PIH - a signal from the processor which indicates that there are no PI cycles in progress or currently held.

PIR 9-12 - are the page IR 9-12, and holds the AC field of the current instruction while it is being executed and is decoded for the Execute relocated and the State Word instruction.

PMB Ø-35 is the page memory buffer and is loaded during references for paging entries of a Load State Word instruction

PMCYC - a signal from the paging device to the processor which is used to inhibit the response of the memory sub-routine on the memory buss. It is asserted during page word fetches, State Word instructions and Store time check cycles (ST).

PRFLT - is a signal which indicates that a protection fault is occurring during the memory reference and is used to generate the FSTR pulse.

PR OK - true when the current page is legally referenced. Developed from the condition bits of the page entry.

PURE - is a signal driven from the processor which indicates that the program counter bit pure, bit 7, is true and all instruction references are to be from Read Only pages.

PWNG - true when the current page information is not contained within the bounds specified fpr tje selected DBR.

PW - true during the first part of the memory reference to the page table. Controls the routing of the page number through the adder into the MA output MIXER.

PWC - true during the second part of the page table reference. Controls pulses generated after RD RS. Also gates off the RQ DØ, RQ Dl time pulse to be started over after the page fetch.

PWF - true when fetching page words, executing State Word instruction, or referencing relocated by the AC pointer. Controls the gating of the MA mixer.

PWR - a pulse that sets the MC RQ FF after the page table address is sent to the MA.

PWS - pulse that sets PW FF. Occurs if the current page is not in the associative memory and the page entry does not exceed the length of the appropriate page table.

QOF - pulse that occurs as the quantum counter increments from 777777 to 1,ØØØ,ØØØ.

QT 17-35 - quantum counter register that counts at a 1 MHZ rate. Counting is suppressed when PI is in progress, during Load or Store State word instructions or when overflow has occurred (QT 17=1).

RACK - acknowledge pulse that only occurs during memory cycles for the processor.

RBCØ-3 - The four bit counter that points to the next word in associative memory to be reloaded.

REL - true if any condition for mapping an address is true. User mode references, EXEC references above 4ØØ,ØØØ and XCTR references assert this level.

RELA - REL signal that is inhibited during page references that require selecting the adder input to the MA mixer.

RELC - decodes the condition for mapping XCTR references. If ACl2=1, then read cycles are mapped; ACll=1 implies write cycles.

RQ CYC - flipflop in the paging device that generates RQ CYC level on meory buss. Set by processor references, page word references, State Word references, and AC references recorded by the AC pointer.

RQ ENB - pulse which initiates an RQ CYC for the processor if the contents of the selected associative memory permit this reference.

RQ DØ - pulse that comes true 140 us after the processor request comes on.

RQ D1 - pulse that follows RQ DØ.

RST AR - pulse that clears all associative registers in the A memory. This is done by setting the natch bits to zero during an LPM instruction that specifies reset (AC11=1).

RT1 - a pulse that follows RD RS from the memory. It is used to restart timing chains in the paging box.

SØ, S1 - select lines to the four-input mulitplexer that select DBR1, 2, 3 or the ACP.

SCLR - a clear pulse that terminates SW instruction (LPM, SPM) and ST checks.

SCON - a pulse that restarts the processor at the Store cycle of the current instruction.

SET DBLF)
SET NACC) outputs of gates that decode error conditions
SET PURF) during a memory fault. Used to set bits in
SET ROF) the status register.
SET WRF)

SET MPF - pulse sent to processor which sets the memory protection flag in the processor status register. Eventually causes an interrupt on the processor PI channel.

SRQ - pulse from the processor initiating an ST check. This is done before the store cycle of instructions that store both AC and memory. If the memory reference will cause a page fault, the instruction is aborted before the contents of the AC are destroyed.

ST Ø9-17 - The paging status register.

ST OK - pulse generated after the check for the store cycle is completed. Generates SCOY and SCLR.

ST - flipflop set by SRQ. Starts the RQDØ and RQD1 delays.

SW (A, B, E) - levels true during a State Word instruction (LPM, SPM).

SWCØ-3 - four bit counter. Eight states are used during a state word instruction to address the registers in the paging device.

SWC7 - level ture during the last reference of an SW instruction.

SWD - pulse at end of SW instruction. Generates SCLR and SCON.

USER - level used to match with the A memory. Indicates reference uses DBR1 or DBR2.

VMA 18-25 - Buffered version of MA from processor.

VMASEL - level which lselects an unmapped address for input to the MA mixer.

XCTR TØ - pulse at the beginning of XCTR execution .

XCTR - flipflop set by XCTR TØ and cleared at the beginning of next instruction.

XREL - flipflop set by AT6 if XCTR is set. Enables mapping of references generated after the effective address cycle of the instruction executed.