Hardware Memo 3

PDP-6/10 MAGIC SWITCHES

3/3/70

1A   RIM SUBR: Up: Processor references to Ø-17 go to memory
                      system.
                 Down: References go to Fast memory (except when
                      in Read In mode)
                 (In general, this switch should always be down
                 unless PDP-6 Fast memory is inoperative.)

1B   DEC MEMORY: Up: MA17(Ø) line is Gnd when special mode FF
                      is off.
                 Down: MA17(Ø) is high (-3v.) Special mode FF
                      complements state of MA17(Ø) line.

2A   PROCESSOR SELECT: Up: Hardwired devices are connected to
                      PDP-1Ø.
                 Down: Hardwired devices are connected to PDP-6
                 (PDP-6 is PB)

2B   IO RESET SELECT: Up: IO reset driven from PDP-1Ø
                 Down: IO reset from PDP-6

3A   P1 ENB: Up: Processor 1 enabled (DISK)

3B   P1 MA17:   Up; MA17(1) must be Gnd for selection
                 Down: MA17(Ø) must be Gnd for selection

3C   P1 MA21:   Up: MA21 must be a "one" for selection
                 Down: MA21 must be a "zero" for selection

4A   P2 ENB: Up: Processor 2 enabled (PDP-1Ø)

4B   P2 MA17:   Up: MA17 must be a "zero"
                 Down: MA17 must be a "one"

4C   P2 MA21:   Up: MA21 must be a "one"
                 Down: MA21 must be a "zero"

5A   P3 ENB: Up: Processor 3 enabled (PDP-6)

5B   P3 MA17:   Up: MA17(1) must be Gnd
                 Down: MA17(Ø) must be Gnd

5C   P3 MA21:   Up: MA21 must be a "one"
                 Down: MA21 must be a "zero"

6A   PØ ADDRESS MODE: Up: MA17(Ø) Gnd 16K-256K
         (PDP-6)   MA17(Ø) -3v. 0-16K
                 Down: MA17(Ø) Gnd 16K-256K
                      MA17(Ø) -3v. 0-256K

6B   P1 ADDRESS MODE: Up: MA17($\emptyset$) Gnd   0-256K
                                       MA17($\emptyset$) -3v.
                 Down: MA17($\emptyset$) Gnd   16K-256K
                                         MA17($\emptyset$) -3v.   0-16K

6C   P2 ADDRESS MODE: Up: MA17($\emptyset$) Gnd   16K-256K
                                         MA17($\emptyset$) -3v.   0-16K
                 Down: MA17($\emptyset$) Gnd   16K-256K
                                       MA17($\emptyset$) -3v.   0-256K

7A   PDP-1$\emptyset$ MA17:   Left: MA17 normally a "one"
                      Right: MA17 normally a "zero"
                (MA17($\emptyset$) -3v., MA17(1) Gnd)

8A   DISC CONTROL: F1P Gnd, F1S -3v.
                DISC MA17 is a "one"
           F1P -3v. and F1S Gnd
                DISC MA17 is a "zero"

	P$\emptyset$	P1	P2	P3	
MOBY MEMORY	PDP-6	PDP-1$\emptyset$	DISC		P2 is highest priority
DEC 16K		DISC	PDP-1$\emptyset$	PDP-6	P$\emptyset$ is highest priority
AMPEX 16K	PDP-1$\emptyset$	DISC			P$\emptyset$ is highest priority

9A   Disk enable for Ampex Memory

9B-9F   High order bits of MA for responding to disk
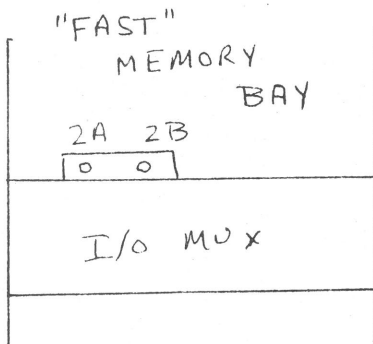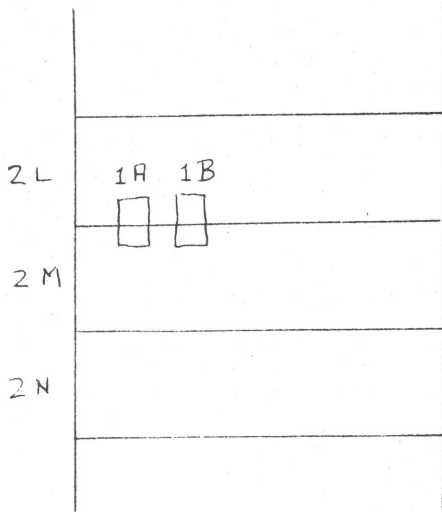
10A   PDP-1$\emptyset$ enable for Ampex Memory

10B-10F   High order bits of MA for responding to PDP-1$\emptyset$
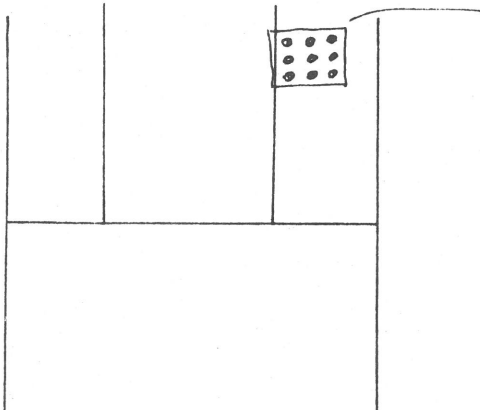
11A   Mass Memory enable, Port $\emptyset$, PDP-6

11B   Mass Memory enable, Port 1, PDP-1$\emptyset$
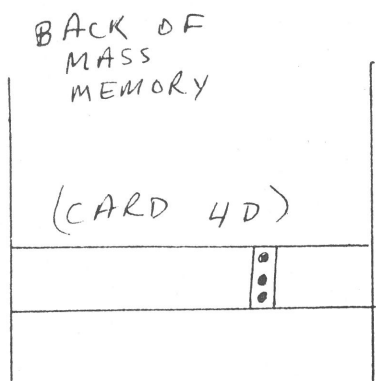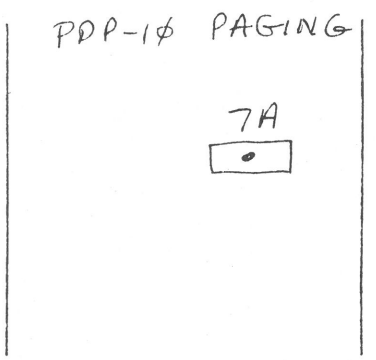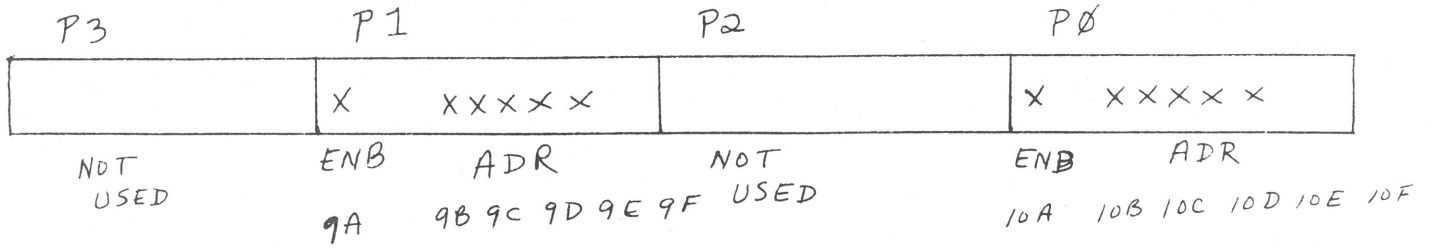
11C   Mass Memory enable, Port 2, DISK

PDP-6 PROCESSOR

2L 1A 1B

2M

2N

"FAST"
  MEMORY
        BAY

2A   2B

I/O MUX

DEC 16K MEMORY

3A   3B   3C
4A   4B   4C
5A   5B   5C

BACK OF
MASS
MEMORY

4

(CARD 4D)

6A
6B
6C

DISK CONTROL

8A

PDP-10 PAGING

7A

Ampex Memory Interface

P3	P1		P2	PØ	
	X	X X X X X		X	X X X X X

NOT USED   ENB   ADR   NOT USED   ENB   ADR

9A   9B 9C 9D 9E 9F   10A   10B 10C 10D 10E 10F
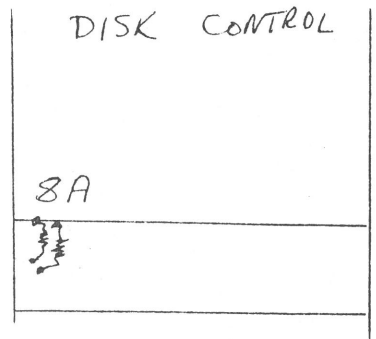
Mass Memory (inside right front door)
Port enable switches

X   X X
P_0 P_1 P_2

PDP-6   DISK
   PDP-10

11A   11B   11C

NORMAL SWITCH CONFIGURATION

To run TS on 1Ø, 16K non-TS on 6 (with DEC memory)
   Use Ampex Memory

1)   1A down
     1B up

2)   2A up
     2B up

3)   3A down, 3B, 3C irrelevant, may as well be down

4)   4A up
     4B up
     4C up

5)   5A up
     5B down
     5C down

6)   6A down (doesn't really matter)
     6B down
     6C down

7)   7A left

8)   F1S = -3 = resistor
     F1P - Gnd

9)   9A up
     9B, 9C, 9D, 9E down
     9F up

10)   10A up
      10B, 10C, 10D, 10E down
      10F up

11)   11A) down
      11B) up
      11C) up

To time share on 6, 1Ø out of TS

(differences from normal
underlined)

1) 1A down
    <u>1B down</u>

2) <u>2A down</u>
    <u>2B down</u>

3) 3A down; 3B, 3C irrelevant, may as well be down

4) 4A up
    <u>4B down</u>
    <u>4C down</u>

5) 5A up
    5B down
    5C down

6) 6A down
    6B down (doesn't really matter)
    6C down

7) <u>7A right</u>

8) <u>F1S = Gnd</u>
    <u>F1P = resistor = -3</u>

9) 9A down
    9B, etc. doesn't matter

10) 10A up for 32K (in 1Ø), down otherwise
    10B up for 32K, doesn't matter otherwise
    10C, D, E, F <u>down</u> for 32K, doesn't matter otherwise

<u>Also</u> remember to use PDP-6 ITS