Hardware Memo 10
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ARPA Network Interface

Before coming to me with questions concerning this memo one should read either BBN Report #1822, Specifications for the Interconnection of a Host and an IMP or my thesis, DSK:F;TH TJ6ED.

The AI IMP Interface lives in the bay just to the left of GAMMA Bay marked "INCREMENTAL DISPLAY". It is composed of one Augat board, a row of DEC sockets, and a lamp panel, all near the top of the bay. There are the standard power switches for the row of DEC sockets which control the power to the level converters which are plugged into the sockets along with the I-O Buss and the cable to the IMP. These do not use standard DEC voltages and one should not arbitrarily plug in DEC cards in this rack. There is no margin supply for these voltages, so up is off. If necessary, the device may be safely powered down and up with the system running if the network is not being used. This is done by turning the negative voltages (first and third switches from the bottom) off first and on last by a margin of a few seconds. There are two toggle switches on the mounting frame for the Augat board. The upper of these is power

for the Augat board, up is off. The other toggle switch operates on an angle and is to select which processor the device is assigned to, up-right being the time-sharing machine and down-left being the non-time-sharing machine.

The Mathlab interface is located in the bottom of the right-most of the two bays housing their disk controller. It is identical to the AI unit except as described in the rest of this paragraph. It is much more neatly wired. It has no lights at the time of this writing. There is no processor select switch. Power to the Augat board cannot be shut off locally. The four switches on the mounting frame for the Augat board don't do anything. It is connected to a different computer. It is connected to a different IMP port (AI is Host 206, Mathlab is Host 306).

The device number is 460. Both the transmitter (toward the IMP) and the receiver (from the IMP) have independently selectable 36 and 32 bit modes. In 36 bit mode the entire word is used on DATAI and DATAO. In 32 bit mode the transmitter ignores the low four bits of the word sent in a DATAO. The receiver, in 32 bit mode, only fills the high order 32 bits with data and makes the low four bits zero. No data is lost or added; the next bit transferred by the transmitter after bit-31 of a word is bit-0 of the next word if it is in 32 bit mode, and the next bit received by the receiver after the one that it puts in bit-31 of a word is placed in bit-0 of the next word.

When a DATAO is done the word sent from the processor is stored in the device, the TBUSY flag is set, the TDONE flag is cleared, and the word starts to be sent to the IMP serially, bit-0 first. When the number

of bits specified by the mode (36 or 32) have been sent: the transmission process stops, TBUSY is cleared, TDONE is set, and the LHW flag is cleared; except that if the LHW flag was set then the last bit sent was marked as the last bit in the message. (LHW should be set with a CONO just before the last word in a message is DATAOed.)

When a DATAI is done, a 36 bit word stored in the receiver is sent to the processor, the LIW flag is cleared, the RBUSY flag is set, and the RDONE flag is cleared. The receiver then lets the IMP send it bits and puts them into its 36 bit storage register starting with bit-0 until either it has received the number of bits specified by the mode or the IMP marks one of the bits as the last bit in a message. The receiver then stops the IMP from sending bits, fills out the rest of its storage register with zeroes, clears RBUSY, and sets RDONE. If the IMP marks a bit as the last bit in the message the receiver sets LIW.

The IMP asserts a condition known as IMP Ready, which, if it ever goes away, is reason for discarding any messages currently in progress in either direction, since in normal operation it means that the IMP has crashed. If this flag ever goes away, IMP Error, a flag internal to the interface is set. IMP Error is cleared by setting Interrupt on IMP Ready. The interface maintains a flag called Host Error, the inversion of which is called Host Ready and is used to send similar information to the IMP. This signal is sent to the IMP through a relay so one should wait a few milliseconds for the contacts to close and stop bounceing after clearing Host Error before sending any messages. Host Error is set if a CONI to the device had not been done in the last 3 to 5 seconds and

attempts to clear Host Error will fail unless a CONI has been done within the appropriate time.

The device will interrupt on its assigned channel if TDONE is 1, if RDONE is 1, if Host Error is 1 and DIHE is 0, if IMP Error is 1 and IIR is 0, or if IMP Ready is 1 and IIR is 1. Additionally, the AI and Mathlab PDP-10s are equipped with a PI Channel 1 multiplexing feature. If assigned to Channel 1 of such a processor the interface will interrupt on Pseudo PI Channel 4 (location 70) instead of normal PI Channel 1 if RDONE is 1 and LIW is 0, and on Pseudo PI Channel 5 (location 72) if TDONE is 1.

Various flags internal to the device may be examined by doing a CONI. Here is a table of bits and the flags or information that they represent:

Bit	Information
20	LIW
21	DIHE, Don't Interrupt on Host Error
22	HR, Host Ready
23	HE, Host Error
24	IIR, Interrupt on IMP Ready if 1, Error if 0
25	IR, IMP Ready
26	IE, IMP Error
27	TBUSY
28	T32, Transmitter in 32 bit mode if 1, 36 bit mode if 0
29	TDONE
30	RBUSY
31	R32, Receiver in 32 bit mode if 1, 36 bit mode if 0
32	RDONE
33-35	PIA, Number of the PI Channel to which the device is assigned

The status of the device may also be affected by a CONO. Here is a table of what bits do what:

Bit	Action
19	Set LHW if 1
21	DIHE copied from this bit
23	Clear HE
24	IIR copied from this bit
26	Set TDONE
27	Clear T32 (transmitter enters 36 bit mode)
28	Set T32 (transmitter enters 32 bit mode)
29	Clear TDONE
30	Clear R32 (receiver enters 36 bit mode)
31	Set R32 (receiver enters 32 bit mode)
32	Clear RDONE
33-35	PIA copied from these bits