

Laboratório de Sistemas Digitais para Computação

Aula 2

Sumário

- Quartus II
 - Criação de projetos
 - Desenvolvimento dos módulos (Verilog HDL)
 - Importação do arquivo de atribuição dos pinos (DE2 pin assignments)
- Modelsim
 - Simulação dos módulos
- Quartus II
 - Comunicação com a placa

Quartus II

- Software para síntese, isto é, geração de um circuito digital.
- Software usado para comunicação com o equipamento: placa DE2 que contém um FPGA.

Quartus II: Criação do projeto

Detalhes importantes:

1. Escolha do diretório do projeto: Sempre crie uma nova pasta.
2. Seleção do dispositivo: Família Cyclone II e modelo EP2C35F672C6.
3. Simulador ModelSim-Altera, Verilog HDL

Windows XP – Parallels Desktop

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units Revisions

Tasks Flow: Compilation Customize...

Task

- Compile Design
 - Analysis & Synthesis
 - Edit Settings
 - View Report
 - Analysis & Elaboration
 - Partition Merge
 - Netlist Viewers

QUARTUS® SOFTWARE v13.0:
BOOST PERFORMANCE WITH THE WORLD'S FASTEST FPGAS
BOOST PRODUCTIVITY WITH 25% FASTER COMPILATION
[Download Free 30-Day Trial >](#)
MEASURABLE ADVANTAGE™

ALTERA®

QUARTUS® II

Version 12.1

Download New Software Release

Documentation

All

Type ID Message

Messages

System Processing

0% 00:00:00

Start Quartus II 32-bit

12:39 PM

Windows XP – Parallels Desktop

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help Search altera.com

Project Navigator

Compilation Hierarchy

New Project Wizard

Introduction

The New Project Wizard helps you create a new project and preliminary project settings, including the following:

- Project name and directory
- Name of the top-level design entity
- Project files and libraries
- Target device family and device
- EDA tool settings

You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.

Tasks

Flow: Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Edit Settings
 - View Report
 - Analysis & Elaboration
 - Partition Merge
 - Netlist Viewers

All <<Search>>

Type	ID	Message
------	----	---------

Don't show me this introduction again

< Back Next > Finish Cancel Help

Download New Software Release

Documentation

Messages

System Processing

0% 00:00:00

Start Quartus II 32-bit

12:39 PM

Windows XP – Parallels Desktop

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units Revisions

Tasks

Flow: Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Edit Settings
 - View Report
 - Analysis & Elaboration
 - Partition Merge
 - Netlist Viewers

All <<Search>>

Type	ID	Message

Messages

System Processing

New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?
\\psf\\Home\\Desktop\\aula2

What is the name of this project?
aula2

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
aula2

Use Existing Project Settings...

< Back Next > Finish Cancel Help

Download New Software Release

Documentation

Start

Quartus II 32-bit

0% 00:00:00

12:40 PM

Windows XP – Parallels Desktop

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units Revisions

Tasks

Flow: Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Edit Settings
 - View Report
 - Analysis & Elaboration
 - Partition Merge
 - Netlist Viewers

All <<Search>>

Type ID Message

Messages

System Processing

New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?
\\psf\\Home\\Desktop\\aula2

What is the name of this project?
aula2

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
aula2

Use Existing Project Settings...

Quartus II

Directory "\\psf\\Home\\Desktop\\aula2" does not exist. Do you want to create it?

Yes No

< Back Next > Finish Cancel Help

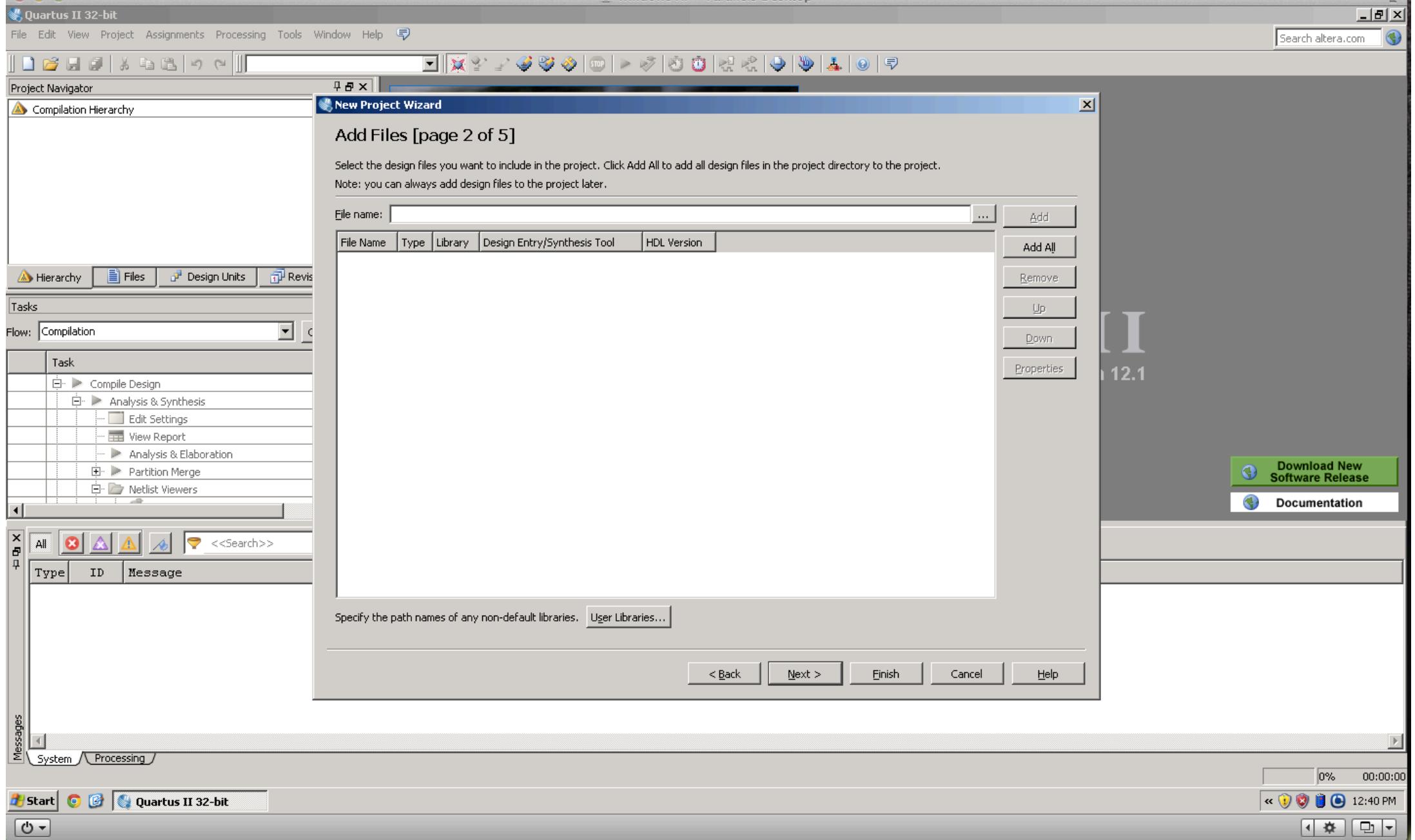
Download New Software Release

Documentation

Start Quartus II 32-bit Quartus II

0% 00:00:00

12:40 PM



File Edit View Project Assignments Processing Tools Window Help



Project Navigator

Compilation Hierarchy

Hierarchy

Files

Design Units

Revis

Tasks

Flow: Compilation

Task

Compile Design

- Analysis & Synthesis
 - Edit Settings
 - View Report
- Analysis & Elaboration
- Partition Merge
- Netlist Viewers



Type

ID

Message

Messages

System Processing

0% 00:00:00

Start Quartus II 32-bit

< 12:40 PM

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone II

Devices: All

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter:

 Show advanced devices HardCopy compatible only

Target device

 Auto device selected by the Fitter Specific device selected in 'Available devices' list Other: n/a

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	G
EP2C35F484C7	1.2V	33216	322	483840	70	4	16
EP2C35F484C8	1.2V	33216	322	483840	70	4	16
EP2C35F484I8	1.2V	33216	322	483840	70	4	16
EP2C35F672C6	1.2V	33216	475	483840	70	4	16
EP2C35F672C7	1.2V	33216	475	483840	70	4	16
EP2C35F672C8	1.2V	33216	475	483840	70	4	16
EP2C35F672I8	1.2V	33216	475	483840	70	4	16

Companion device

HardCopy:

 Limit DSP & RAM to HardCopy device resources

< Back

Next >

Finish

Cancel

Help

Download New Software Release

Documentation

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units Revisions

Tasks

Flow: Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Edit Settings
 - View Report
 - Analysis & Elaboration
 - Partition Merge
 - Netlist Viewers

All <<Search>>

Type	ID	Message
------	----	---------

Messages

System Processing

0% 00:00:00

12:40 PM

New Project Wizard

EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	Verilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

Download New Software Release

Documentation

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units Revisions

Tasks

Flow: Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Edit Settings
 - View Report
 - Analysis & Elaboration
 - Partition Merge
 - Netlist Viewers

All <<Search>>

Type	ID	Message

Messages

System Processing

0% 00:00:00

12:40 PM

New Project Wizard

Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory: \\psf\Home\Desktop\aula2

Project name: aula2

Top-level design entity: aula2

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: Cyclone II

Device: EP2C35F672C6

EDA tools:

Design entry/synthesis: <None> (<None>)

Simulation: ModelSim-Altera (Verilog HDL)

Timing analysis: 0

Operating conditions:

Core voltage: 1.2V

Junction temperature range: 0-85 °C

< Back Next > Finish Cancel Help

Download New Software Release

Documentation

Quartus II

- Desenvolvimento do projeto



QUARTUS® II SOFTWARE v13.0:
BOOST PERFORMANCE WITH THE WORLD'S FASTEST FPGAS
BOOST PRODUCTIVITY WITH 25% FASTER COMPILATION

[Download Free 30-Day Trial >](#)

MEASURABLE ADVANTAGE™



ALTEA®

QUARTUS® II

Version 12.1

[Download New Software Release](#)

[Documentation](#)



Tasks

Flow: Compilation

Customize...

Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers

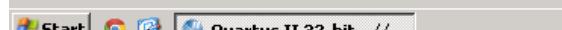


Type ID Message



System Processing

0% 00:00:00



12:40 PM



Windows XP – Parallels Desktop

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

File Edit View Project Assignments Processing Tools Window Help

New... Ctrl+N

Open... Ctrl+O

Close Ctrl+F4

New Project Wizard...

Open Project... Ctrl+J

Save Project

Close Project

Save Ctrl+S

Save As...

Save All Ctrl+Shift+S

File Properties...

Create / Update

Export...

Convert Programming Files...

Page Setup...

Print Preview

Print... Ctrl+P

Recent Files

Recent Projects

Exit Alt+F4

Windows XP – Parallels Desktop

Search altera.com

ala2

QUARTUS® II SOFTWARE v13.0:
BOOST PERFORMANCE WITH THE WORLD'S FASTEST FPGAS
BOOST PRODUCTIVITY WITH 25% FASTER COMPILATION
[Download Free 30-Day Trial >](#)
MEASURABLE ADVANTAGE™

ALTEA

QUARTUS® II

Version 12.1

Download New Software Release

Documentation

All

<<Search>>

Type ID Message

Creates a new file

System Processing

Start Quartus II 32-bit - //...

0% 00:00:00

12:40 PM

Messages

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

Windows XP - Parallels Desktop

File Edit View Project Assignments Processing Tools Window Help

Search altera.com



Project Navigator

Entity

Cyclone II: EP2C35F672C6

aula2

Hierarchy

Files

Design Units

Revisions

Tasks

Flow: Compilation

Customize...

Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers

All <<Search>>

Type ID Message

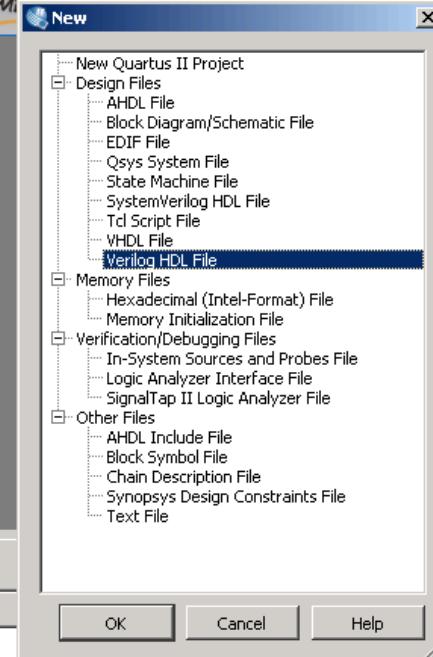
Messages

System Processing

0% 00:00:00

Start Quartus II 32-bit - //...

12:40 PM



ALTERA®

QUARTUS® II
Version 12.1

Download New Software Release

Documentation

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

Search altera.com

File Edit View Project Assignments Processing Tools Window Help



Project Navigator

Entity

Cyclone II: EP2C35F672C6

aula2

Hierarchy

Files

Design Units

Revisions

Tasks

Flow: Compilation

Customize...

Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers

Verilog1.v*

```
1 module aula1_0 (x1, x2, f);
2     input x1, x2;
3     output f;
4     assign f = x1 & ~x2 | ~x1 & x2;
5 endmodule
6
7
8 module aula1(SW, LEDR);
9     input [17:0] SW;
10    output [17:0] LEDR;
11
12 aula1_0 a1 ( SW[0] , SW[1] , LEDR[0]);
13
14 endmodule
```



All Type ID Message

Type	ID	Message

Messages System Processing

Ln 7 Col 1

Verilog HDL File

0% 00:00:00

Start Quartus II 32-bit - //...

12:41 PM



Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity Cyclone II: EP2C35F672C6 aula2

Stop Processing Ctrl+Shift+C

Start Compilation Ctrl+L

Analyze Current File Start Update Memory Initialization File

Compilation Report Ctrl+R Dynamic Synthesis Report

PowerPlay Power Analyzer Tool SSN Analyzer Tool

Verilog1.v*

```

module aula1_0 (x1, x2, f);
    input x1, x2;
    output f;
    assign f = x1 & ~x2 | ~x1 & x2;
endmodule

module aula1(SW, LEDR);
    input [17:0] SW;
    output [17:0] LEDR;
    aula1_0 a1 ( SW[0] , SW[1] , LEDR[0]);
endmodule

```

Hierarchy Files Design Units Revisions

Tasks Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers

All <<Search>>

Type	ID	Message
System Processing Starts a new compilation 0% 00:00:00		

Start Quartus II 32-bit - //... 12:41 PM

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

File Edit View Project Assignments Processing Tools Window Help

Search altera.com



Project Navigator

- Entity
 - Cyclone II: EP2C35F672C6
 - aula2

Hierarchy **Files** **Design Units** **Revisions**

Tasks

Flow: Compilation **Customize...**

Task	Progress
Compile Design	9%
Analysis & Synthesis	4%
Edit Settings	
View Report	
Analysis & Elaboration	
Partition Merge	
Netlist Viewers	
RTL Viewer	
State Machine Viewer	
Technology Map Viewer (Post-Mapping)	

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- + Analysis & Synthesis

Flow Summary

Parameter	Value
Flow Status	In progress - Thu Oct 17 12:41:59 2013
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	aula2
Top-level Entity Name	aula2
Family	Cyclone II

Messages

Type	ID	Message
Info	12021	Found 2 design units, including 2 entities, in source file aula2.v
Error	12007	Top-level design entity "aula2" is undefined
Error		Quartus II 32-bit Analysis & Synthesis was unsuccessful. 1 error, 0 warnings

System Processing (7)

9% 00:00:04

Start Quartus II 32-bit - //... 12:42 PM

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

File Edit View Project Assignments Processing Tools Window Help

Search altera.com



Project Navigator

Entity

Cyclone II: EP2C35F672C6

aula2



Hierarchy



Files



Design Units



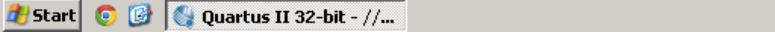
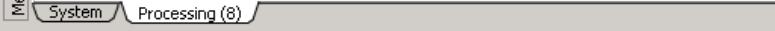
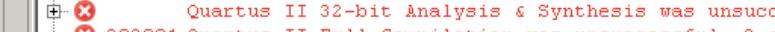
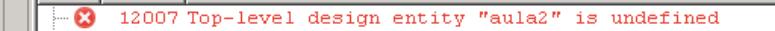
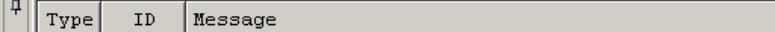
Revisions

Tasks

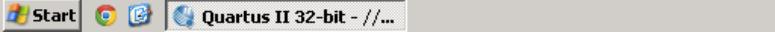
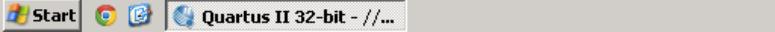
Flow: Compilation

Customize...

Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
RTL Viewer
State Machine Viewer
Technology Map Viewer (Post-Mapping)



All



<<Search>>

Type

ID

Message

- 12007 Top-level design entity "aula2" is undefined
- Quartus II 32-bit Analysis & Synthesis was unsuccessful. 1 error, 0 warnings
- 293001 Quartus II Full Compilation was unsuccessful. 3 errors, 0 warnings



```

Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Dynamic Synthesis Report
PowerPlay Power Analyzer Tool
SSN Analyzer Tool

aula2.v
aula1_0 (x1, x2, f);
put x1, x2;
tput f;
sign f = x1 & ~x2 | ~x1 & x2;
dmodule

dmodule aula2 (SW, LEDR);
input [17:0] SW;
output [17:0] LEDR;

aula1_0 a1 ( SW[0] , SW[1] , LEDR[0]);
endmodule

```

9

10

11

12

13

14

Starts a new compilation

9% 00:00:04

Quartus II 32-bit - //...

12:42 PM





Project Navigator

Entity

- Cyclone II: EP2C35F672C6
- aula2

Hierarchy **Files** **Design Units** **Revisions**

Tasks

Flow: Compilation **Customize...**

Task	Tim
39% Compile Design	00:00:00
✓ Analysis & Synthesis	00:00:00
98% Filter (Place & Route)	00:00:00
0% Assembler (Generate programming files)	00:00:00
0% TimeQuest Timing Analysis	00:00:00
0% EDA Netlist Writer	00:00:00
Program Device (Open Programmer)	

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- + Analysis & Synthesis
- + Filter

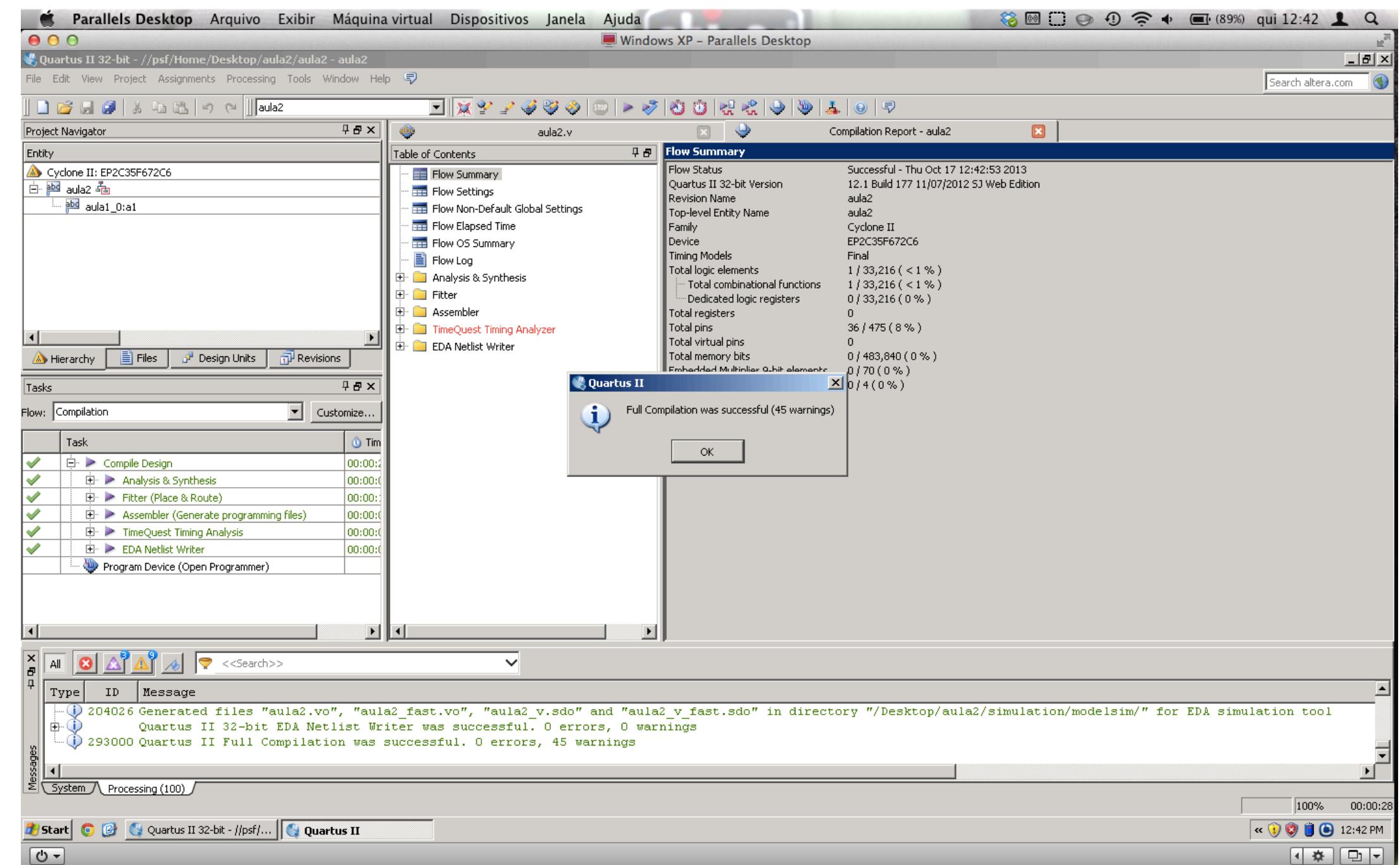
Flow Summary

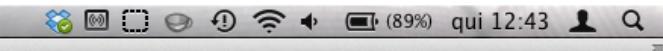
Flow Status	In progress - Thu Oct 17 12:42:32 2013
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	aula2
Top-level Entity Name	aula2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	1
Total combinational functions	1
Dedicated logic registers	0
Total registers	0
Total pins	36
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Messages

Type	ID	Message
Info	306005	Delay annotation completed successfully
Info	306004	Started post-fitting delay annotation
Info	306005	Delay annotation completed successfully

System Processing (49) 39% 00:00:12 12:42 PM





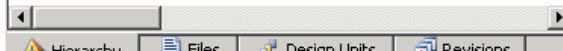
Project Navigator

Entity

Cyclone II: EP2C35F672C6

aula2

aula1_0:a1



Tasks

Flow: Compilation

Customize...

	Task	Tim
✓	Compile Design	00:00:2
✓	Analysis & Synthesis	00:00:0
✓	Filter (Place & Route)	00:00:0
✓	Assembler (Generate programming files)	00:00:0
✓	TimeQuest Timing Analysis	00:00:0
✓	EDA Netlist Writer	00:00:0
	Program Device (Open Programmer)	

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- + Analysis & Synthesis
- + Filter
- + Assembler
- + TimeQuest Timing Analyzer
- + EDA Netlist Writer

Flow Summary

Flow Status	Successful - Thu Oct 17 12:42:53 2013
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	aula2
Top-level Entity Name	aula2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	1 / 33,216 (< 1 %)
Total combinational functions	1 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	36 / 475 (8 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier Q-bit elements	0 / 70 (0 %)
Q-bit elements	0 / 4 (0 %)

Quartus II

Full Compilation was successful (45 warnings)

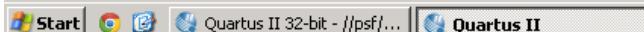
OK



Type	ID	Message
Info	204026	Generated files "aula2.vo", "aula2_fast.vo", "aula2_v.sdo" and "aula2_v_fast.sdo" in directory "/Desktop/aula2/simulation/modelsim/" for EDA simulation tool
Info		Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
Info	293000	Quartus II Full Compilation was successful. 0 errors, 45 warnings

System Processing (100)

100% 00:00:28



12:43 PM



m moodle.cefetmg.br/course/view.php?id=317&sesskey=AmYynEH179&switchrole=5

csg.csail.m...Examples.pdf homepage...hazards.pdf An Introduct...s in Verilog Processador... como bits CBN - Jorna... do governo Apple Google Maps Yahoo! YouTube Wikipedia Notícias Popular

Curso: Laboratório de Sistemas Digitais para Computação Gmail – Inbox

Laboratório de Sistemas Digitais para Computação Você acessou como Jeferson Figueiredo Chaves: Participante (Retomar a minha função normal)

• CEFET-MG
• ► Array

Participantes Participantes

Atividades Fóruns Recursos

Pesquisar nos Fóruns Vai Pesquisa Avançada

Administração Notas Perfil

Meus cursos

- Arquitetura e Organização de Computadores I
- Departamento de Computação
- Documentação de Procedimentos do DRI
- Laboratório de Arquitetura e Organização de Computadores I
- Laboratório de Organização e Arquitetura de Computadores I
- Laboratório de Sistemas Digitais para Computação
- Seminários de Pesquisa do DECOM (Semana C&T 2010)
- Sistemas Digitais para Computação

Programação

Fórum de Notícias - 2 sem. 2013

1 DE2 Pins Assigments

- Referências Verilog (seções do livro do Morris Mano)
- Aula 1 - 10/10
- Aula 1 - 10/10 - Introdução ao Quartus

2 Não disponível

3

4

5

6

7

8

9

10 Não disponível

Retomar a minha função normal

Últimas Notícias

12 Dec, 00:17 Jeferson Figueiredo Chaves Notas Finais e Exame Especial mais...

29 Nov, 00:23 Jeferson Figueiredo Chaves Notas mais...

2 Sep, 00:28 Jeferson Figueiredo Chaves Relatório mais... Tópicos antigos ...

Próximos Eventos

Não há nenhum evento próximo

Calendário... Novo evento...

Atividade recente

Atividade desde Wednesday, 16 October 2013, 17:22 Relatório completo da atividade recente Nenhuma novidade desde o seu último acesso

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

File Edit View Project Assignments Processing Tools Window Help

Device... Settings... Ctrl+Shift+E

Project Navigator

Entity

Cyclone II: EP2C35F672C6

aula2

aula1_0:a1

TimeQuest Timing Analyzer Wizard...

Assignment Editor Ctrl+Shift+A

Pin Planner Ctrl+Shift+N

Remove Assignments...

Back-Annotate Assignments...

Import Assignments... (selected)

Export Assignments...

Assignment Groups...

LogicLock Regions Window Alt+L

Design Partitions Window Alt+D

Hierarchy Files Design Units

Tasks Flow: Compilation Customize...

Flow Status Successful - Thu Oct 17 12:42:53 2013

Quartus II 32-bit Version 12.1 Build 177 11/07/2012 SJ Web Edition

Revision Name aula2

Top-level Entity Name aula2

Family Cyclone II

Device EP2C35F672C6

Timing Models Final

Total logic elements 1 / 33,216 (< 1 %)

- Total combinational functions 1 / 33,216 (< 1 %)
- Dedicated logic registers 0 / 33,216 (0 %)

Total registers 0

Total pins 36 / 475 (8 %)

Total virtual pins 0

Total memory bits 0 / 483,840 (0 %)

Embedded Multiplier 9-bit elements 0 / 70 (0 %)

Total PLLs 0 / 4 (0 %)

Flow Summary

Timing Analyzer Writer

All <<Search>>

Type ID Message

204026 Generated files "aula2.vo", "aula2_fast.vo", "aula2_v.sdo" and "aula2_v_fast.sdo" in directory "/Desktop/aula2/simulation/modelsim/" for EDA simulation tool

Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings

293000 Quartus II Full Compilation was successful. 0 errors, 45 warnings

System Processing (100)

Imports assignments from other sources

100% 00:00:28

Start Quartus II 32-bit - //... 12:44 PM

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

File Edit View Project Assignments Processing Tools Window Help

Search altera.com



aula2

Project Navigator

Entity

Cyclone II: EP2C35F672C6

aula2

aula1_0:a1

aula2.v

 Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Filter
- Assembler
- TimeQuest Timing Analyzer
- EDA Netlist Writer

Flow Summary

Flow Status	Successful - Thu Oct 17 12:42:53 2013
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	aula2
Top-level Entity Name	aula2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	1 / 33,216 (< 1 %)
Total combinational functions	1 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	36 / 475 (8 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Import Assignments

Specify the source and categories of assignments to import.

 File name: Categories...

 Copy existing assignments into aula2.qsf.bak before importing

Advanced...

OK

Cancel

Help

Tasks

Flow: Compilation

Customize...

Task

- Compile Design
- Analysis & Synthesis
- Filter (Place & Route)
- Assembler (Generate programming files)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

 All <<Search>>

Type ID Message

- (i) 204026 Generated files "aula2.vo", "aula2_fast.vo", "aula2_v.sdo" and "aula2_v_fast.sdo" in directory "/Desktop/aula2/simulation/modelsim/" for EDA simulation tool
- (i) Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
- (i) 293000 Quartus II Full Compilation was successful. 0 errors, 45 warnings

System Processing (100)

100% 00:00:28

Start Quartus II 32-bit - //...

12:44 PM



Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

File Edit View Project Assignments Processing Tools Window Help

Search altera.com



aula2

Project Navigator

Entity

Cyclone II: EP2C35F672C6

aula2

aula1_0:a1

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- + Analysis & Synthesis
- + Filter
- + Assembler
- + TimeQuest Timing Analyzer
- + EDA Netlist Writer

Flow Summary

Flow Status	Successful - Thu Oct 17 12:42:53 2013
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	aula2
Top-level Entity Name	aula2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	1 / 33,216 (< 1 %)
Total combinational functions	1 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	36 / 475 (8 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Import Assignments

Specify the source and categories of assignments to import.

File name: //psf/Home/Desktop/DE2.qsf

Categories...

 Copy existing assignments into aula2.qsf.bak before importing

Advanced...

OK

Cancel

Help

Tasks

Flow:

Compilation

Customize...

Task

- Compile Design
- Analysis & Synthesis
- Filter (Place & Route)
- Assembler (Generate programming files)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

<<Search>>

Type ID Message

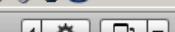
- (i) 204026 Generated files "aula2.vo", "aula2_fast.vo", "aula2_v.sdo" and "aula2_v_fast.sdo" in directory "/Desktop/aula2/simulation/modelsim/" for EDA simulation tool
- (i) Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
- (i) 293000 Quartus II Full Compilation was successful. 0 errors, 45 warnings

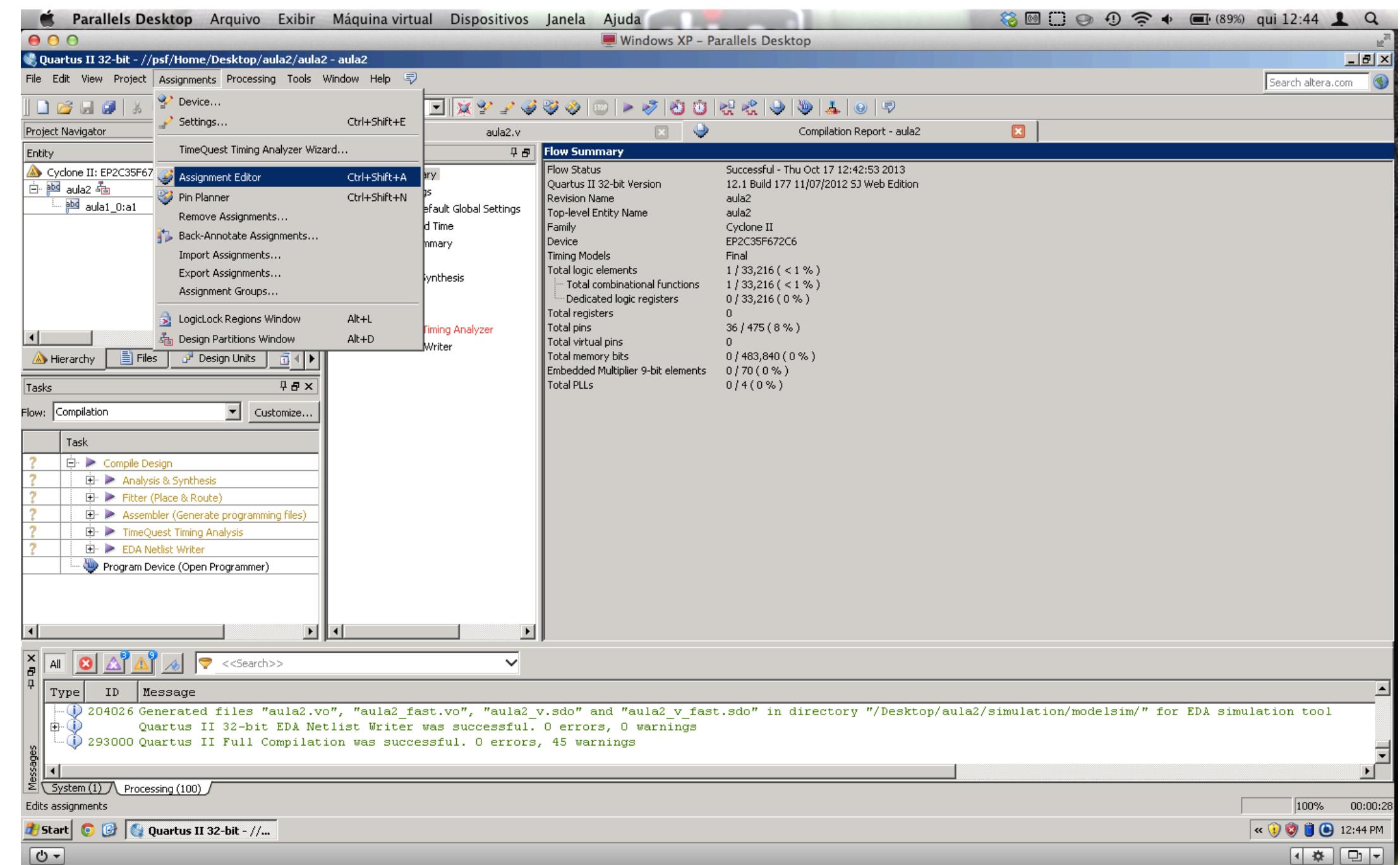
System Processing (100)

100% 00:00:28

Quartus II 32-bit - //...

12:44 PM





Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

Search altera.com

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Entity aula2.v Compilation Report - aula2 Assignment Editor

Entity: Cyclone II: EP2C35F672C6
 aula2
 aula1_0:a1

Tasks Flow: Compilation Customize...

#	att	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✓		in SW[0]	Location	PIN_N25	Yes			
2	✓		in SW[1]	Location	PIN_N26	Yes			
3	✓		in SW[2]	Location	PIN_P25	Yes			
4	✓		in SW[3]	Location	PIN_AE14	Yes			
5	✓		in SW[4]	Location	PIN_AF14	Yes			
6	✓		in SW[5]	Location	PIN_AD13	Yes			
7	✓		in SW[6]	Status: Ok	PIN_AC13	Yes			
8	✓		in SW[7]	Location	PIN_C13	Yes			
9	✓		in SW[8]	Location	PIN_B13	Yes			
10	✓		in SW[9]	Location	PIN_A13	Yes			
11	✓		in SW[10]	Location	PIN_N1	Yes			
12	✓		in SW[11]	Location	PIN_P1	Yes			
13	✓		in SW[12]	Location	PIN_P2	Yes			
14	✓		in SW[13]	Location	PIN_T7	Yes			
15	✓		in SW[14]	Location	PIN_U3	Yes			
16	✓		in SW[15]	Location	PIN_U4	Yes			
17	✓		in SW[16]	Location	PIN_V1	Yes			
18	✓		in SW[17]	Location	PIN_V2	Yes			
19	?		DRAM...R[0]	Location	PIN_T6	Yes			
20	?		DRAM...R[1]	Location	PIN_V4	Yes			
21	?		DRAM...R[2]	Location	PIN_V3	Yes			
22	?		DRAM...R[3]	Location	PIN_W2	Yes			
23	?		DRAM...R[4]	Location	PIN_W1	Yes			
24	?		DRAM...R[5]	Location	PIN_U6	Yes			
25	?		DRAM...R[6]	Location	PIN_U7	Yes			
26	?		DRAM...R[7]	Location	PIN_U5	Yes			

Messages All <<Search>>

Type	ID	Message
Info	204026	Generated files "aula2.vo", "aula2_fast.vo", "aula2_v.sdo" and "aula2_v_fast.sdo" in directory "/Desktop/aula2/simulation/modelsim/" for EDA simulation tool
Info	Quartus II 32-bit EDA Netlist Writer was successful.	0 errors, 0 warnings
Info	293000	Quartus II Full Compilation was successful. 0 errors, 45 warnings

System (1) Processing (100)

100% 00:00:28

Start Quartus II 32-bit - //... 12:45 PM



Entity

- Cyclone II: EP2C35F672C6
 - aula2
 - aula1_0:a1

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Filter

Flow Summary

Flow Status	In progress - Thu Oct 17 12:45:30 2013
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	aula2
Top-level Entity Name	aula2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	1
Total combinational functions	1
Dedicated logic registers	0
Total registers	0
Total pins	36
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Hierarchy **Files** **Design Units**

Tasks

Flow: Compilation Customize...

Task	Progress
Compile Design	26%
Analysis & Synthesis	100%
Filter (Place & Route)	0%
Assembler (Generate programming files)	0%
TimeQuest Timing Analysis	0%
EDA Netlist Writer	0%
Program Device (Open Programmer)	0%

Messages

All <<Search>>

Type	ID	Message
Info	176235	Finished register packing
Warning	15705	Ignored locations or region assignments to the following nodes
Info	171121	Fitter preparation operations ending: elapsed time is 00:00:01

System (1) Processing (33)

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

Search altera.com

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity
Cyclone II: EP2C35F672C6
 a2
 a2
 a2_0:a1

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

	Task
✓	Compile Design
✓	Analysis & Synthesis
✓	Filter (Place & Route)
✓	Assembler (Generate programming files)
✓	TimeQuest Timing Analysis
✓	EDA Netlist Writer
	Program Device (Open Programmer)



Type	ID	Message
Info	204026	Generated files "aula2.vo", "aula2_fast.vo", "aula2_v.sdo" and "aula2_v_fast.sdo" in directory "/Desktop/aula2/simulation/modelsim/" for EDA simulation tool
Info		Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
Info	293000	Quartus II Full Compilation was successful. 0 errors, 435 warnings

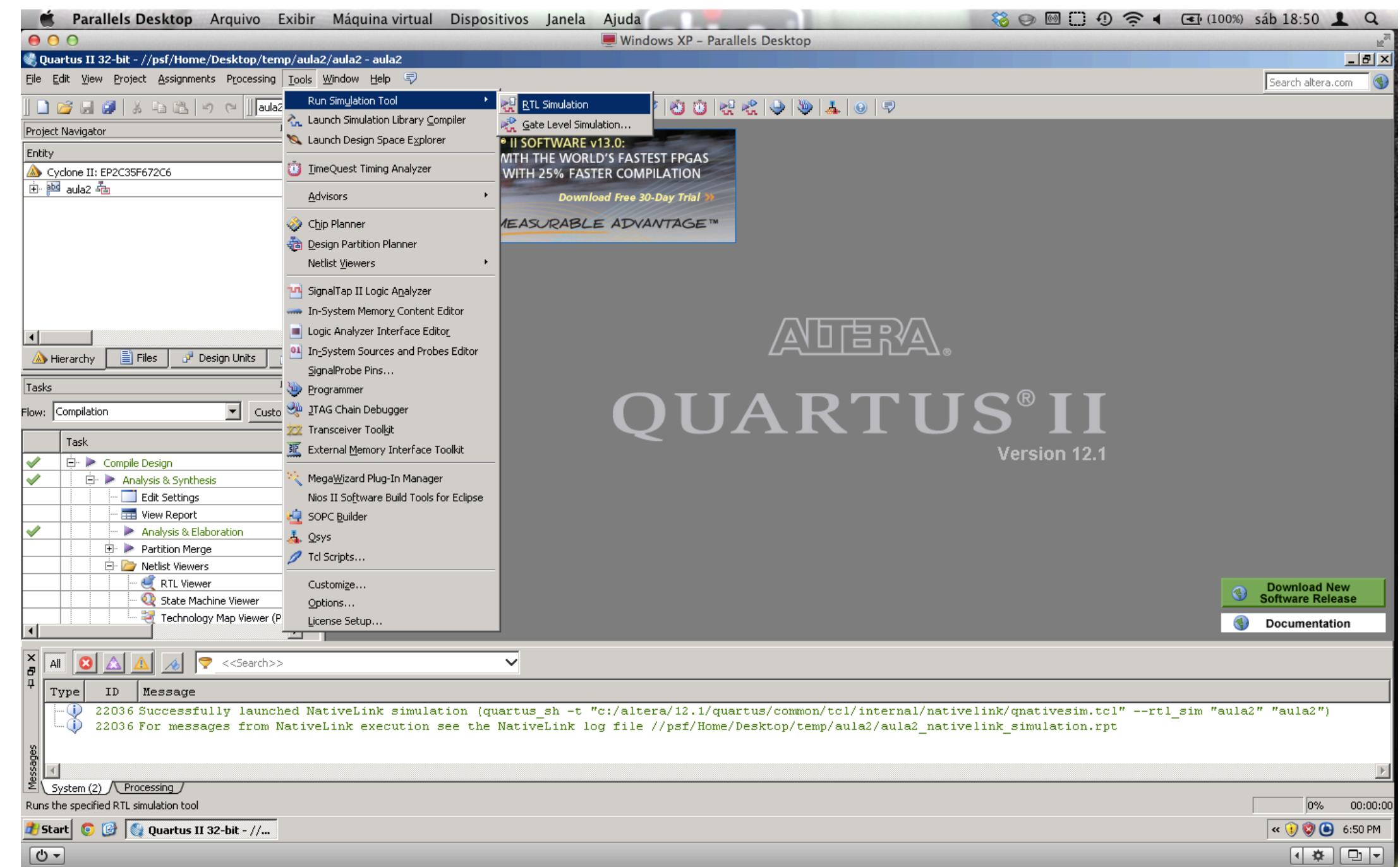
System (1) Processing (99)

100% 00:00:28

Start Quartus II 32-bit - //psf/... Quartus II

12:45 PM





Modelsim

- Software direcionado à simulação.

Windows XP - Parallels Desktop

ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path

Objects

Name	Value	Kind	Mode

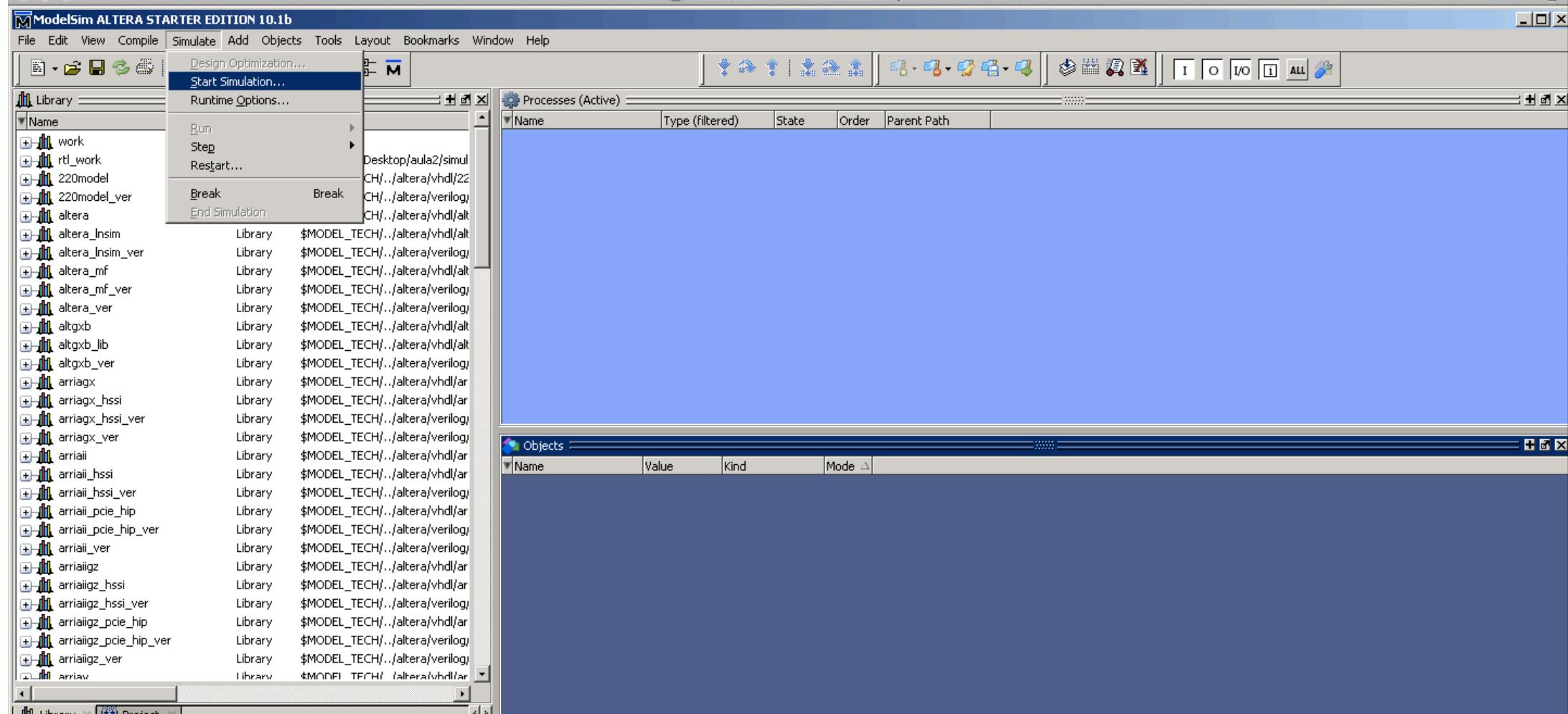
Library Project Transcript

Top level modules:
aula2
#

ModelSim>

<No Design Loaded> rtl_work

Start Quartus II 32-bit - //psf/... ModelSim ALTERA ST... 12:46 PM

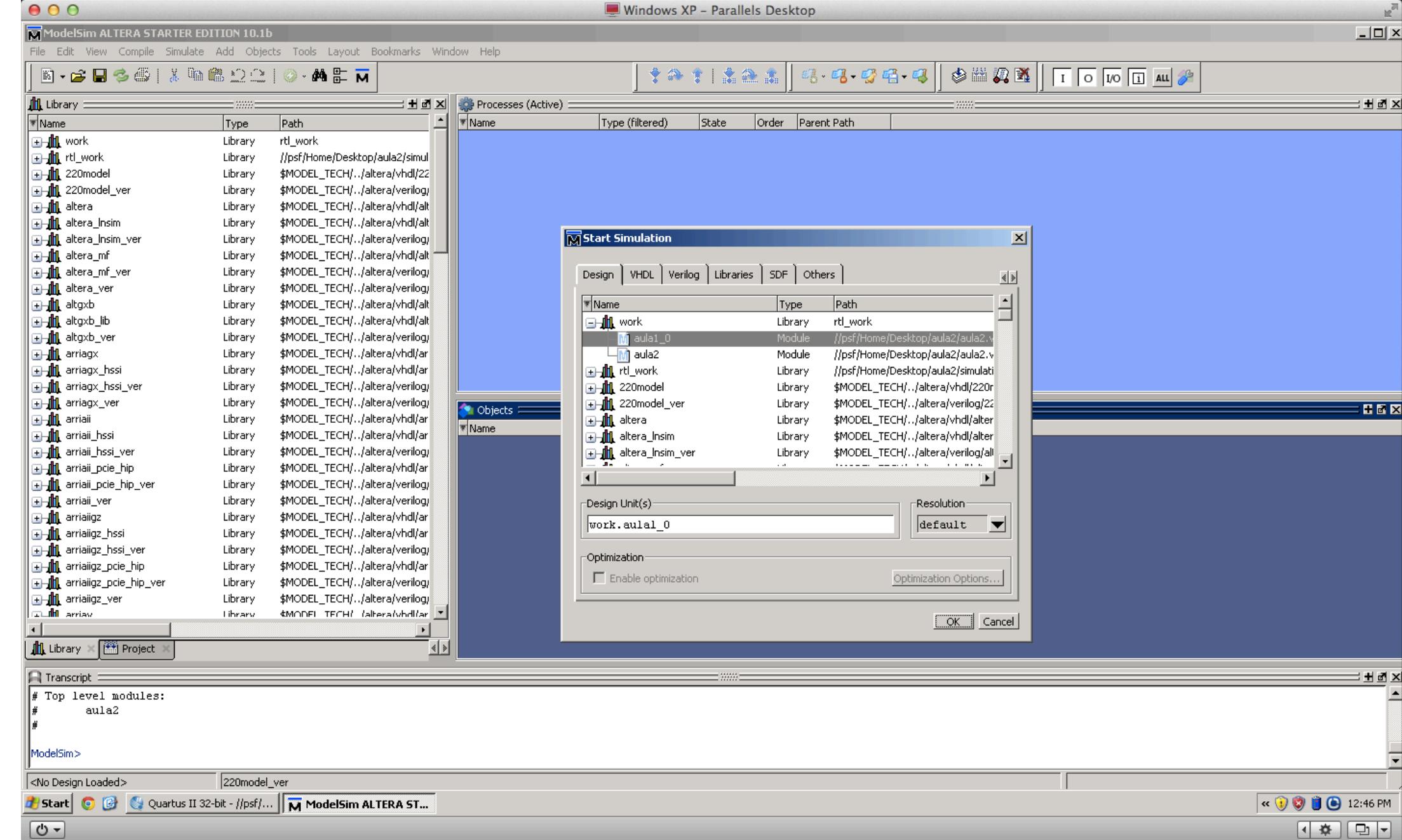


```
# Top level modules:
#     aula2
#
ModelSim>
```

<No Design Loaded> rtl_work

Start Quartus II 32-bit - //psf/... ModelSim ALTERA ST...

12:46 PM



ModelSim ALTERA STARTER EDITION 10.1b

Windows XP – Parallels Desktop

File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help

sim - Default

Instance	Design unit	Design unit type	Visibility	Total coverage
aula1_0	aula1_0	Module	+acc=<...	
#ASSIGN#4	aula1_0	Process	+acc=<...	
#vsim_capacity#		Capacity	+acc=<...	

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
#ASSIGN#4	Assign	Active	1	/aula1_0

Objects

Name	Value	Kind	Mode
x1	HIZ	Net	In
x2	HIZ	Net	In
f	StX	Net	Out
sim:/aula1_0/f			

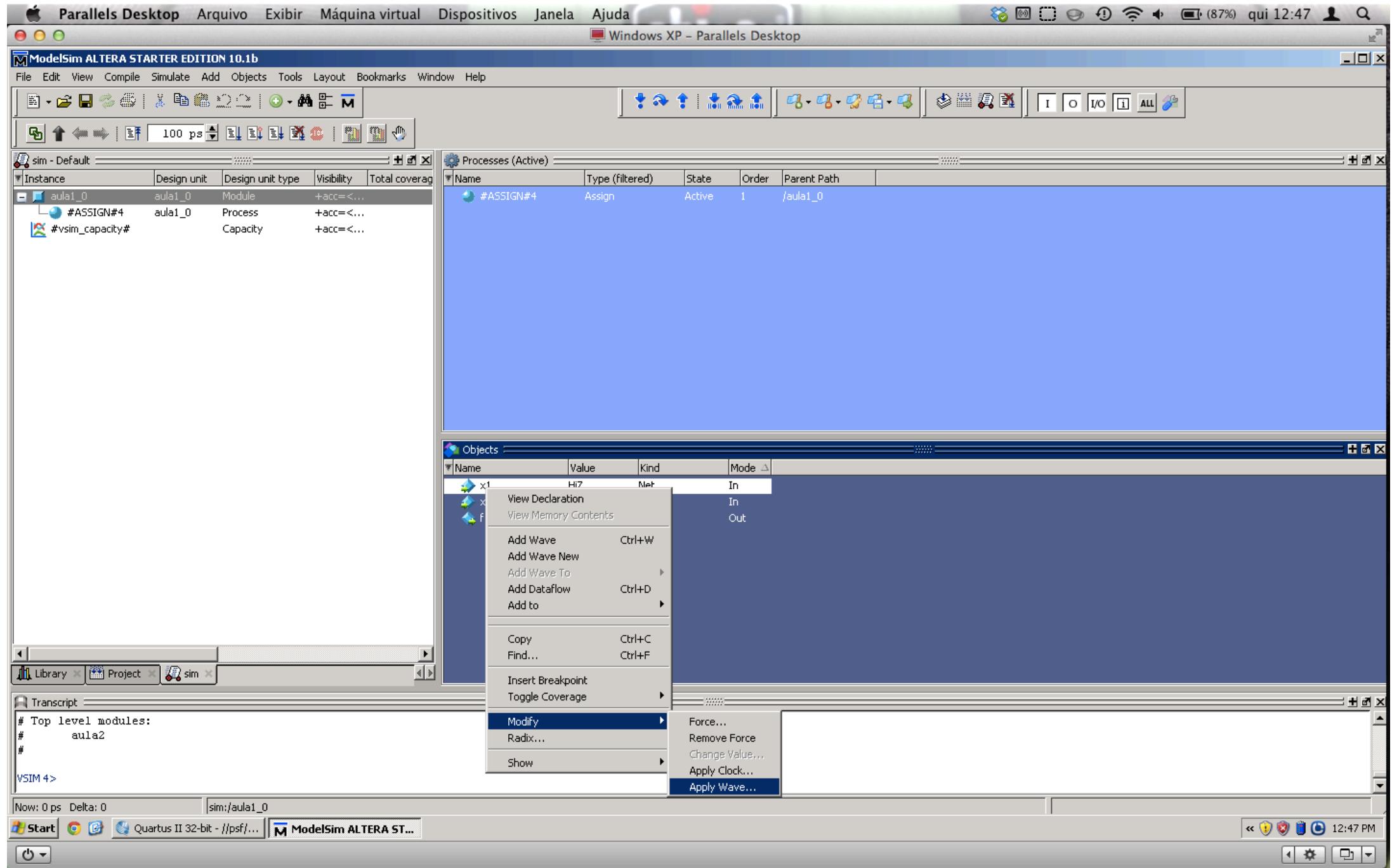
Library Project sim

Transcript

```
# Top level modules:
#     aula2
#
VSIM 4>
```

Now: 0 ps Delta: 0 f

Start Quartus II 32-bit - //psf/... ModelSim ALTERA ST... 12:47 PM



ModelSim ALTERA STARTER EDITION 10.1b

Windows XP - Parallels Desktop

File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help

sim - Default

100 ps

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
#ASSIGN#4	Assign	Active	1	/aula1_0

Create Pattern Wizard

Generate a waveform for any signal for the chosen pattern.

The allowed patterns are:

- Constant
- Clock
- Random
- Repeater
- Counter

Select Pattern

Patterns:

- Clock
- Constant
- Random
- Repeater
- Counter

Signal Name: sim:/aula1_0/x1

Start Time: 0 End Time: 400 Time Unit: ps

< Previous Next > Cancel

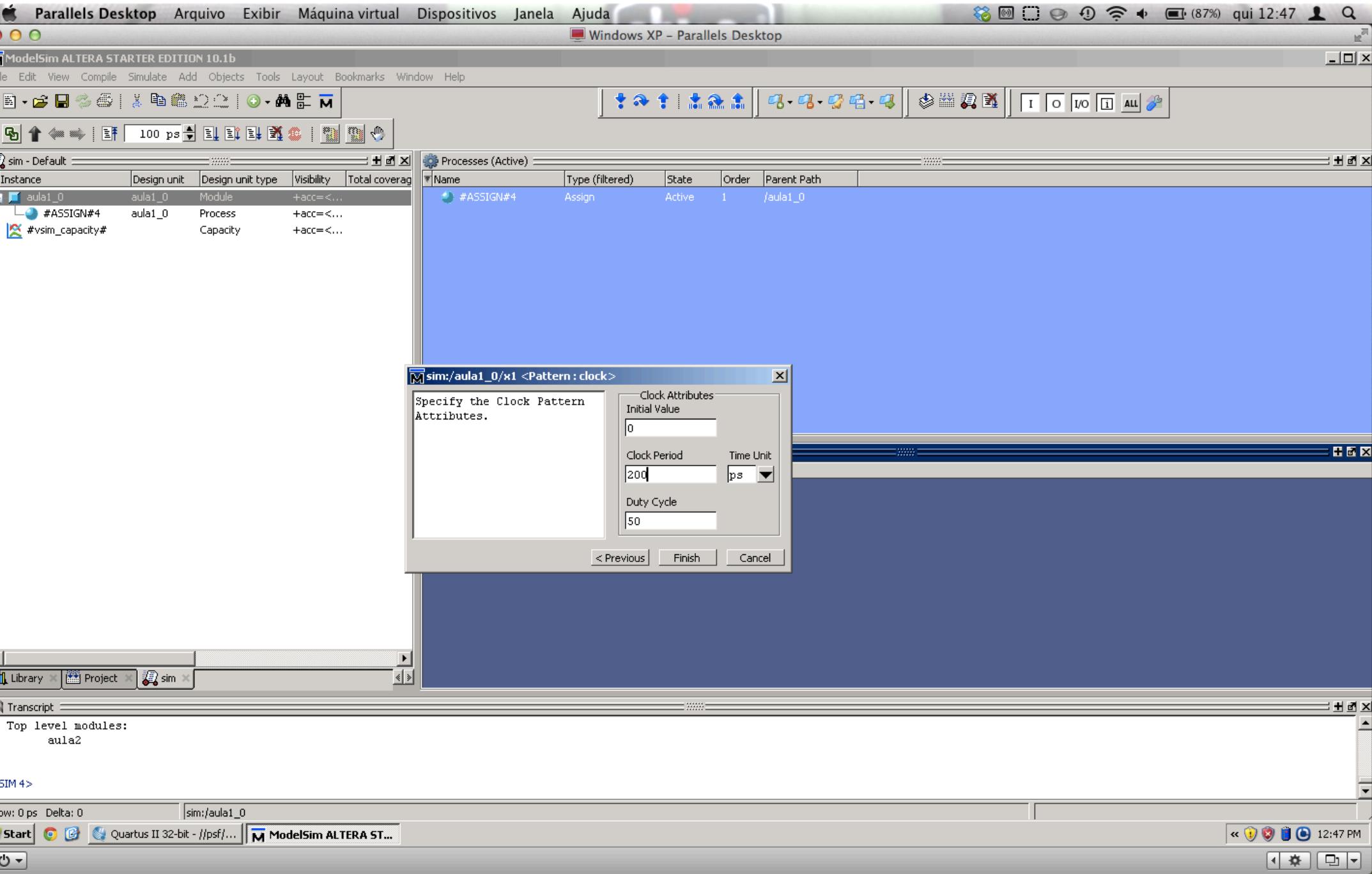
Library Project sim

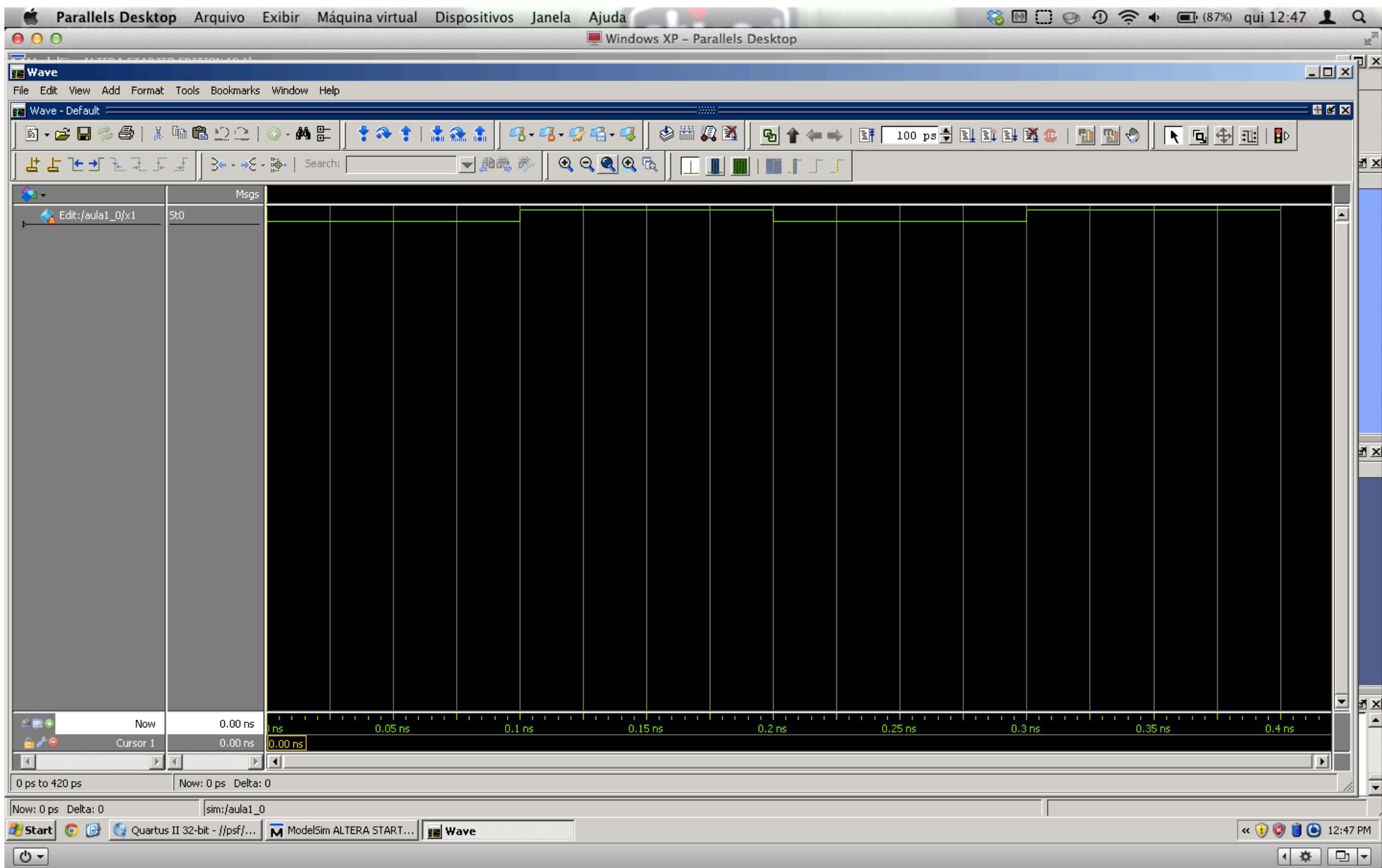
Transcript

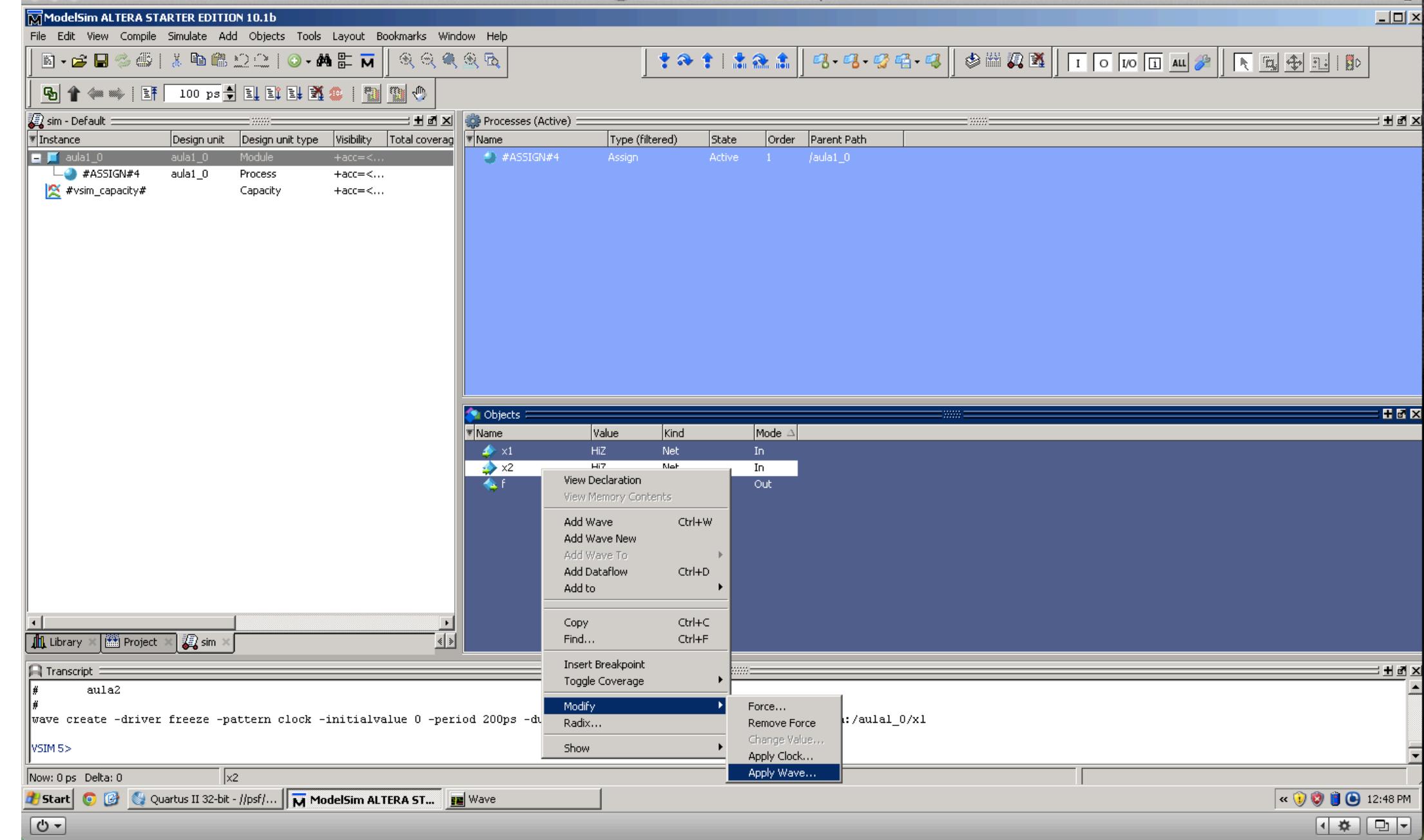
```
# Top level modules:
#   aula2
#
VSIM 4>
```

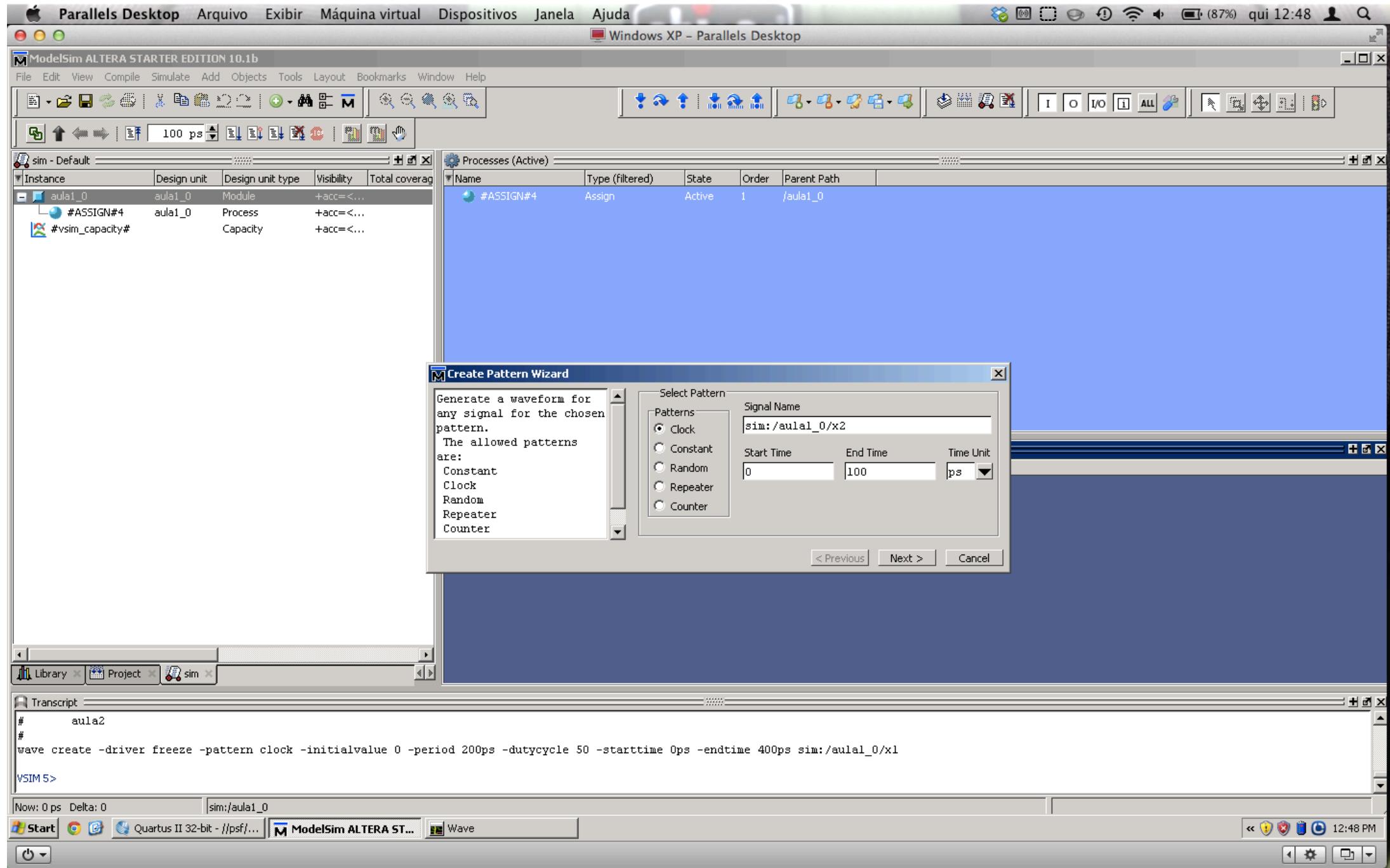
Now: 0 ps Delta: 0 sim:/aula1_0

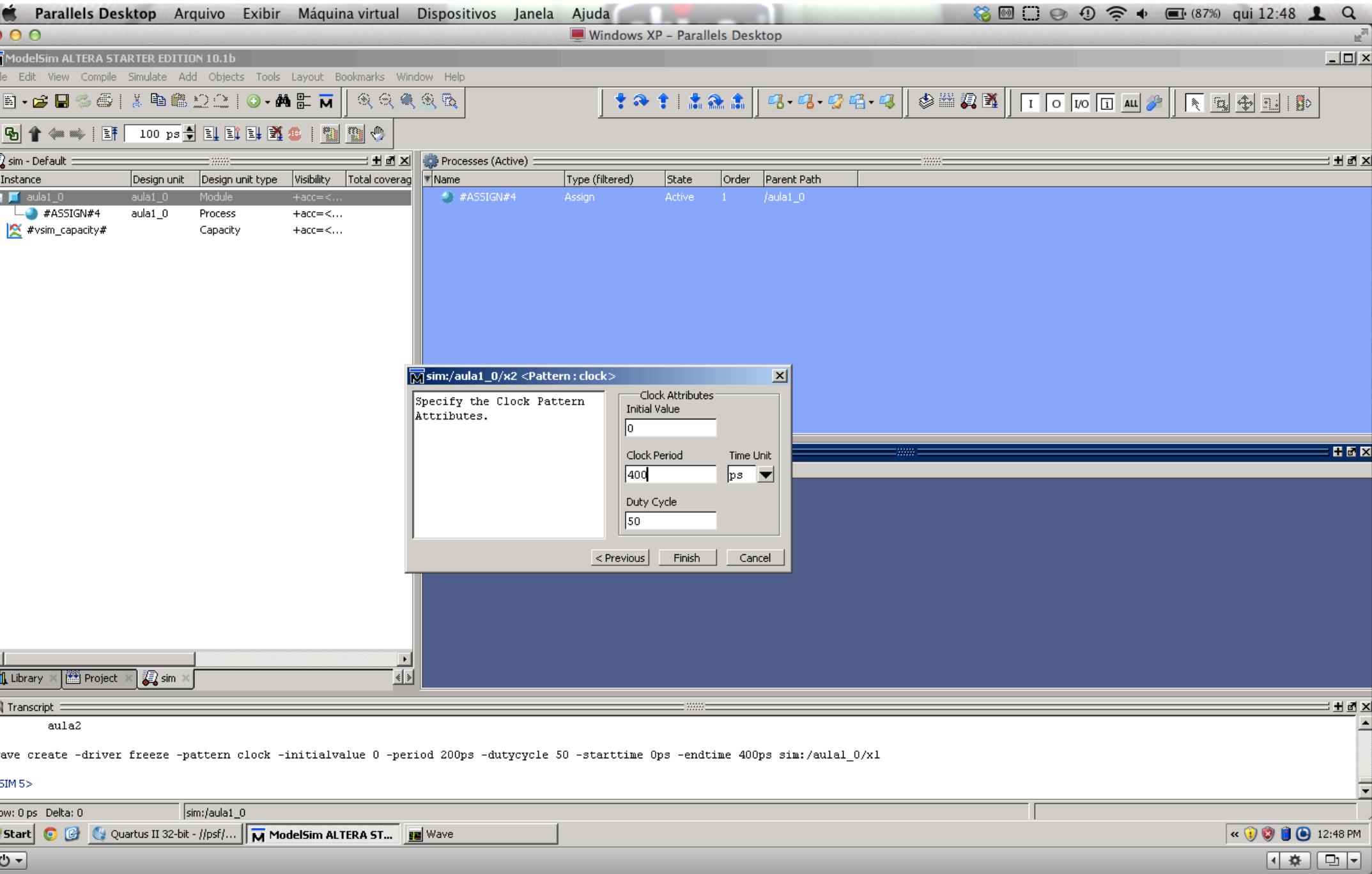
Start Quartus II 32-bit - //psf/... ModelSim ALTERA ST... 12:47 PM

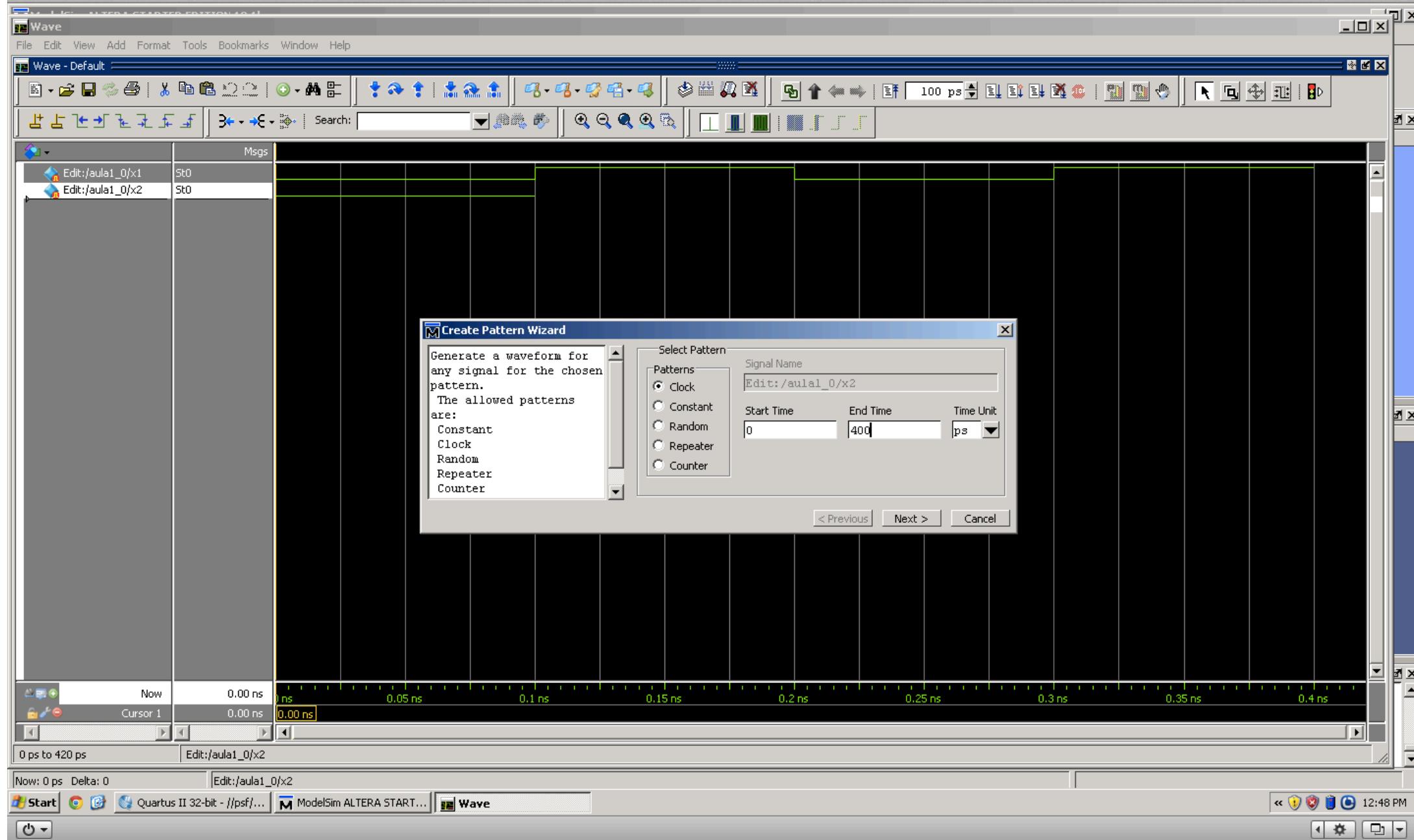


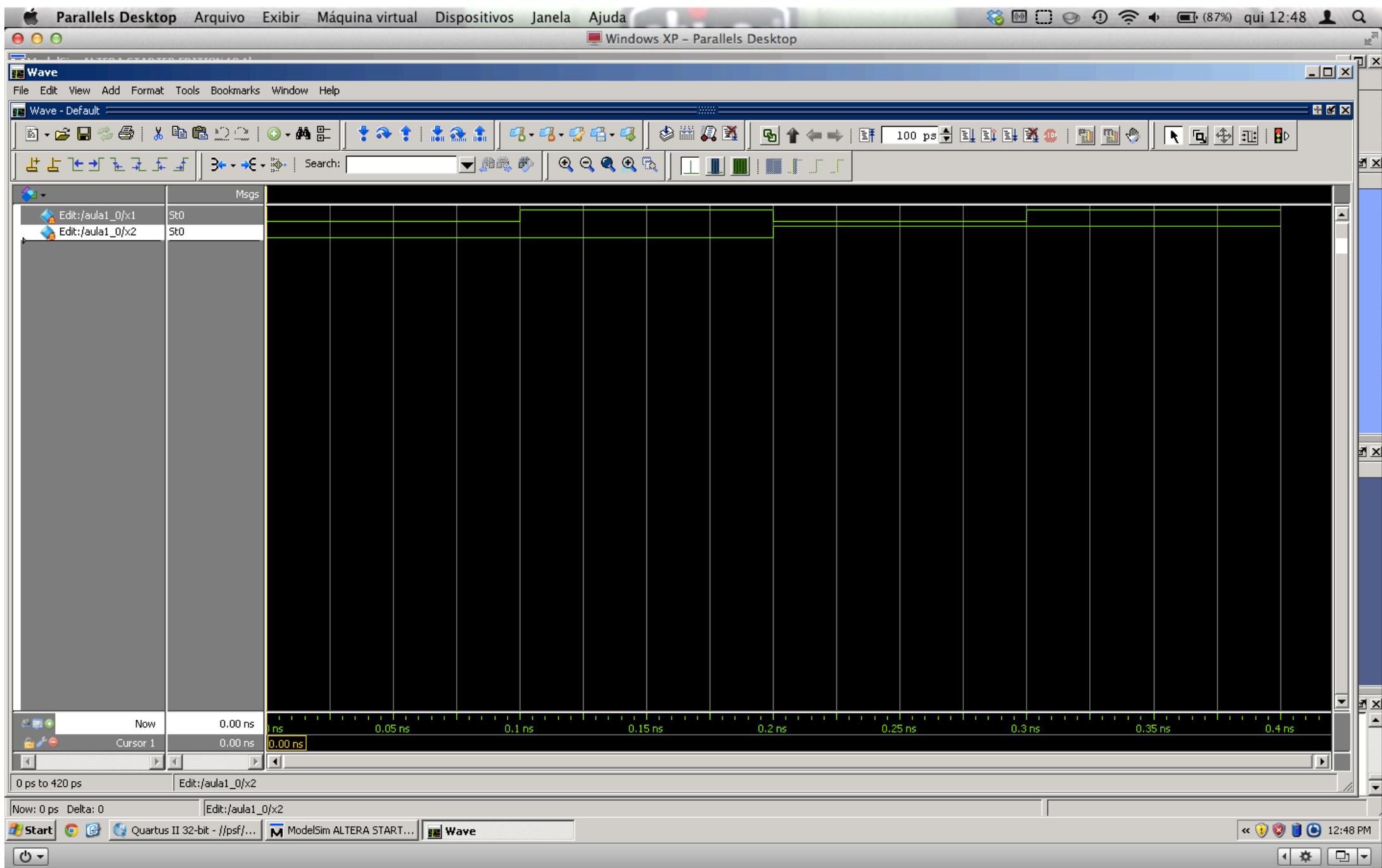


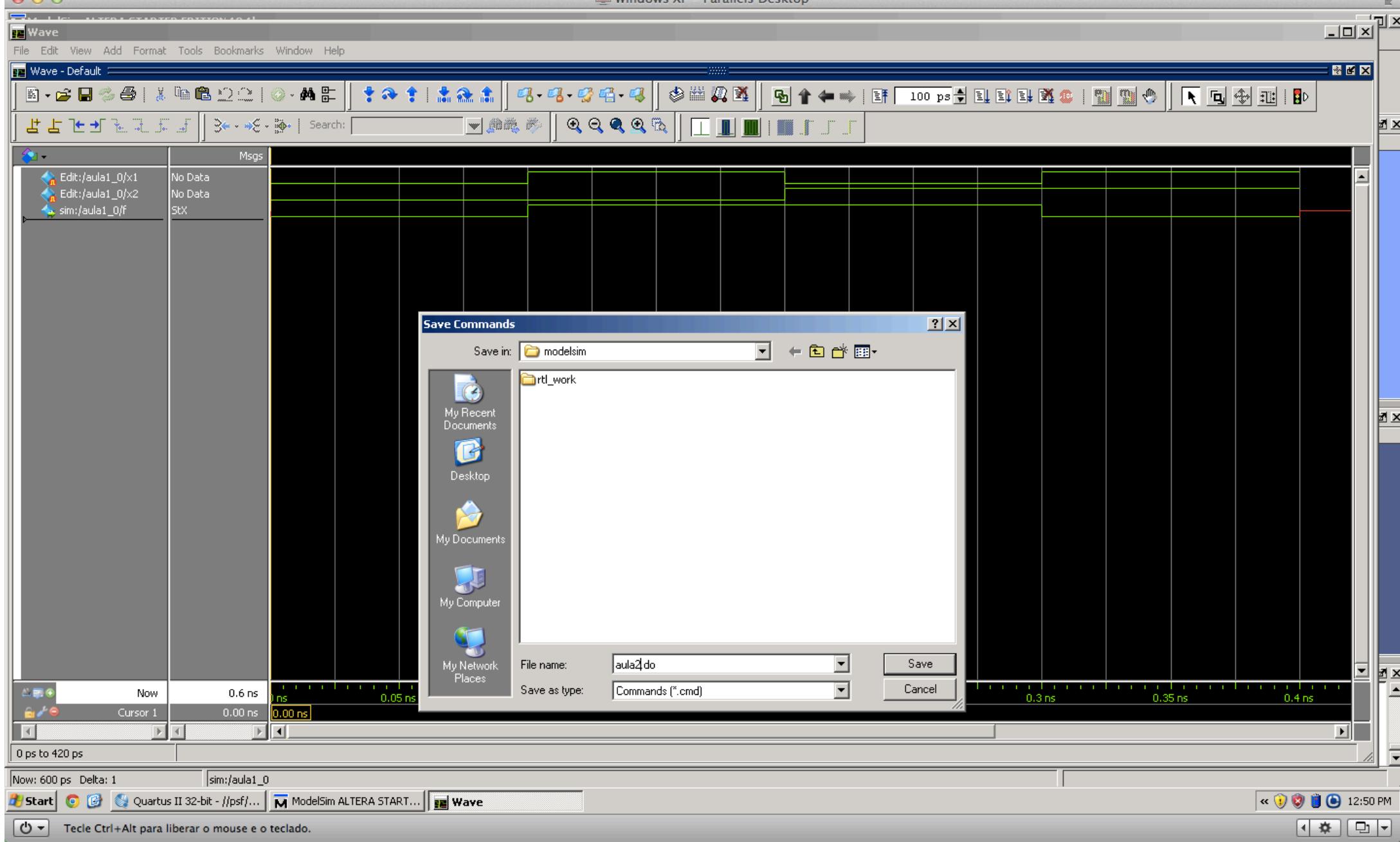












Tecle Ctrl+Alt para liberar o mouse e o teclado.

Windows XP – Parallels Desktop

ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help

sim - Default 100 ps

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path

Objects

Name	Value	Kind	Mode
x1	HIZ	Net	In
x2	HIZ	Net	In
f	StX	Net	Out

Library Project sim

Transcript

```
sim:/aula1_0/f
VSIM 8> run -all
wave editwrite -file //psf/Home/Desktop/aula2/simulation/modelsim/aula2.do
VSIM 10>
```

Now: 600 ps Delta: 1 sim:/aula1_0

Start Quartus II 32-bit - //psf/... ModelSim ALTERA ST... 12:50 PM

Tecle Ctrl+Alt para liberar o mouse e o teclado.

Quartus II: Comunicação com a placa

- A placa deverá estar energizada.
- O cabo USB (cinza) deverá estar ligado no conector mais próximo ao cabo de alimentação.

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

File Edit View Project Assignments Processing Tools Window Help Search altera.com

Project Navigator Entity aula2.v Compilation Report - aula2

Table of Contents Flow Summary

Flow Status Successful - Thu Oct 17 12:45:50 2013
 Quartus II 32-bit Version 12.1 Build 177 11/07/2012 SJ Web Edition
 Revision Name aula2
 Top-level Entity Name aula2
 Family Cyclone II
 Device EP2C35F672C6
 Timing Models Final
 Total logic elements 1 / 33,216 (< 1 %)
 Total combinational functions 1 / 33,216 (< 1 %)
 Dedicated logic registers 0 / 33,216 (0 %)
 Total registers 0
 Total pins 36 / 475 (8 %)
 Total virtual pins 0
 Total memory bits 0 / 483,840 (0 %)
 Embedded Multiplier 9-bit elements 0 / 70 (0 %)
 Total PLLs 0 / 4 (0 %)

Hierarchy Files Design Units Tasks

Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Filter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

All <<Search>>

Type ID Message

140120 Import completed. 430 assignments were written (out of 440 read). 6 non-global assignments were skipped because of entity name mismatch.
 22036 Successfully launched NativeLink simulation (quartus_sh -t "c:/altera/12.1/quartus/common/tcl/internal/nativelink/qnativesim.tcl" --rtl_sim "aula2" "aula2")
 22036 For messages from NativeLink execution see the NativeLink log file //psf/Home/Desktop/aula2/aula2_nativelink_simulation.rpt

Messages System (3) Processing (99)

100% 00:00:28

Start Quartus II 32-bit - //... 12:52 PM

Quartus II 32-bit - //psf/Home/Desktop/aula2/aula2 - aula2

Search altera.com

File Edit View Project Assignments Processing Tools Window Help

Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer
TimeQuest Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
SignalProbe Pins...
Programmer
JTAG Chain Debugger
Transceiver Toolkit
External Memory Interface Toolkit
MegaWizard Plug-In Manager
Nios II Software Build Tools for Eclipse
SOPC Builder
Qsys
Tcl Scripts...
Customize...
Options...
License Setup...

Flow Summary

Flow Status	Successful - Thu Oct 17 12:45:50 2013
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	aula2
Top-level Entity Name	aula2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	1 / 33,216 (< 1 %)
Total combinational functions	1 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	36 / 475 (8 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Hierarchy Files Design Units Tasks Flow: Compilation Custom

Task

- Compile Design
- Analysis & Synthesis
- Filter (Place & Route)
- Assembler (Generate programming)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

All <<Search>>

Type ID Message

- 140120 Import completed. 430 assignments were written (out of 440 read). 6 non-global assignments were skipped because of entity name mismatch.
- 22036 Successfully launched NativeLink simulation (quartus_sh -t "c:/altera/12.1/quartus/common/tcl/internal/nativelink/qnativesim.tcl" --rtl_sim "aula2" "aula2")
- 22036 For messages from NativeLink execution see the NativeLink log file //psf/Home/Desktop/aula2/aula2_nativelink_simulation.rpt

Messages System (3) Processing (99)

Opens a Programmer window

Start Quartus II 32-bit - //... 100% 00:00:28 12:52 PM

Windows XP – Parallels Desktop

Programmer - //psf/Home/Desktop/aula2/aula2 - aula2 - [output_files/aula2.cdf]

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup...

No Hardware

Mode:

JTAG

Progress:

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
output_files/aula2.sof	EP2C35F672	002F8BAF	FFFFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>						

Start

Stop

Auto Detect

Delete

Add File...

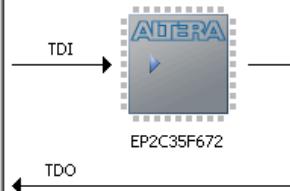
Change File...

Save File

Add Device...

Up

Down



Start

Stop

Quartus II 32-bit - //psf/... | Programmer - //psf/...

12:52 PM

Power

12:52 PM

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup... No Hardware

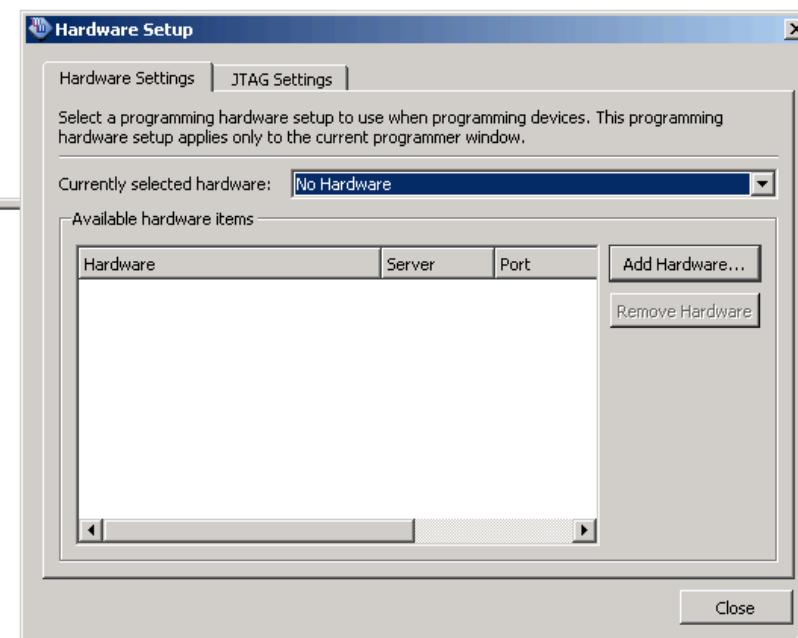
Mode: JTAG

Progress:

 Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

- Start
- Stop
- Auto Detect
- Delete
- Add File...
- Change File...
- Save File
- Add Device...
- Up
- Down

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
output_files/aula2.sof	EP2C35F672	002F8BAF	FFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>						



Windows XP – Parallels Desktop

Programmer - //psf/Home/Desktop/aula2/aula2 - aula2 - [output_files/aula2.cdf]

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup... No Hardware Mode: JTAG Progress:

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/aula2.sof	EP2C35F672	002F8BAF	FFFFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>					

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

TDI →  EP2C35F672 ← TDO

Hardware Setup

Hardware Settings JTAG Settings

Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.

Currently selected hardware: No Hardware

Available hardware items

Hardware	Server	Port
USB-Blaster	Local	USB-0

Add Hardware... Remove Hardware Close

Programmer - //psf/Home/Desktop/aula2/aula2 - aula2 - [output_files/aula2.cdf]

Windows XP - Parallels Desktop

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup... No Hardware

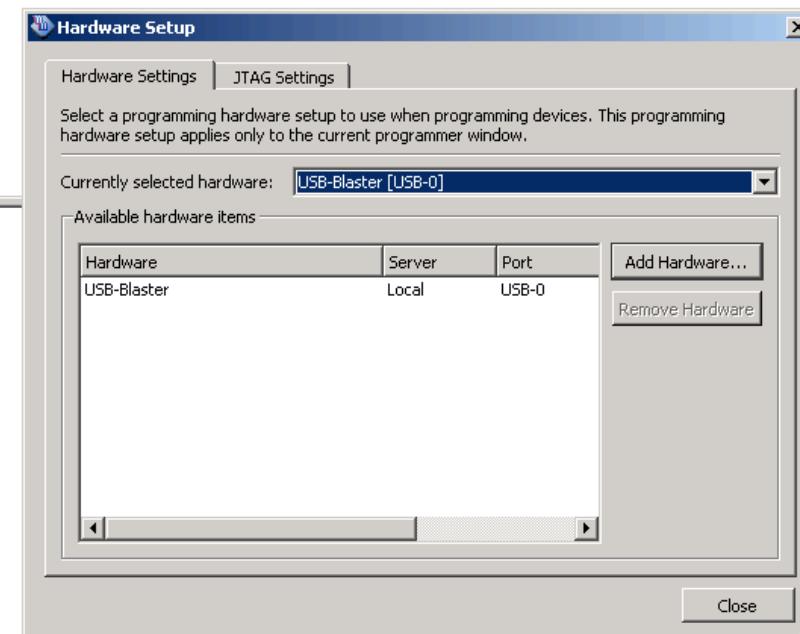
Mode: JTAG

Progress:

 Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
output_files/aula2.sof	EP2C35F672	002F8BAF	FFFFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>						



Programmer - //psf/Home/Desktop/aula2/aula2 - aula2 - [output_files/aula2.cdf]

Windows XP - Parallels Desktop

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup...

No Hardware

Mode: JTAG

Progress:

 Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Start

Stop

Auto Detect

Delete

Add File...

Change File...

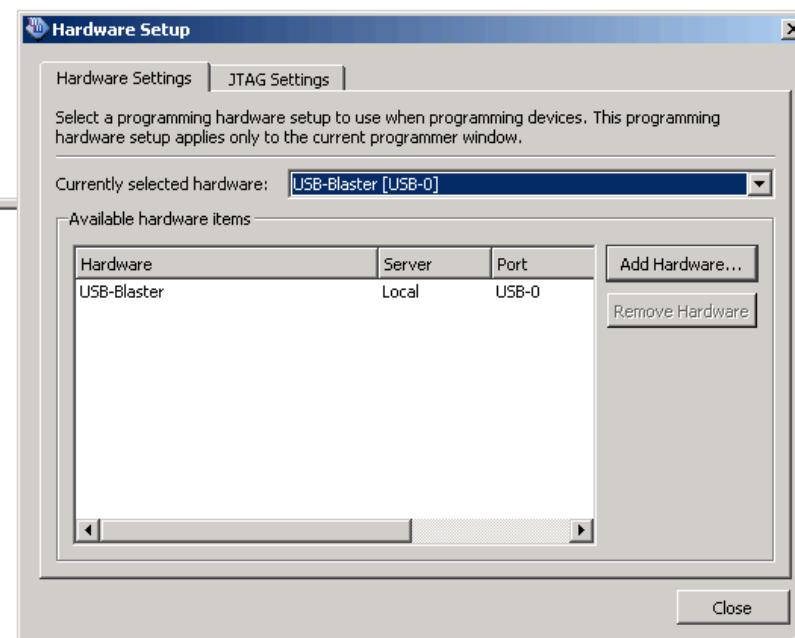
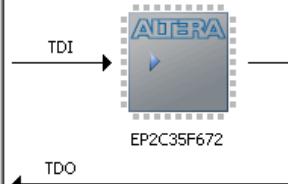
Save File

Add Device...

Up

Down

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/aula2.sof	EP2C35F672	002F8BAF	FFFFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>					



Programmer - //psf/Home/Desktop/aula2/aula2 - aula2 - [output_files/aula2.cdf]

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup...

USB-Blaster [USB-0]

Mode: JTAG

Progress:

100% (Successful)

Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Start

Stop

Auto Detect

Delete

Add File...

Change File...

Save File

Add Device...

Up

Down

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
output_files/aula2.sof	EP2C35F672	002F8BAF	FFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>						

