

A Microcontroller-based, Optically-centric Communication System for Underwater Applications

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Abstract

Abstract

We live on a water planet. Over seventy percent of the Earth's surface is covered in water. Yet, we cannot communicate underwater. There currently exists no high-bandwidth communication system for use in oceanic environments. Blue light is the key to underwater communication.

Short visible wavelengths have low attenuation rates in both fresh water and saltwater.

Additionally, visible light is unregulated spectrum and is a secure, line-of-sight data carrier.

A microcontroller-based system has been developed to use blue light to create a dynamic, full-duplex communication system with self-aligning capabilities. A collimated beam is supplied from a high-power laser diode driven by an integrated driver using Manchester coding techniques. The microcontroller's ADC module facilitates data/clock recovery operations, maintaining optical alignment using a novel sampling approach, and monitoring important voltage and current sense measurements across the system. Concurrently, a set of analog servos are used in a gimbal to align the optics of each transceiver.

This system is built with intentions to be used on the OpenROV. This underwater rover will inherit a pair of transceivers to replace its long tether. By interfacing through Ethernet, this system is noninvasive and entirely reversible. Additionally, the system can easily be realized to replace existing wired links in other Ethernet networks.

Error-free data rates up to 125kHz have been achieved with the current transceiver pair. This is half the original data rate envisioned for this system. Simple modifications to this design can easily scale the bandwidth by a factor of 20 or more. Additionally, improvements need to be made to the alignment processes to be able to accurately correct misalignments at greater distances. Regardless, this system is a significant step in underwater communications.

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List of Abbreviations

ADC	Analog-to-Digital Converter
BER	Bit Error Rate
DAC	Digital-to-Analog Converter
FSO	Free-Space Optical Communication
GBW	Gain-bandwidth product
MCU	Microcontroller Unit
PD	Photodiode
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
QP	Quadrant Photodiode
RF	Radio Frequency
SAR	Successive Approximation
S/H	Sample and Hold
SPI	Serial Peripheral Interface
SPICE	Simulation Program with Integrated Circuit Emphasis
USB	Universal Serial Bus

1 Introduction

1.1 Communication on a water planet

Today, the world and its citizens are more connected than ever before. Thousands of miles can be overcome with a simple tap or keystroke. This is all thanks to communication.

Communication technology has given rise to this new era in which we are said to be more accessible than ever. However, one does not need to look far to find a place where connectivity is lost, the ocean.

Current communication networks rely on radio frequency- and microwave frequency-centric infrastructures. The lower frequency end of the RF spectrum is used for relatively low bandwidth operations such as radio. The higher frequency end of RF spectrum and parts of the microwave spectrum are used for higher bandwidth operations such as GPS, radar, and cellular communications. These choices to use RF and microwave makes sense for their use cases.

However, the frequencies relied on by most modern wireless communication systems share one thing in common. They are not able to traverse underwater environments. This can be easily shown by taking a cell phone in a waterproof casing and placing it a few meters underwater. Indubitably, the cell phone will show it has lost service. Cellular, GPS, Wi-Fi, and Bluetooth signals used in modern phones rely on RF signals that attenuate quickly in water.

This leaves the large majority of the current communication infrastructure in a state where it cannot communicate wirelessly with endpoints under the surface of the oceans. This is significant since the Earth is a water planet. Seventy-one percent of earth's surface is covered by some form of water. Current methods to communicate in underwater environments rely on very

low-frequency RF. These methods are extremely low bandwidth and are not suited for audio or video transmission.

To be able to communicate in a variety of environments, a high-bandwidth, wireless communication system needs to be developed that can operate effectively in oceanic environments. The proposal is to create a dynamic, full-duplex communication link that uses visible light as the carrier and a microcontroller as a DSP/controller.

1.2 Applications

There is no shortage of applications for the novel communication system being proposed. Many of the benefits of this system are shared with those of proposed LiFi systems. LiFi is a term coined by Professor Harald Haas to refer to high-speed, bidirectional visible light communication systems utilizing existing LED technologies [1]. By using visible light, this system is utilizing a data carrier in the unregulated spectrum. This means it does not need to conform to existing RF standards and will not interfere with present RF technologies. Additionally, the proposed system will be line-of-sight unlike RF communication. This results in a system that ensures endpoint security and is less hackable by requiring visibility for communication.

Applications for such a system may find their place in hospital rooms. Secure indoor point-to-point communication links could be connected to medical sensors to actively monitor a patient's health. Since the system utilizes visible light, the communication link can be localized to a single patient's room without the fear of breach of data or confidentiality. Likewise, a miniaturized visible light communication system may be useful for wearable technologies. A high-bandwidth communication system might help wearables interface with other wearables nearby or facilitate the secure export of data to a host device.

The system being proposed would be especially useful in oceanic environments where other communication systems struggle. While most of the current research with LiFi is based on nondirectional LEDs, the system being proposed here has additional advantages by being a directional FSO. Directionality will increase the effective range of the communication link. A light-based FSO could have a theoretically range magnitudes greater than an RF system using the same amount power because of spectral attenuation. This type of system could be used in untethered rover exploration technologies or even high-bandwidth submarine communication systems.

1.3 Research Objectives

The objective of this research project is to create a microcontroller-based, full-duplex, high-bandwidth communication system for use in underwater environments. To begin this process, a theoretical analysis will take place to determine the best method to obtain optimal results in this underwater FSO system. A better understanding of optical principles relevant to data transmission in fresh water and saltwater environments will be gained. A determination of the exact EM frequency to use as the data carrier will be chosen based on this analysis. Additionally, an investigation will take place to decide the method of aligning the directional FSO.

With this theoretical analysis, the project will shift gears into a determination of system architecture and component selection. The system will need to be designed to create a full-duplex system achievable of 250KHz data rates. This system must be designed to integrate with the OpenROV without requiring any permanent modifications. The communication link must be robust and protect against outside noise sources, signal lost events, and attenuation during transmission. The FSO system should be self-aligning meaning that once it is initially aligned,

the system will actively maintain alignment of its optics. This system should then be tested in a free space environment with normal ambient lighting.

2 Literature Review and Theoretical Analysis

2.1 EM Attenuation

2.1.1 Overview

There are three main inherent optical properties of water that are of interest when analyzing light's interaction with water. These are absorption, scattering, and refractive index [2]. For the purposes of this project, only the first two will be described in depth. Refractive index is important but is beyond the scope of this initial investigation. However, it is important to note that refraction will play a complex role in the interactions of the FSO light beam as it passes through water currents, temperature gradients, and the surface of the body of water.

Ideally, the envisioned system will operate in clear waters. Even though this might not always be true, a discussion of the clearest natural waters will be more productive since this is a possible usage environment. Certain natural bodies of water such as the blue-violet waters of the South Pacific Gyre near Easter Island and Crater Lake in Oregon have water so clear it is hard to replicate a similar purity in a laboratory environment [2].

2.1.2 Attenuation Coefficient

The attenuation coefficient describes a signal's ability to propagate through a given material [3]. The coefficient "c" represents the attenuation coefficient which has units of (1/m). The attenuation coefficient is the combination of the absorption coefficient, "a" and the scattering coefficient, "b", as shown in Equation (2-1). In gases, scattering effects dominate the attenuation coefficients. However, in liquids, absorption is the dominating effect on total attenuation. In the continuing sections, brief descriptions of absorption and scattering effects will be given along with experimentally obtained values for their corresponding coefficients.

$$c_{total} = a_{total} + b_{total} \quad (2-1) [4]$$

A theoretical derivation will be given here to better understand the role that the attenuation coefficient plays in light degradation. A plane wave with a complex amplitude U travels through a medium in the direction z [3]. The magnitude of the plane wave will change as a function of distance. If there is attenuation in the medium, the intensity will be proportional to the absolute value of the complex amplitude squared. The resulting attenuation factor can be represented by Equation (2-2) .

$$\left| e^{-\frac{1}{2}\alpha z} \right|^2 = e^{-\alpha z} \quad (2-2) [3]$$

Furthermore, Beer-Lambert's Law (also known as Bouguer's Law) can be used to generate an expression for the intensity of the signal as a function of distance [5]. This relationship is shown in Equation (2-3).

$$I(z) = I(0)e^{-\alpha z} \quad (2-3) [5]$$

This expression in Equation (2-3) will be useful in further sections for determining the half power distance of absorption and scattering effects. This half power distance is the distance where the signal intensity is half of that of the original signal.

2.1.3 Absorption Coefficient

Absorption is the result of EM radiation transferring its energy to the molecular structure of the medium of travel [6]. In the case of light traveling through water, the light is absorbed based on the O-H vibrational modes of the water molecules. Different frequencies of light will interact differently with these vibrational modes and have different absorption rates as a result. The full expression for the absorption coefficient is shown by Equation (2-4).

$$a_{total} = a_{pure\ water} + a_{particles} + a_{dissolved\ organics} \quad (2-4) [4]$$

Generally, absorption coefficients of liquids are determined using transmission techniques and then corrected for scattering. However, in certain investigations, the absorption coefficient is measured with techniques inherently insensitive to scattering effects such as those presented by Sogandares and Fry [5]. The aggregation of absorption coefficients as a function of wavelength from various papers is shown in Figure 2.1. Additionally, the half power distance was calculated using Beer-Lambert's Law in Equation (2-3) considering only absorption effects with the results of these calculations shown in Figure 2.2.

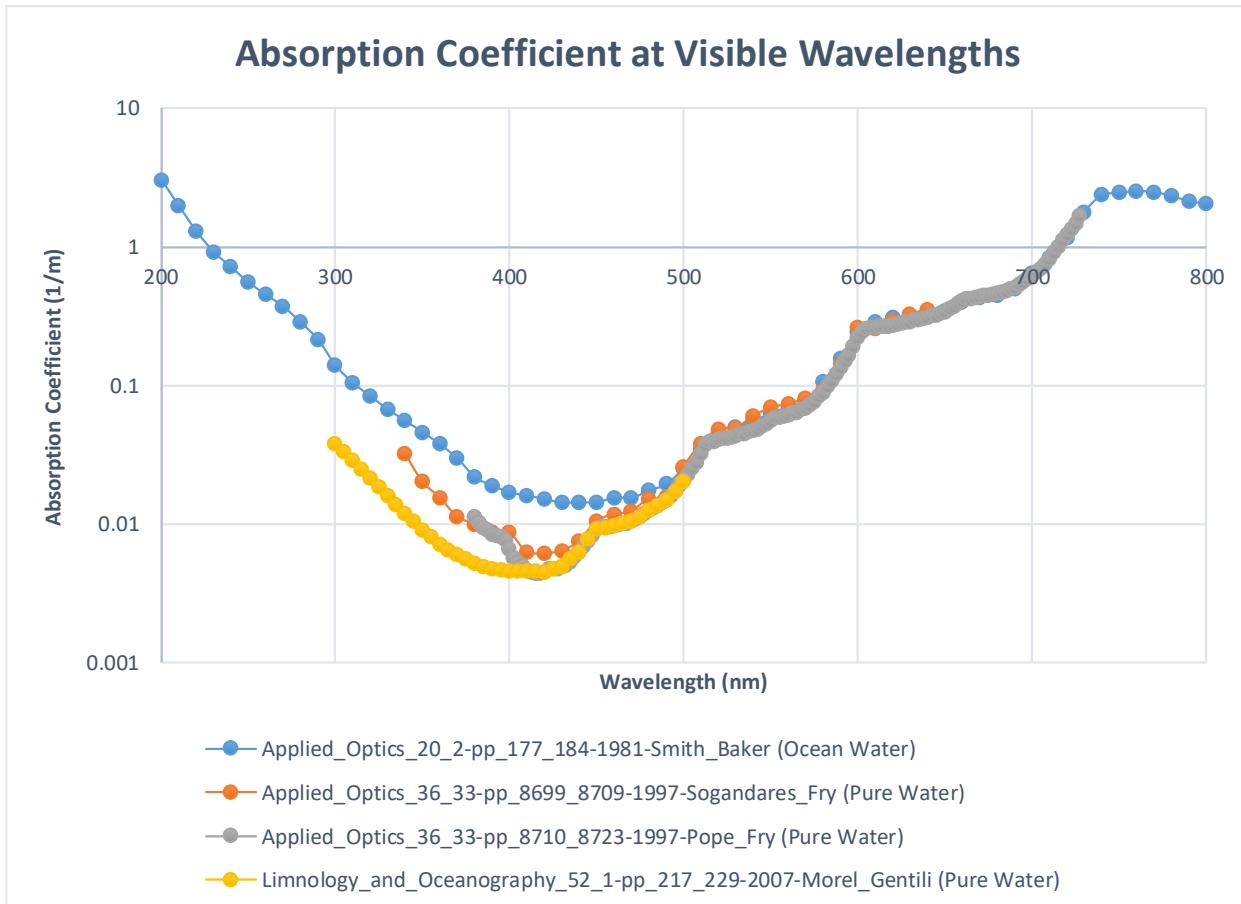


Figure 2.1: Absorption coefficient comparison from various sources

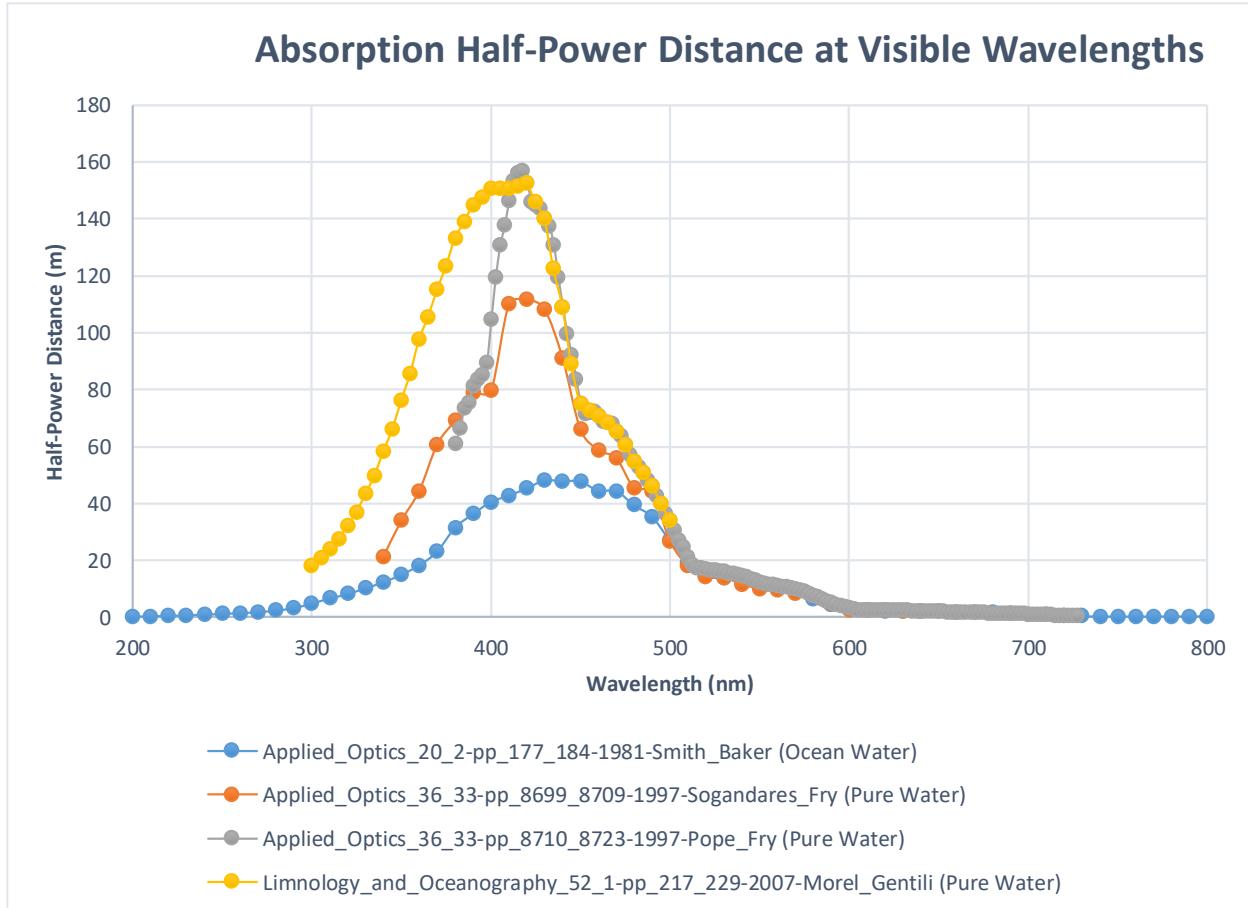


Figure 2.2: Theoretical half-power distance calculations considering only absorption effects

2.1.4 Scattering Coefficient

Scattering effects were first observed by Lord Rayleigh who discovered "...that an optically pure medium scattered [light] because of the discontinuous structure of matter," [7]. Scattering can be broken up into two parts: forward scattering and backward scattering. Scattering can be caused by suspended particulate matter as well as density fluctuations in an entirely pure liquid [8]. The full expression for the scattering coefficient is shown by Equation (2-5).

$$b_{total} = b_{molecular \text{ for } pure \text{ water}} + b_{molecular \text{ for } particles} \quad (2-5) [4]$$

Scattering coefficients are very difficult to measure for the following reasons: the absolute calibration of the measurement tools, the presence of ambient light, and the purification of water

[7]. Scattering is seen to increase as the salinity of the water increases. This means there should be different system performance in fresh water versus saltwater. The combination of scattering coefficients as a function of wavelength from various papers is shown in Figure 2.3. Additionally, the half power distance was calculated using Beer-Lambert's Law in Equation (2-3) considering only absorption effects with the results of these calculations shown in Figure 2.4.

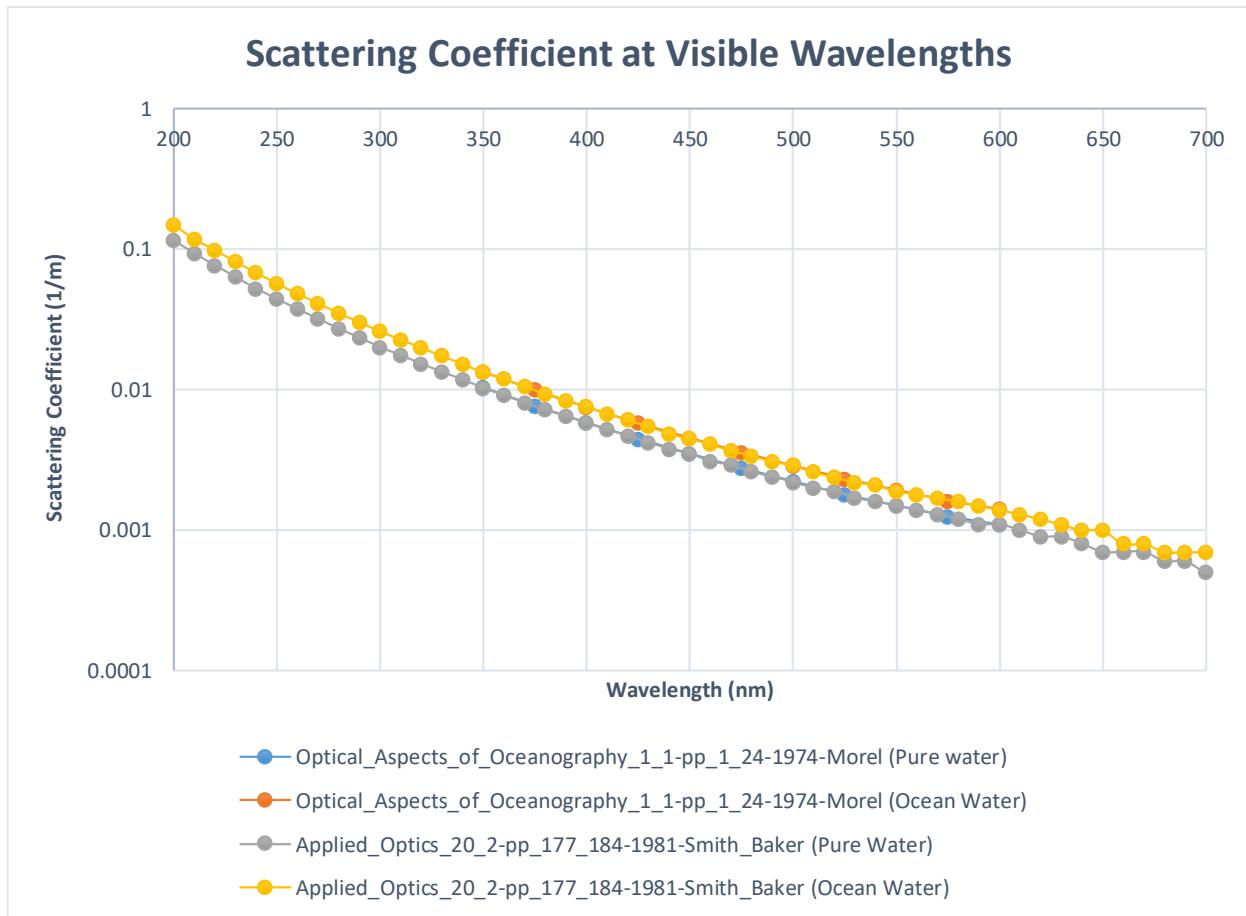


Figure 2.3: Scattering coefficient comparison from various sources

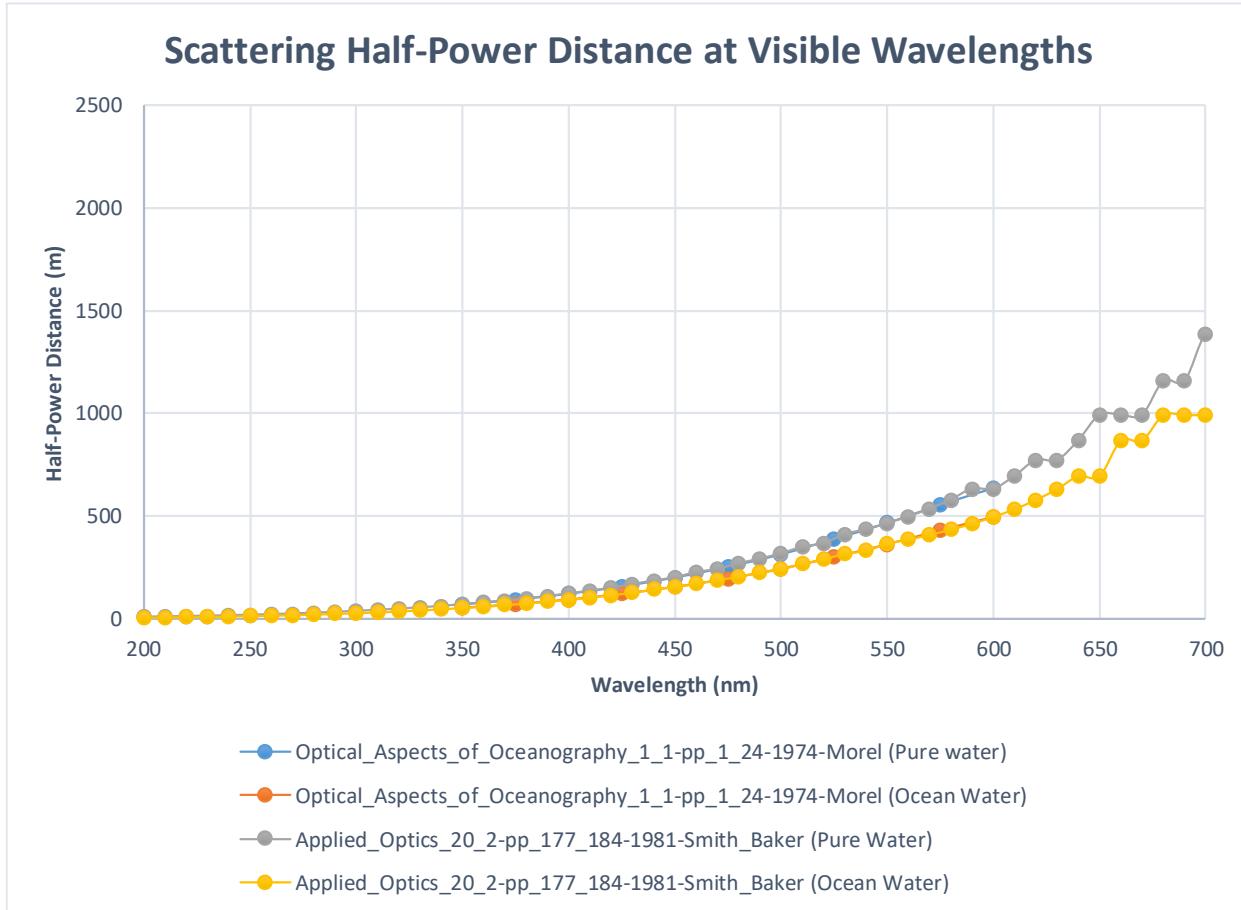


Figure 2.4: Theoretical half-power distance calculations considering only scattering effects

2.2 Controls

2.2.1 Quadrant Photodiode

A quadrant photodiode (QP) will act as the main device to interpret light signals from the distant laser diode. A brief theoretical description will be given here to understand the sensor's role in this system. The QP consists of a high-resistivity semiconductor substrate, four quadrant regions of opposite conductivity types, and V-shaped grooves to refract incident light redirecting them toward their corresponding quadrants [9]. The positional resolution is determined by the distance between adjacent quadrant electrodes as well as the optical crosstalk between adjacent regions.

An illustration of a QP from the original patent is shown in Figure 2.5.

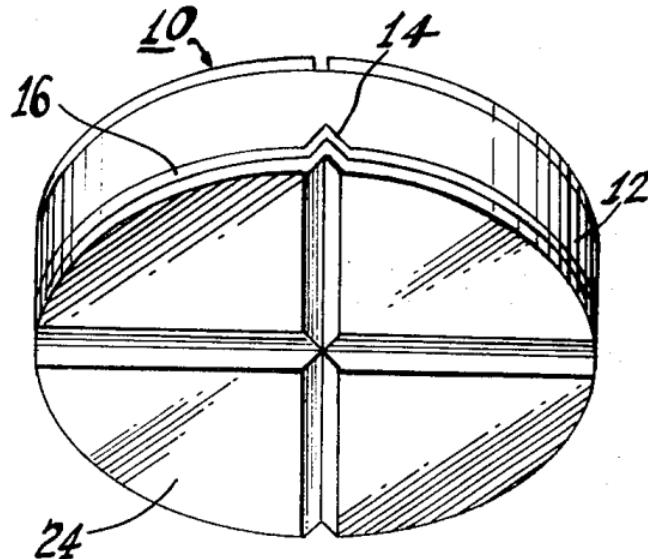


Figure 2.5: Original drawing of QP with symmetric quadrants separated by V-shaped grooves

QPs are commonly used in laser beam tracking systems. The position of the beam can be determined by measuring the response of the different quadrant electrodes. As light is incident on each quadrant, the voltages on each quadrant will be proportional to the amount of light power incident [10]. It is often helpful to derive directional components from the QP response. This can be done by determining the horizontal components of the response as shown in Equation (2-6) and Equation (2-9) and the vertical components of the response as shown in Equation (2-8) and Equation (2-9)¹.

$$V_{Left} = V_1 + V_4 \quad (2-6) [10]$$

$$V_{Right} = V_2 + V_3 \quad (2-7) [10]$$

$$V_{Top} = V_1 + V_2 \quad (2-8) [10]$$

$$V_{Bottom} = V_3 + V_4 \quad (2-9) [10]$$

¹ These equations assume the top-left quadrant is designated quadrant one and numbering continues in a counterclockwise fashion.

Using these components, the control alignment activities of the QP become more obvious. As these values drift, one may become larger than the others. If this occurs, the distant transceiver should try to correct for this misalignment by steering away from that quadrant toward the origin. An example response of the QP's horizontal components as a laser beam traverses laterally across the QP is shown in Figure 2.6².

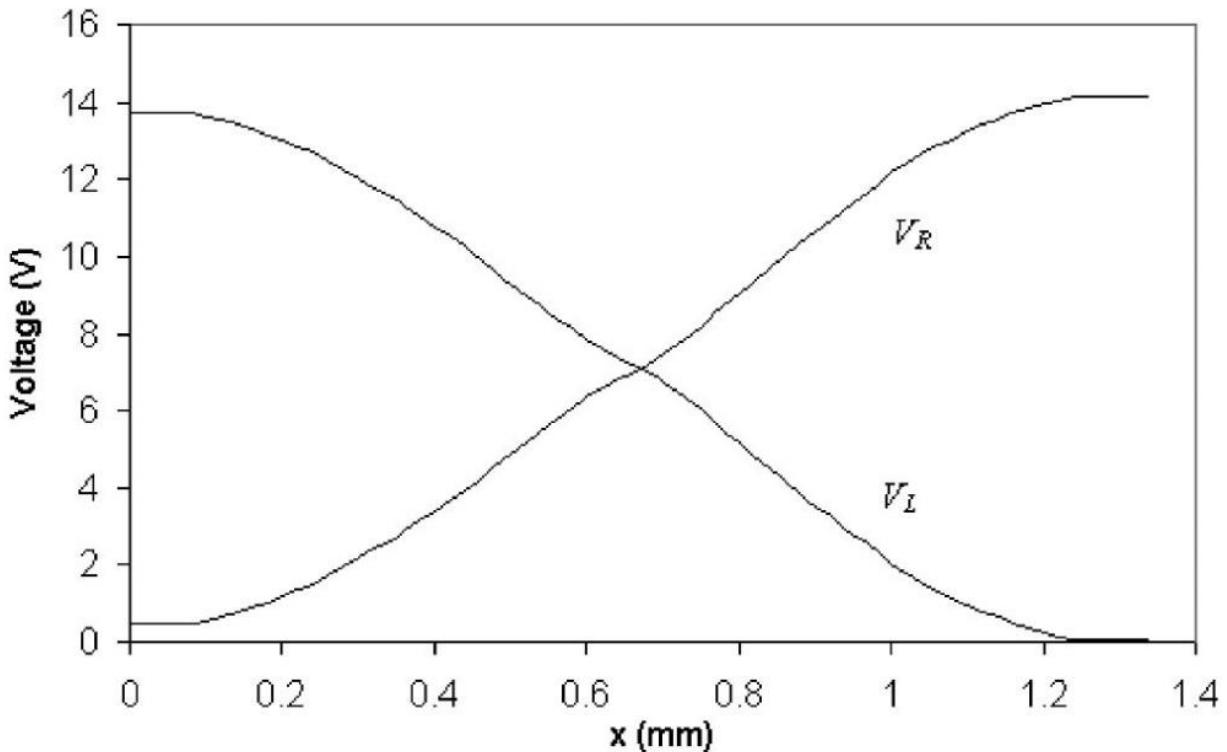


Figure 2.6: QP response of the left (VL) and right (VR) components during lateral movement

² This assumes the laser beam is centered vertically on the QP throughout.

3 System Design

3.1 System Level

The high-level system design of the transceiver is shown in Figure 3.1. The core components of each transceiver (excluding interfaces) are the following: the transmitter module, the receiver module, and the control module. The two main external interfaces are the debug interface and Ethernet interface. These interfaces are used for miscellaneous debugging and Ethernet packet input/output, respectively. The transmitter and receiver module along with the debug and ethernet interfaces form the data plane. The control module is the sole block in the control plane. Together, the data plane and control plane construct the entirety of a single transceiver which satisfies all requirements as outlined for this research project.

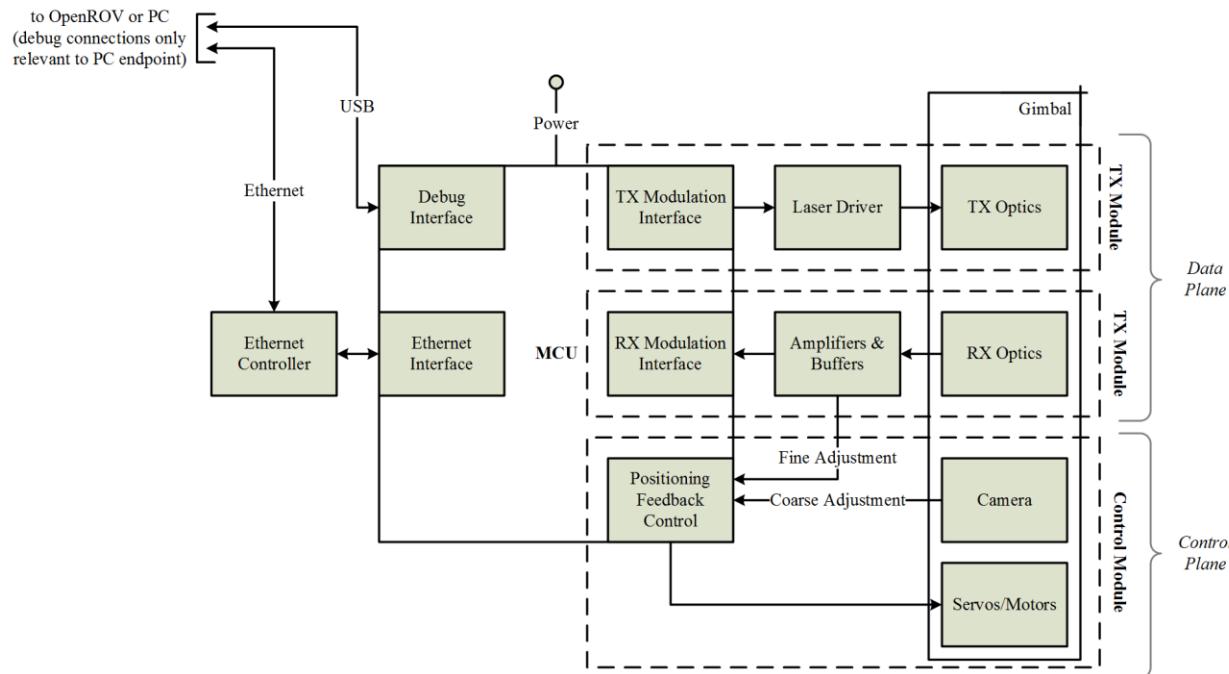


Figure 3.1: High-level system design of single transceiver

The physical manifestation of the high-level design is the combination of four separate PCBs. These PCBs are integrated to satisfy the functional blocks detailed in Figure 3.1. A detailed

description of the integration of these different boards into the final system will be given in the system integration section. These four boards are the MikroElektronika Clicker 2 PIC32MX development board containing the MCU, the MikroElektronika Ethernet Click daughtercard containing the RJ45 interface and Ethernet controller, the MikroElektronika Camera Click daughtercard containing the CMOS image sensor and processor, and the custom optics board containing the transmitter and receiver modules. Figure 3.2 gives a graphical briefing of the interconnection and scale of these different boards. This also serves as the initial architecture and layout for the optics board. It does not represent the final system, only an initial revision for feasibility and scale.

The main deliverable of each transceiver is Ethernet packets. Ethernet packets are received from the PC/OpenROV endpoint via the Ethernet daughtercard and sent to the distant transceiver via the transmitter module. Likewise, Ethernet packets are received from the distant transceiver via the receiver module and passed on to the connected PC/OpenROV endpoint via the Ethernet daughtercard. Additional information is embedded in the data transmission and used for control purposes. Because of this, the transceivers have inherent overhead in the data stream. This may be a benefit for future work as the protocol is structured to have full control over the flow of data which could lead to easy improvements for error correction processing such as minimum Hamming distance.

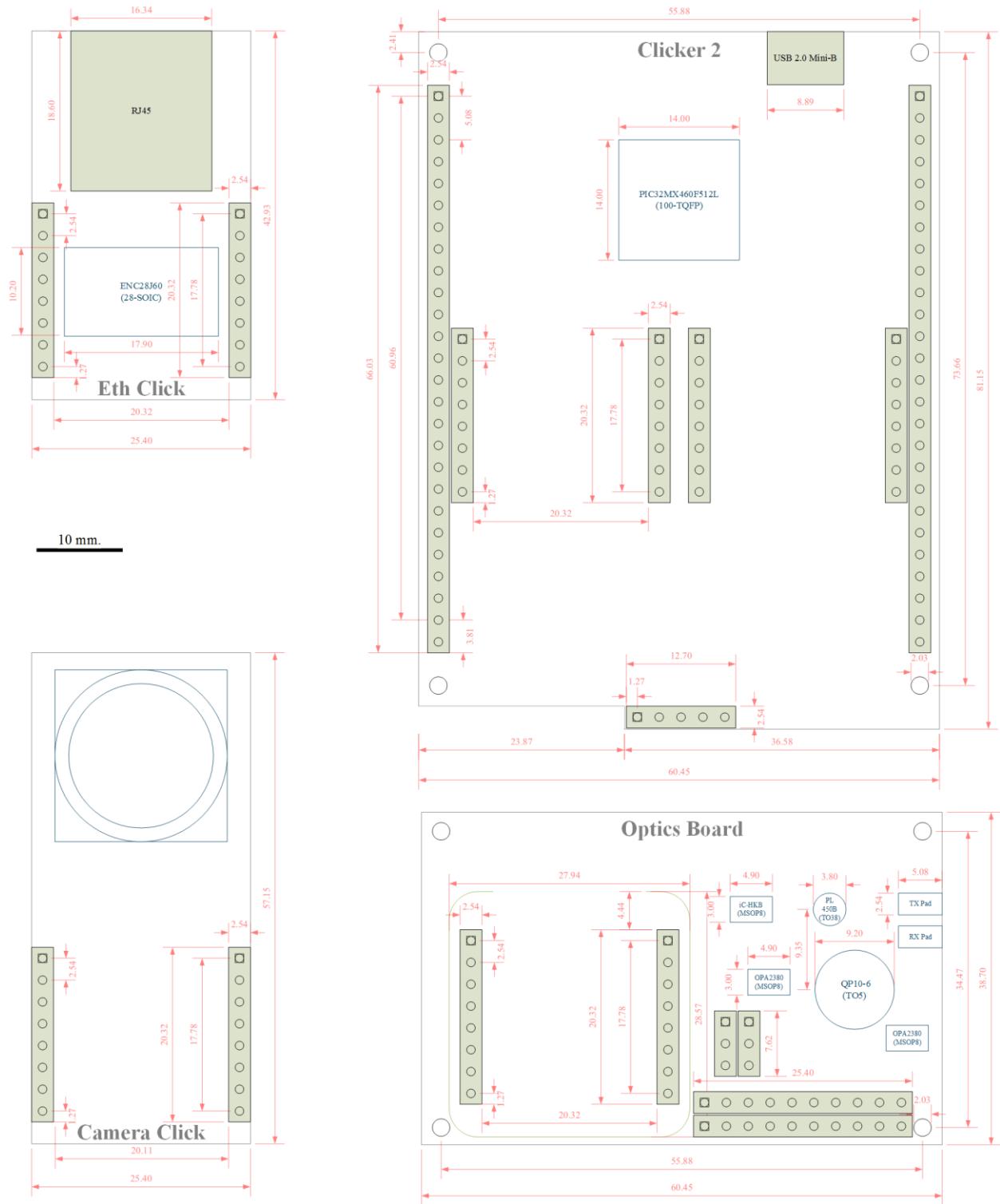


Figure 3.2: Initial layout detailing four PCBs of single transceiver³

³ Does not reflect final layout or architecture of optics board, PCB size and components are to accurate scale as per legend, all units are in millimeters unless otherwise state

3.2 Microcontroller Unit (MCU)

Having a single MCU to handle asynchronous operations to keep the incoming and outgoing data streams up while still having sufficient operating margin to maintain alignment operations presents an interesting problem. However, the benefits of having a single onboard controller per transceiver are numerous: smaller system size, more maintainable code base, and the interoperability between shared resources (i.e. Ethernet controller, debugging interface).

A 32-bit microcontroller was chosen since an 8- or 16-bit MCU would be largely underpowered to maintain a full-duplex, high-bandwidth communication link. Additionally, 32-bit MCUs offer additional capabilities for peripherals and networking such as pluggable image sensor daughterboards, onboard MAC and PHY, and readily available TCP/IP stacks to interact with Ethernet-friendly LAN networks.

There were many considerations for choosing an MCU best suited for this system. A multi-channel, high-resolution ADC would be necessary to service the four receiver channels on the QP as well as monitor important voltage/current sense measurements. PWMs would be central in controlling analog servos for movement capabilities capacity. SPI functionally would be needed to interact with Ethernet controllers or image sensor daughterboards. A large program memory should be available to comfortably hold the execution commands for all the tasks within the data and control planes. Additionally, preference to MCUs in packages more conducive to prototyping (i.e. no BGA or QFN packages) were given to allow for easy hand-soldering and reworks especially in the desire to eventually move the entire transceiver to a single PCB.

Microchip's PIC32MX (hereafter referred to as "MCU") was chosen as the main microcontroller to execute data and control plane operations. This MCU offers all capabilities needed for the transceiver system to be built. Specially, a PIC32MX4XX family MCU was selected which

boasts the following capabilities as per Microchip's PIC32MX3XX/4XX Family Data Sheet [11]:

- 80MHz operating frequency (1.56DMIPS/MHz)
- Separate PLLs for CPU and USB
- Two SPI modules (needed to interface with Ethernet and Camera daughtercards)
- Five 16-bit Timers (two pairs can be combined to form two 32-bit timers)
- Five PWM outputs
- High-speed I/O pins (up to 800MHz)
- 16-channel 10-bit ADC (1Msps at +/-1LSB)

3.2.1 Pin Description and Usage

The PIC32MX460F512L is a 100-pin TQFP device that is present on the Clicker 2 PIC32MX development board. An illustration of the pins utilized in this system and their general function is shown in Figure 3.3. In this figure, the pins have been color-colored to help visualize their usage within the proposed system. Only the pins essential to this system have been marked.

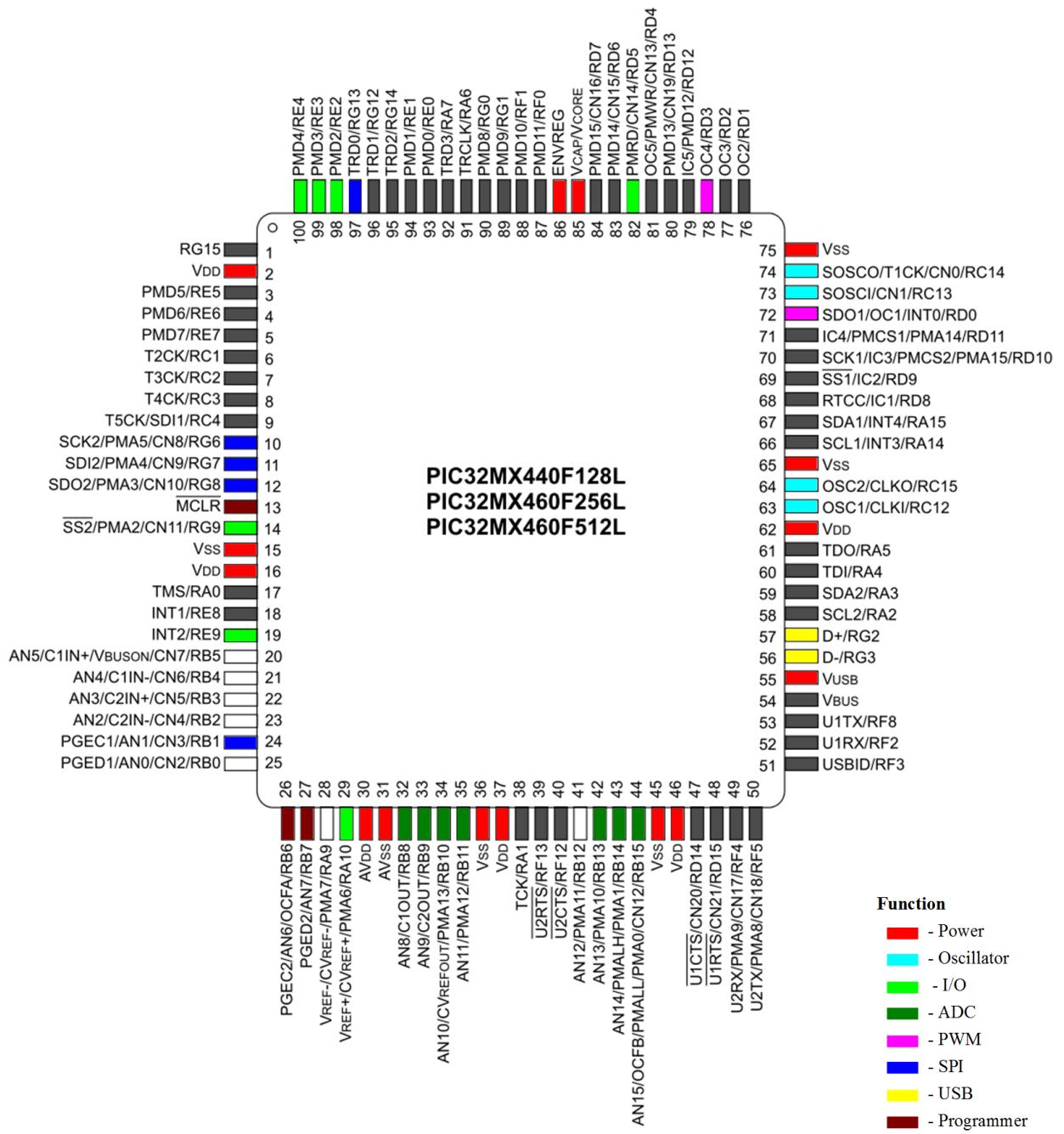


Figure 3.3: Description of pins in the system and their general function

Likewise, Table 3.1 lists a more detailed description of utilized pins and their specific function.

This pin mapping was used in the firmware code to define a separate hardware configuration file allowing for a modular system that is not necessarily dependent on this certain MCU. This type

of abstraction is crucial in creating a system that could be upgraded to a higher-performing PIC32 device such as the PIC32MZ or another MCU entirely.

Table 3.1: Summary of utilized pins and their function⁴

Pin	Pin Function	Usage (Clicker 2)
63, 64	OSC1, OSC2	8MHz oscillator
73, 74	SOSCI	32kHz oscillator
56, 57	D-, D+	USB differential pair data lines
72, 78	OC1, OC4	PWM for pan/tilt servos
10, 11, 12	SCK2, SDI2, SDO2	Ethernet/camera SPI SCK, MISO, MOSI
97	RG13	Ethernet SPI slave select
18, 98	INT1, RE2	Ethernet interrupt, reset line
24	RB1	Camera slave select
19	INT2	Camera interrupt
82	RD5	Laser load switch enable
79, 80	RD12, RD13	Laser control channel 1 and 2
32	AN8	Laser voltage sense ADC channel
33, 34	AN9, AN10	Laser low-side current sense ADC channels
35, 42, 43, 44	AN11, AN13, AN14, AN15	Receiver amplifier output 1, 2, 3, and 4 for ADC channels
99, 29	RE3, RA10	Debug LEDs (LED1, LED2)
100, 14	RE4, RG9	Debug Switches (T2, T3)

3.2.2 Oscillator Configuration

The MCU features a primary and secondary oscillator. Both oscillators have options to use either internal or external sources. To ensure stability and consistency of clocking between both transceivers, external sources are used in the case of the primary and secondary oscillator. An external 8MHz crystal oscillator is provided as the source for the primary oscillator while an external 32.768kHz crystal is provided for the input to the secondary oscillator to the PIC32MX [12]. These external crystals are mounted on the Clicker 2 PIC32MX development board.

The primary oscillator passes through different scalers and PLLs to provide the system clock, the peripheral bus clock, and the USB clock in the custom configuration shown in Figure 3.4. The secondary oscillator supplies the initial source to the real-time clock. Since the current system

⁴ This listing excludes any pins relating to power or ICD programming pins

does not employ any immediate use of real-time clocking applications, the focus of discussion here will be on deriving the system clock, peripheral bus clock, and the USB clock from the primary oscillator.

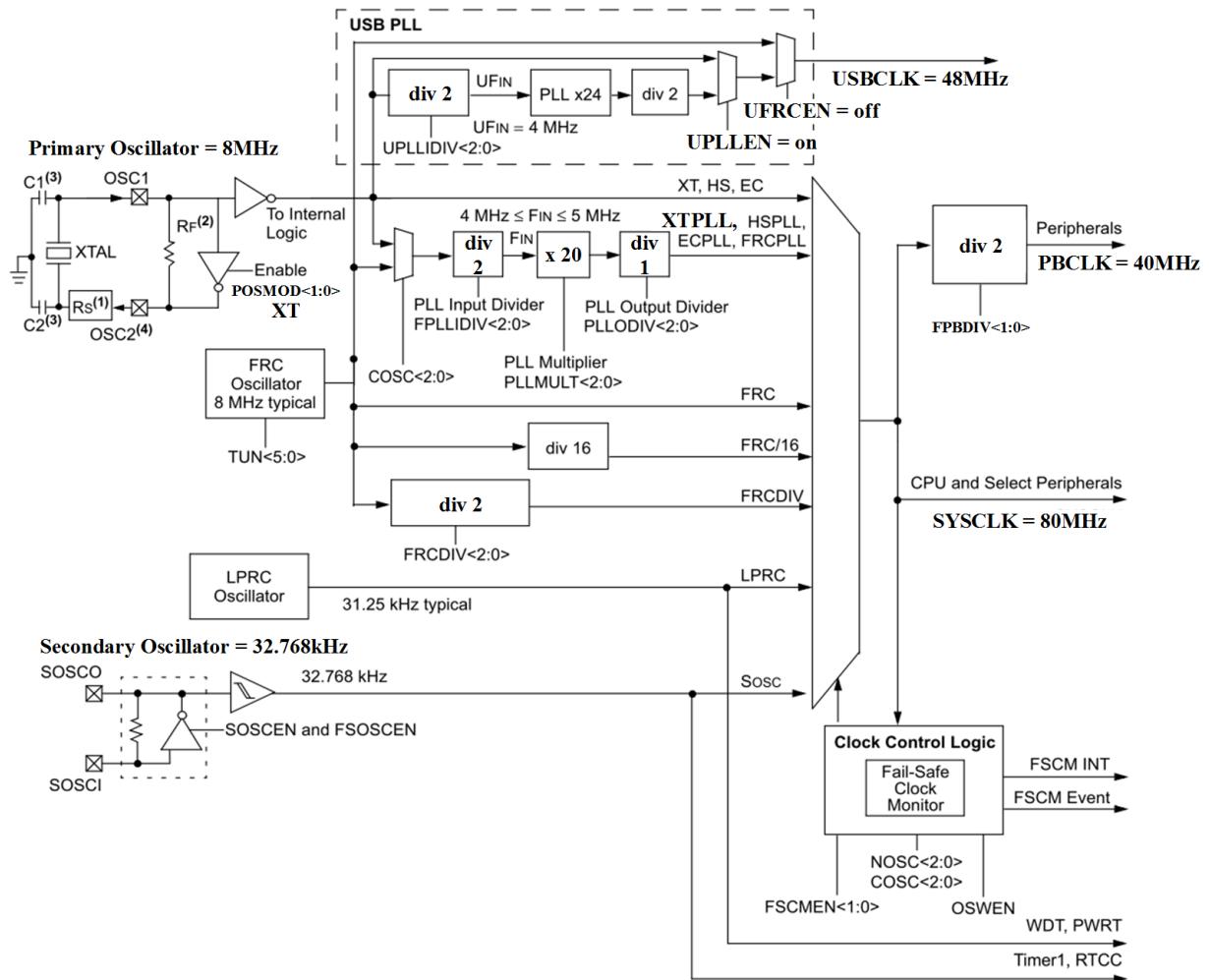


Figure 3.4: Clock configuration as used on MCU⁵ [11]

The system clock is formed by first configuring the POSMOD and FNOSC registers so that the primary oscillator is configured to use an external resonator/crystal source and the main PLL module is enabled. This primary oscillator input will be the source for the MCU's internal PLL that will supply the system clock. The PLL has a configurable input divider (FPLLIDIV),

⁵ Bold text represents user-defined configuration settings specific to this system

multiplier (PLLMULT), and output divider (PLLORDIV) each of which can be configured to the adjust system clock output frequency (FOSC) as shown in Equation (3-1).

$$FOSC = FIN \times \frac{PLLMULT}{PLLORDIV} \quad (3-1)$$

The frequency FIN must be within the range of 4-5MHz and is described by Equation (3-2) where POSC is the primary oscillator input frequency.

$$FIN = POSC \times FPLLIDIV \quad (3-2)$$

Using the clocking illustration in Figure 3.4 for reference, FIN is calculated as 4MHz resulting in a system clock frequency of 80MHz. 80MHz is the fastest this MCU is rated to run and will provide the most margin for successful firmware execution. The peripheral clock bus frequency (FPB) is easily derivable from the system clock frequency as shown in Equation (3-3). FPB is calculated as 40MHz and supplies clocking for many of the MCU's onboard peripherals including the PWM, ADC, and timers. Setting the peripheral clock bus to half the speed of the main system clock will result in quick peripheral servicing.

$$FPB = \frac{FOSC}{FPBDIV} \quad (3-3)$$

Lastly, the USB clock has its own dedicated PLL which must be configured to generate an exact frequency of 48MHz for USB activities. The USB clock frequency (USBCLK) is generated based the PLL input divider (UPLLIDIV) and input values describe by Equation (3-4). Looking at Figure 3.4, it can be seen that a UPLLIDIV divide value of 2 is all that is needed to create a USB clock running at 48MHz.

$$USB = POSC \times \frac{24}{UPLLIDIV \times 2} \quad (3-4)$$

3.2.3 I/O Ports

The PIC32MX460F512L has 85 I/O pins [13]. Since these pins are shared with other peripherals on the MCU, less of these pins will be available for general I/O purposes depending on which modules are enabled. The I/O pins are organized into separate ports labeled A-G. Each I/O port has nine configurable registers associated with the operation of the port along with one control register. Knowledge of a few of these registers is key to understanding the role I/O pins play in this system.

All 85 of these I/O pins can be configured as either digital inputs or digital outputs. At power on, all I/O pins on the device are initially configured as inputs [13]. Each pin has an associated tristate function bit within that port's TRISx⁶ register. This TRISx register controls the pin's configuration as either an input (bit=1) or output (bit=1). When configured as an input, the PORTx register can be used to read the digital representation of voltage at the node of I/O pin. It is important to keep in mind that the I/O pin will act only as a digital input. If a pin is to be set as an analog input for use by the ADC module, that pin must be analog compatible, and its ANSELx bit must be set as well as its TRISx bit.

When configured as a digital output, the I/O pin will be capable of toggling at speeds up to 80MHz [11]. The LATx register bits can be modified to latch desired logic states to the pins. This toggling operation is vital in creating the control signals to modulate laser diode. Additional registers are available for even faster manipulation digital outputs. These registers labeled LATxSET, LATxCLR, and LATxINV guarantee atomic bit manipulations⁷ when used to change the state of the I/O pin [13].

⁶ “x” denotes the port letter of the I/O pin in question

⁷ Atomic bit manipulations are bit changes that occur in a single step relative to other threads

3.2.4 Interrupts

The chosen MCU has 256 interrupt sources that can generate requests from peripheral modules, the processor core, and external inputs [14]. The MCU responds to interrupt events using a multi-vector mode approach giving precedence to events with higher priority levels. Each module capable of generating interrupts (i.e. ADC, USB, timers) can be assigned one of seven interrupt priority levels. Modules with a higher priority level set that generate an interrupt event will cause a break in the current thread to service the higher priority interrupt before returning to the lower priority interrupt. Additionally, modules also have a configurable sub-priority level. A module with the same priority level set but a higher sub-priority will not intrude on an ongoing interrupt of the same priority level but will be serviced before the other interrupt event if both modules have pending interrupt events.

A brief illustration showing the key interrupts for the system along with their priority level ordering is shown in Figure 3.5. The envisioned system uses two interrupt sources for the receiver module (Timer5 for clock recovery and the ADC module for data recovery) and one interrupt source for the transmitter module (Timer4 for the laser diode modulation). Separate interrupt sources for the SPI and USB modules are necessary for interfacing with peripherals.

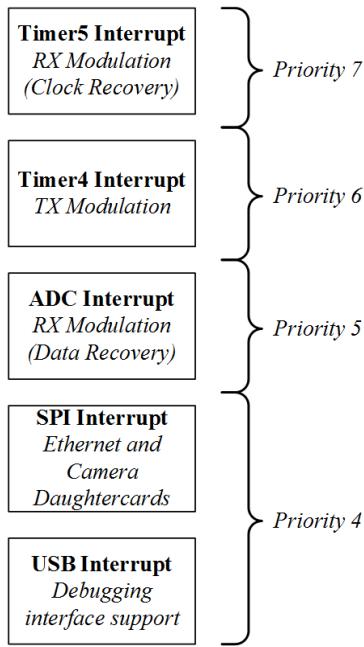


Figure 3.5: Hierarchy of notable interrupt sources and their priority levels

Timing critical interrupts such as clock recovery operations are given precedence over interrupts that have more leeway with regard to timing. Figure 3.5 may be misleading without fully considering other architectural factors. For example, the ADC module is configured to generate an interrupt once every eight conversion sequences while filling the opposite eight ADC buffers. This allows the ADC module to be serviced much more rarely than other modulation tasks.

3.2.5 Timers

The MCU has five 16-bit timers each with dedicated clock prescalers controls [15]. Two pairs of these timers can be configured as 32-bit timers although this functionality is not used in the current system. A visual overview of the timer modules available on the MCU and their general usage is illustrated in Figure 3.6. Two timers are devoted to modulation activities while another timer is used in PWM timing for servo control. Another unconventional timer exists on board Microchip's MIPS M4K core devices, the core timer. Unlike other timers, the core timer has a resolution of 32-bits, a fixed 1:2 prescaler, and is fed directly by the system clock. This makes it ideal to use for benchmarking, interrupt service timing, and miscellaneous main thread tasks.

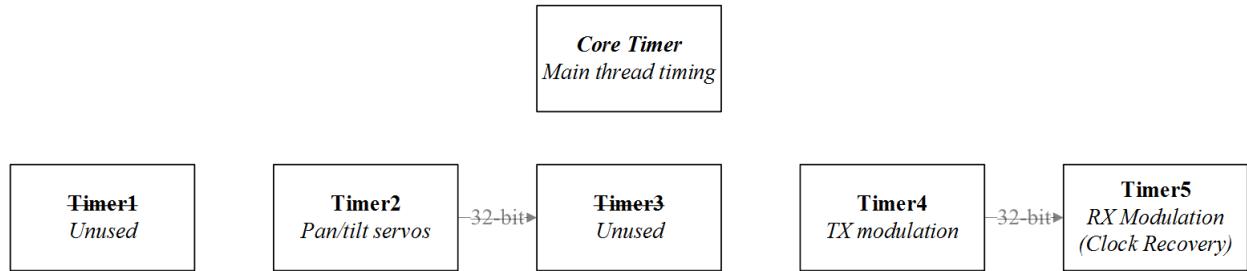
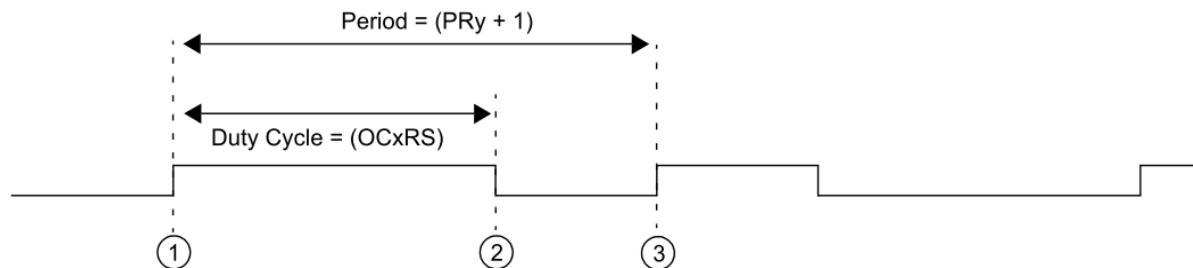


Figure 3.6: Summary of timers used in system and their function⁸

3.2.6 Output Compare/Pulse Width Modulation (PWM)

The MCU has five output compare modules that can generate pulses in response to time events [11]. These output compare modules can be used in intricate 32-bit time base dual compare modes or in simple PWM manners. For the purposes of this system, output compare modules will only be used in PWM capacities to generate a train of pulses to control the analog servos for the gimbal. The general waveform and operation of an output compare module to create a PWM pulse is shown in Figure 3.7.



- ① Timery is cleared and the new duty cycle value is loaded from OCxRS into OCxR.
- ② Timer value equals the value in the OCxR register; OCx Pin is driven low.
- ③ Timer overflow; value from OCxRS is loaded into OCxR; OCx pin is driven high. TylF interrupt flag is asserted.

Figure 3.7: PWM model waveform and register configuration [16]

A single 16-bit timer will be used as the time base for the PWM module controlling the pan/tilt servos. The control registers corresponding to each servo's PWM module will be configured so

⁸ Components with strikethroughs represent unused functions/modules

that the period and duty cycle of the signals drive the servos. It is generally good practice to run analog servo PWM control signals with a period of 20ms. Equation (3-5) can be used to obtain this period where PR is the timer period register and TPB is peripheral clock period.

$$\text{PWM Period} = [(PR + 1) \times TPB \times (\text{Timer Prescale Value})] \quad (3-5)$$

[16]

This PWM period is set in firmware by using custom functions to set the associated timer to the minimum prescaler that still allows the timer to reach the desired period. This allows for dynamic setting of the time base of the PWM module generating the most accurate period possible. Observing the control registers after setting a desired period of 20ms to a 16-bit timer, it is seen that the timer period register (PR) holds a value of 49,999 and the timer prescaler is 1:16. Given a peripheral clock period of 25ns, these control register values indicate a PWM period of exactly 20ms as per Equation (3-5). This illustrates how these custom functions set the PWM period with maximum accuracy.

The maximum PWM resolution can be calculated using Equation (3-6). Considering a 16-bit timer for the PWM module's time base and a period of 20ms, the maximum PWM resolution can be calculated as 15.6 bits. If a 32-bit timer were to be used for the time base, the PWM module would have a maximum resolution of 19.6 bits. The increase in PWM resolution resulting from using a 32-bit timer will be seen in later sections as unproductive.

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}(PR + 1)}{\log_{10}(2)} \quad (3-6)$$

[16]

The duty cycle of the signal is controlled by a separate register, OCxRS⁹. The value in this register corresponds to the duty cycle relative to the time base set for the output compare module. The gimbal uses Hitec HS-645MG servos for both the pan and tilt movements. These servos have an operating range of 180 degrees with a neutral position corresponding to a pulse width of 1.5ms [17]. Like the PWM period, custom functions automate the setting of the PWM duty cycle. This results in the greatest resolution of control over the duty cycle. Sample calculations for a 1.5ms duty cycle results in a OCxRS register value 3750 which can be verified by Equation (3-7)(2-9).

$$\text{PWM Duty Cycle} = \frac{\text{OCxRS} \times (\text{Timer Prescaler Value})}{\text{FPB}} \quad (3-7)$$

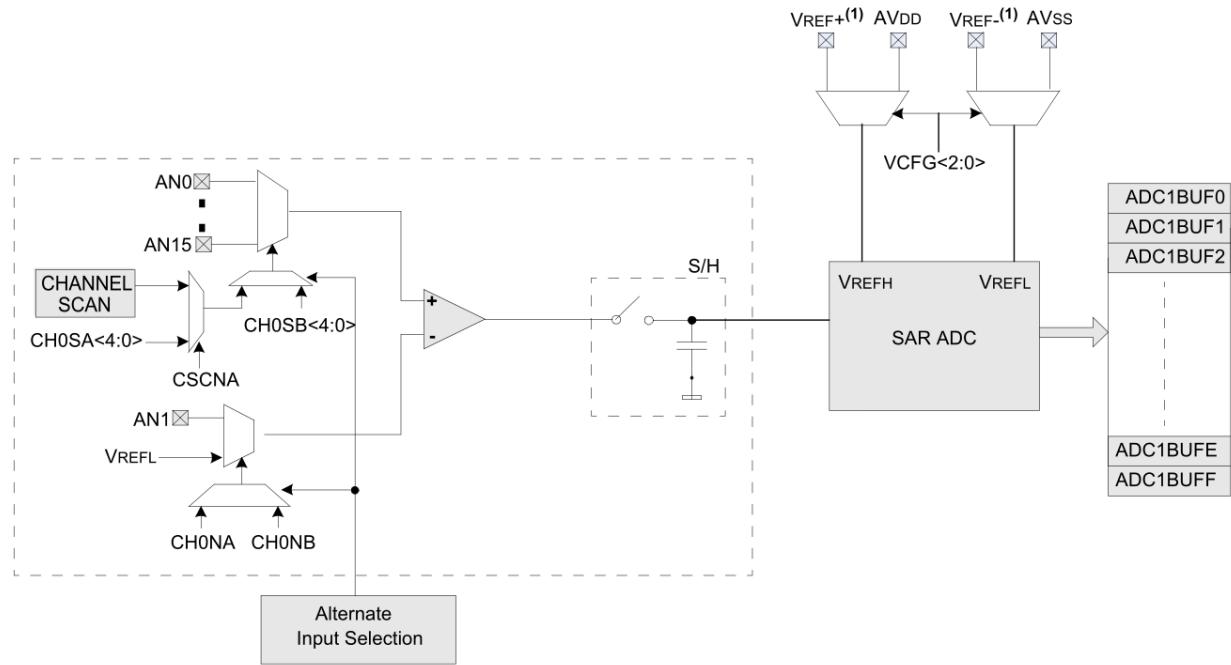
3.2.7 Analog-to-Digital Converter (ADC)

Overview

The ADC module is the focal MCU peripheral of the entire system. Its proper operation is essential in keeping a constant data link up as well as sensing for optical misalignment. A theoretical overview of ADC functioning will first be described followed by application specifics of its usage in the transceiver.

The MCU being used is equipped with a single 10-bit SAR ADC module capable of running at 1Msps [18]. Within the module's circuitry, 16 analog inputs are directed into two independent multiplexors leading to a S/H amplifier. The module is capable of automatic scan modes even during CPU sleep and idle modes. A high-level illustration of the module is shown in Figure 3.8.

⁹ “x” denotes the output compare module being utilized



Note 1: VREF+, VREF- inputs can be multiplexed with other analog inputs.

Figure 3.8: Block diagram of ADC module with the SAR ADC abstracted [11]

To sample an analog input, the input node is selected by the active multiplexer using register controls. The analog input's voltage is then connected to the S/H amplifier during the sample sequence of the ADC. The ADC module then disconnects the S/H amplifier from the analog input and proceeds to convert the voltage held in the S/H amplifier to a digital value using a SAR approach. During this conversion sequence, a different analog input is multiplexed to the S/H amplifier if necessary. This ADC sample and conversion sequence is shown in Figure 3.9.

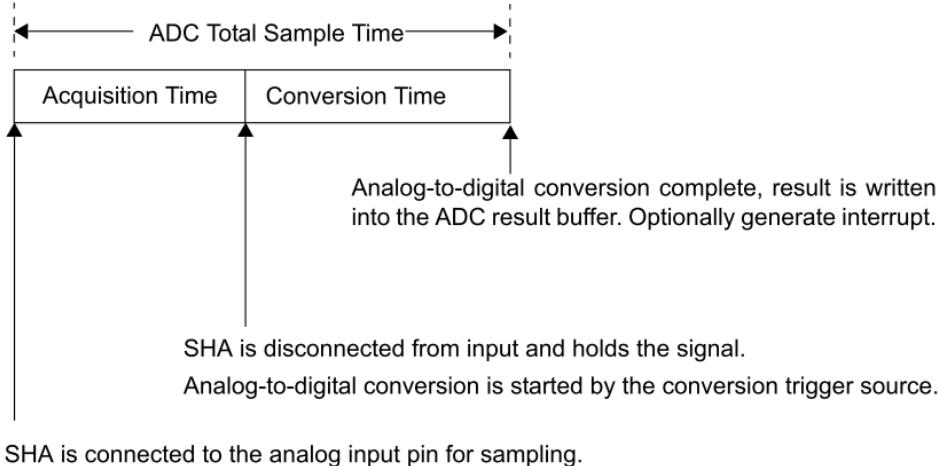


Figure 3.9: ADC sample/conversion sequence [18]

After conversion, the buffer will hold a digital value representing the voltage of the analog input recently sampled and converted. However, the accuracy of the result held in the buffer will be constrained by both the resolution of the ADC (10-bits) and sources of noise. An ideal transfer function of a theoretical 3-bit ADC module considering no noise is shown in Figure 3.10.

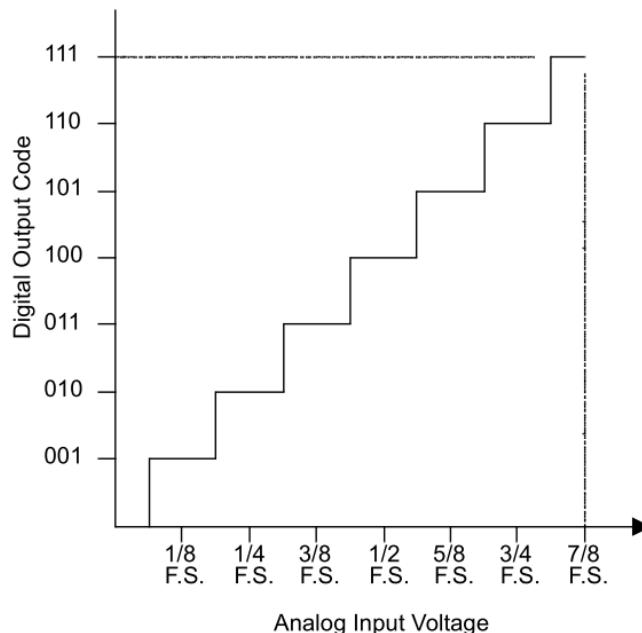


Figure 3.10: Ideal transfer function of theoretical 3-bit ADC [19]

Even though this graphic represents a 3-bit ADC, this transfer function can easily be extrapolated for a 10-bit ADC. Another important note here is that the quantization error of a noiseless ADC

measuring a linear ramp signal will be +/- 0.5LSB at its maximum [19]. This quantization error phenomenon can be shown graphically as in Figure 3.11. Additionally, external noise sources can be limited by using a differential analog input to cancel out common mode noise.

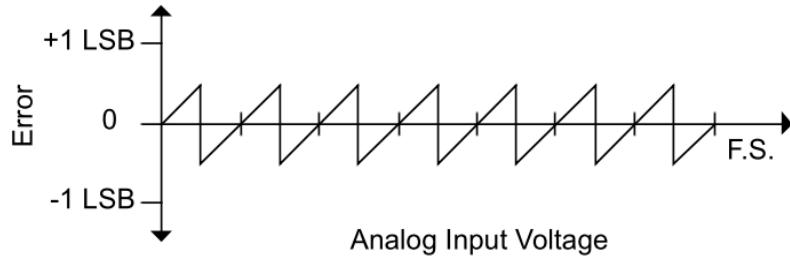


Figure 3.11: Quantization error of linear ramp signal due to limitations of SAR ADC [19]

Calculations for 1Msps Operation

Sample calculations to show the MCU's maximum sampling speed will be given since maximum speed will be needed to accurately interpret signals captured by the ADC module from the QP channels. To achieve 1Msps operation, the ADC module is operated in auto-sample and auto-convert modes to ensure predictable timing sequences. There are two control registers responsible for timing [18]:

- SAMC – controls the auto-sample time of each ADC sample/conversion sequence
- ADCS – sets the ADC clock cycle, TAD, which is based off the peripheral clock source

The following limitations of the MCU's ADC module need to be kept in mind during timing configuration [11] [18]:

- Minimum TAD = 65ns
- Minimum sampling time = 132ns
- Minimum ADC conversion clock cycles = 12 TAD (1 TAD per bit plus 2 TAD)
- MCU voltage supply requirement: $3.0V < VDD < 3.6V$

The total ADC sampling/conversion sequence is the combined time required to sample plus the time required to complete conversion as shown in Equation (3-8). On the other hand, the ADC clock cycle period is a function of the peripheral clock frequency (TPB) and the ADCS register value as shown in Equation (3-9).

$$(Total\ Sequence\ Time) = (Sampling\ Time) + (Conversion\ Time) \quad (3-8)$$

$$TAD = 2 \times [TPB \times (ADCS + 1)] \quad (3-9) [18]$$

With a peripheral clock frequency of 40MHz, an adequate configuration for the ADCS register would set the ADC conversion clock to half the frequency of the peripheral clock so that a TAD equals 50ns. Assuming 12 TAD will be needed per conversion cycle (conversion time = 600ns), setting the SAMC register to 8 TAD (sampling time = 400ns) results in 1Msps ADC operation.

Signal Capture Approach

The ADC module is run in auto-scan mode with Multiplexor A (MUX A) cycling through each channel of the QP (CH1-CH4). Meanwhile, Multiplexor B (MUX B) is set to sample the channel of the QP that has the greatest signal strength. This allows Multiplexor B to focus on sampling the communication stream at a high rate while Multiplexor A continually keeps track of the other channels of the QP for alignment and channel switching purposes. Figure 3.12 shows this scanning approach to sampling/conversion where channel 2 is currently the main data communication channel set to Multiplexor B.

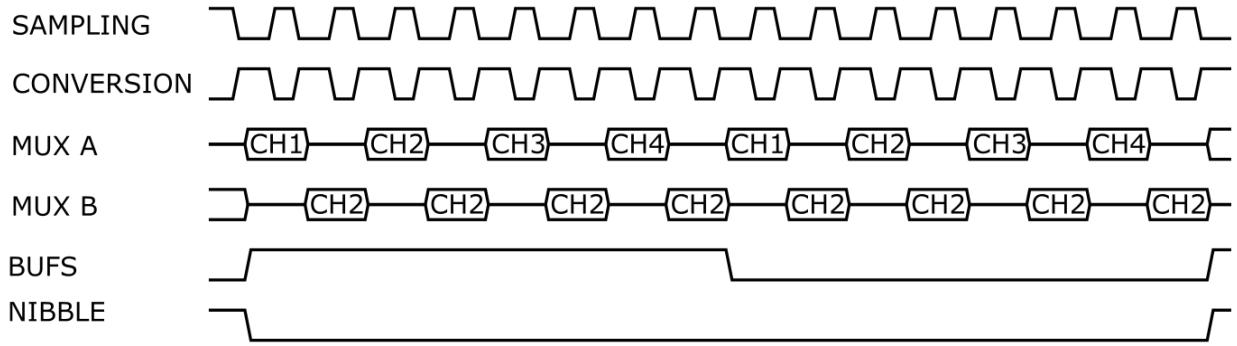


Figure 3.12: Signal diagram architecture for sampling/converting ADC channels from QP

3.2.8 Serial Peripheral Interface (SPI)

The SPI module provides a synchronous serial interface that is standard for communicating with external peripherals connected to the MCU [20]. On this particular MCU, the SPI module supports configurable 8-, 16-, and 32-bit data widths with maximum transmit/receive capabilities up to 80MHz. The transceiver will use SPI to interface with the Ethernet and Camera daughtercards. Microchip offers a driver for the Ethernet controller through their MPLAB Harmony integration. Therefore, the SPI interface is handled solely by the ENC28J60 driver firmware code.

3.2.9 Universal Serial Bus (USB)

A USB On-The-Go module is available on the MCU chosen. It provides full speed USB 2.0 for data transfers as either a host or device [21]. Microchip provides a fully functional USB stack that is self-contained in its own MPLAB Harmony application installation for easy integration. USB is not integral to the operation of this system but is necessary if the debugging interface needs to be monitored. Since the operation of the transceiver is not dependent on USB operation (if the debugging interface is not needed), only a short description of the specific USB implementation will be given here.

The Clicker 2 PIC32MX development board includes a USB 2.0 Mini-B connector as seen in Figure 3.2. A PC endpoint is interfaced with the MCU using connector which is responsible for transmitting/receiving all data to and from the debugging interface. In this two-endpoint system, the PC is the host device polling for packets every 125ms. The MCU responds to the PC host using an interrupt method with the priority detailed in Figure 3.5. USB packets are sent and received as 64-byte application-specific buffers. The buffer content does not follow any standard packet organization but an example is outlined by Figure 3.13. This figure shows a single 64-byte buffer with increasing detail progressing downward.

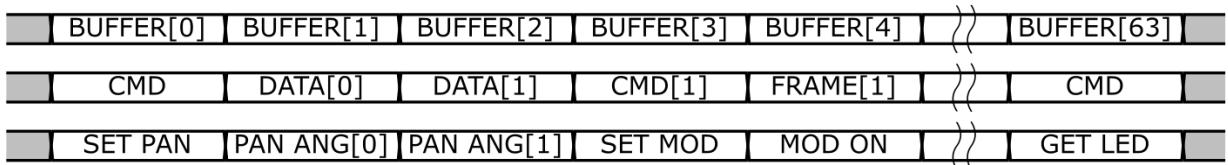


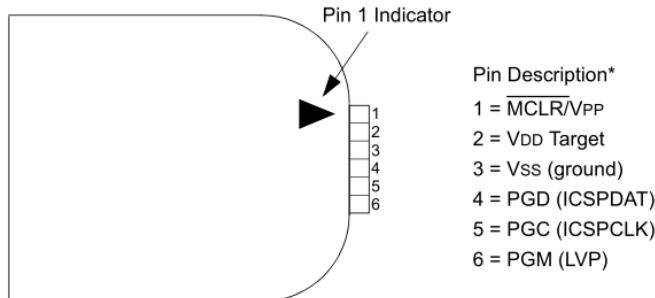
Figure 3.13: Signal diagram of application-specific USB buffer transaction

Each buffer begins with a command byte followed by a variable number of data bytes associated with that command. Notice how certain commands in Figure 3.13 warrant multiple data bytes (i.e. setting the pan servo angle needs two bytes to transfer a 16-byte unsigned integer) while other commands require no subsequent data bytes at all (i.e. requesting LED state). Proper handling of the buffers requires both endpoints to have knowledge of the number of data bytes following each command byte. It is not guaranteed that the number of data bytes following a command byte received at the PC endpoint will equal the number of data bytes following that same command byte received at the OpenROV endpoint.

3.2.10 IDE and Programming

Microchip offers MPLAB X IDE as a free integrated development environment to program all of their PIC devices. ANSI C is the main programming language used to write. This code will be compiled using MPLAB XC32 complier to ultimately generate a .hex file to be uploaded to the

MCU. Microchip's PICkit 3 programmer will be used to upload the .hex file onto the MCU's on-chip memory as well as for in-circuit debugging. The pinout of the PICkit 3 is shown in Figure 3.14.



* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

Figure 3.14: PICkit 3 programmer/debugger pinout [22]

Since the Clicker 2 PIC32MX development board's programmer pins have a different pinout than the PICkit 3 programmer, an adapter must be created. The adapter can easily be created using the color-coded illustration in Table 3.2.

Table 3.2: Pinout adapter for PICkit 3 to Clicker 2 programming pins¹⁰

Clicker 2 Endpoint					
Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	
VSS	MCLR	PGD	PGC	VDD	
MCLR	VDD	VSS	PGD	PGC	PGM
Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6

PICkit3 Endpoint

A large double-headed vertical arrow is positioned between the Clicker 2 Endpoint and the PICkit3 Endpoint rows, indicating the mapping between the two pinouts.

¹⁰ Pin 6 on the PICkit 3, PGM, does not need to be connected for programming/debugging

3.3 Transmitter Module

3.3.1 Overview

The transmitter module is responsible for all tasks relating to the proper transmission of a visible light data carrier to create a communication link. It is composed of multiple functional blocks whose final deliverable is the modulated signal emitted from the laser diode. A block diagram description of the entire transmitter module is shown in Figure 3.15.

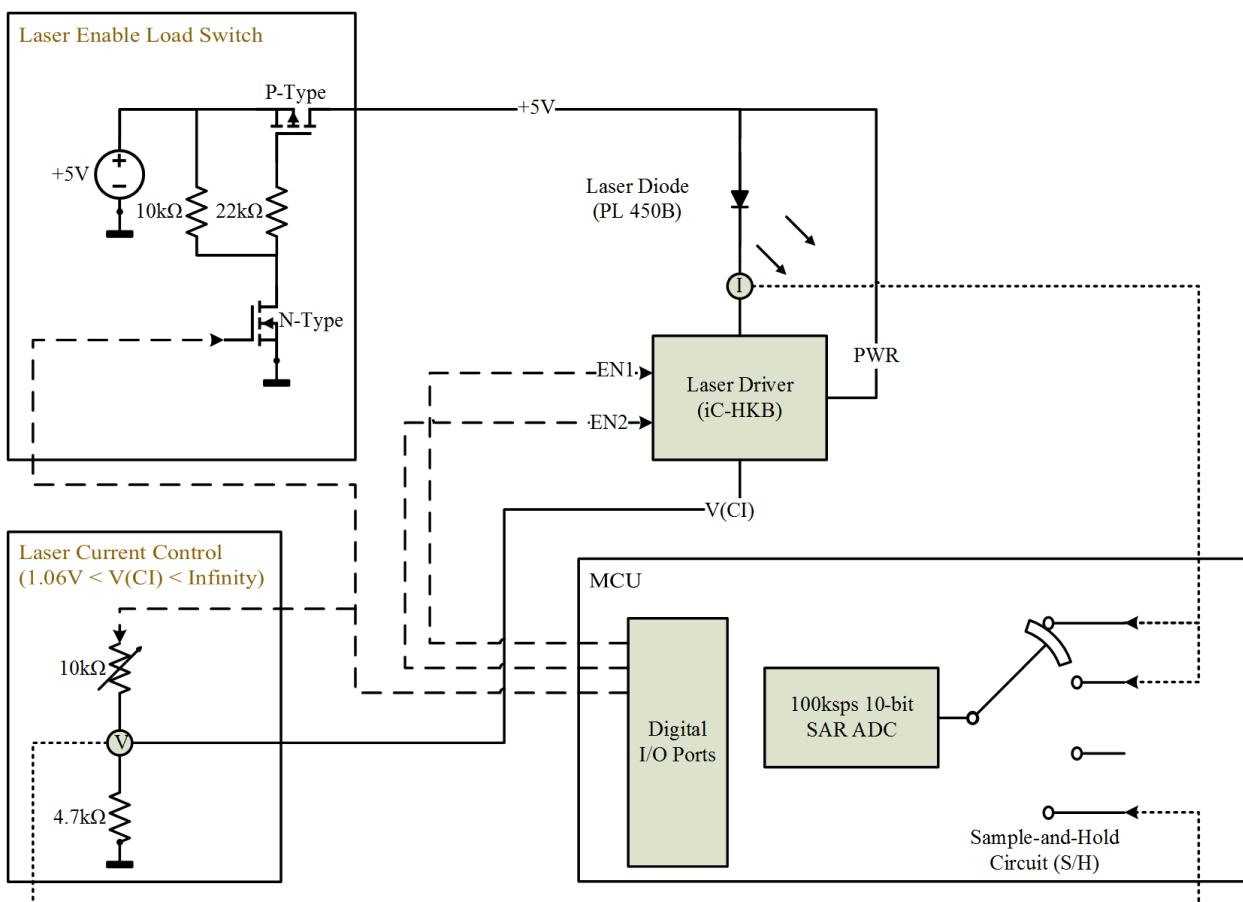


Figure 3.15: Block diagram of transmitter module and submodules

The transmitter module contains the following function blocks which boast the following capabilities:

- Laser diode with collimating lens

- Current sensing via ADC module and sense resistor
- Laser driver to safely modulate the laser diode at high-switching speeds
- Load switch to control all power supplies for laser diode and laser driver circuitry
 - Slow 5us turn on time
 - Minimal power dissipation during operation and idle
- Laser current control circuit to set the laser current set point
 - Variable potentiometer to tune laser to different power outputs
 - Monitoring of voltage reference set point via ADC module

3.3.2 Laser Diode and Sensing

A blue laser diode in conjunction with a collimating lens is used to create a directional, high-power data carrier that can travel through water with little attenuation. The reasoning behind choosing blue light has been explained extensively in the theoretical analysis. Specifically, an OSRAM Opto Semiconductors PL 450B laser diode is used as the source for light emission. A generic 445nm three-element glass collimating lens is used to collimate the light emissions from the laser diode. The selection of these two components have been the focus of a capstone project supporting the requirements for a student's Master of Engineering degree [23]. Thus, discussion relating to their selection will be omitted with attention only given to their application in the transceiver.

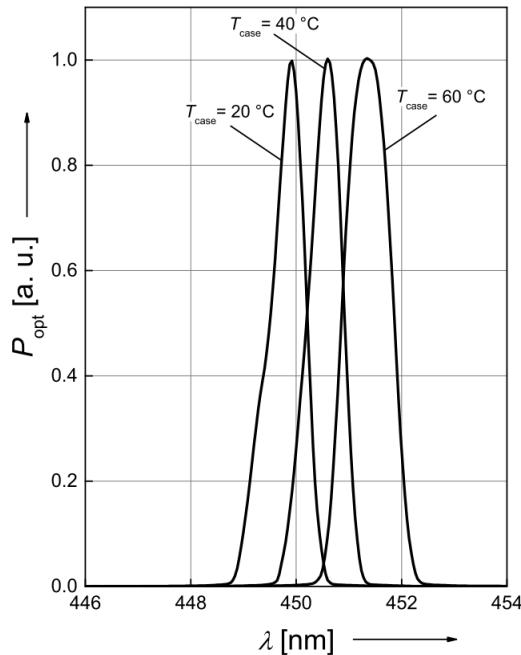


Figure 3.16: Relative spectral emission of PL 450B laser diode at various temperatures [24]

The laser diode is biased using the load switch-controlled 5V rail which can be seen in Figure 3.15. This voltage is sufficient to drive the laser diode to approximately 62mA as per Figure 3.17. This driving current is below the typical operating current of the laser diode, 100mA, and even further below the maximum operating current, 165mA [24]. Regardless, 62mA is enough to properly drive the laser diode with the PL 405B's typical threshold current being 30mA. This design decision was made in an attempt to reduce the number of supply voltages needed as well as limit thermal effects on the diode.

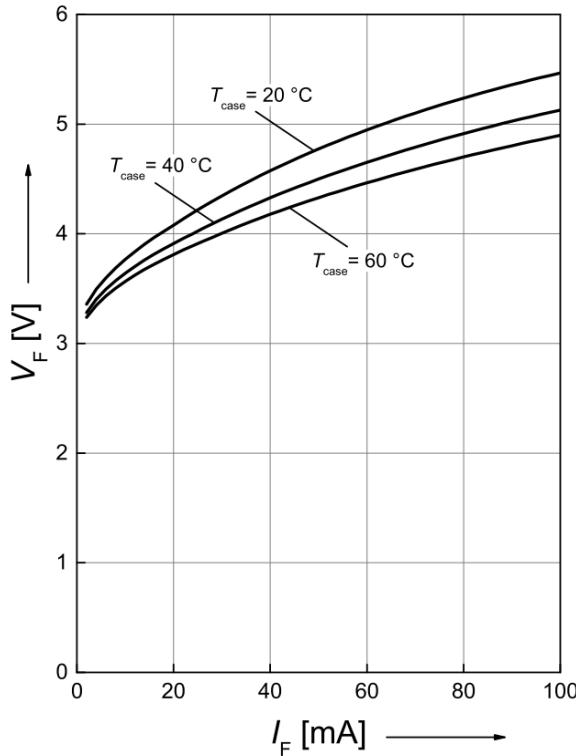


Figure 3.17: Operating voltage of PL 450B laser diode at various temperatures [24]

A simple low-side current sensing resistor is placed in series with the laser diode to coarsely monitor the current draw from the diode. This is done by measuring the voltage at both sides of the sense resistor using the ADC module and calculating the current using Ohm's Law. This method could be improved by placing an opamp difference amplifier across the sense resistor to increase the measurement resolution and decrease the number of ADC channels needed by a factor of 2. The resolution of the current sense circuit is dependent on the sense resistor value (RSENSE), the reference voltage of the ADC, and the resolution of the ADC as expressed by Equation (3-10).

$$\text{Current Sense Resolution (per bit)} = \frac{\text{(ADC Reference Voltage)}}{2^{\text{(ADC Resolution)}} \times RSENSE} \quad (3-10)$$

A sense resistor value was chosen that is minimal compared to the equivalent series resistance of the operating laser diode. The equivalent series resistance specification was not given for the PL

450B laser diode, but in general, it can be said that single mode, Fabry-Perot-style laser diodes have an equivalent series resistance of about 5ohms [25]. Using this equivalent series resistance value and assuming the absolute maximum current draw of the laser diode, a 1ohm resistor will dissipate 0.1375mW of power. Considering the ADC module's 10-bit resolution and its 3.3V reference voltage, a Vishay 0.82ohm 1% sense resistor was deemed appropriate for this task which is shown in the schematic section of Figure 3.18. This results in a current sense resolution of 3.93mA/bit and a maximum power dissipation of 0.116mW.

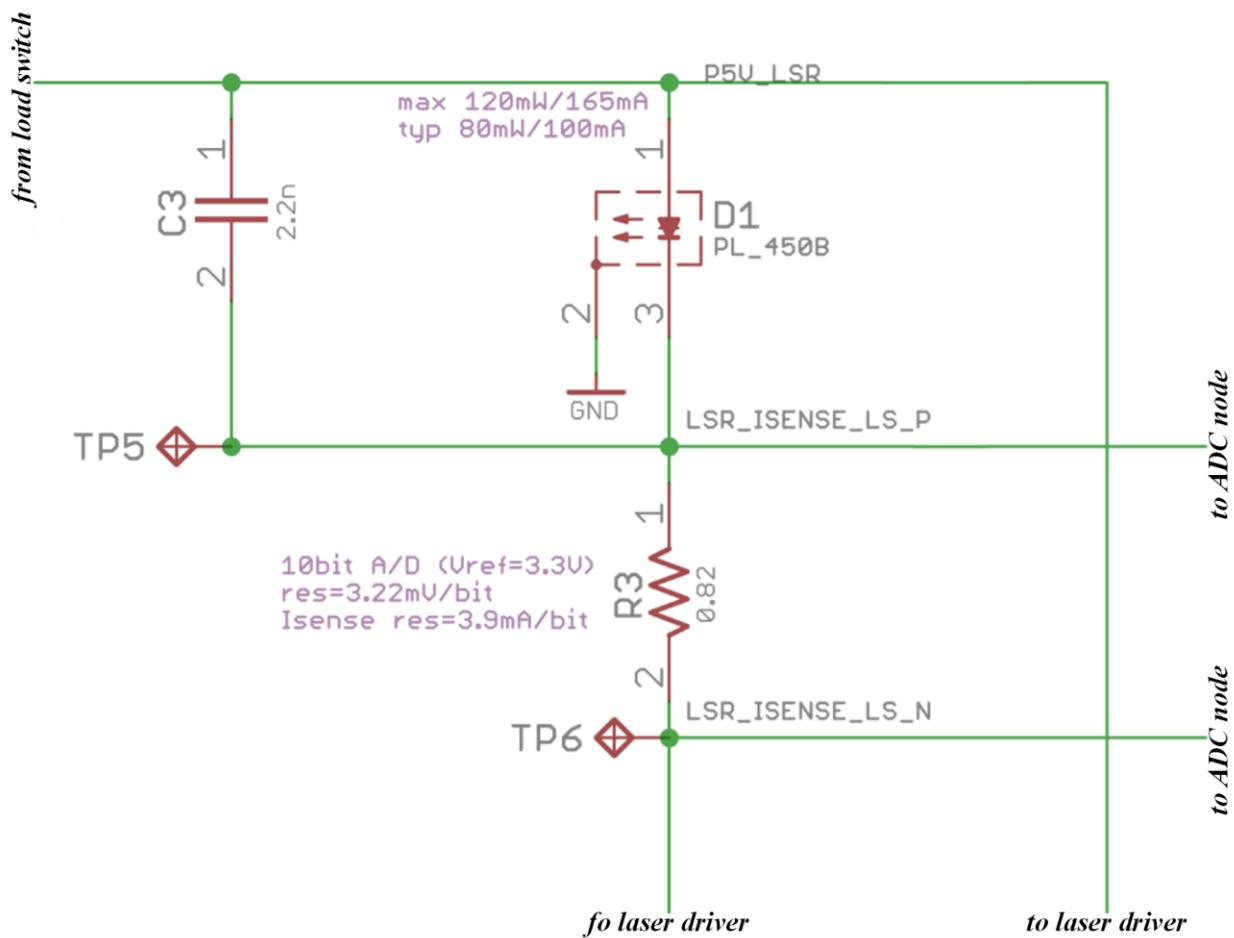


Figure 3.18: Simplified schematic section showing laser diode and sense resistor

3.3.3 Laser Driver and Current Control

The laser driver is responsible for rapidly forcing the laser diode into different current draw states. It is important for the chosen driver to not only be capable of switching the laser diode at high frequency but to do this without damaging the diode. An integrated circuit device is used since integrated drivers generally have better switching and protection circuitry than discrete solutions. The ic-HKB was chosen as the laser driver which is shown in Figure 3.19 and boasts the following capabilities [26]:

- Operation as a voltage-controlled current source
- Spike-free switching up to 155MHz supplying 700mA per channel
- Thermal shutdown and protective ESD circuits specific to blue laser diodes

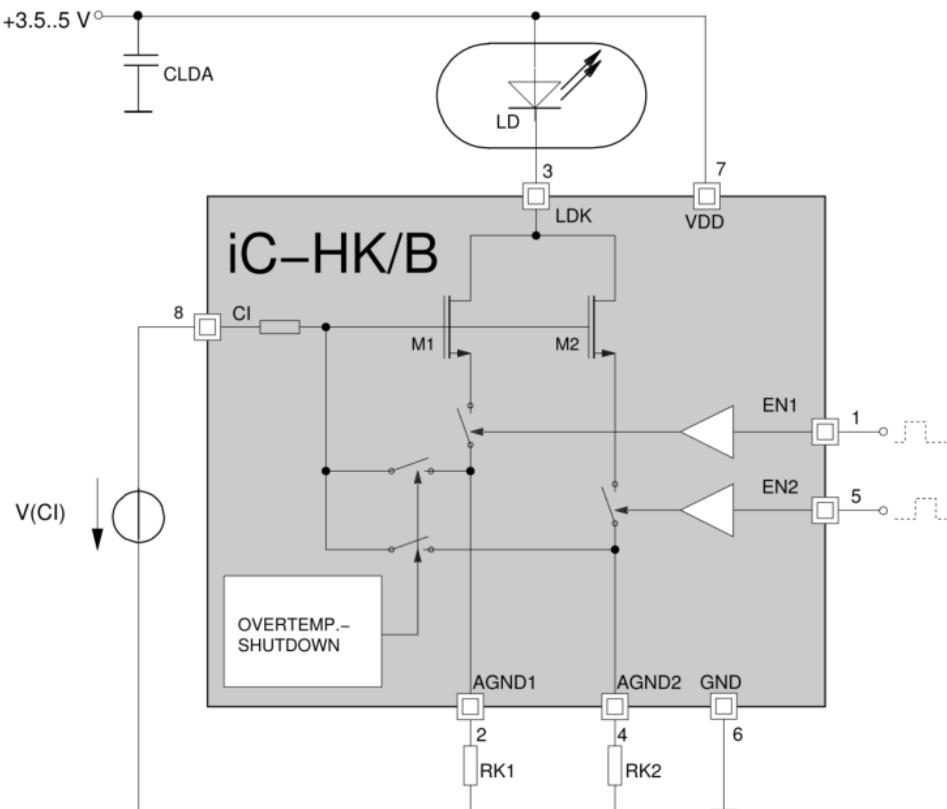


Figure 3.19: Block diagram of iC-HKB laser driver [26]

The modulation of the laser diode is controlled by switching inputs EN1 (pin 1) and EN2 (pin 5). Diode current is set by the voltage at the current control pin, VCI (pin 8), as well as the ratio of resistors RK1 and RK2. Since dual switching is not necessary for this system, EN2 is unused and RK1 and RK2 are shorted to ground to simplify operation as seen in Figure 3.20.

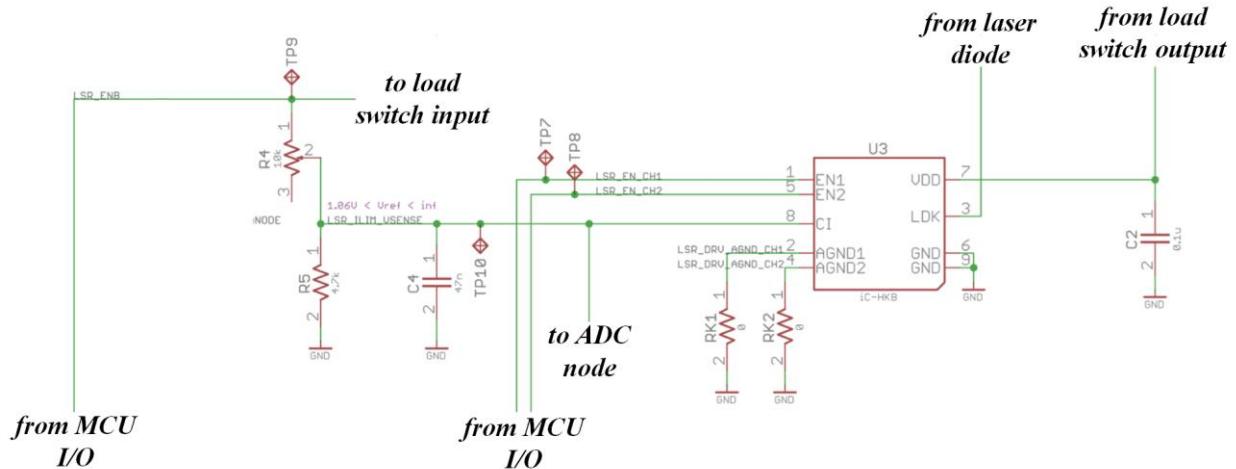


Figure 3.20: Simplified schematic section showing laser driver and current control

A voltage divider network is used to set the voltage at the current control pin of the driver. This voltage is tunable by potentiometer, R4, as shown in Figure 3.20. A 10kohm potentiometer in series with a 4.7kohm resistor was chosen as the voltage divider network which gives the voltage reference, $V(CI)$, a range expressed by Equation (3-11).

$$1.06V < V(CI) < infinity \quad (3-11)$$

This voltage reference range in Equation (2-9) translates to a driving current of about 10mA to the maximum operating current of the iC-HKB device. Comparing this to the specifications of the PL 450B laser diode, this current control network can take the laser diode from its off state (<30mA) to its normal operating condition (100mA) all the way to its absolute maximum operating conditions (165mA). This is shown graphically by the highlighted sections in Figure 3.21.

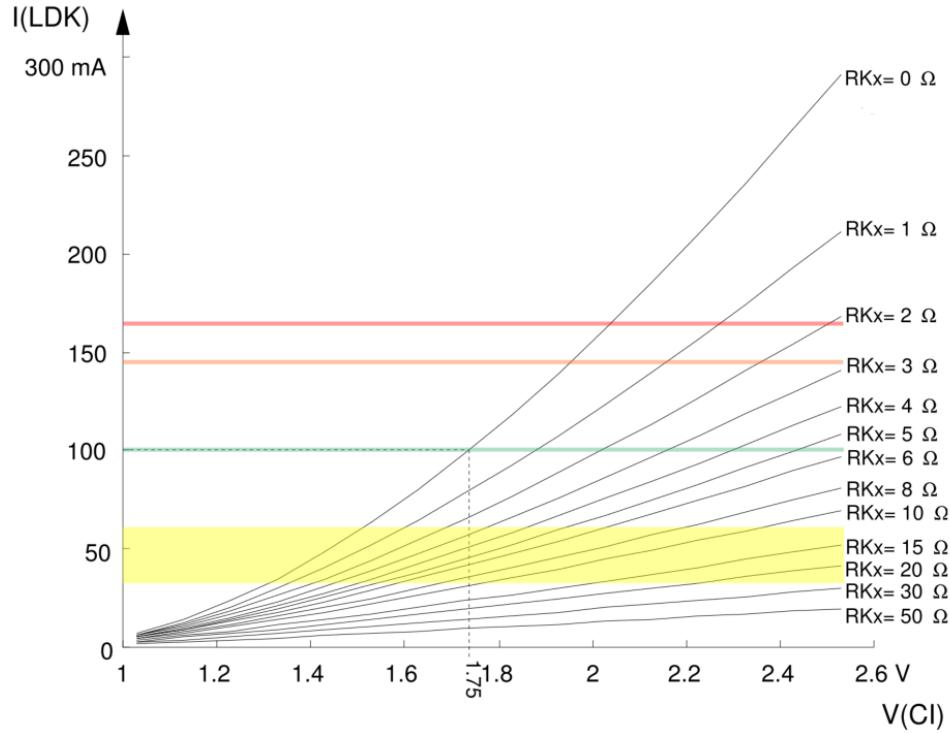


Figure 3.21: Current variations of iC-HKB laser driver relative to reference voltage¹¹ [26]

3.3.4 Load Switch

A load switch to control the power rail supplying voltage for the laser diode and laser driver was deemed necessary for the following two reasons:

- Premature turn-on of laser diode could result in a safety danger
- Power rails may be too noisy or overshoot during power on damaging the laser diode

A proper load switch solves both of these issues by keeping the supply off until an I/O pin on the MCU shifts high. The load switch was built around the Vishay Si2333DDS which is a P-channel MOSFET with an on-state drain-to-source resistance, VGS, of 0.014ohm [27]. This low drain-to-source resistance will minimize the voltage drop across the load switch as well as lessen the

¹¹ Yellow, green, orange, and red highlighted areas refer to the PL 450B's threshold current, typical operating current, recommended maximum operating current, and absolute maximum operating current, respectively [24]

power consumption of the circuit. The simplified schematic of the load switch circuit is shown in Figure 3.22

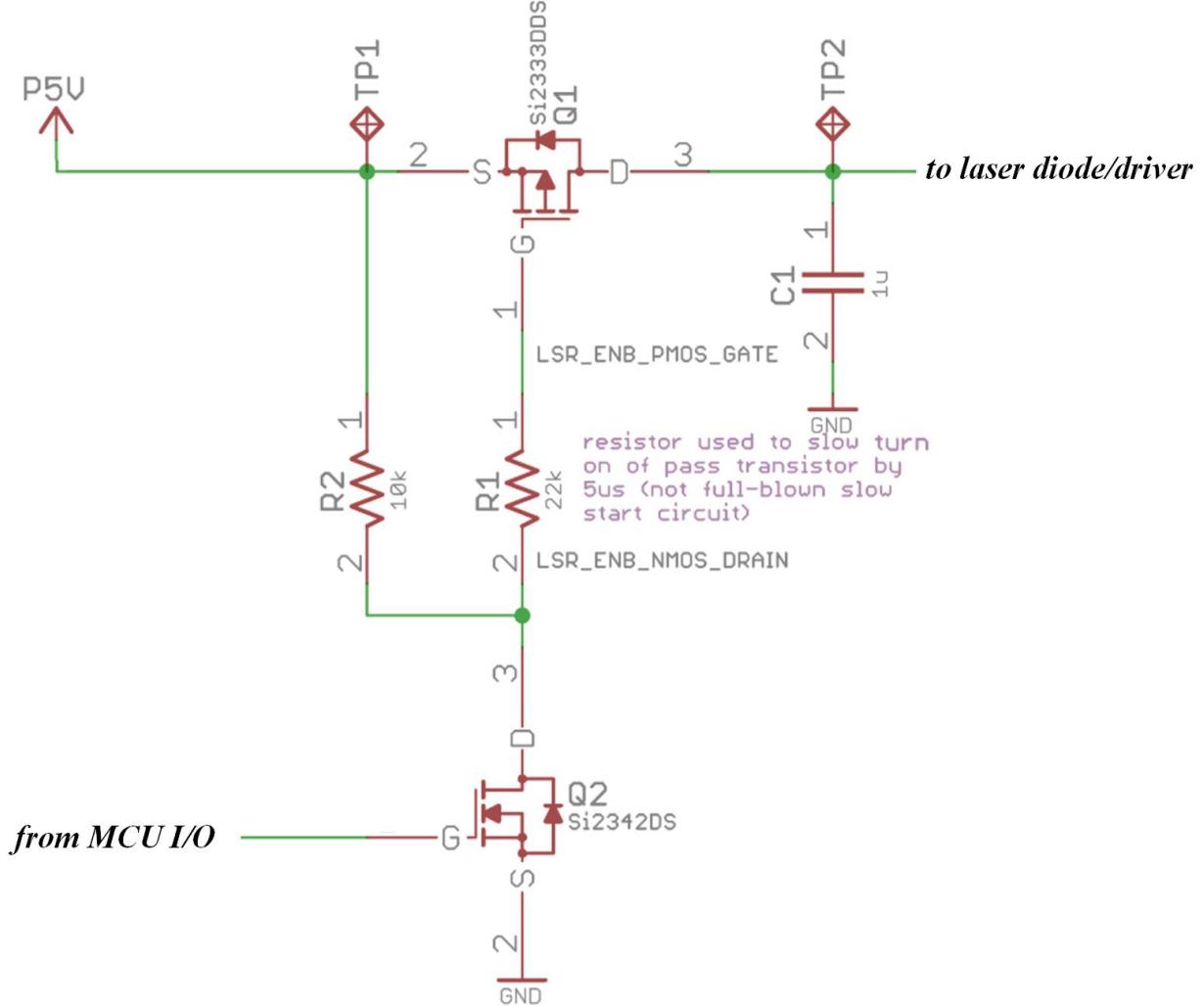


Figure 3.22: Simplified schematic section of load switch circuitry

The P-channel MOSFET's gate is pulled up by a resistor, R2, to keep it in the off state as soon as the main 5V rail comes up. An N-channel MOSFET is used to turn the P-channel MOSFET on when a logic high is applied at its gate. R2 is given a large enough value to limit the leakage current that will flow from the main 5V rail through R2 and the N-channel MOSFET to ground when the load switch is on. A value of 10kohm leads to R2 dissipating a negligible 2.5mW.

Additionally, a resistor, R1, is placed at the gate of the P-channel MOSFET to slow the output rise time and limit the inrush current to the gate. This is important as too much inrush current can lead to PCB trace damage, power supply failure, or a drop in the input voltage [28].

The load switch circuit in Figure 3.22 was modeled in LTspice IV before physically constructing it. Different values for the resistor R1 were simulated to find the ideal value to ensure a slow-start turn-on time for the output rail. A transient SPICE simulation was conducted over 1.2ms with the main 5V rail (RAIL) turning on at 0.5ms and the I/O pin controlling the N-channel MOSFET gate (SWITCH) triggering at 1ms. Additionally, an abominable 1V overshoot with a linear decrease over 10us was superimposed on the main 5V rail at turn on. These simulations and the results on the laser/driver output rail (VOUT) are shown in Figure 3.23.

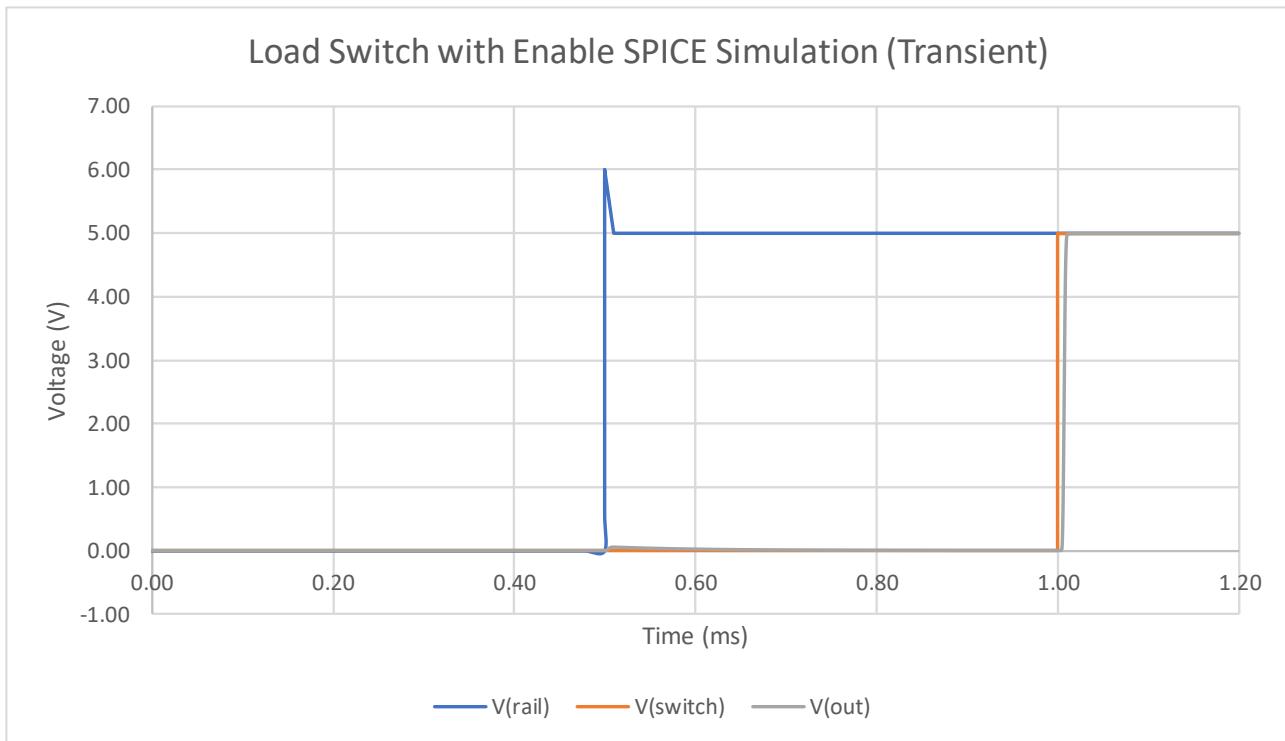


Figure 3.23: Transient SPICE simulation of load switch circuitry

As can be seen in Figure 3.23, the main 5V rail turns on with a large overshoot but does not have an effect on the output rail¹². This isolation allows predictable, safe turn on of the transmitter optics and supporting electronics by having control of their supply rail. Additionally, the rise time of the output rail is slowed by a 22kohm value for R1 on the gate of the P-channel MOSFET. The output rail (VOUT) rises slowly over the course of 5us as seen by Figure 3.24. This ensures the laser diode is not subject to any type of current spiking at turn on.

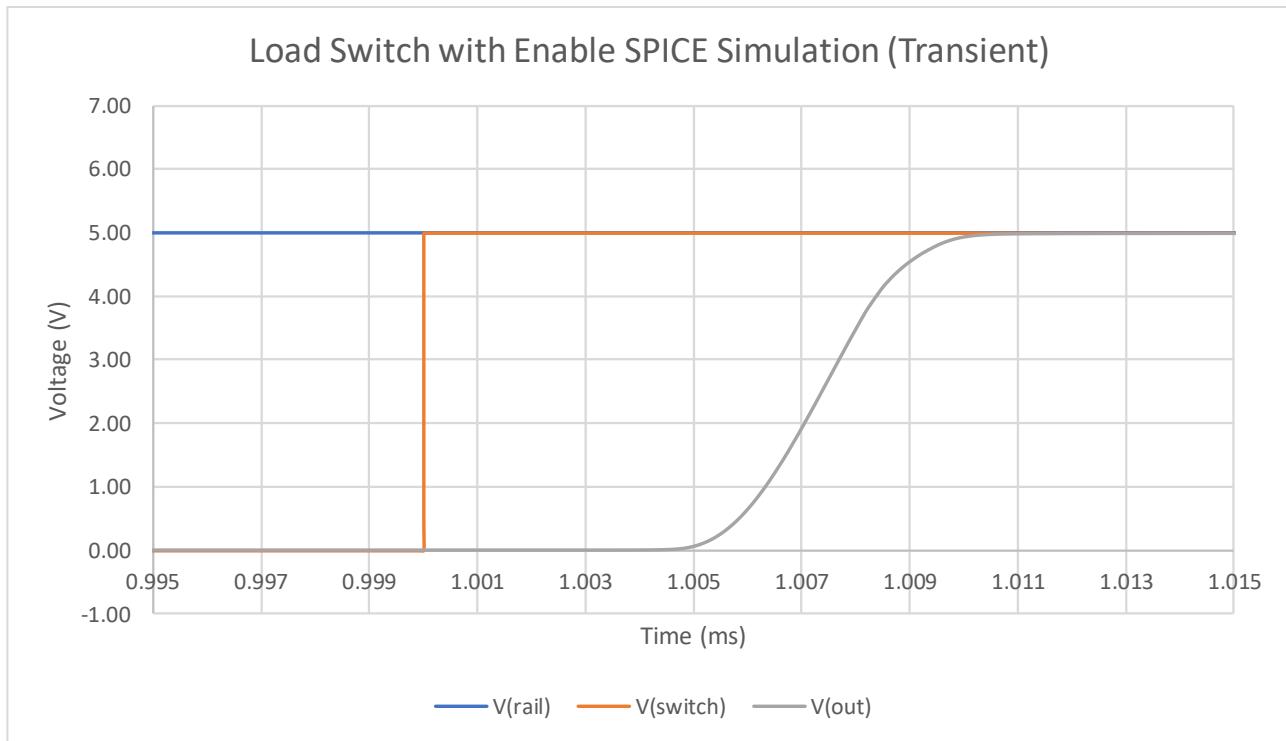


Figure 3.24: Transient SPICE simulation of load switch circuitry showing slow-start

3.3.5 Firmware Logic

The transmitter submodules described above are all that is needed for the physical implementation the transmitter module. However, the MCU must be properly programmed to support the functioning of each of these submodules. The logic that the transceiver module follows as modulation begins is outlined by Figure 3.25. The modulation engine is abstracted

¹² The voltage at the switch and the output never reach more than 55mV during the overshoot

here since it is shared with the receiver module and will be talked about in depth in a future section.

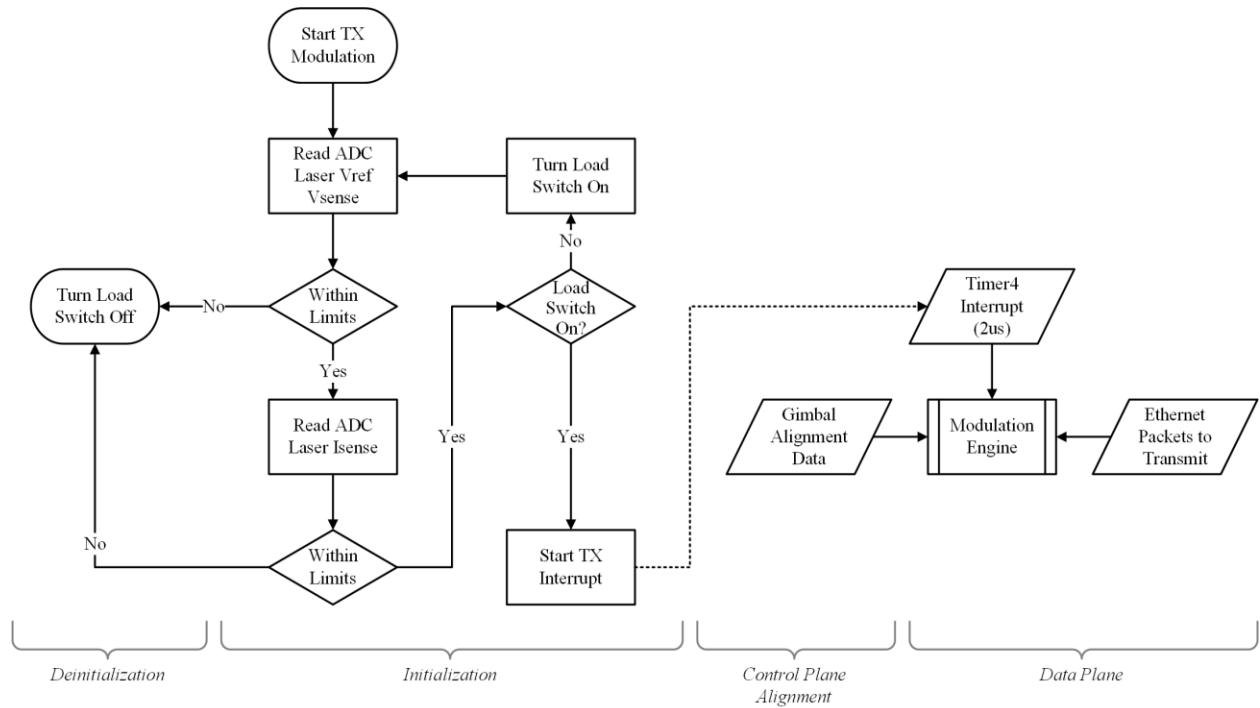


Figure 3.25: Flowchart of transmitter module firmware logic

Some important notes about the transmitter module firmware logic:

- The load switch will not turn on unless the voltage reference for current control is within limits.
- This check will be made again once the load switch has been turned on.
- Only then will the modulation engine be started.

3.4 Receiver Module

The receiver module handles receiving and extracting the data stream from the visible light data carrier. It is composed of multiple functional blocks whose final deliverable is recovered

Ethernet packets and control alignment data from the distant transceiver. A block diagram description of the entire receiver module is shown in Figure 3.26.

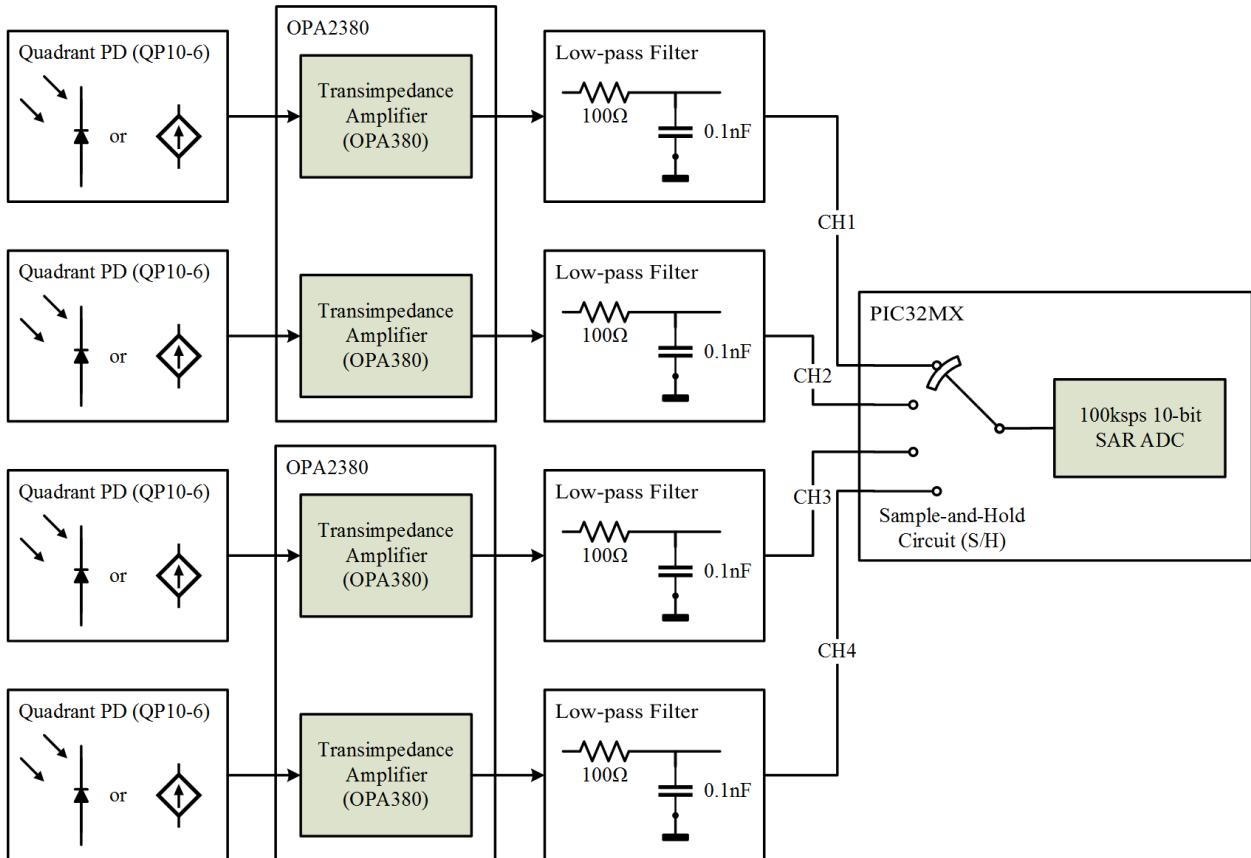


Figure 3.26: Block diagram of receiver module and submodules

The receiver module boasts the following capabilities:

- QP and isolated bias network
- Array of four transimpedance amplifiers for translating the QP channels to stable voltage
 - High gain with limited bandwidth of 10.08MHz
- Low-pass filter to remove high-frequency harmonics before ADC sampling

3.4.1 Quadrant Photodiode (QP)

A QP is used in two capacities in the system. It must be able to capture the incoming data stream as well as perform control feedback to maintain alignment between transceivers. A QP is a good candidate because it is a proven device that has been successfully implemented in systems involving atomic force microscopy, particle tracking, and photothermal diffusivity measurements [10]. It has a symmetric geometry that would otherwise be difficult to achieve using a discrete PD solution. Additionally, the V-shaped grooves between quadrants help to refract incident light redirecting them toward their corresponding quadrants preventing optical cross-talk between regions [9]. Table 3.3 presents a comparison chart of available QPs to help with the component selection decision. Many factors were taken in consideration including the following:

- Cost (high-cost sensor reduces potential for scalability and marketability)
- Spectral response (tradeoffs must be considered between spectral attenuation rates and QP spectral response)
- Active area (larger quadrant area reduces chance of completely losing signal by increasing alignment margins and increases signal amplitude for larger beam diameters)

Table 3.3: Comparison chart of various QPs and notable characteristics

Quadrant PD	Cost	MFR	Peak Wavelength	Response Time (ns)	Active Area (mm^2) each	Package Type	Responsivity (A/W) @ Wavelength (nm)						
							400	450	480	500	580	600	640
OPR5925	\$5.98	TT Electronics/Opte	890	-	0.75	Waffle/Chip Tray (surface mount)	0.14	0.19	0.21	0.22	0.31	0.345	0.4
SD118-23-21-021	\$72.38	Luna Optoelectronics	660	13ns	1.145	TO-5 (through hole)	0.14	0.19	0.21	0.22	0.31	0.35	0.4
SD085-23-21-021	\$107.81	Luna Optoelectronics	660	13ns	2.25	TO-5 (through hole)	0.14	0.19	0.21	0.23	0.32	0.35	0.4
SD197-23-21-041	\$100.05	Luna Optoelectronics	660	13ns	2.355	TO-8 (through hole)	0.14	0.18	0.205	0.23	0.315	0.35	0.4
SD225-23-21-041	\$93.02	Luna Optoelectronics	660	13ns	5.222	TO-8 (through hole)	0.14	0.18	0.21	0.22	0.32	0.345	0.4
PDB-C203	\$60.36	Luna Optoelectronics	950	13ns	1.69	TO-5 (through hole)	0.12	0.2	0.24	0.28	0.36	0.4	0.45
QP1-6	\$40.00	First Sensor	900	20ns	0.25	TO-52 (through hole)	0.18	0.175	0.2	0.23	0.325	0.38	0.42
QP5.8-6	\$44.54	First Sensor	633	20ns	1.44	TO-5 (through hole)	0.1	0.15	0.18	0.215	0.35	0.39	0.45
QP10-6	\$52.25	First Sensor	900	20ns	2.45	TO-5 (through hole)	0.09	0.165	0.2	0.225	0.33	0.38	0.42
QP50-6	\$142.37	First Sensor	850	40ns	12	TO-8 (through hole)	0.09	0.16	0.2	0.23	0.33	0.38	0.42
QP100-6	\$156.44	First Sensor	633	50ns	24.35	Surface Mount	0.09	0.18	0.205	0.225	0.35	0.38	0.42

Ultimately, the First Sensor QP10-6 was chosen which has a total active area of 9.8mm², a peak spectral sensitivity at 900nm, and a rise time of 20ns¹³ [29]. Each channel of the QP is setup in a reverse bias configuration to reduce rise times during high-frequency signal reception. Discrete values of visible wavelengths were chosen to estimate the electrical response of the laser beam based on the QP10-6's spectral sensitivity and the theoretical analysis done on light traveling through water. The theoretical calculations are displayed graphically in Figure 3.27.

¹³ Rise time specification is for a reverse voltage of 10V, wavelength of 850nm, and load of 50ohms

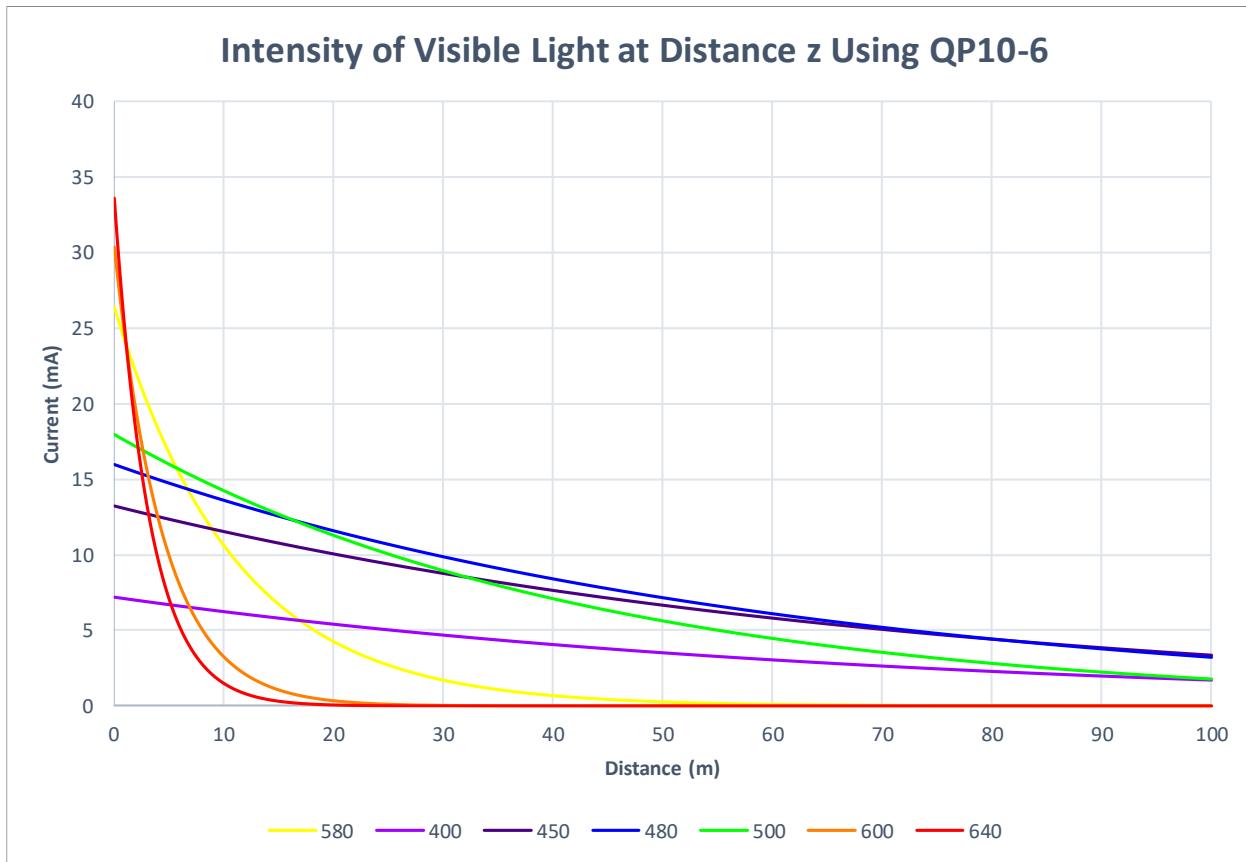


Figure 3.27: Theoretical electrical response of QP10-6 QP with different wavelengths

3.4.2 Transimpedance Amplifier and Low-Pass Filter

A transimpedance amplifier is a current-to-voltage amplifier whose main goal is to convert a small current to a steady voltage using an opamp. It does so by designing itself to be low-impedance at the input node to and results in a transimpedance gain from the input to output (A/V). Texas Instruments' OPA2380 high-speed transimpedance amplifier was chosen which has the following specifications [30]:

- Dual package device containing two OPA380 in a single MSOP-8 package¹⁴ (a single OPA380 device is detailed in Figure 3.28)

¹⁴ OPA2380 is the dual package version of the OPA380

- Measurement of signal currents as small as 1nA
- GBW of 90MHz with a dynamic range up to 5 decades

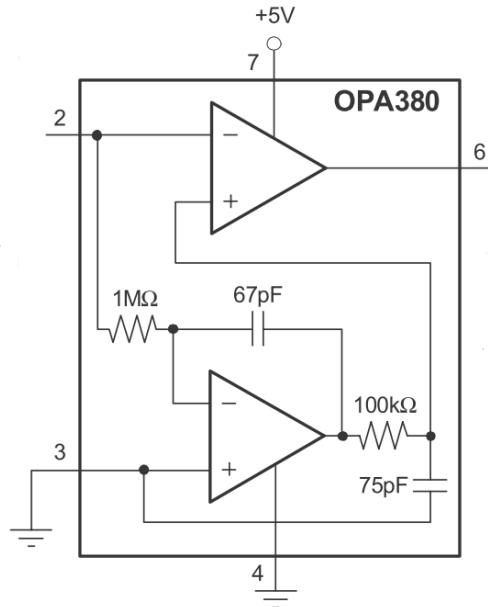


Figure 3.28: Block diagram of single OPA380 transimpedance amplifier device [30]

Four independent transimpedance amplifiers are needed in process signals from each of the channels on the QP. Therefore, two OPA380 packages are sufficient to satisfy these requirements as seen graphically in Figure 3.26. The final simplified schematic of a single transimpedance amplifier and low-pass filter is shown in Figure 3.29 for reference. To simplify the architecture of the amplifier, the non-inverting input has been tied to ground. In future iterations of this project, it may be desirable to set the non-inverting node to a stable bias point in to allow the amplifier to output a true zero PD measurement which will also remove the delay associated with overcoming the negative rail [30].

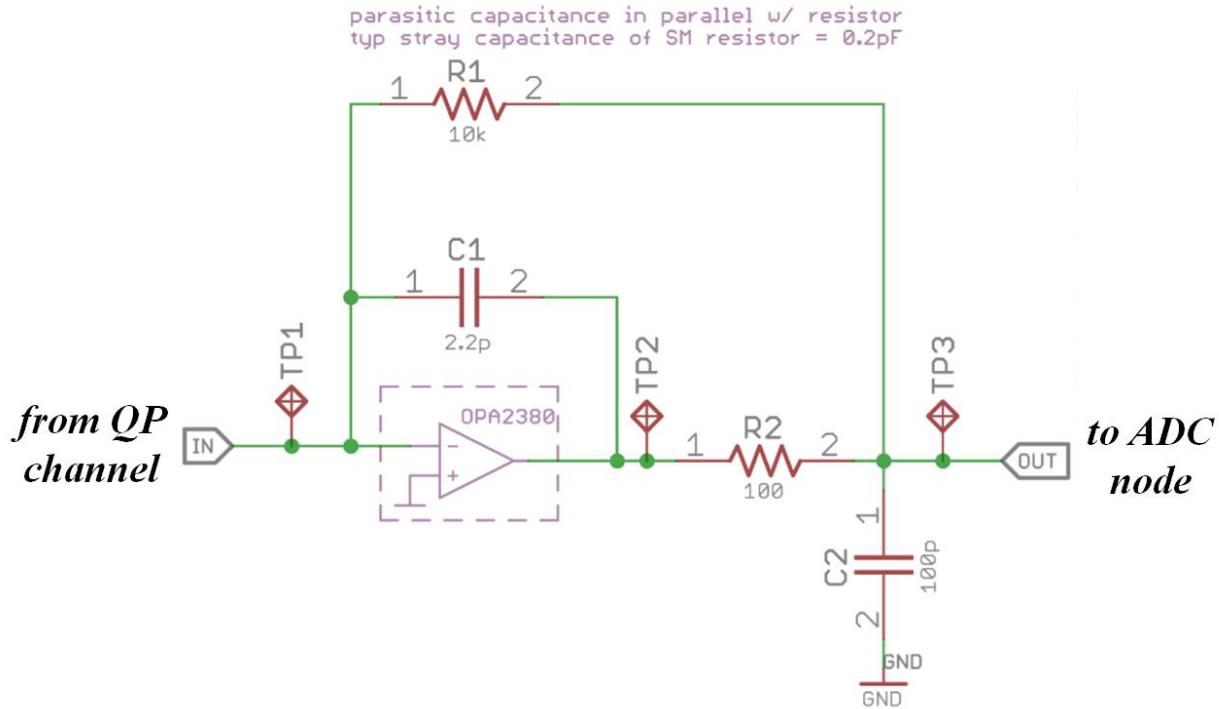


Figure 3.29: Simplified schematic section of transimpedance amplifier and low-pass filter

A modest transimpedance gain was set for the amplifier stage using the feedback resistor, R1, which will help to limit noise produced by the circuit. A feedback capacitor, C1, is used to prevent gain peaking and limit the bandwidth of the circuit [30]. This value was chosen by satisfying Equation (3-12) which will result in Butterworth frequency response. CSTRAY indicates the stray capacitance of the feedback resistor which is 0.2pF for a typical surface-mount device. CTOT represents the total input capacitance of both the PD and opamp (14.1pF).

$$\frac{1}{2\pi \times R1 \times (C1 \times CSTRAY)} = \sqrt{\frac{GBW}{4\pi \times R1 \times CTOT}} \quad (3-12) [30]$$

This results in a feedback capacitor value of 2pF. The bandwidth of the transimpedance amplifier of this stage is calculated as 10.08MHz using Equation (3-13) .

$$f(-3dB) = \sqrt{\frac{GBW}{2\pi \times R1 \times CTOT}} \quad (3-13) [30]$$

A low-pass filter is placed inside the feedback loop of the transimpedance amplifier to reduce output noise by creating a second high-frequency pole. In choosing values for this feedback resistor (R2) and capacitor (C2), it is beneficial to choose values in line with Equation (3-14) to result in a Butterworth filter that is “...maximally flat in the passband...” [30].

$$C1 \times R1 = 2 \times C2 \times R2 \quad (3-14) [30]$$

A value of 100ohms for the filter resistor and 100pF for the filter capacitor satisfy this expression. These values will add a second pole at 24MHz as per Equation (3-15). This combined transimpedance amplifier/low-pass filter should result in a final circuit that rolls off high-frequencies components at 40dB/decade.

$$f(-3dB) = \frac{1}{2\pi\sqrt{R1 \times R2 \times C1 \times C2}} \quad (3-15) [30]$$

The circuit shown in Figure 3.29 was simulated in LTspice IV to verify these theoretically calculated characteristics. A transient SPICE simulation was conducted over 15us with a 0.5mA square wave current source modeling a single QP channel. The simulation takes into consideration the parasitic common-mode capacitance of the OPA2380 device (3pF) as well as its differential-mode input capacitance (1.1pF) [30]. Additionally, a QP channel capacitance of 5pF and a shunt resistance of 250Mohms were used as per the QP10-6 datasheet [29]. The results of this simulation are shown in Figure 3.30.

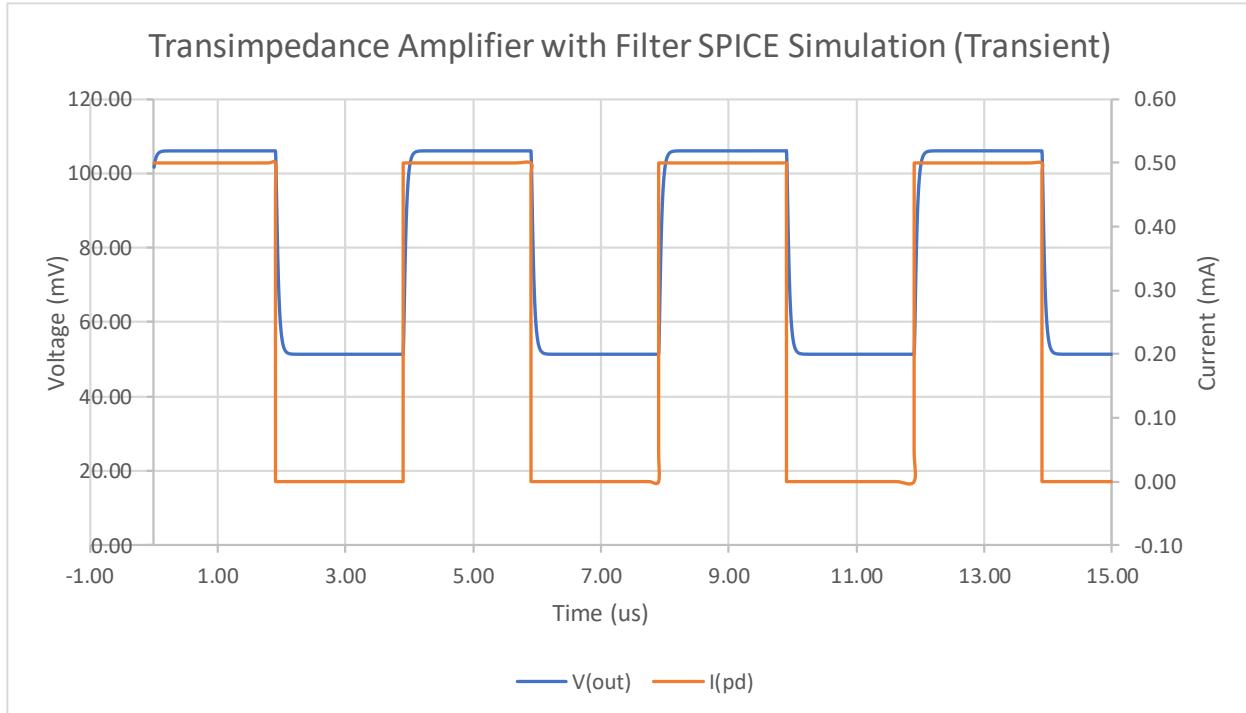


Figure 3.30: Transient SPICE simulation of transimpedance amplifier/filter¹⁵

In addition to a transient response, a frequency response was simulated using a AC sweep from 10Hz to 1GHz. As predicted, the circuit is relatively flat-band until its -3dB frequency of 4.2MHz at which it begins to roll off at about 30dB/decade as shown in Figure 3.31.

¹⁵ A 250mA current DC source was added in parallel to model ambient light

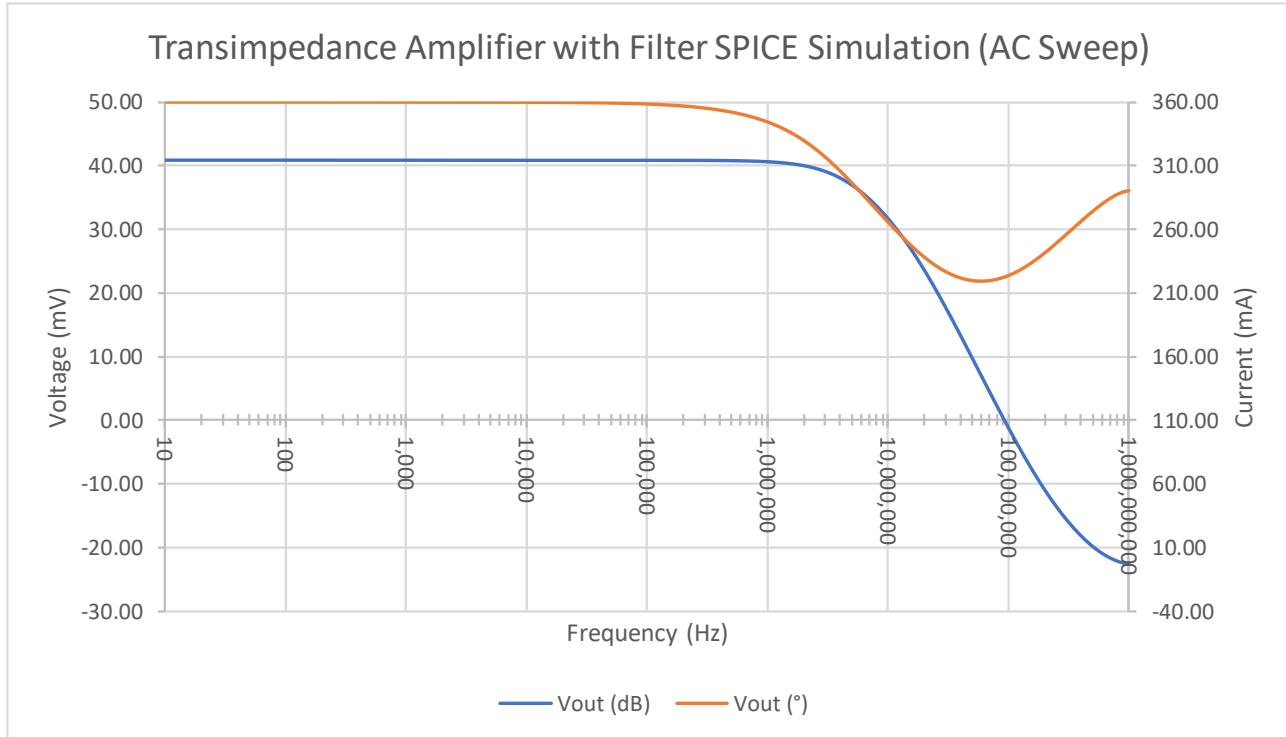


Figure 3.31: AC frequency sweep SPICE simulation of transimpedance amplifier/filter

3.4.3 Firmware

The receiver submodules described above are controlled by the firmware on the MCU to support their proper functioning. The logic the receiver module follows is outlined by Figure 3.32. The modulation engine is abstracted here since it is shared with the transmitter module and will be described in a future section.

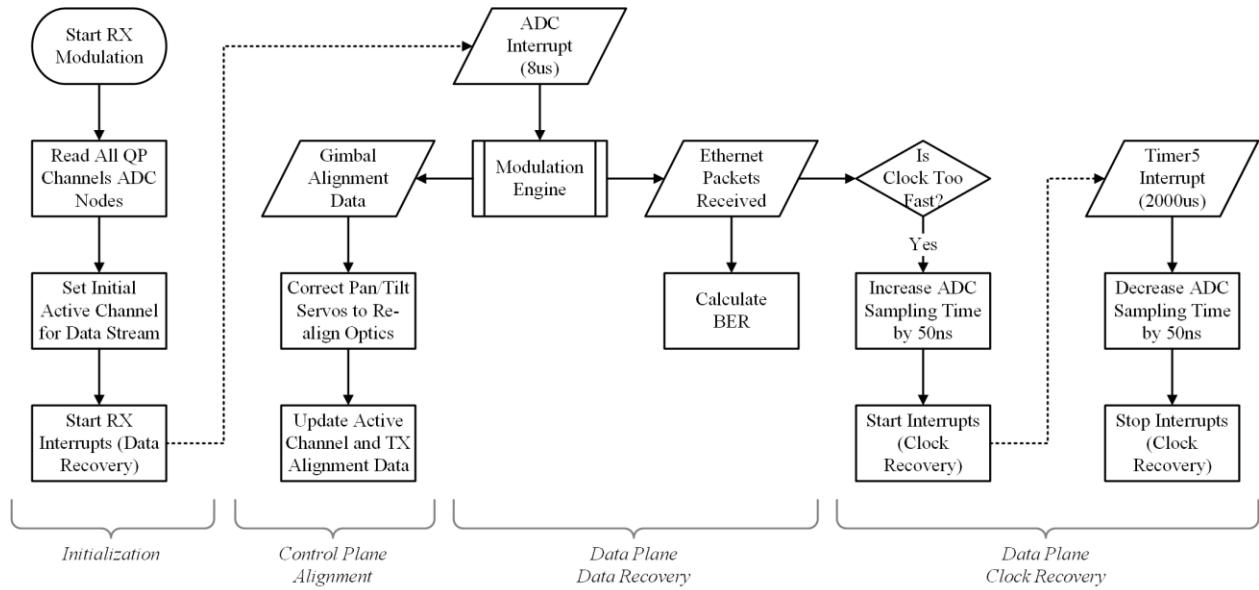


Figure 3.32: Flowchart of receiver module firmware logic

Some important notes about the receiver module firmware logic:

- A single channel of the QP is set as the active channel for recovering the data stream (data recovery)
 - This is set initially by reading all channels during initialization
 - It is actively updated every ADC interrupt cycle based on strongest channel signal
- Received Ethernet packets are used to calculate BER and determine if clock recovery operations need to occur
- Clock recovery works by allowing transmitter to run slightly faster than ADC sampling/conversion sequence and increasing the ADC sampling time by 50ns when needed in order to keep clocks synchronized

3.5 Modulation

3.5.1 Manchester Encoding

An encoding/decoding protocol needs to be chosen to properly send and receive data to and from the transceivers. Originally, a basic non-return-to-zero encoding scheme was envisioned for this system. This type of encoding would be suitable for data rates needed by this application but does not offer additionally clock recovery benefits for asynchronous communication systems.

Other encoding schemes such as Manchester encoding solve the clock recovery problem by introducing extra edges at the middle of every bit [31]. This means that twice the data rate is needed to send a Manchester encoded signal as compared to sending a non-return-to-zero signal. Ultimately, Manchester encoding was chosen for this inherently asynchronous system to simplify clock recovery as well as the following reasons:

- Guaranteed phase changes every bit to make data recovery baseline independent (as signal intensity changes, bit values are easily determined by comparing first and second parts of the bit)
- Extra edges on non-active quadrant channels could present additional opportunities for clock recovery (if the beam is recoverable on multiple quadrants)
- Assured knowledge that signal is being received and aligned properly at initial lock and operation (string of zeros or string of ones could look like non-present beam or saturation of QP channel by ambient light, respectively)

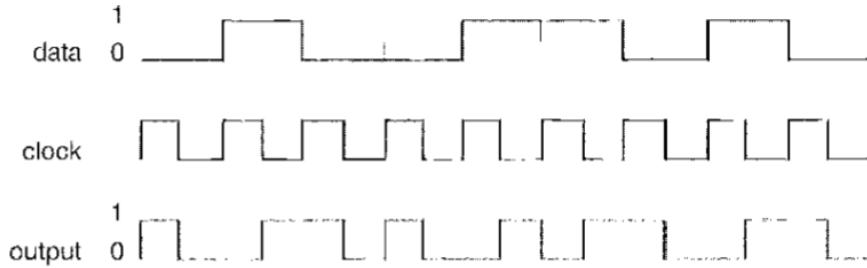


Figure 3.33: Manchester coding specification [32]

The more straightforward coding of bits followed by IEEE 802.3 will be used in this system [32].

This defines a logic 0 as a transition from high to low over the course of a single sequence.

Conversely, a transition from low to high as a single sequence represents a logic 1 bit. The presence of an edge in between bit sequences is not definite and is entirely dependent on the pattern of data being sent as seen in Figure 3.33.

3.5.2 Framing

The data being sent will be partitioned into frames. This is necessary as additional control plane alignment data needs to be embedded alongside the data plane's Ethernet packets. During modulation, frames are sent consecutively. Each frame is further divided into two parts: the header and the data. The structure of a single example frame with increasing detail progressing downward is shown in Figure 3.34.

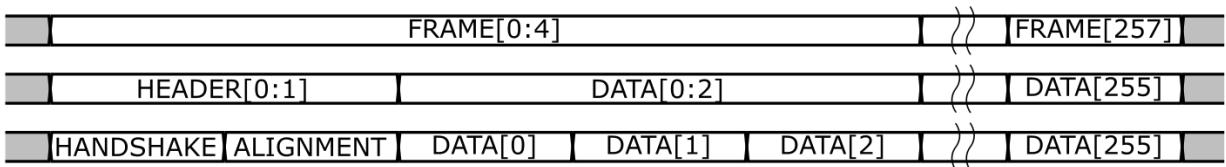


Figure 3.34: Signal diagram of frame structure for modulated signal

The header itself only contains the following two bytes:

- Handshake byte – indicates the signal lock state (see firmware section with modulation engine description) and must be seen to verify signal presence and start of frame

- Alignment byte – contains control plane alignment information to send to distant transceiver based on the bit mapping of Table 3.4
 - Bits 0-2 indicates the horizontal correction needed for re-alignment (negative values denote a leftward motion; positive values denote a rightward motion)
 - Bits 4-6 indicates the horizontal correction needed for re-alignment (negative values denote a downward motion; positive values denote an upward motion)
 - Bits 3 and 7 are currently unused

Table 3.4: Bit mapping of frame's alignment byte and corresponding correction needed

Bits	Horizontal Alignment Correction <6:4>	Vertical Alignment Correction <2:0>
000_2	+0	+0
001_2	-1	-1
010_2	+1	+1
011_2	-2	-2
100_2	+2	+2
101_2	-3	-3
110_2	+3	+3
111_2	n/a	n/a

The data portion of the frame contains exactly 256 bytes of Ethernet packet data retrieved from the Ethernet controller using the MCU's SPI interface. These packets are meant to be received by the distant transceiver and forwarded to the Ethernet controller again using the SPI interface.

3.5.3 Timing

The timing of the modulation presents some interesting challenges. With the ADC module sampling at 1Msps, the minimum sampling frequency of the received signal using the Nyquist frequency of Equation (2-9) is 500kHz. This translates to a data rate of 250kHz when considering a Manchester encoded signal. However, the ADC module is not only used to sample

the active channel receiving the data stream but also the other three quadrant channels to maintain control plane alignment operations. A novel approach to the ADC sampling/conversion sequence has been found that is able to uphold this 250kHz data rate while sampling the other three quadrant channels and performing clock recovery operations.

$$fs = 2 \times fmax \quad (3-16)$$

As discussed in Figure 3.12, the ADC module switches between the active channel collecting the data stream (controlled by multiplexor B) and rest of the channels (controlled by multiplexor A) every other sampling/conversion sequence. This procedure results in the active channel collecting the data stream being sampled three consecutive times every 8 ADC sampling/conversion sequences. It is at this triple data point there is a guaranteed edge on the active channel as specified by Manchester coding and indicated by the arrows in Figure 3.35. It is on this active channel edge that clock recovery operations can occur as specified by Figure 3.32.

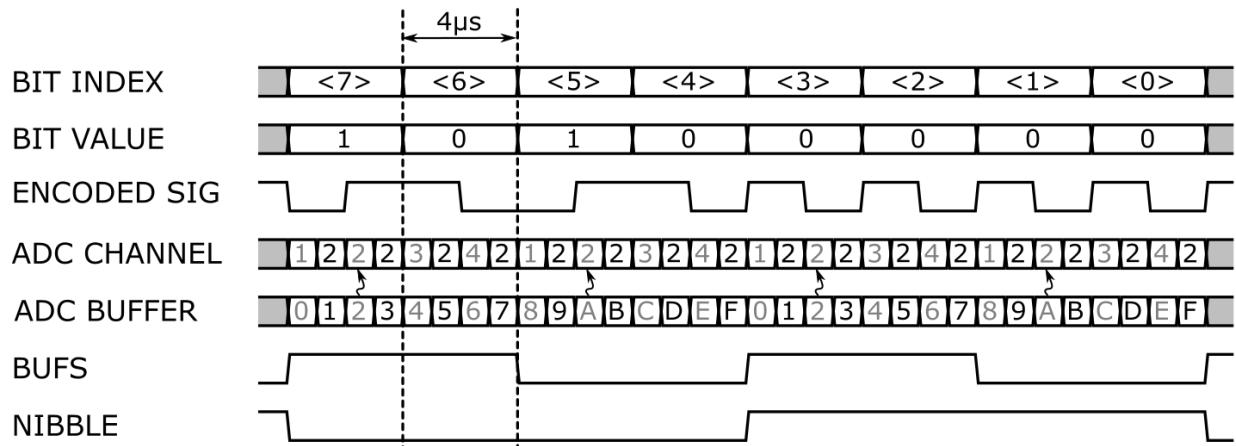


Figure 3.35: Signal diagram of timing for clock/data recovery of encoded signal¹⁶

¹⁶ Gray indices on ADC buffer and channel rows indicate multiplexor A inputs (auto-scan through quadrant channels) while black indices indicate multiplexor B inputs (active channel for data stream)

3.5.4 Firmware/Modulation Engine

The following state machine in Figure 3.36 details the modulation engine that has been previously abstracted in Figure 3.25 and Figure 3.32. This state machine is meant to serve as a visual aid in understanding the process by which the master and slave transceivers seek to connect (signal lock state of 1), begin handshaking and ready themselves for data transmission (signal lock state of 2), and transmit/receiver data nominally (signal lock state of 3).

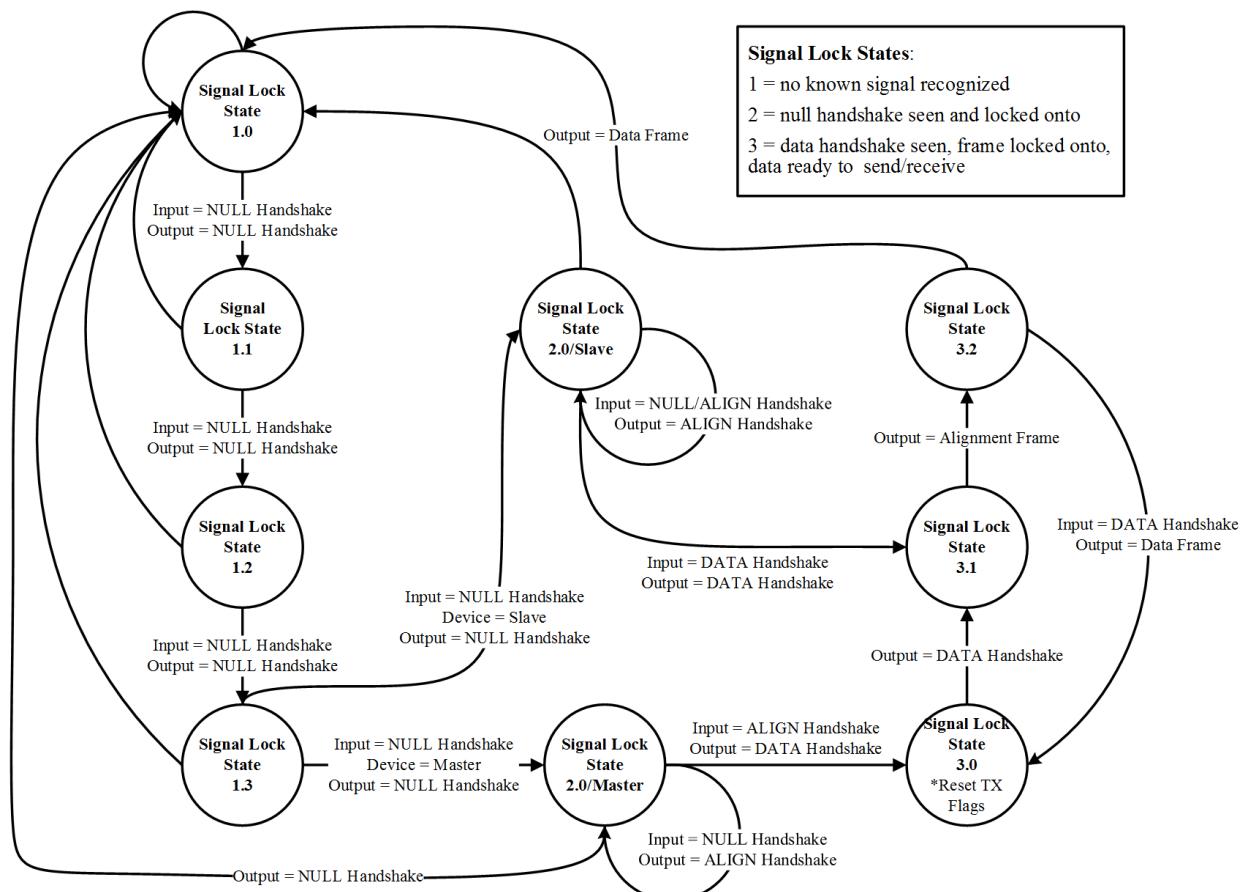


Figure 3.36: State machine of signal lock firmware logic¹⁷

¹⁷ State transitions arrows are labeled with required input for change as well as output of that event (arrows with missing input label encompass every other case not defined for that state)

3.6 Debugging Interface

The transceiver pair acts as a standalone communication link to replace the wired Ethernet connectivity between two endpoints. Therefore, no setup is needed for normal operation other than obtaining a transceiver set and supplying power. However, a debugging interface has been envisioned to allow for easy troubleshooting and data capture during development. This debugging interface utilizes a Chrome App to interface with the USB module on the MCU. A screenshot of the debugging interface in operation is shown in Figure 3.37. To setup the debugging interface, the following steps need to be completed [33]:

- Install Google Chrome on a Windows/Mac/Linux machine
- Download debugging interface source code files¹⁸
- Open Chrome and go to *Menu > (More) Tools > Extensions*
- Click *Developer mode > Load unpacked extensions...* and browse to the */app/* directory within the download Chrome App source files
- Click *Launch*

¹⁸ Chrome App source code files located under */app* directory from main GitHub repository at github.com/joshandnoodles/Thesis/

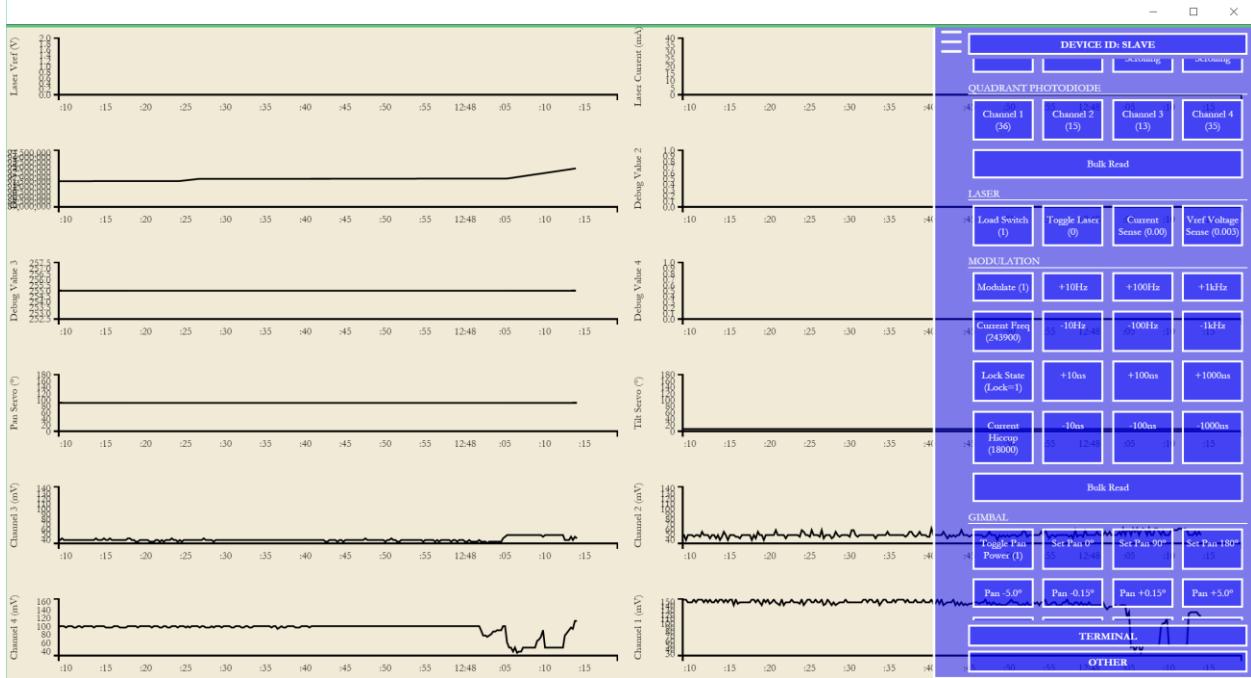


Figure 3.37: Screenshot of debugging interface graphing and control

3.7 Gimbal

A rotation mechanism is used to apply control plane alignment movements to each transceiver. A dual-servo pan/tilt gimbal is used to accomplish these multi-dimensional movements. Hitec HS-645MG servos are used as the motor feedback device for both pan and tilt motions for the following reasons [17]:

- Ability to operate using pre-existing 5V power supply
- Analog operation allows for smoother, more continuous movement as compared to digital servos and associated jitter during angle adjustments
- 180degree operating range (allows for half sphere movement radius)

Custom plastic brackets were made using a MakerBot 3D printer to create the gimbal system. In total, the following three plastic forms were created: a base that affixes to the pan servo acting to stabilize the entire system, a bracket to connect the pan and tilt servos, and an arm driven by the

tilt servo to support the optics board. The servos are mounted on the brackets using machine screws in conjunction with four-arm servo wings. Each 3D printed part was first model in the open-source Blender application before being exported and sent to be printed. A complete rendering of all 3D printed parts as well as additional system components can be seen in Figure 3.43.

3.8 System Integration

3.8.1 Multiple Boards

The four-board system presented in the design section overview and displayed in Figure 3.2 must be interfaced together to create a usable transceiver. This is done largely by the Clicker 2 PIC32MX development board's daughtercard socket headers and 30cm female-to-female jumper wires. A detailed illustration of interconnections between PCBs is shown in Figure 3.38.

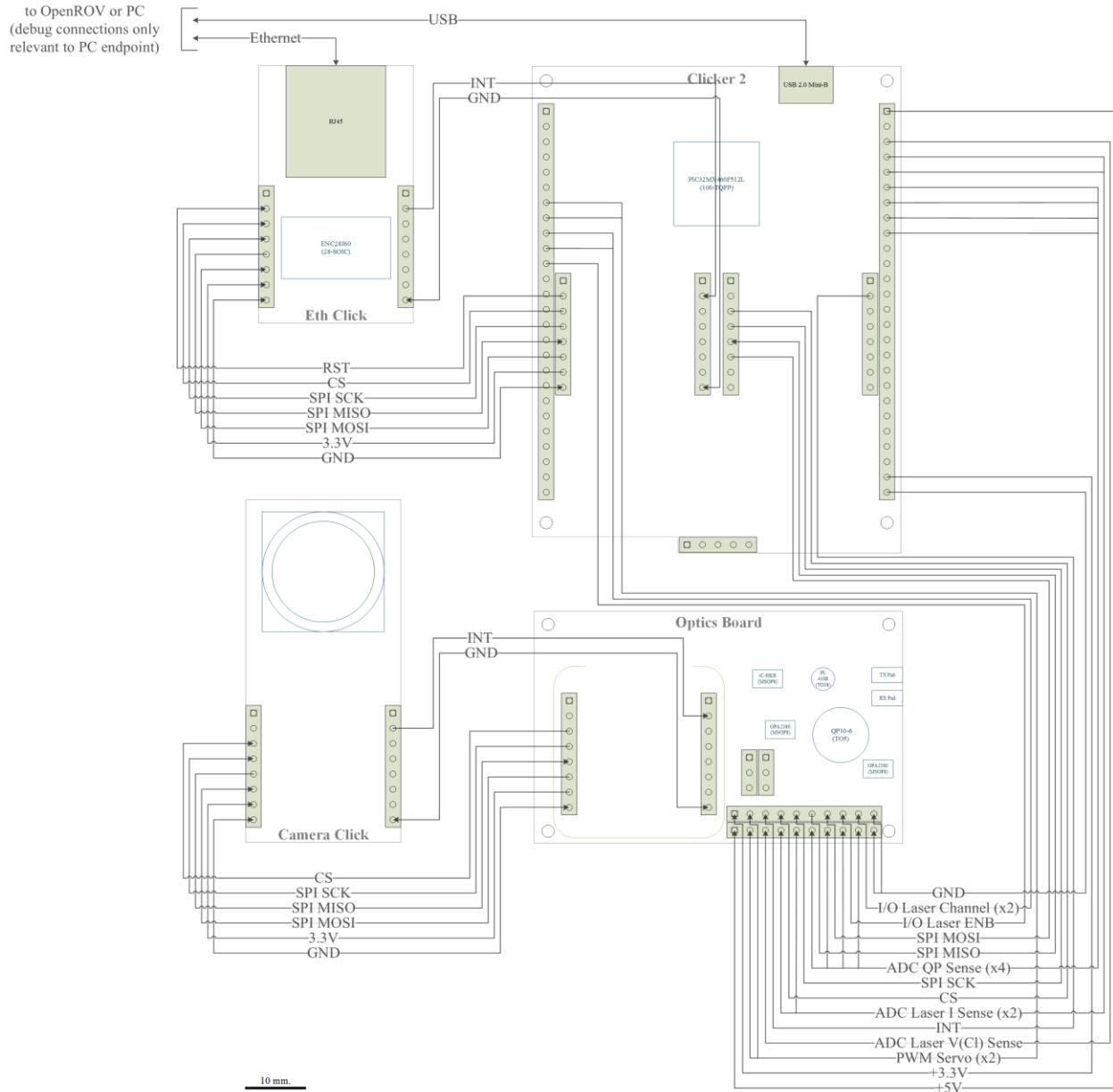


Figure 3.38: Connectivity of four board transceiver system¹⁹

3.8.2 OpenROV Integration

An initial investigation into the OpenROV system showed that the rover's 100m long tether communication is driven by a pair of Tenda Homeplug Adapter devices. These devices convert Ethernet packets into signals that travel down the long twisted-pair tether. These Tenda

¹⁹ Does not reflect final layout or architecture of optics board, PCB size and components are to accurate scale as per legend

Homeplug adapters can easily be replaced in the OpenROV with the envisioned system by rerouting the Ethernet cable into the Ethernet daughtercard of the transceiver. This upgrade requires no hardware modification and leaves the initial system intact. The OpenROV's main functionalities were analyzed and the resulting high-level integration with the transceiver is shown in Figure 3.39. However, one should keep in mind that the transceiver needs to be capable of the data rate requirements of the OpenROV.

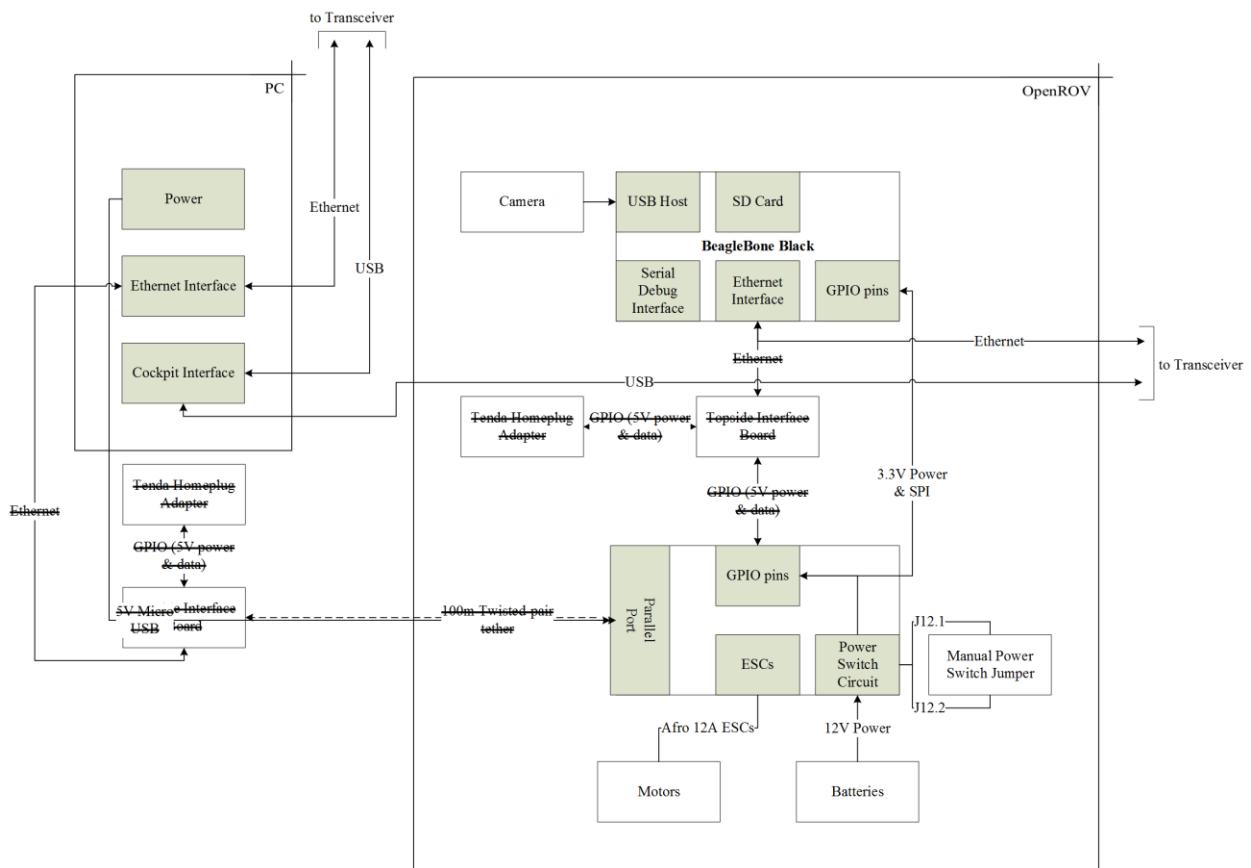


Figure 3.39: Block diagram of OpenROV and its integration with the pair of transceivers²⁰

To better understand the data rate requirements of OpenROV, the windows tool NetWorx was used to collect real-time bandwidth monitoring of the OpenROV's network interface. The tool allows collection of both upstream and downstream traffic of the network interface (in this case

²⁰ Components with strikethroughs represent those rendered unnecessary by this system

eth0). Measurements of the OpenROV's bandwidth usage shows that it outputs 25Mbps of upstream data and consumes a negligible amount of downstream data at nominal resolution/frames per second (1280x1024/30fps). The upstream data rate of the OpenROV decreases to about 2.5Mbps after reducing the frames per second to 3fps as seen in Figure 3.40²¹. This same scalability is seen by reducing the video resolution. These results show that although the OpenROV nominally utilizes a large bandwidth of 25Mbps, it can be modified to fit specifications by simply scaling the resolution and frames per second.

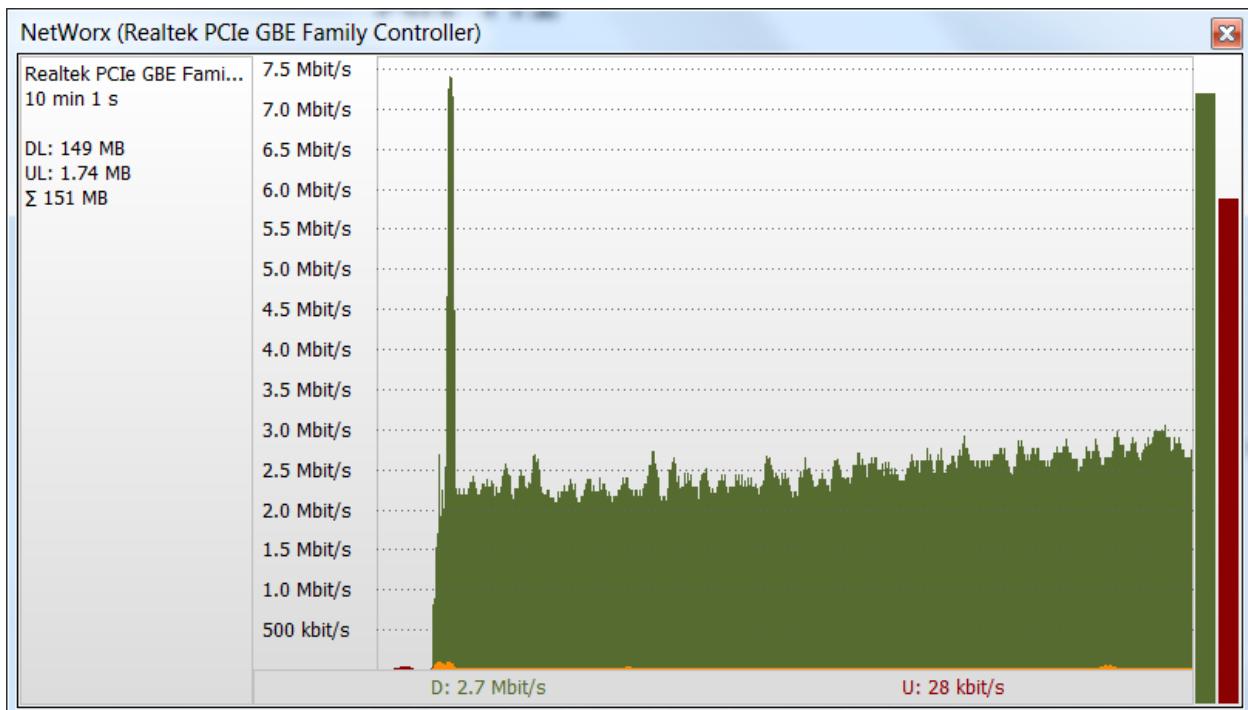


Figure 3.40: Bandwidth usage of OpenROV collected using NetWorx after reducing fps to 3
An analysis of the OpenROVs power supplies is needed to ensure the rover can supply enough power for the transceiver. The OpenROV system was reverse engineered using the openly available schematics. An overview of the OpenROV's power sources, regulators, and high-

²¹ Video resolution and frame rate were modified by using Putty to alter node.js configuration file located at /opt/openrov/cockpit/src/lib/config.js on the BeagleBone SD card

power consumers is shown in Figure 3.41. This analysis shows there is ample margins for the transceiver to operate by piggybacking off the 5V and 3.3V rails on the rover.

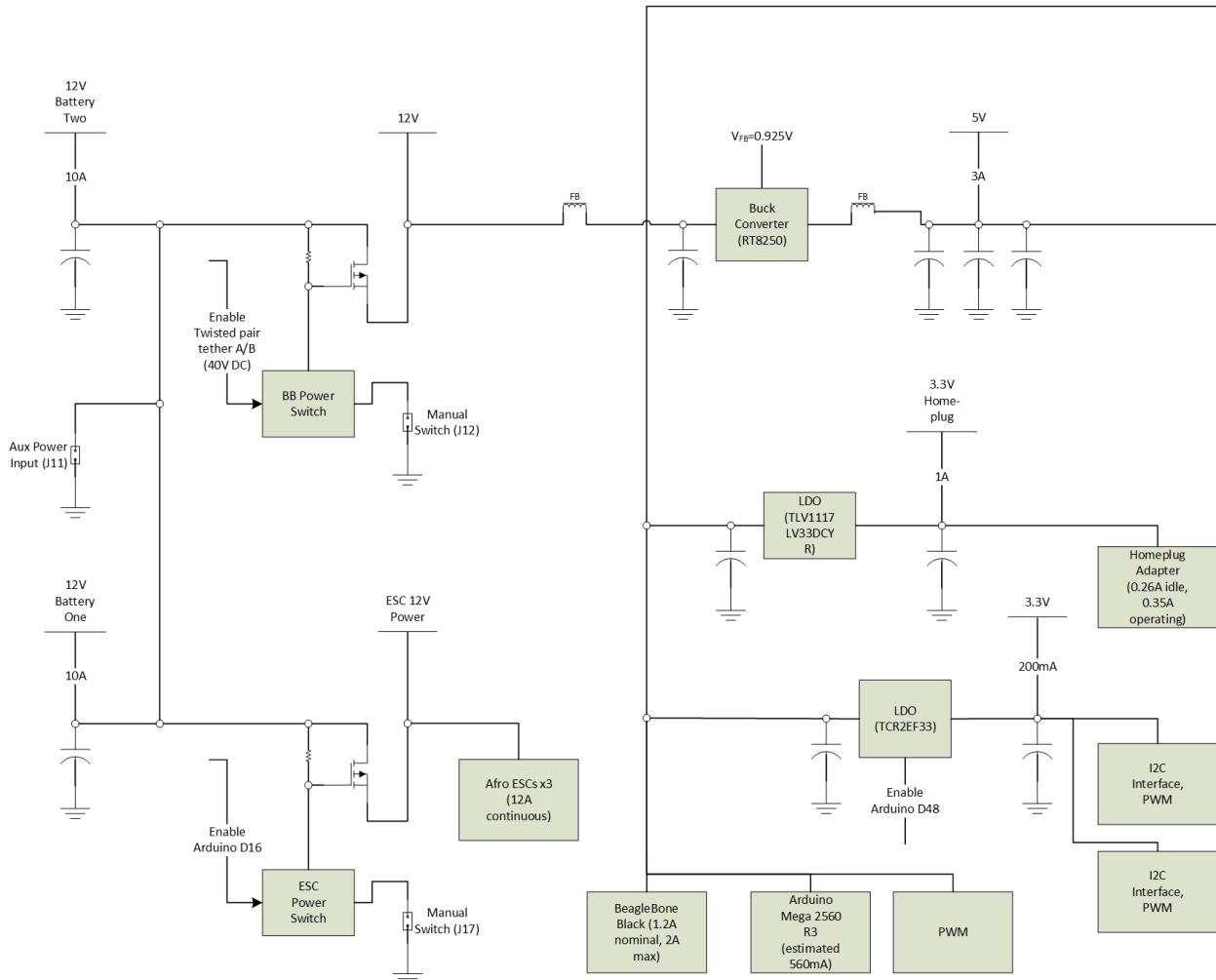


Figure 3.41: Block diagram of OpenROV's power supplies and major consumers

Another issue exists with being able to power-on the OpenROV without the tether. Normally, the OpenROV does not provide power to its main MCU (BeagleBone) until an appropriate voltage is seen on the tether from the Homeplug Adapter device. This becomes an issue when the transceiver is installed as there is no device to tell the OpenROV's MCU to power on. This can be overcome using a built-in override within the OpenROV's architecture. A two-pin header can be installed at location J12 on the OpenROV Controller board highlighted in Figure 3.42 to automatically turn on the MCU when shorted with a jumper.

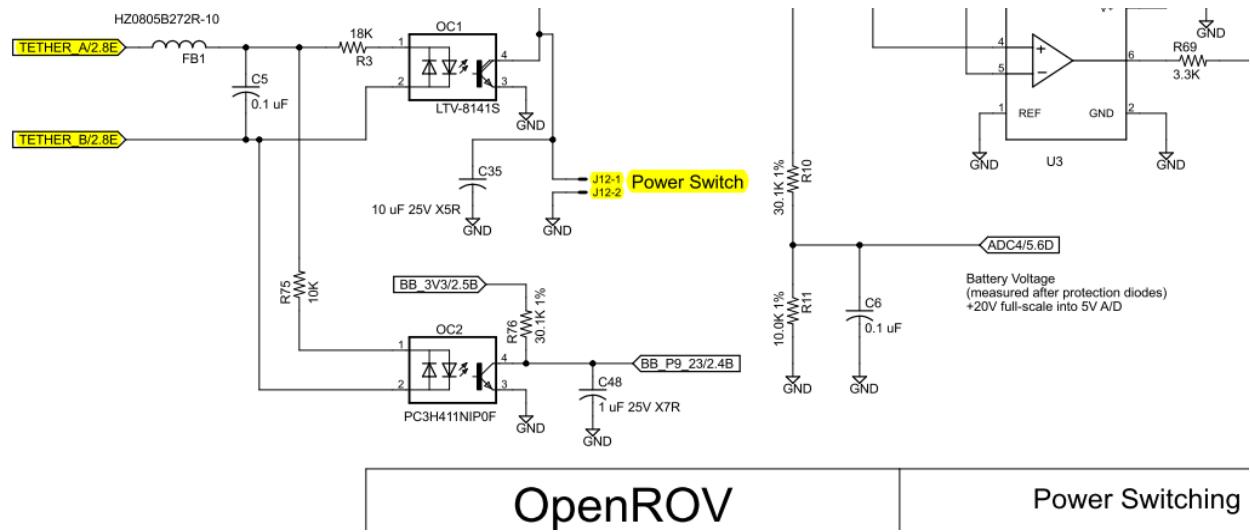


Figure 3.42: OpenROV schematic section showing MCU power-on override [34]

3.8.3 Gimbal and Optics Board

The optics board is mounted on the upper tilt arm of the gimbal using a machine screw, a nylon nut, and spacers to protect the PCB components. This is necessary to direct the transmitter and receiver optics on the optics board. Figure 3.43 shows a complete rendering of mechanical integration of the gimbal and optics board created in Blender.

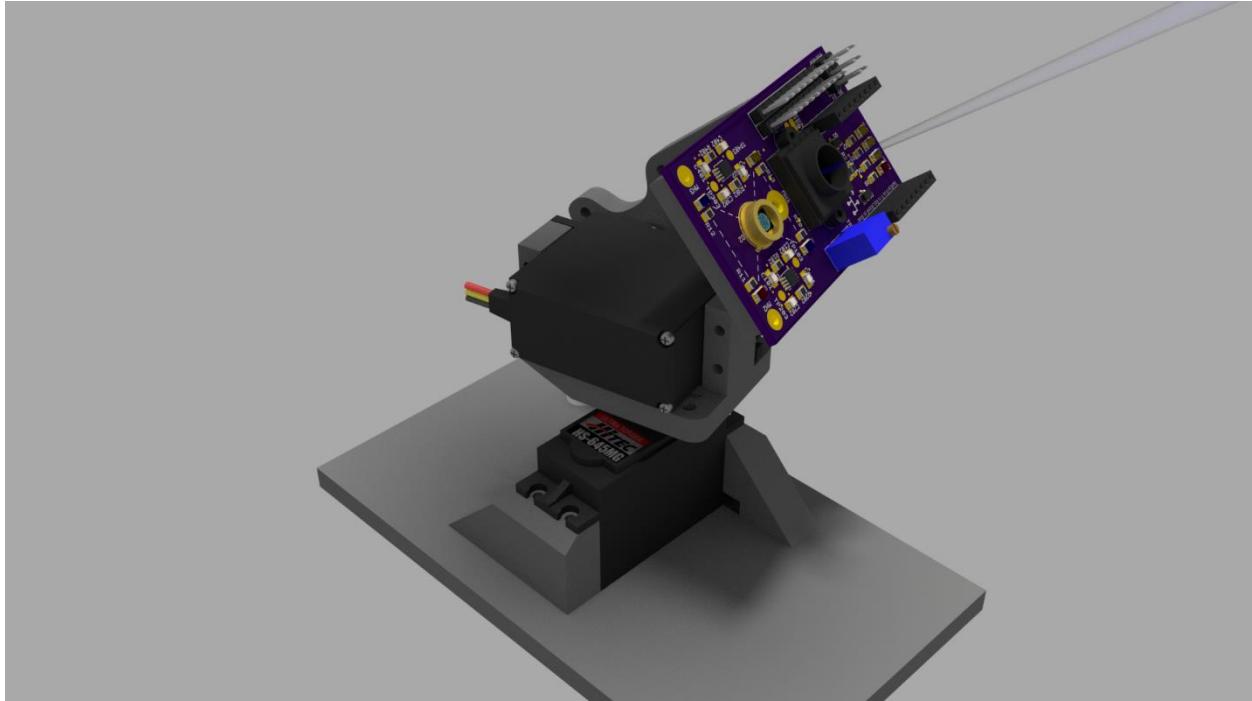


Figure 3.43: Rendering of entire gimbal and optics board using Cycles engine in Blender²²

²² Servo model and servo wing model courtesy of Phil Maddox

3.9 Optics Board Schematic and PCB

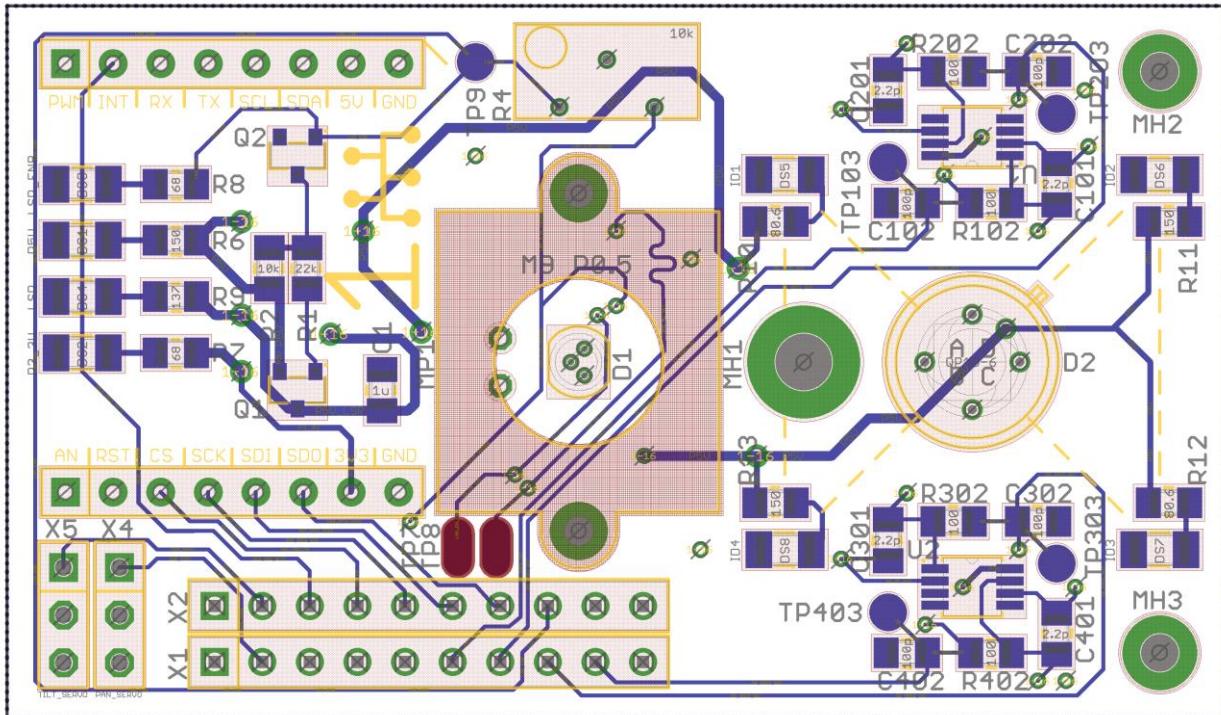


Figure 3.44: Optics board top-side layout

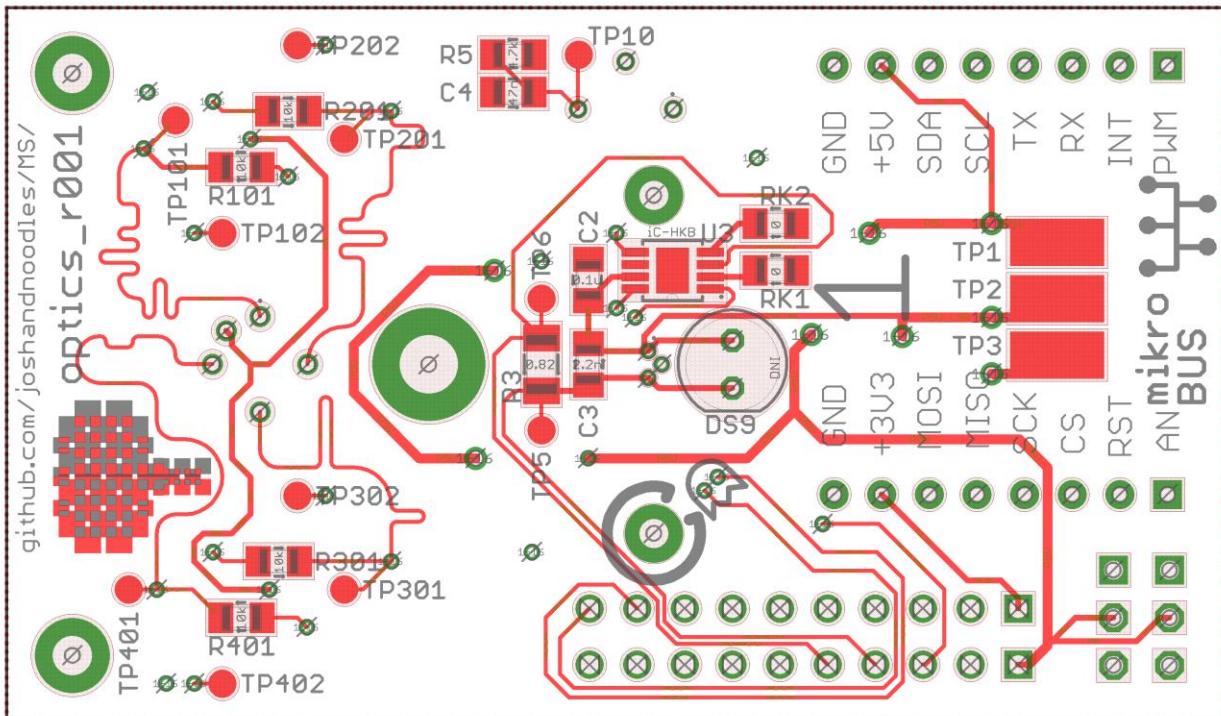


Figure 3.45: Optics board bottom-side layout

4 Results

4.1 Experimental Setup

All data published in this results section took place on the 9th floor of Rhodes Hall at the University Cincinnati. An image of the setup for a single data point of one of the experiments can be seen in Figure 4.1. For longer distance measurements, certain functionalities of the system were disabled (i.e. control plane alignment and momentum). Unless otherwise noted, the setup of all experiments was as follows:

- Bright ambient lighting conditions (fourteen 40W fluorescent lights spaced evenly across 10' ceiling directly above testing)
- Normal air particle count for non-clean room laboratory environment
- Voltage reference current control for laser driver tuned to 2V using potentiometer
- External 1A USB wall adapter power source per transceiver
- Collimating lens focused for minimum spot size at 30m
- Transceivers operating at half rate (125Mbps)

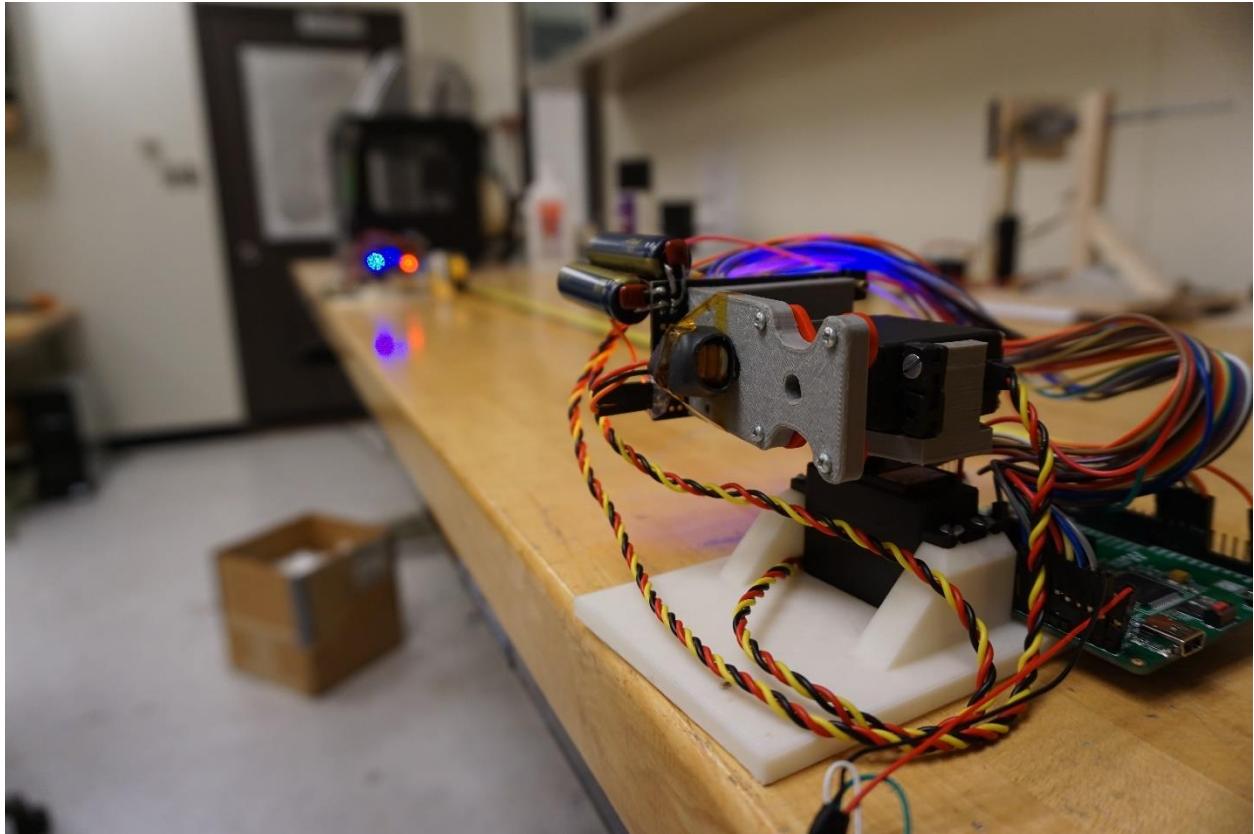


Figure 4.1: Photograph of experimental setup during 1m BER distance measurement

4.2 Hardware Validation

Each PCB was brought up using a specific procedure to minimize damage to sensitive components while verifying different board-level functionalities. During bring-up and development, mistakes were found in the initial hardware design and were corrected by applying reworks. These reworks were corrected in revision 2 of the optics board schematic as shown in Appendix I. Revision 2 of the PCB should be used for any further progression of this project. The following is a summary of reworks applied to correct revision 1 of the design:

- 10kohm potentiometer nets incorrectly connected in voltage divider setting voltage reference current control

- 4700uF electrolytic capacitor added to each servo to reduce effect of current surges on main 5V rail
- Main 5V rail to noisy to bias QP channels, replaced with external 12 batteries (this also decreases fall time of QP channel response)
- 440pF capacitance added to laser control lines to reduce rise time and subsequent overshoot that created resonances on receiver amplifier outputs

The load switch's functionality was tested to ensure its proper operation before mounting the laser diode. As predicted, the load switch output remained at 0V until the MCU's I/O switched the P-channel MOSFET on. Additionally, the load switch prevented overshoot of the output rail by using a slow start circuitry. The actual rise time of the load switch was measured to be 7us as seen in Figure 4.2.

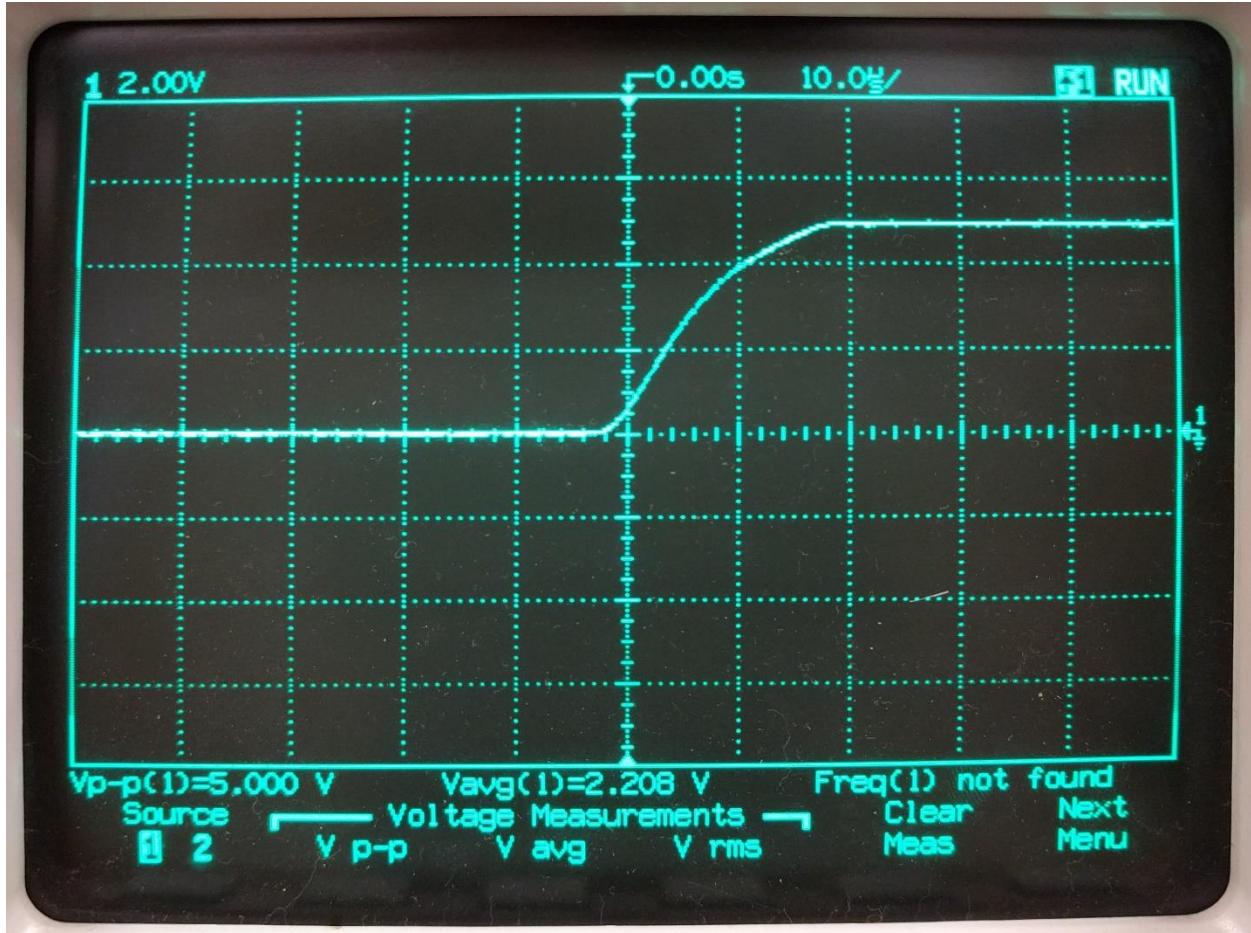


Figure 4.2: Waveform of the output node of the load switch (channel 1) during turn on

With the laser diode mounted, measurements were taken of the main 5V rail and the current draw of the main 5V rail from the optics board. A Fluke Y8100 device was used to collect the current measurements. It was configured to have a scaled output of 2V:20A. The resulting voltage and current measurements are shown in Figure 4.3. This shows that the main 5V rail remained steady during laser modulation, and the optics board had a constant draw of about 106.9mA.

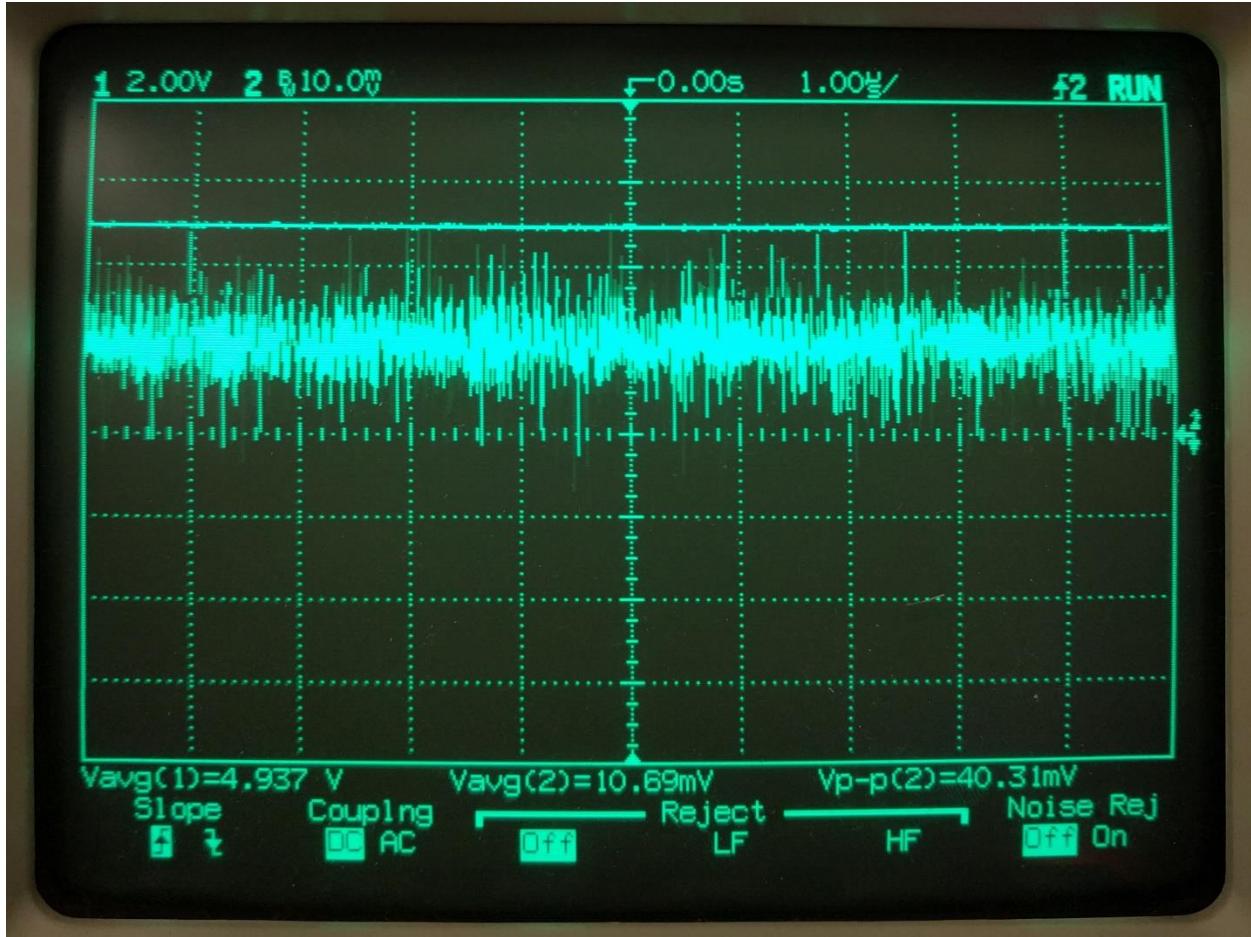


Figure 4.3: Waveform of the 5V rail (channel 1) and the current draw of the optics board from the 5V rail (channel 2) during laser modulation activities

Finally, the receiver circuitry was tested by modulating the distant transceiver with a steady stream of zeros. At half-rate using Manchester encoding, this translates to a 125kHz square wave. This signal was aligned to one of the channels of the nearby transceiver's QP. Measurements were then taken at the output of the channel's transimpedance amplifier/low-pass filter. The resulting waveform of this node (channel 2) as compared to the distant transceiver's laser control line (channel 1) is shown in Figure 4.4.

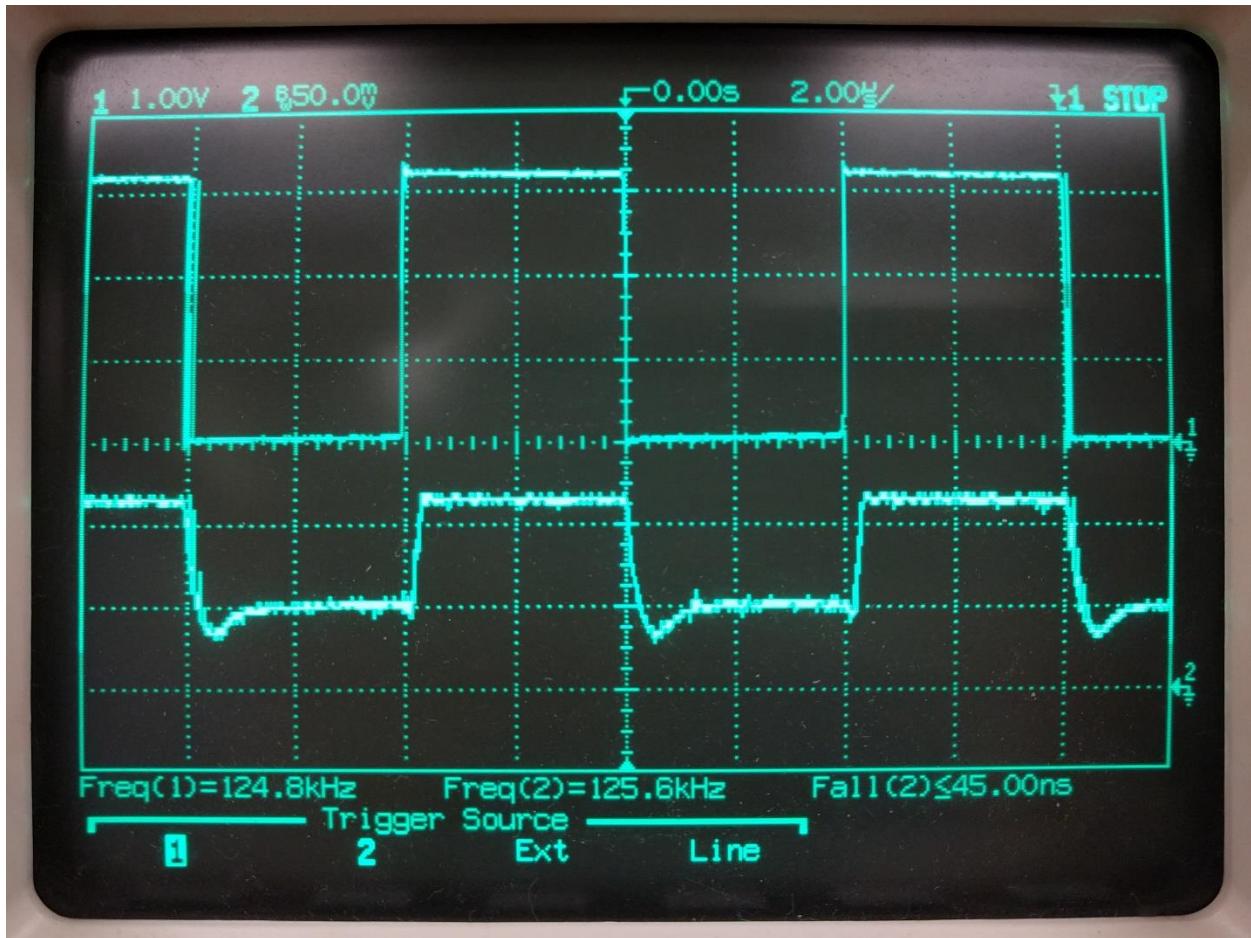


Figure 4.4: Waveform of laser control (channel 1) and receiver amplifier output (channel 2)

This shows that the receiver module can appropriately reconstruct the data stream from the visible light carrier. The reconstructed signal is sharp with a fall time of less than 45ns. The amplitude of the signal is more than sufficient for sampling using the ADC module. Another interesting characteristic to note is that there is a noticeable delay between these two signals in Figure 4.4. This delay is small (<100ns) and may be propagating from either the laser driver, laser diode, QP, receiver amplifier, or a combination of these. However, this is not an issue since the transceivers are operating asynchronously.

4.3 Free-space Testing

The culmination of testing for a communication system is its ability to transmit/receive data without errors. Additionally, it is important to test the system over various distances to try to understand how it behaves at different ranges. Distances starting at 10cm were tested all the way up to 3m. Additional testing setup follows those outline in the Experimental Setup section and shown in Figure 4.1. An image of single transceiver that was one endpoint of testing can be seen in Figure 4.5.

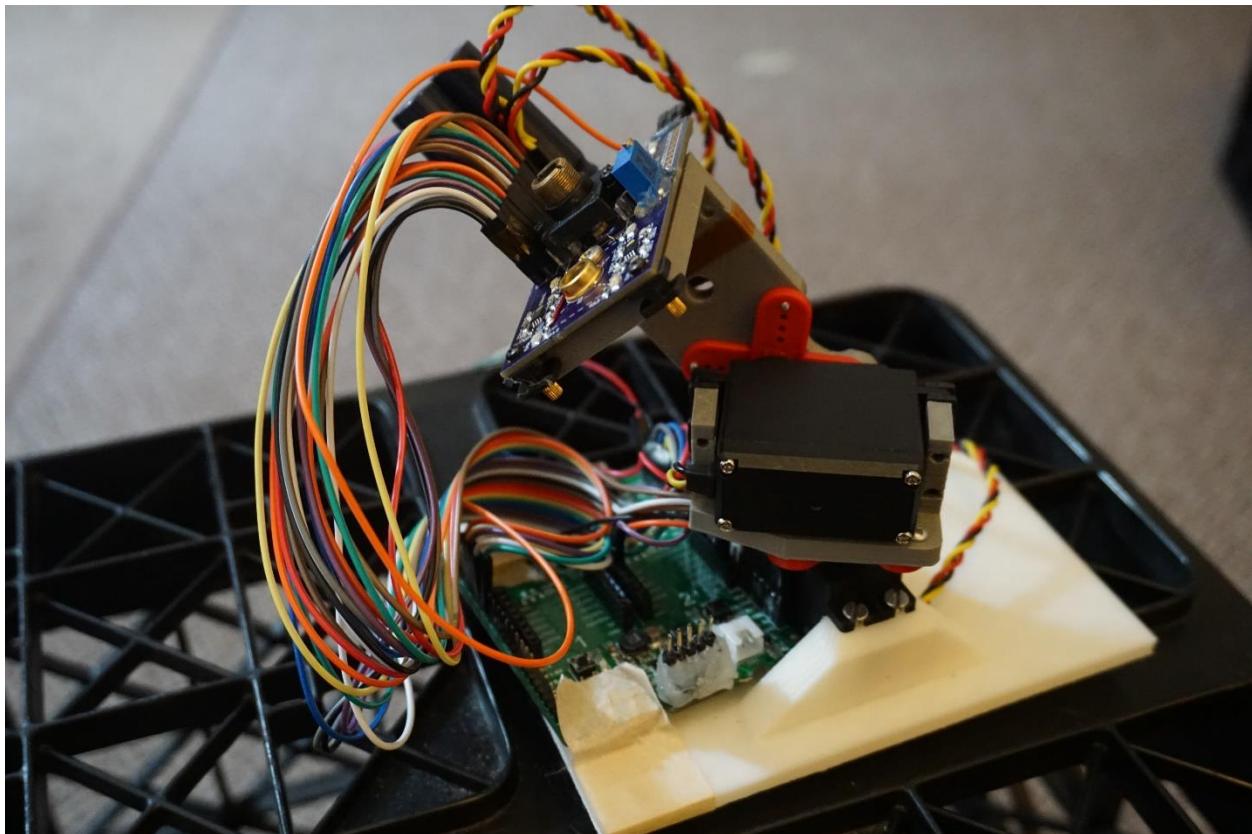


Figure 4.5: Photograph of final transceiver built for project

The bit error results of testing at these different distances is display graphically in Figure 4.6. Likewise, the bit error rate is shown in Figure 4.7. Bit error measurements were collected from the MCU using the debugging interface every 250ms over the course of 60s. Shorter distances generally had better BER performance. However, there does not seem to be a noticeable pattern

of when these bit errors occur. For example, the 2m distance trial had a large number of bit errors in the first five seconds but no other errors the rest of the interval. It can be assumed this is the result of alignment errors of the laser on the active channel of the QP. Accurately aligning the system at longer distances using the gimbal is simply not feasible and even achieving manually alignment becomes cumbersome and unreliable.

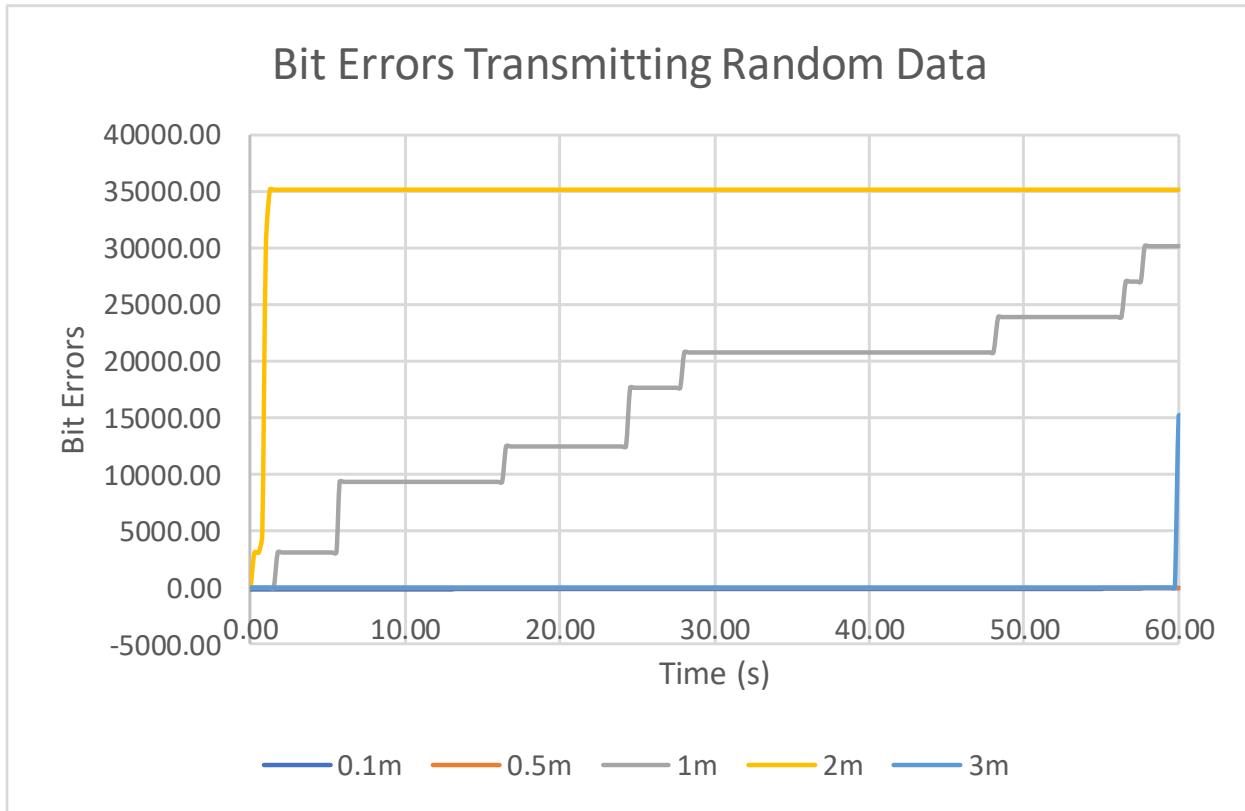


Figure 4.6: Bit error accumulation at varying distances²³

²³ Dummy data set was constructed by randomly sampling a sequential set of bytes valued from 0 to 255 without replacement

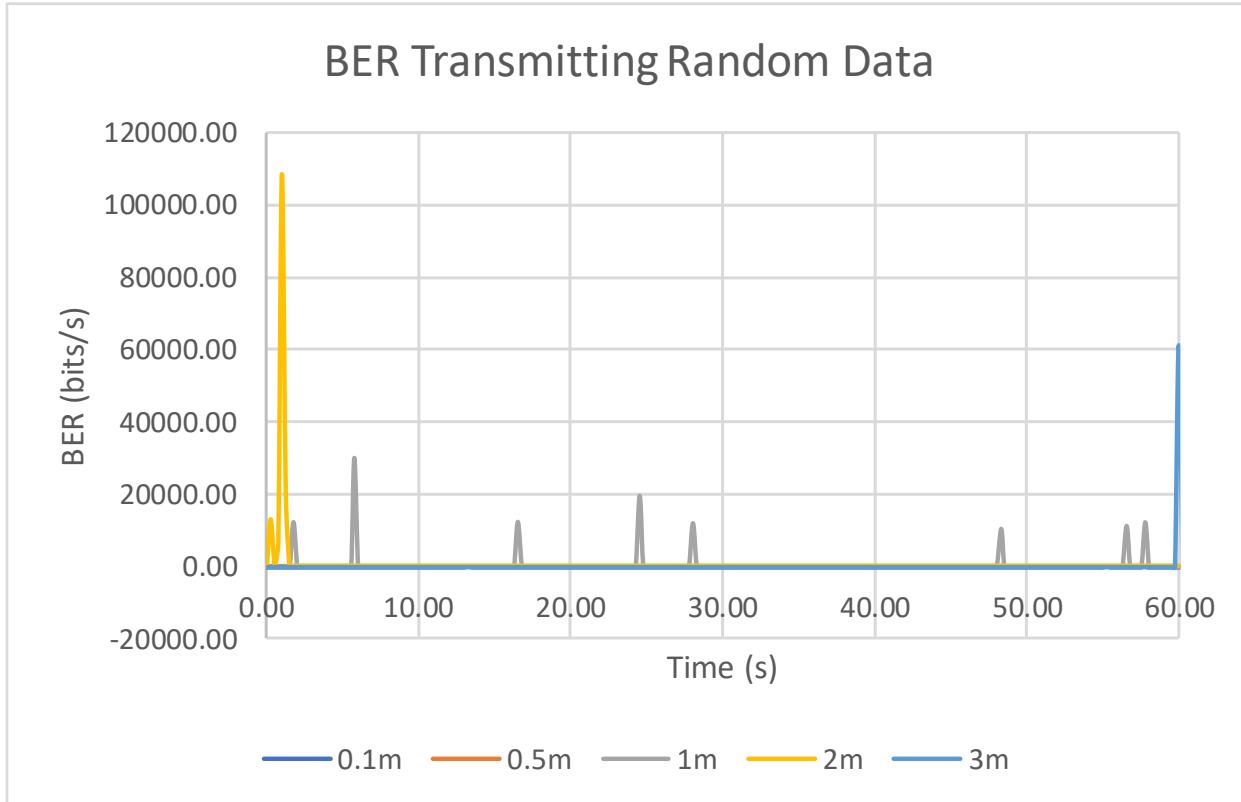


Figure 4.7: BER at varying distances²⁴

²⁴ Dummy data set was constructed by randomly sampling a sequential set of bytes valued from 0 to 255 without replacement

5 Conclusion and Future Work

5.1 Summary

This project began as a proposal to create a communication system suitable for oceanic environments. Initial investigations presented in the Literature Review and Theoretical Analysis section shows that an underwater communication system would benefit from using blue collimated light as the data carrier. This particular wavelength of light has low attenuation rates in both fresh water and saltwater while having the additional benefit of residing in unregulated spectrum. The main deliverable to develop a pair of microcontroller-based transceivers using QPs for both data capture and control alignment is detailed in the Research Objectives section.

The System Design section provides a meticulous discussion of the exact architecture of the proposed system including component selection and integration. Microchip's PIC32MX460F512L is used as the main MCU both data plane and control plane tasks. Its ADC module is crucial in both data/clock recovery operations, maintaining optical alignment using a novel sampling approach, and monitoring important voltage and current sense measurements across the system. The transmitter module uses a Manchester coding approach to modulate the laser diode using an integrated driver. On the receiver side, the modulated signal is deconstructed to retrieve the control plane alignment information as well as the Ethernet packets. These Ethernet packets are constantly sent and received from the network by interfacing with the pluggable Ethernet daughtercard.

A thorough investigation into how the proposed system integrates with the OpenROV is given in the System Integration section. In this section, an analysis of the bandwidth required by the OpenROV showed that the data rates are easily scalable by adjusting the video resolution and

frame rate of the real-time video stream. The power supplies and other hardware on board the OpenROV have been reverse engineered to ensure the transceiver can be integrated into the original OpenROV system. Additionally, volatile solutions are given for any modifications that need to be made to guarantee system coexistence.

An objective examination of the implemented system's performance is given in the Results section. A description of the procedure and setup used to obtain the data is given for comparison with future system implementations. Transient waveforms were collected to validate important aspects of the hardware design. Finally, an inclusive performance analysis was then conducted by analyzing the BER of the transceiver pair at increasing distances.

5.2 Conclusion

The constructed system tasked to accomplish the outlined research objectives performs well in certain capacities and undesirably in others. Before these details are discussed, a word about the physical design and integration should be noted. The overall design of this system is a significant step in the development of a dynamic, underwater communication system. The hardware and firmware design execution proceeded with minimal reworks and other complications. This is confirmed by the hardware validation done in Section 4.2. Besides this, there are two main areas of the system to be assessed: the data plane functionality and the control plane functionality.

The data plane performs admirably to sustain a full-duplex, long-distance communication link at 125kbps. It is able to recover from bit errors and lost signal events with little interruption. Additionally, the choices for modulation and clock recovery operations involve minimal hardware and require sampling rates very near the Nyquist frequency. The custom framing structure's modularity allows for quick changes during operation and encourages future improvements. Most importantly, the transceivers are able to sustain a communication link at

distance error-free. However, the data plane is only able to support data rates of 125kbps (half the rate envisioned for the proposed system). This limitation is due to in the execution speed of the MCU and the ADC sampling speed. There is not enough bandwidth for the MCU to service all interrupts and execute main thread operations if modulation is set to 250kbps. Additionally, the ADC module can only operate up to 1Msps which limits the maximum data rate this system can achieve. This data rate limitation is the only major shortcoming in the data plane.

The control plane's operation comes less close to meeting the objectives proposed for this system. The gimbal does not have resolution needed to make fine enough adjustments while maintaining alignment with the QP. This issue is two-parted. First, the analog servos being used have a minimum movement granularity of 0.15degrees. At a distance of 1m, this translates to a movement of 2.62mm at the distant transceiver. Secondly, the QP quadrants are extremely small with each quadrant being 1.77mm wide along its longest axis. This means that even a relatively small servo adjustment resulting in a 2.62mm movement at the distant transceiver may result in the laser moving fully off the QP.

5.3 Discussion and Future Work

The benefits of having a high-bandwidth communication system to use in underwater applications are many. Not only could this further ocean exploration technologies but additional uses could be envisioned for a dynamic system such as those discussed in the Applications section (i.e. a secure point-to-point link for medical devices). Regardless, the work presented in this paper furthers the progress of a system that could be used in these types of applications.

The final result of this project is a full-duplex communication system operable up to 125Mbps with self-alignment capabilities at small distances. There are inherent shortcomings of the design of this system as discussed in the Conclusion section. However, many of these are correctable

with either minor modifications or the selection of higher-grade components. These changes could be part of future work carrying on from this project.

The bandwidth limitation of this design can be addressed in multiple manners. A more major change would be to re-architecture the design to use separate MCUs for the data plane and control plane operations. Even further, separate MCUs could be used for the transmitter module and receiver module within the data plane. This would give each MCU more bandwidth to complete its individual tasks at higher speeds. A simpler modification would be to use the same single-MCU architecture but with a faster MCU. Microchip offers higher performing 32-bit MCUs that can run at speeds up to 252MHz (i.e. the PIC32MZ EF family). Regardless of the approach chosen, the ADC module needs to be able to sample at faster rates to interpret high-frequency signals. This is again easily solved by either using a higher performing MCU (the PIC32MZ EF family offers 12-bit ADC modules capable of 18Msps) or interfacing with a discrete ADC module.

The control plane alignment limitations of this system are more severe than the bandwidth limitations but are still solvable with future work. A simple solution to increase achievable alignment distance would be to replace the current QP with a QP that has quadrants with larger active areas. This would help to decrease the chances that the gimbal would move off the QP causing optical misalignment. Likewise, a focal lens or light pipe in front of the QP could be used to redirect incoming laser light creating a larger effective area for the QP. Conversely, the gimbal could be improved by either using a finer resolution motoring system or by placing an additional translation stage on the top of the pan arm. This translation stage could make minor adjustments of the distant transceiver's optics negating the trigonometric effects that moving the servos have on the laser position at the distant transceiver (being distant rotational stages). Using

one or a combination of these improvements will result in reliable self-alignment at greater distances.

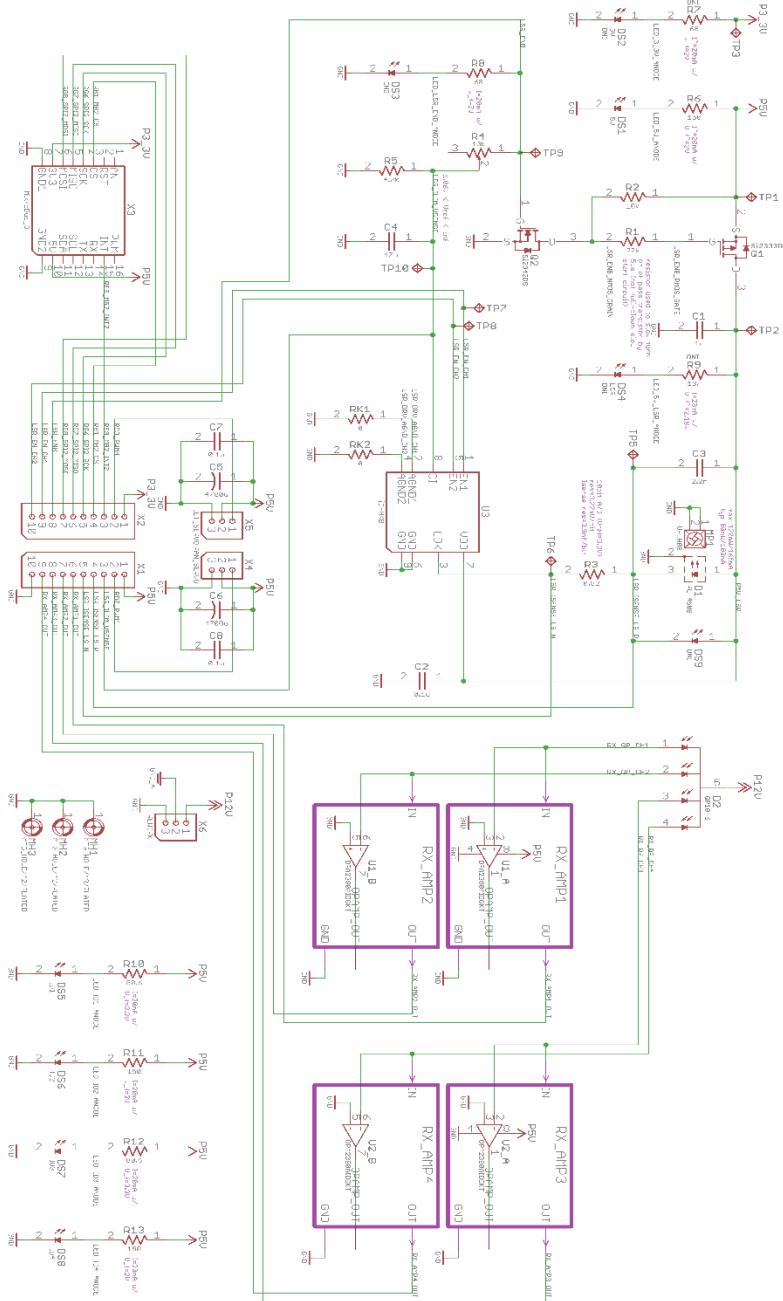
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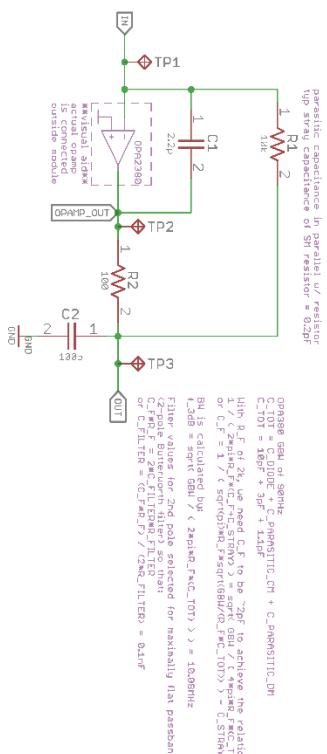
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Appendix I



Title: optics_I_002
 Author: Joshua Alexander
 Date: 6/13/2017 2:31 PM Sheet: 1/1
 REV: R002



Title:	optics_r002
Author:	Joshua Alexander
Date:	6/13/2017 11:25 AM
Sheet:	1/1