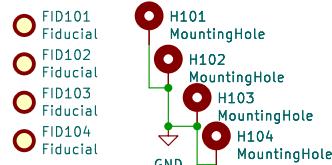
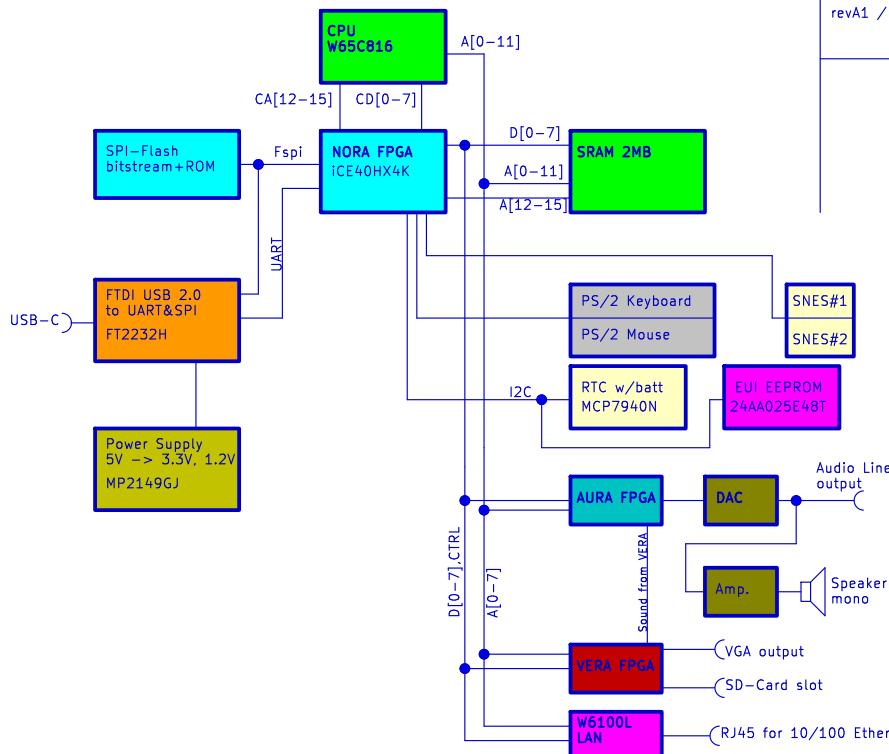


# X65 SBC rev.A1

Single-Board-Computer WITH THE 65816 (6502) CPU,  
2MB RAM, VGA, Sound, 2x PS/2, 2x SNES Joypad, Ethernet LAN

Block Diagram:

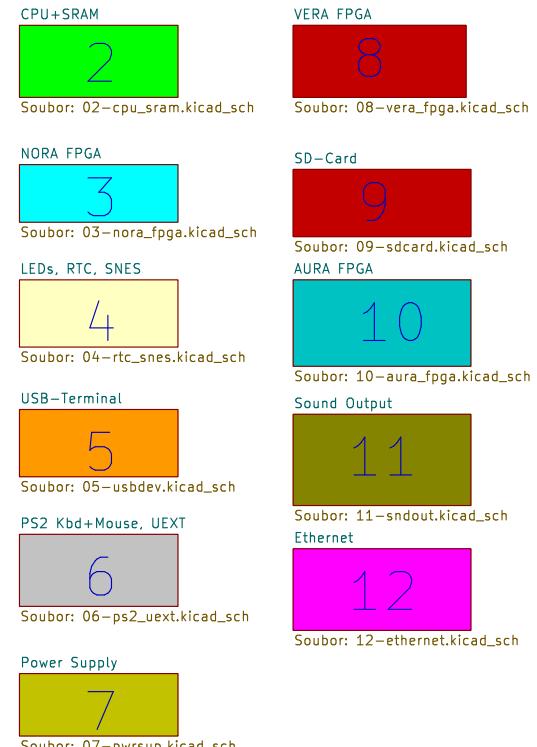


Important Links:  
[x65.eu](http://x65.eu)  
[www.jsykora.info](http://www.jsykora.info)  
[github.com/jsyk/x65](https://github.com/jsyk/x65)

Revision History:

revA1 / 13.1.2024	Initial design based on MOBO+VABO rev001. PCB 180x100mm, 4-L.
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Schematic sheets:



X65 IS  
OPEN SOURCE:  

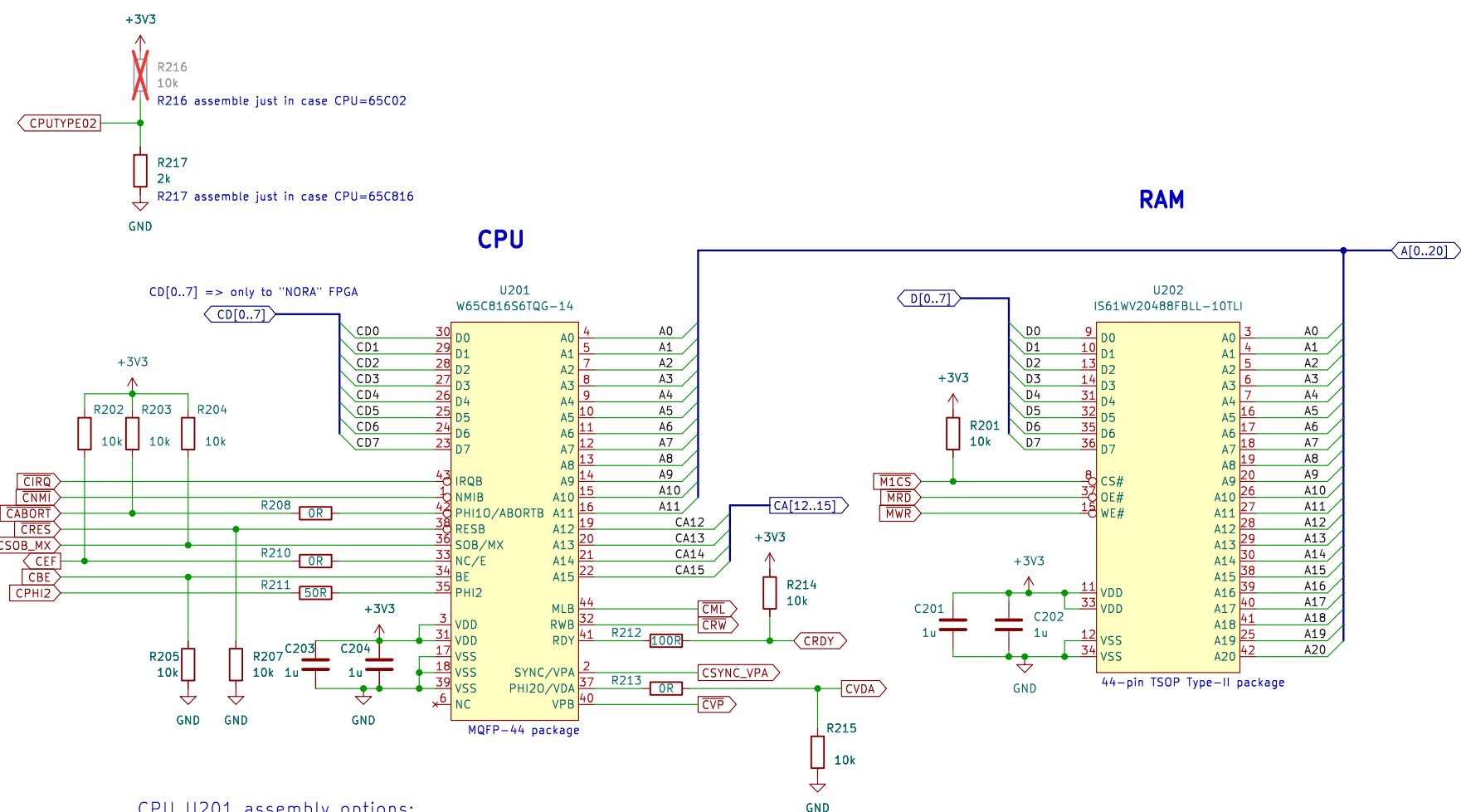
- + CIRCUIT SCHEMATIC
- + PCB LAYOUT
- + VERILOG FPGA DESIGN
- + TOOLS USED
- + ORIGINAL SOFTWARE

X65 Single Board Computer  
FOR X65.EU DESIGNED BY JSYKORA.INFO  
Sheet: /  
File: x65-sbc-revA1.kicad\_sch

Title: X65-SBC

Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

Rev: revA1  
Id: 1/12



65816 CPU, 2MB SRAM  
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /CPU+SRAM/  
File: 02-cpu\_sram.kicad\_sch

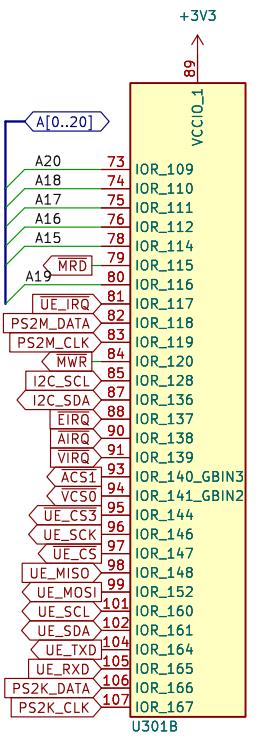
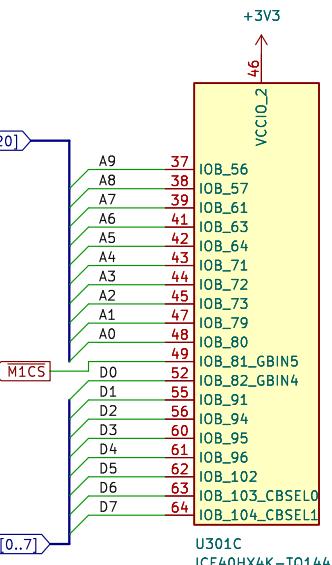
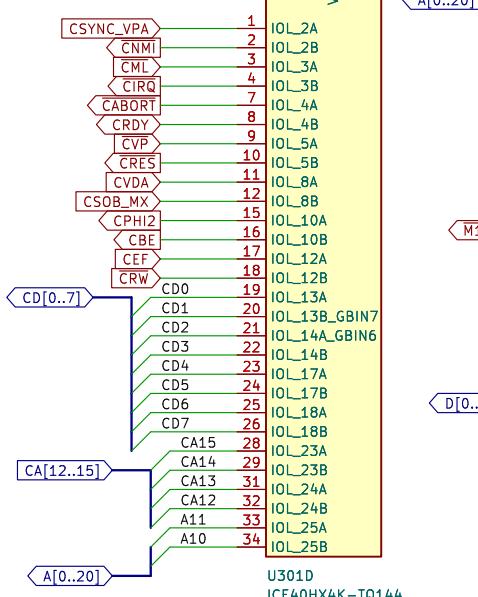
**Title: X65-SBC**

Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

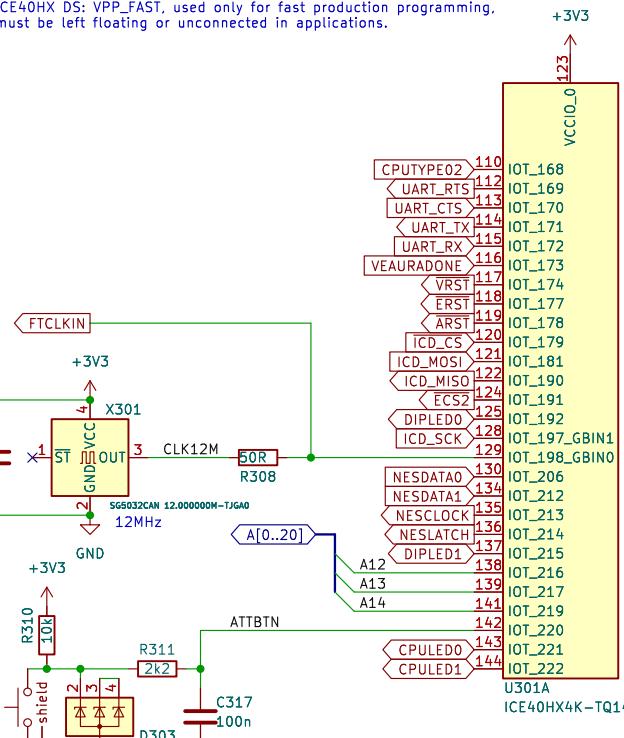
Rev: revA1  
Id: 2/12

## NORA FPGA

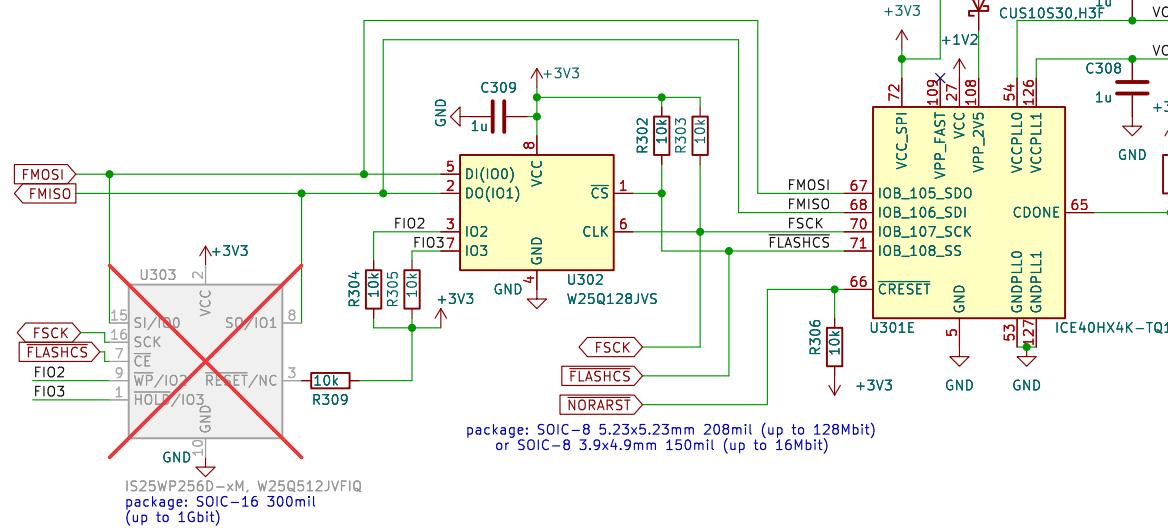
= NORth Adapter



ICE40HX DS: VPP\_FAST, used only for fast production programming,  
must be left floating or unconnected in applications.



## UNIFIED ROM



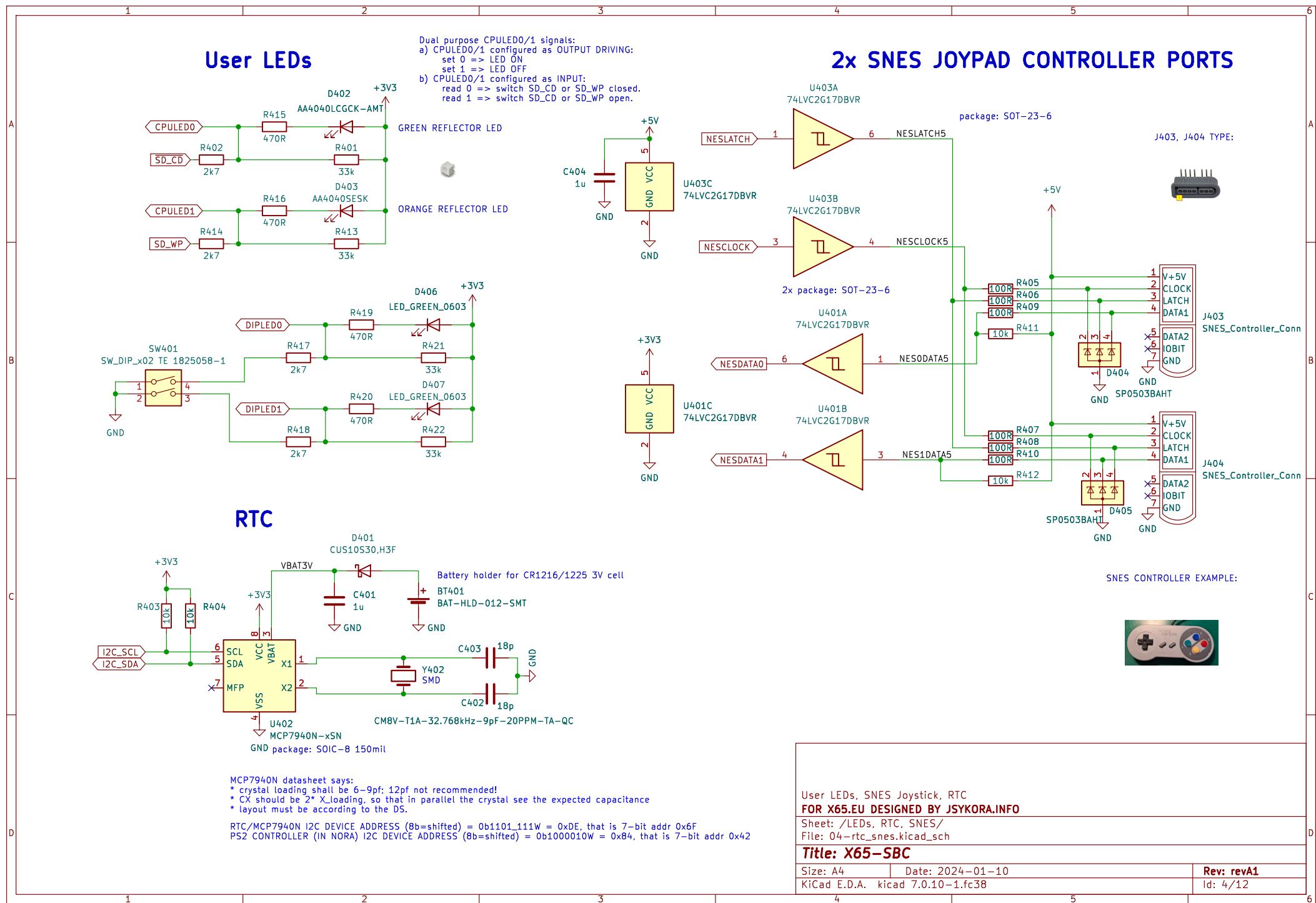
NORA FPGA with UNIFIED ROM SPI-Flash  
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /NORA FPGA/  
File: 03-nora\_fpga.kicad\_sch

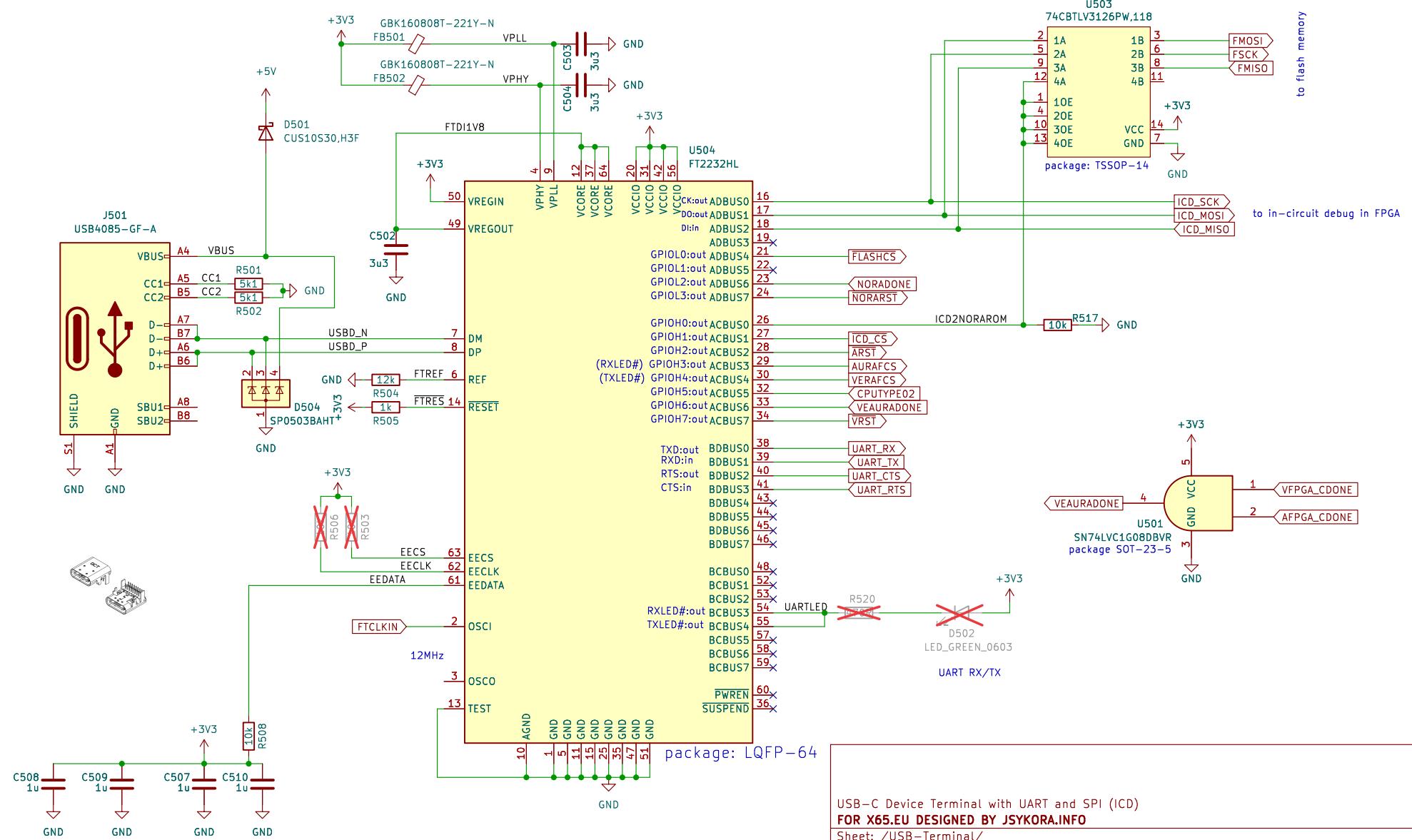
Title: X65-SBC

Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

Rev: revA1  
Id: 3/12



# USB 2.0 WITH USB-C / UART TERMINAL AND ICD (In-Circuit Debugger)



USB-C Device Terminal with UART and SPI (ICD)  
FOR X65.EU DESIGNED BY JSYKORA.INFO

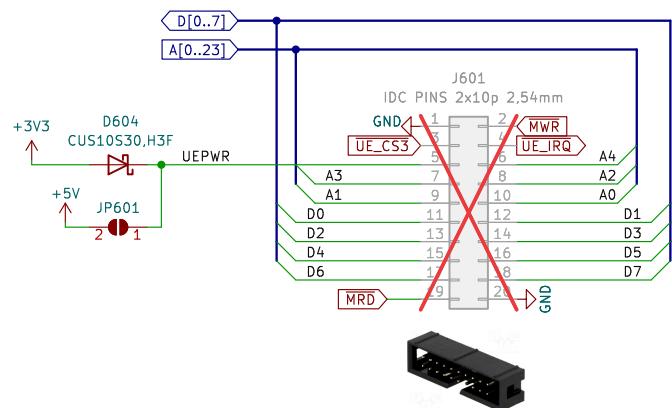
Sheet: /USB-Terminal/  
File: 05-usbdev.kicad\_sch

Title: X65-SBC

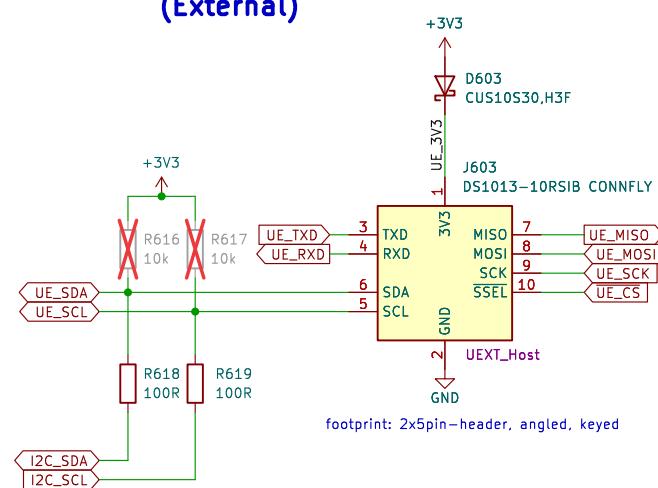
Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

Rev: revA1  
Id: 5/12

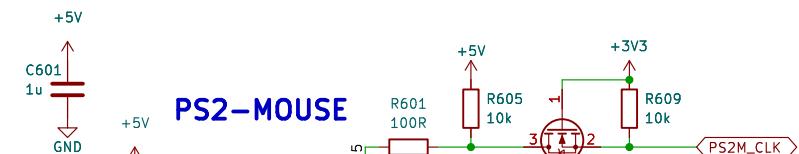
## Extension Connector (Internal)



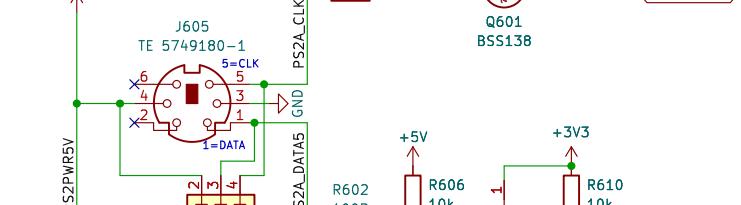
## UEXT HOST Connector (External)



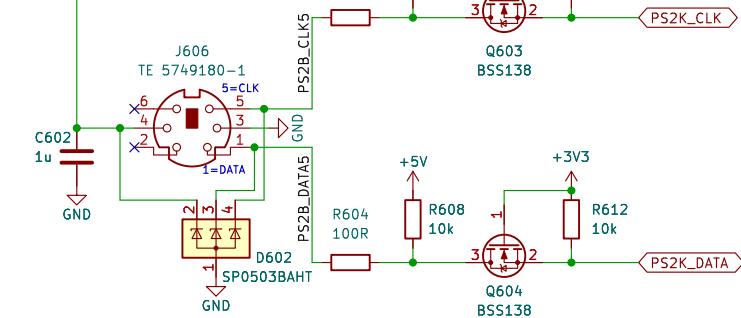
footprint: 2x5pin-header, angled, keyed



## PS2-MOUSE



## PS2-KBD



Extension Connectors, PS2 KBD and Mouse ports  
FOR X65.EU DESIGNED BY JSYKORA.INFO

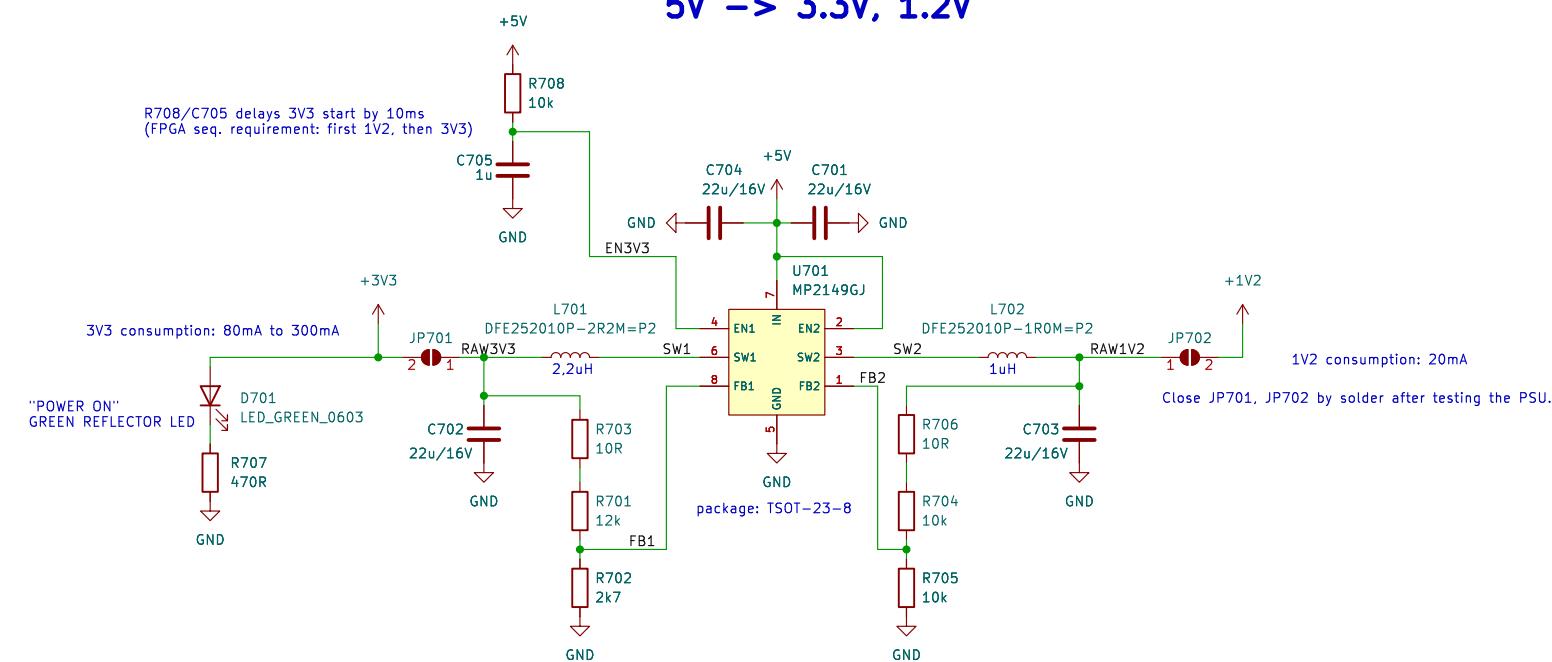
Sheet: /PS2\_Kbd+Mouse, UEXT/  
File: 06-ps2\_uext.kicad\_sch

Title: X65-SBC

Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

Rev: revA1  
Id: 6/12

# POWER SUPPLY 5V → 3.3V, 1.2V



Alternative power input connector



GND testpoints

GND J702 Conn\_01x01

GND J703 Conn\_01x01

GND J704 Conn\_01x01

Power supplies 3.3V and 1.2V  
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /Power Supply/  
File: 07-pwrsup.kicad\_sch

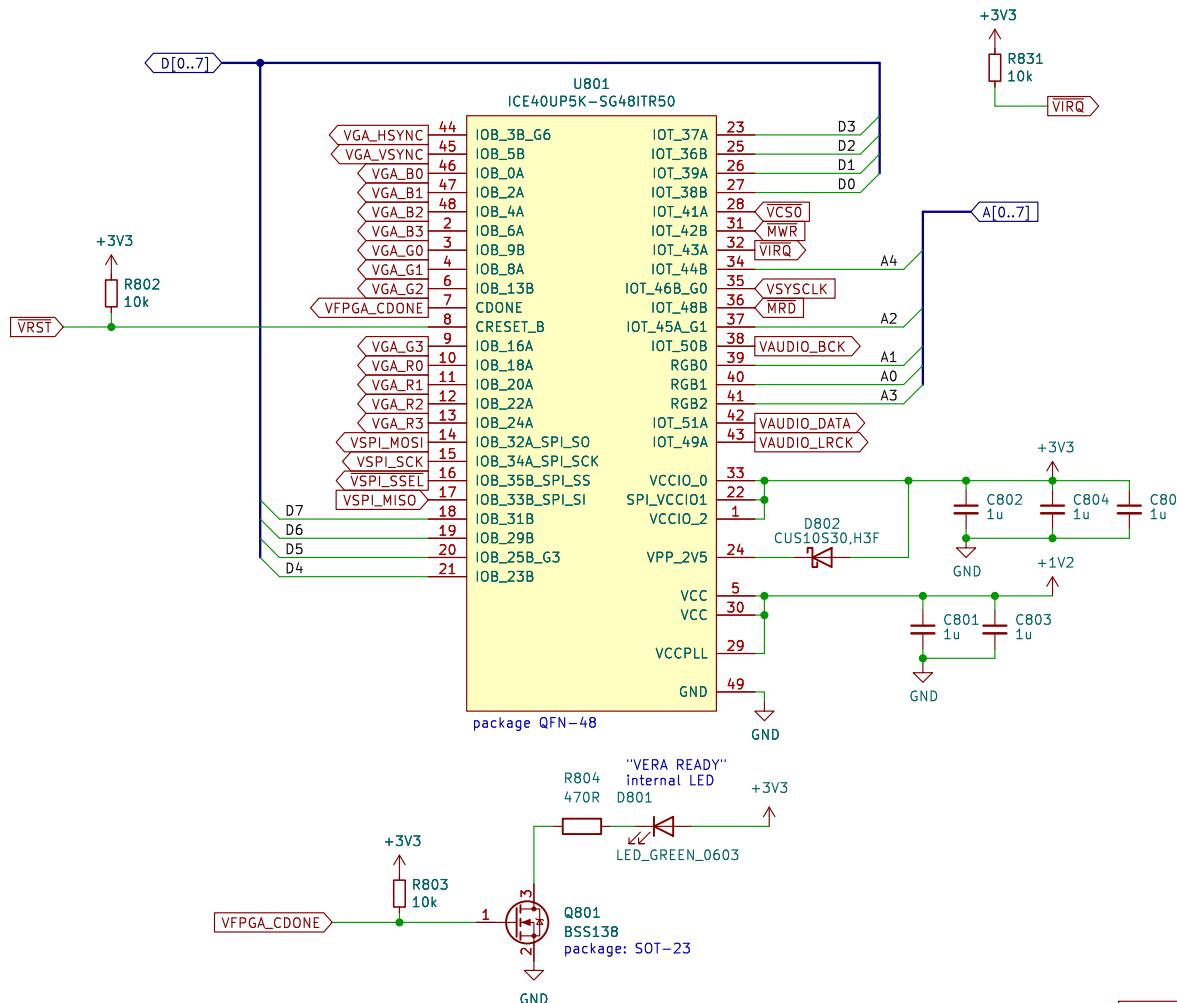
Title: X65-SBC

Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

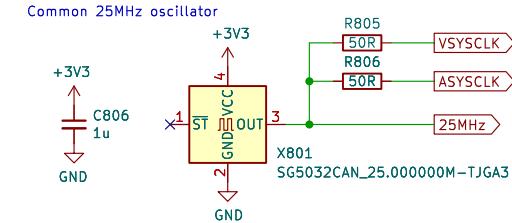
Rev: revA1  
Id: 7/12

# "VERA" FPGA – Video Embedded Retro Adapter

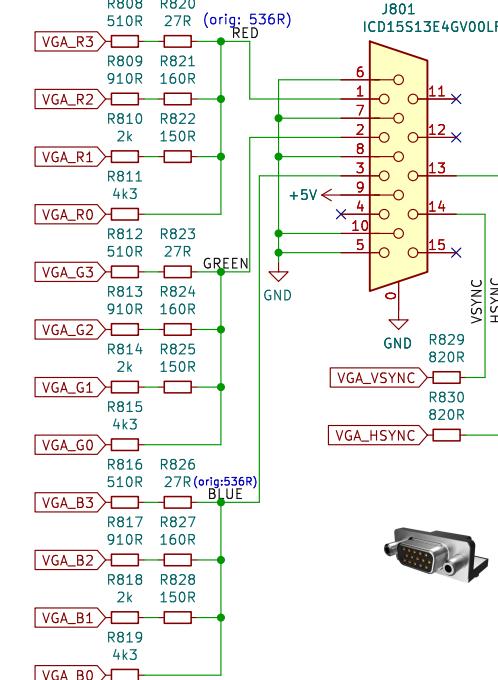
A



B



## VGA interface



C

This schematic contains portions of work done by Frank van den Hoe for the project VERA: <https://github.com/fvdhoef/vera-module>

VERA FPGA – VGA Adapter  
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /VERA FPGA/  
File: 08-vera\_fpga.kicad\_sch

**Title: X65-SBC**

Size: A4 | Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

Rev: revA1  
Id: 8/12

1

2

3

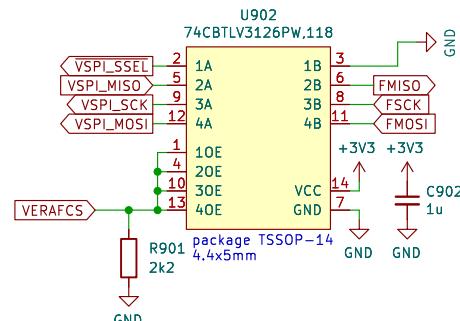
4

5

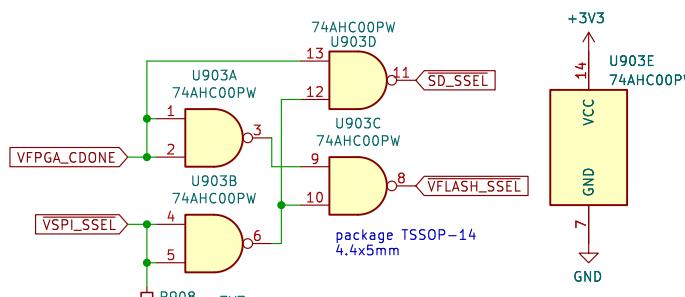
6

1 2 3 4 5 6

### FTDI/ICD access multiplexer to VERA SPI flash memory

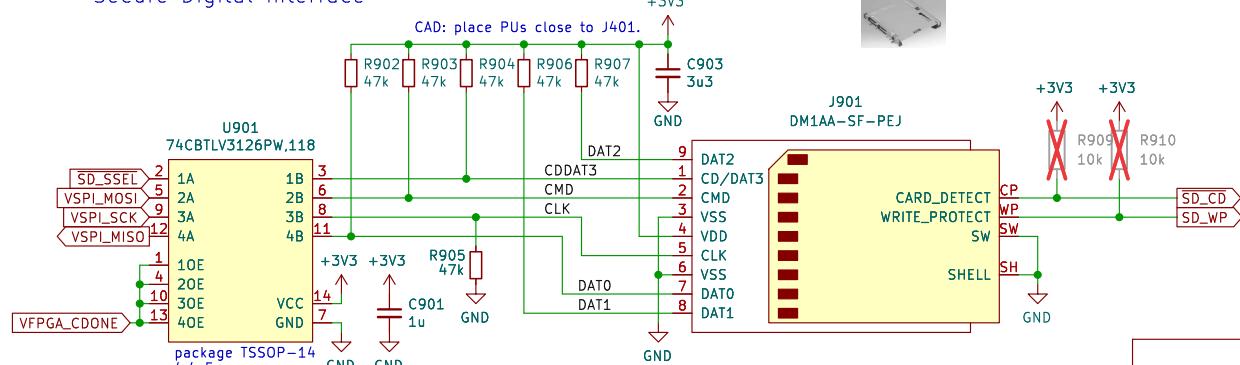


### VERA SPI pins multiplexing

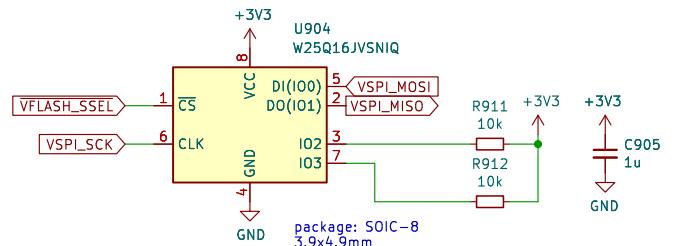


Inputs		Outputs	Description
VFPGA_CDONE	VSPI_SSEL	SD_SSEL	FPGA configuring from the SPI-Flash, or FTDI/ICD accessing.
0	0	1	0
0	1	1	FPGA empty/in-reset
1	0	0	FPGA loaded; User Design r/w to SDC
1	1	1	FPGA loaded; idle

### Secure Digital Interface



### SPI flash for VERA Bitstream



This schematic contains portions of work done by Frank van den Hoe for the project VERA: <https://github.com/fvdhoef/vera-module>

SD-Card slot, SPI-Flash for VERA  
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /SD-Card/  
File: 09-sdcard.kicad\_sch

**Title: X65-SBC**

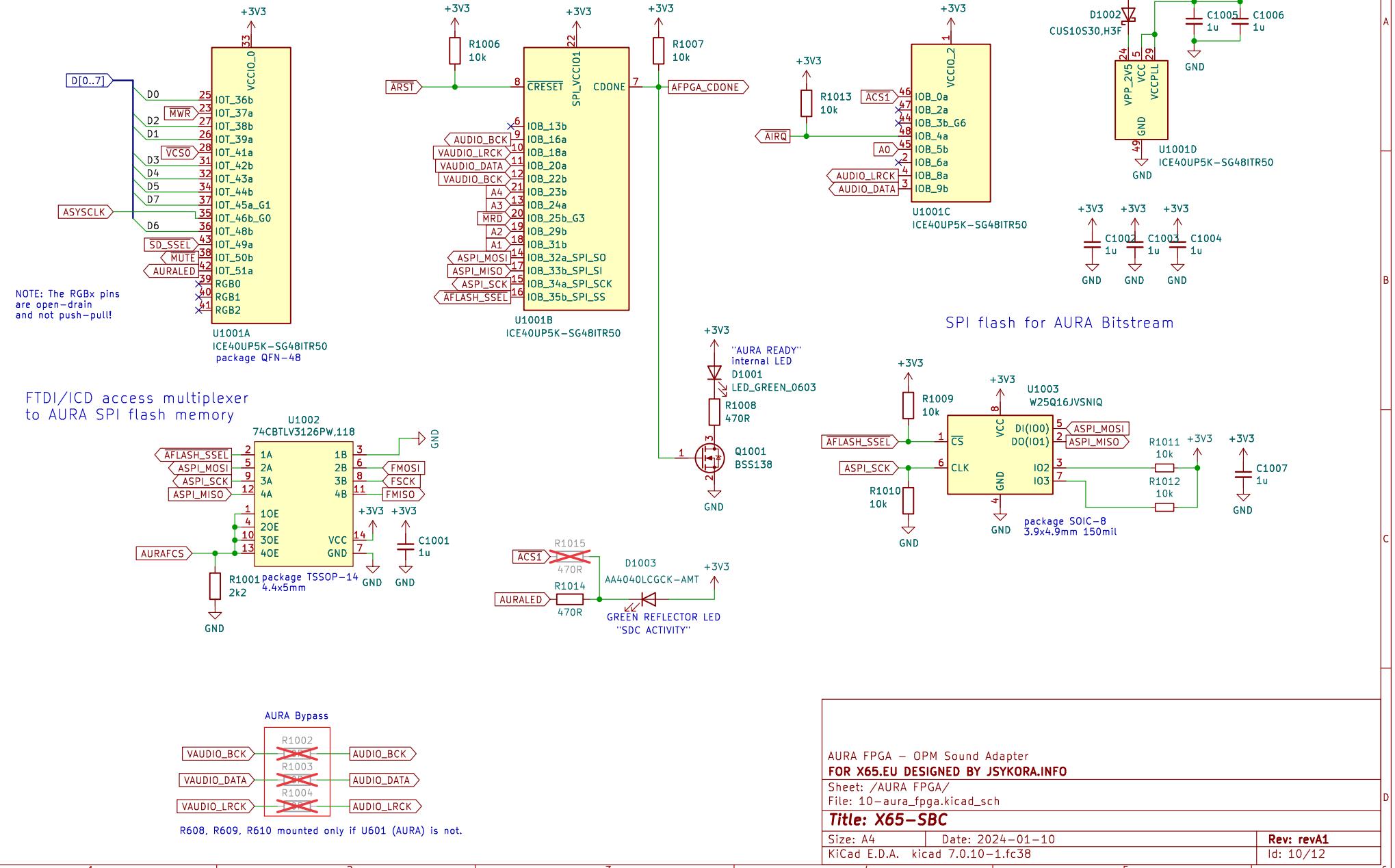
Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

Rev: revA1  
Id: 9/12

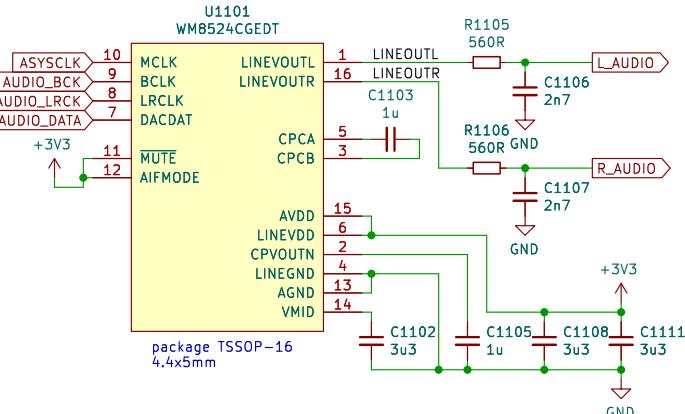
1 2 3 4 5 6

# "AURA" FPGA – Audio Retro Adapter

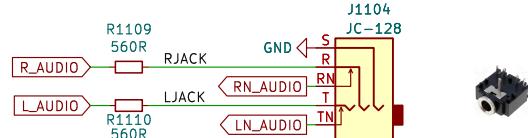
AURA implements the YM2151 FM-Synthesis (the chip is long out of production).  
Design is based on IKAOPM core.



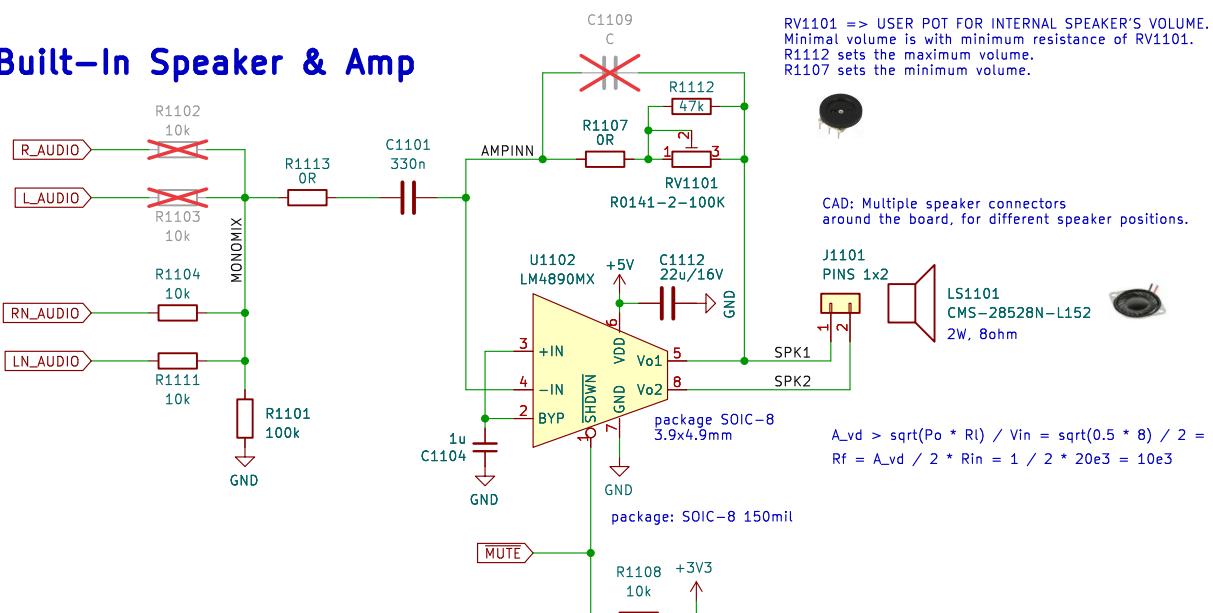
## Audio DAC (PCM/PSG in VERA, FM in AURA)



**3.5mm jack – AUDIO LINE output**



## Built-In Speaker & Amp



Sound DAC and output port  
**FOR X65.EU DESIGNED BY JSYKORA.INFO**

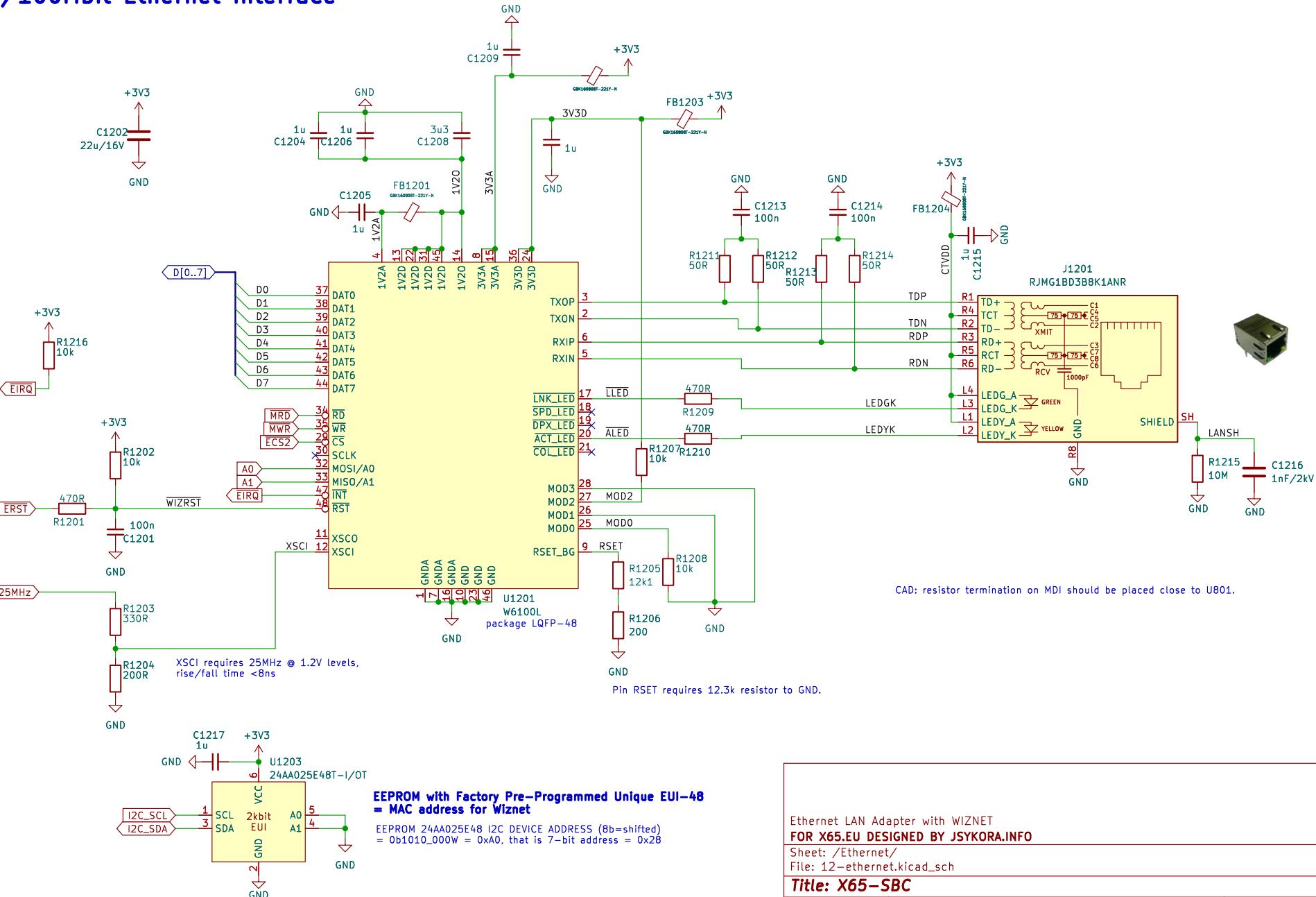
Sheet: /Sound Output/  
File: 11-sndout.kicad\_sch

## Title: X65-SBC

Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38

Rev: revA1  
Id: 11/12

# 10/100Mbit Ethernet Interface



EEPROM with Factory Pre-Programmed Unique EUI-48  
= MAC address for Wiznet

EEPROM 24AA025E48 I<sup>2</sup>C DEVICE ADDRESS (8b=shifted)  
= 0b1010\_000W = 0xA0, that is 7-bit address = 0x28

Ethernet LAN Adapter with WIZNET  
**FOR X65.EU DESIGNED BY JSYKORA.INFO**

Sheet: /Ethernet/  
File: 12-ethernet.kicad\_sch

**Title: X65-SBC**

Size: A4 Date: 2024-01-10  
KiCad E.D.A. kicad 7.0.10-1.fc38



Rev: revA1  
Id: 12/12