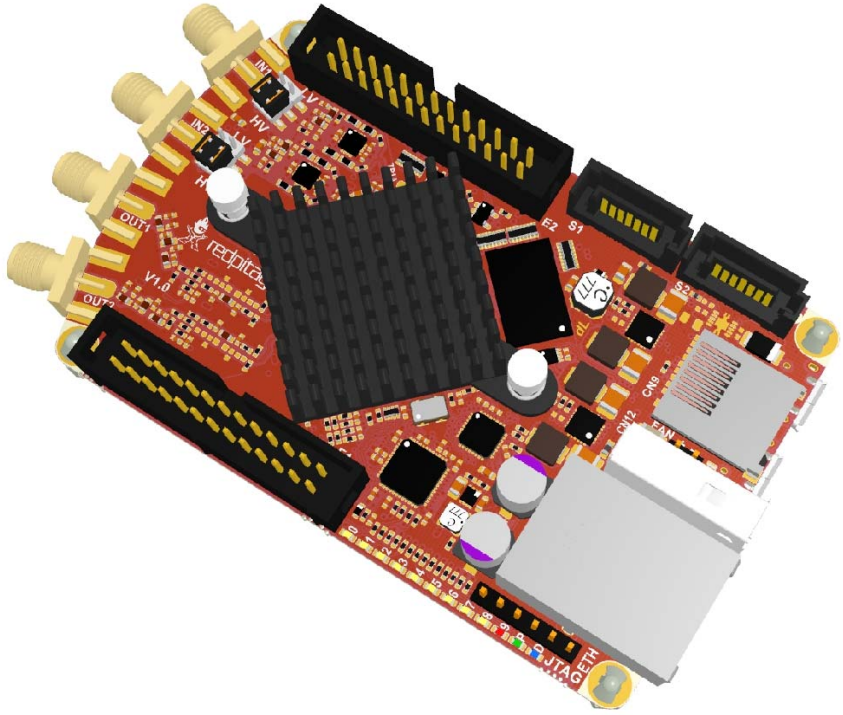


Red Pitaya d.o.o.
Velika pot 22
5250 Solkan
Slovenia

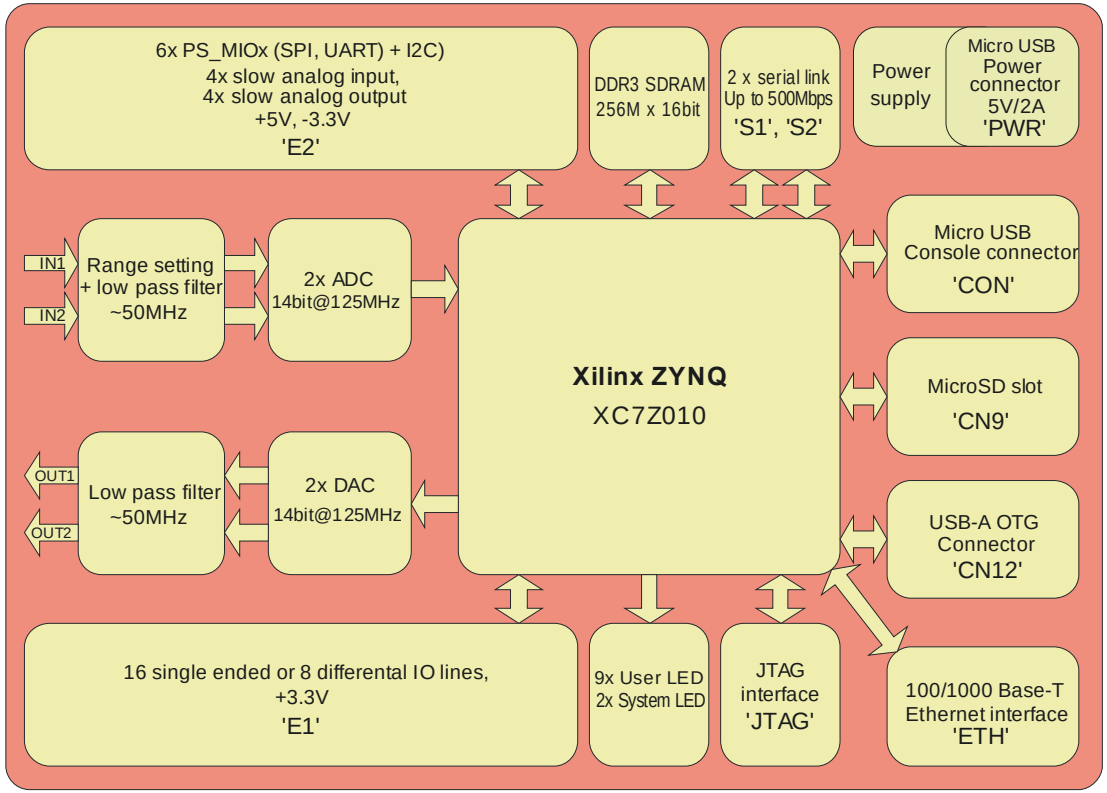
www.redpitaya.com

Electrical schematics for:

name: ***Red Pitaya***
version: ***V1.0.1***
variant: ***Release1***

Designer:	B.B., B.R., Z.L.	Document:	Red_Pitaya_Schematics_v1.0.1	Sheet 1 of 9	
Drawn By:	Z.L.	Modif. Date:	6.3.2014	SCHEMATIC	
Approved By:	R.U.	Print Date:	6.3.2014	Size: A4 H	

Red Pitaya



Designer:	B.B., B.R., Z.L.	Document:	Red_Pitaya_Schematics_v1.0.1	Sheet 2 of 9	
Drawn By:	Z.L.	Modif. Date:	6.3.2014	SCHEMATIC	
Approved By:	R.U.	Print Date:	6.3.2014	Size: A4 H	

Red Pitaya v1.0 block schematics

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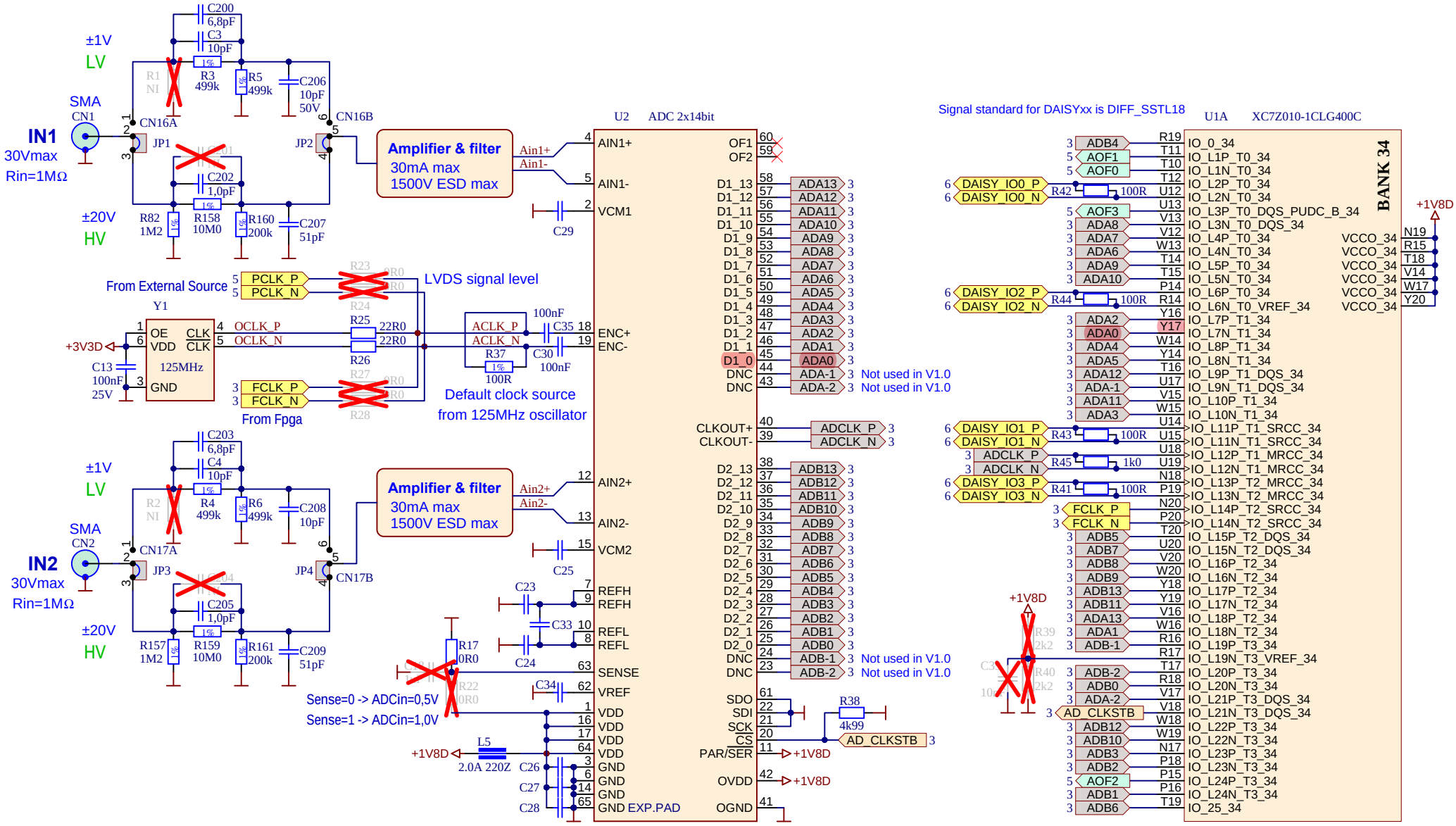
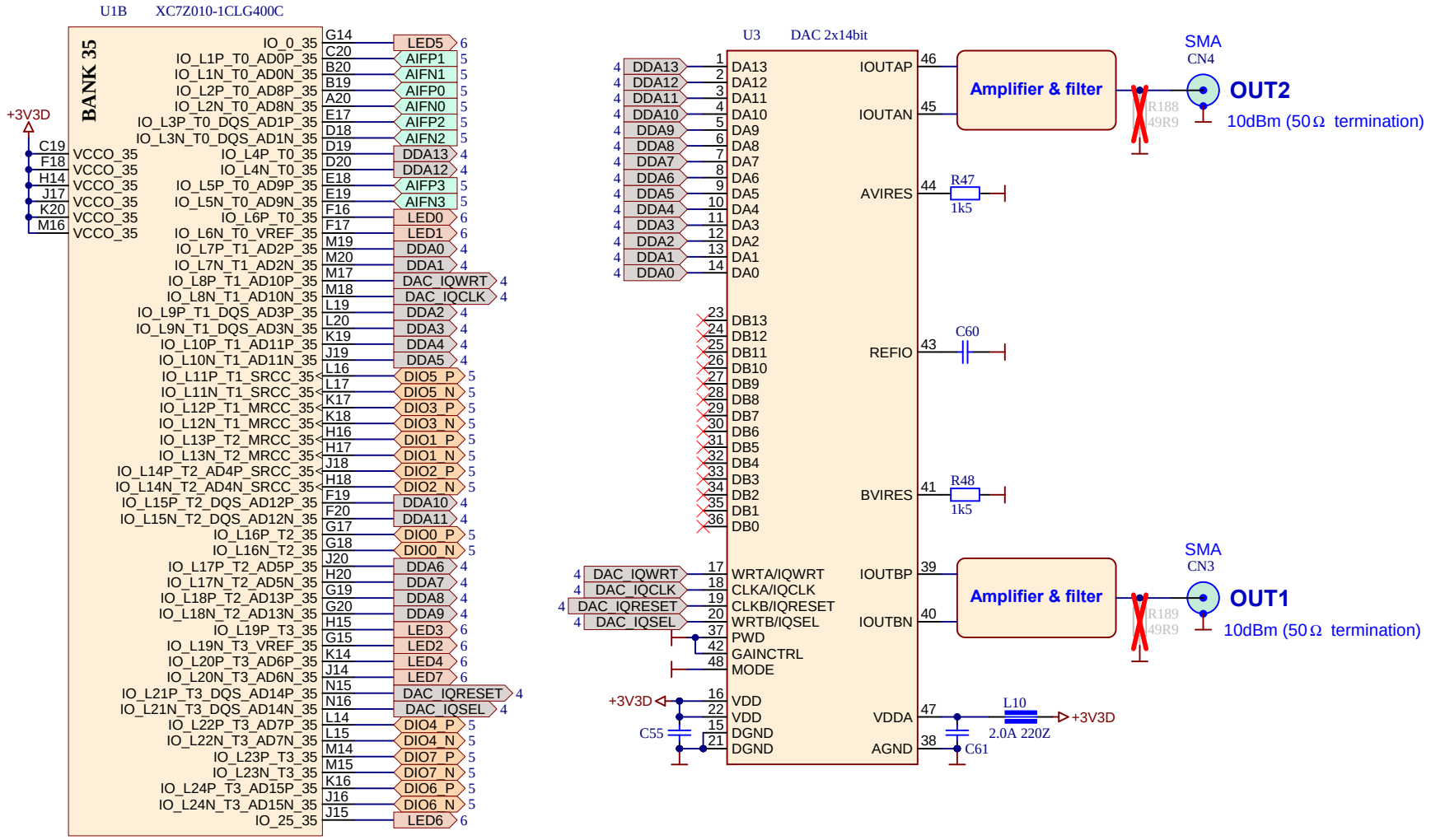

IN1
30Vmax
Rin=1MΩ
SMA
CN1
±1V
LV
±20V
HV
CN16A
CN16B
JP1
JP2
C200 6,8pF
C3 10pF
R3 499k
R5 499k
C206 10pF 50V
C202 1,0pF
R82 1M2
R158 10M0
R160 200k
C207 51pF
Amplifier & filter
30mA max
1500V ESD max
Ain1+
Ain1-
C29
From External Source
PCLK_P
PCLK_N
LVDS signal level
Y1
OE
VDD
CLK
GND
125MHz
+3V3D
C13 100nF 25V
OCLK_P
OCLK_N
R25 22R0
R26 22R0
ACLK_P
ACLK_N
C35 100nF
C30 100nF
R37 100R
FCLK_P
FCLK_N
From Fpga
Default clock source
from 125MHz oscillator
IN2
30Vmax
Rin=1MΩ
SMA
CN2
CN17A
CN17B
JP3
JP4
C203 6,8pF
C4 10pF
R4 499k
R6 499k
C208 10pF
C205 1,0pF
R157 1M2
R159 10M0
R161 200k
C209 51pF
Amplifier & filter
30mA max
1500V ESD max
Ain2+
Ain2-
C25
C23
C33
C24
R17 0R0
C34
Sense=0 -> ADCin=0,5V
Sense=1 -> ADCin=1,0V
L5
2.0A 220Z
C26
C27
C28
+1V8D
U2 ADC 2x14bit
AIN1+
AIN1-
VCM1
AIN2+
AIN2-
VCM2
REFH
REFL
SENSE
VREF
VDD
GND
GND EXP.PAD
OF1
OF2
D1_13 D1_12 D1_11 D1_10 D1_9 D1_8 D1_7 D1_6 D1_5 D1_4 D1_3 D1_2 D1_1 D1_0
DNC
CLKOUT+
CLKOUT-
D2_13 D2_12 D2_11 D2_10 D2_9 D2_8 D2_7 D2_6 D2_5 D2_4 D2_3 D2_2 D2_1 D2_0
SDO
SDI
SCK
CS
PAR/SER
OVDD
OGND
ADA13 ADA12 ADA11 ADA10 ADA9 ADA8 ADA7 ADA6 ADA5 ADA4 ADA3 ADA2 ADA1 ADA0 ADA-1 ADA-2
ADCLK_P
ADCLK_N
ADB13 ADB12 ADB11 ADB10 ADB9 ADB8 ADB7 ADB6 ADB5 ADB4 ADB3 ADB2 ADB1 ADB0 ADB-1 ADB-2
Not used in V1.0
R38 4k99
AD_CLKSTB
Signal standard for DAISYxx is DIFF_SSTL18
U1A XC7Z010-1CLG400C
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_PUDC_B_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
VCCO_34
DAISY_IO0_P
DAISY_IO0_N
DAISY_IO2_P
DAISY_IO2_N
DAISY_IO1_P
DAISY_IO1_N
DAISY_IO3_P
DAISY_IO3_N
R42 100R
R44 100R
R43 100R
R45 1k0
R41 100R
Note: number next to port symbol indicates the sheet where the signal is connected
Designer: B.B., B.R., Z.L.
Drawn By: Z.L.
Approved By: R.U.
Document: Red_Pitaya_Schematics_v1.0.1
Modif. Date: 6.3.2014
Print Date: 6.3.2014
Sheet 3 of 9
SCHEMATIC
Size: A4 H
Analog front-end and analog-digital converter, FPGA bank 34
redpitaya



Note: number next to port symbol indicates the sheet where the signal is connected

Designer:	B.B., B.R., Z.L.	Document:	Red_Pitaya_Schematics_v1.0.1	Sheet 4 of 9
Drawn By:	Z.L.	Modif. Date:	6.3.2014	SCHEMATIC
Approved By:	R.U.	Print Date:	6.3.2014	Size: A4 H

Analog back-end and digital-analog converter, FPGA bank 35

redpitaya

PS_MIO08 is output only and at power-up must be low level (no external pull-ups)!

16 single ended or
8 differential digital I/O
with 3,3V logic levels

E2

CN5

+5VD
50mA MAX! -3V3D
PS_MIO10
PS_MIO11
PS_MIO12
PS_MIO13
Output only! PS_MIO08
PS_MIO09
I2C0 SCL
I2C0 SDA
Ext com.mode (0~+0,5V)
GND
Analog Input 0
Analog Input 1
Analog Input 2
Analog Input 3
Analog Output 0
Analog Output 1
Analog Output 2
Analog Output 3
GND
GND
Ext Adc CLK+
Ext Adc CLK-
GND
GND

1 +5VD
2 -3VD
3 PS_MIO10 7 (SPI1_MOSI)
4 PS_MIO11 7 (SPI1_MISO)
5 PS_MIO12 7 (SPI1_SCK)
6 PS_MIO13 7 (SPI1_CS#)
7 PS_MIO08 7 (TxD1)
8 PS_MIO09 7 (RxD1)
9 I2C0_SCL 7
10 I2C0_SDA 7
11 AIcm
12
13 AI0 5
14 AI1 5
15 AI2 5
16 AI3 5
17 AO0 5
18 AO1 5
19 AO2 5
20 AO3 5
21
22
23 PCLK_P 3
24 PCLK_N 3
25
26

C238 470nF

(alternative ZYNQ function)
3,3V logic levels

0~+3,5Vin

0~+1,8Vout

LVDS signal level

IDC 2.54mm 26 pin low profile

0,5V XADC range

5 AI0 — R85 30k0 — R93 1k0 — AIFP0 4
R89 4k99 — R94 1k0 — C101 220pF — AIFN0 4

5 AI1 — R86 30k0 — R95 1k0 — AIFP1 4
R90 4k99 — R96 1k0 — C102 220pF — AIFN1 4

5 AI2 — R87 30k0 — R97 1k0 — AIFP2 4
R91 4k99 — R98 1k0 — C103 220pF — AIFN2 4

5 AI3 — R88 30k0 — R99 1k0 — AIFP3 4
R92 4k99 — R100 1k0 — C104 220pF — AIFN3 4

Vcm=0V

0R resistor
in place of
capacitor C237 0R0

U22A

common voltage setup

+0V5ref — R176 — XADCREF 6
C242 100nF — R177 1k5 — 1k0

Remove if
external common mode
voltage is used!

5 AO0 — RA8C 3 — 14 100R — AOF0 3
5 AO1 — RA8D 4 — 13 100R — AOF1 3
5 AO2 — RA8E 5 — 12 100R — AOF2 3
5 AO3 — RA8F 6 — 11 100R — AOF3 3

C96 8,2nF
C97 8,2nF
C99 8,2nF
C100 8,2nF

Power supply voltage monitor
0,5V XADC@6,11Vin

+5VD — R139 56k0 — R141 1k0 — AIFP4 6
R140 4k99 — R142 1k0 — C184 10nF — AIFN4 6

E1

CN6

1 +3V3D
2 +3V3D
3 4 DIO0_P PL_DIO0_P
4 4 DIO0_N PL_DIO0_N
5 4 DIO1_P PL_DIO1_P
6 4 DIO1_N PL_DIO1_N
7 4 DIO2_P PL_DIO2_P
8 4 DIO2_N PL_DIO2_N
9 4 DIO3_P PL_DIO3_P
10 4 DIO3_N PL_DIO3_N
11 4 DIO4_P PL_DIO4_P
12 4 DIO4_N PL_DIO4_N
13 4 DIO5_P PL_DIO5_P
14 4 DIO5_N PL_DIO5_N
15 4 DIO6_P PL_DIO6_P
16 4 DIO6_N PL_DIO6_N
17 4 DIO7_P PL_DIO7_P
18 4 DIO7_N PL_DIO7_N
19 NC
20 NC
21 NC
22 NC
23 NC
24 NC
25 GND
26 GND

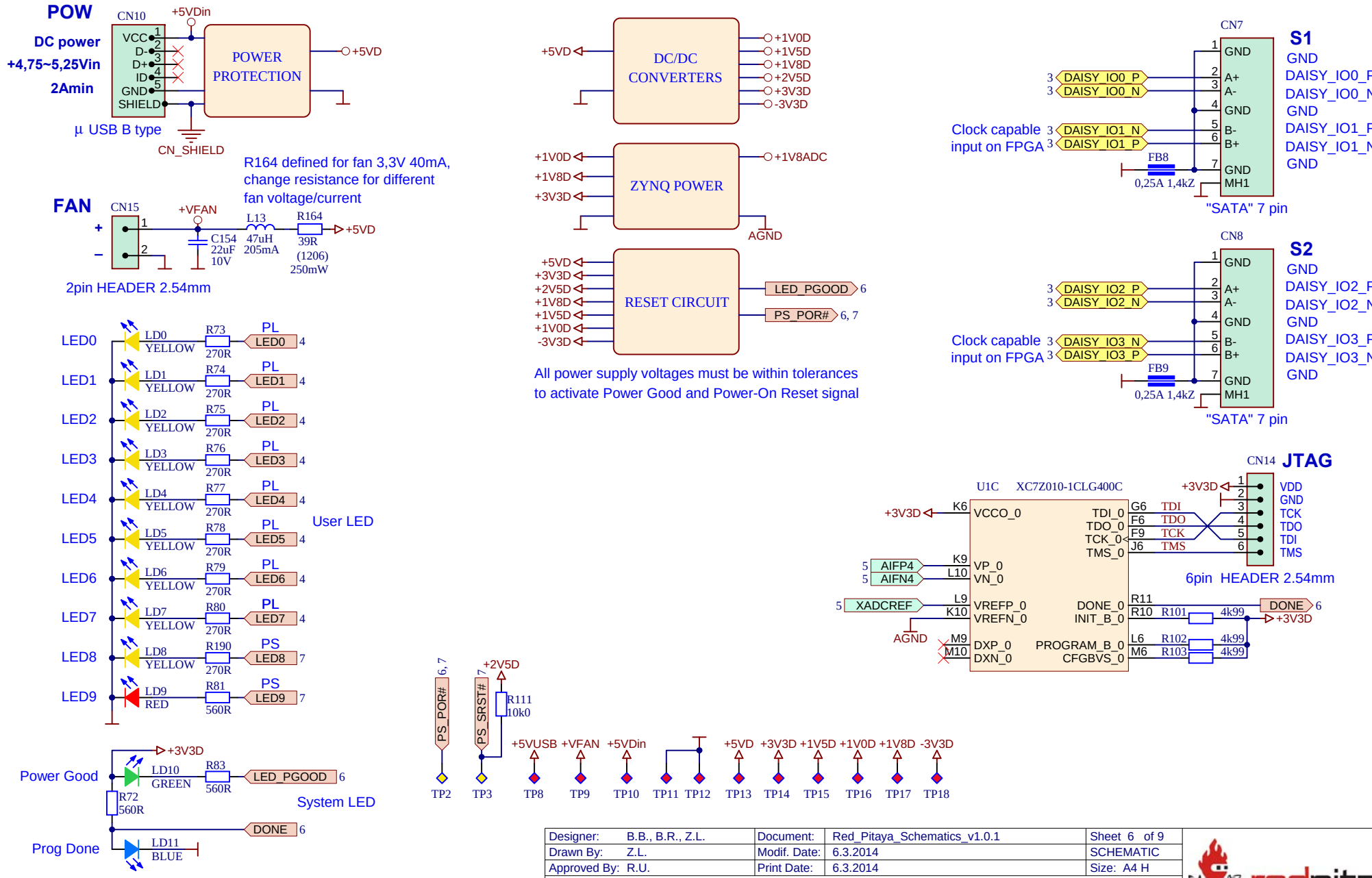
IDC 2.54mm 26 pin low profile

Note: number next to port symbol indicates the sheet where the signal is connected

Designer:	B.B., B.R., Z.L.	Document:	Red_Pitaya_Schematics_v1.0.1	Sheet 5 of 9	
Drawn By:	Z.L.	Modif. Date:	6.3.2014	SCHEMATIC	
Approved By:	R.U.	Print Date:	6.3.2014	Size: A4 H	

I/O digital, I/O slow analog, Extension connectors

redpitaya

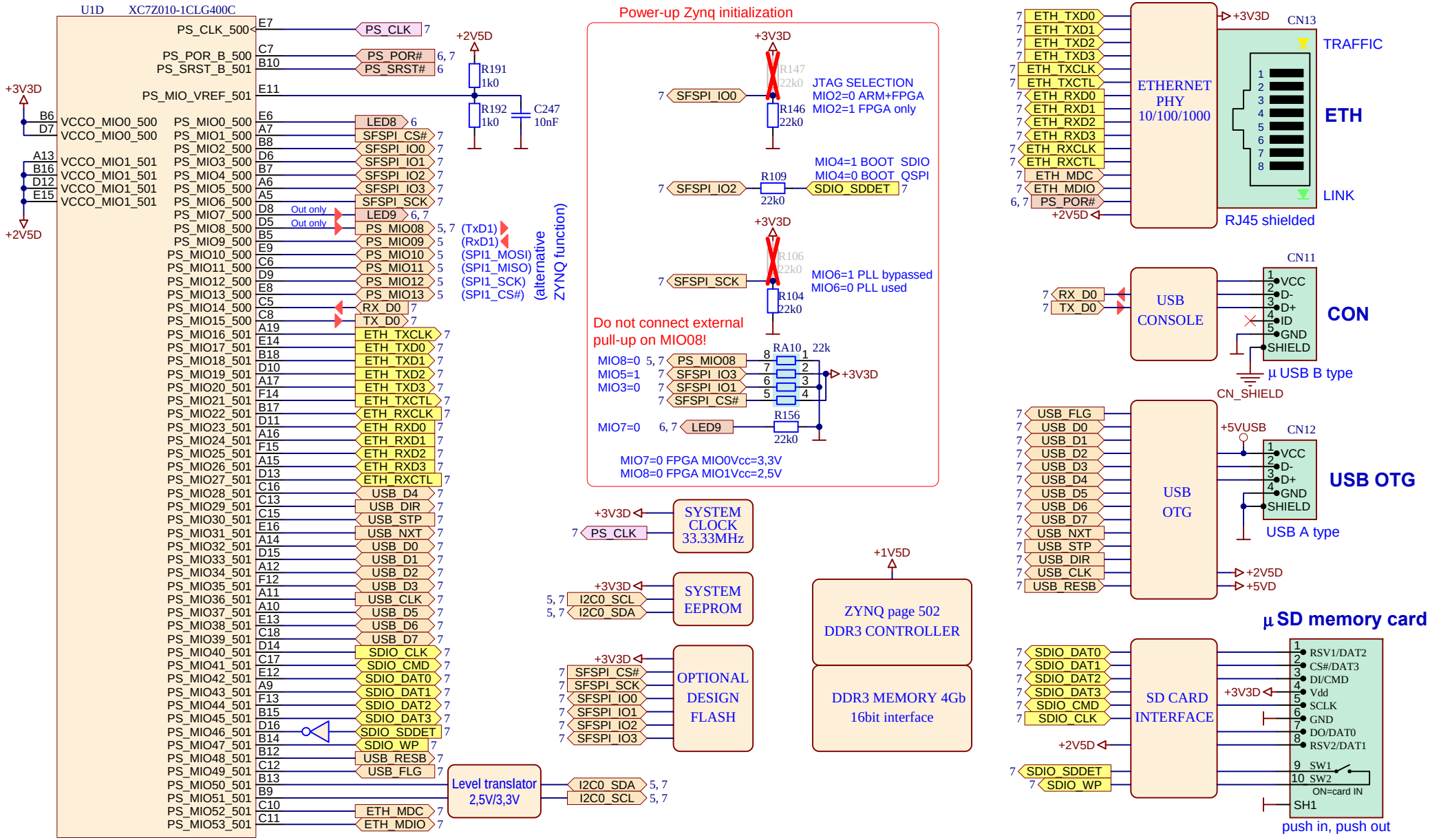


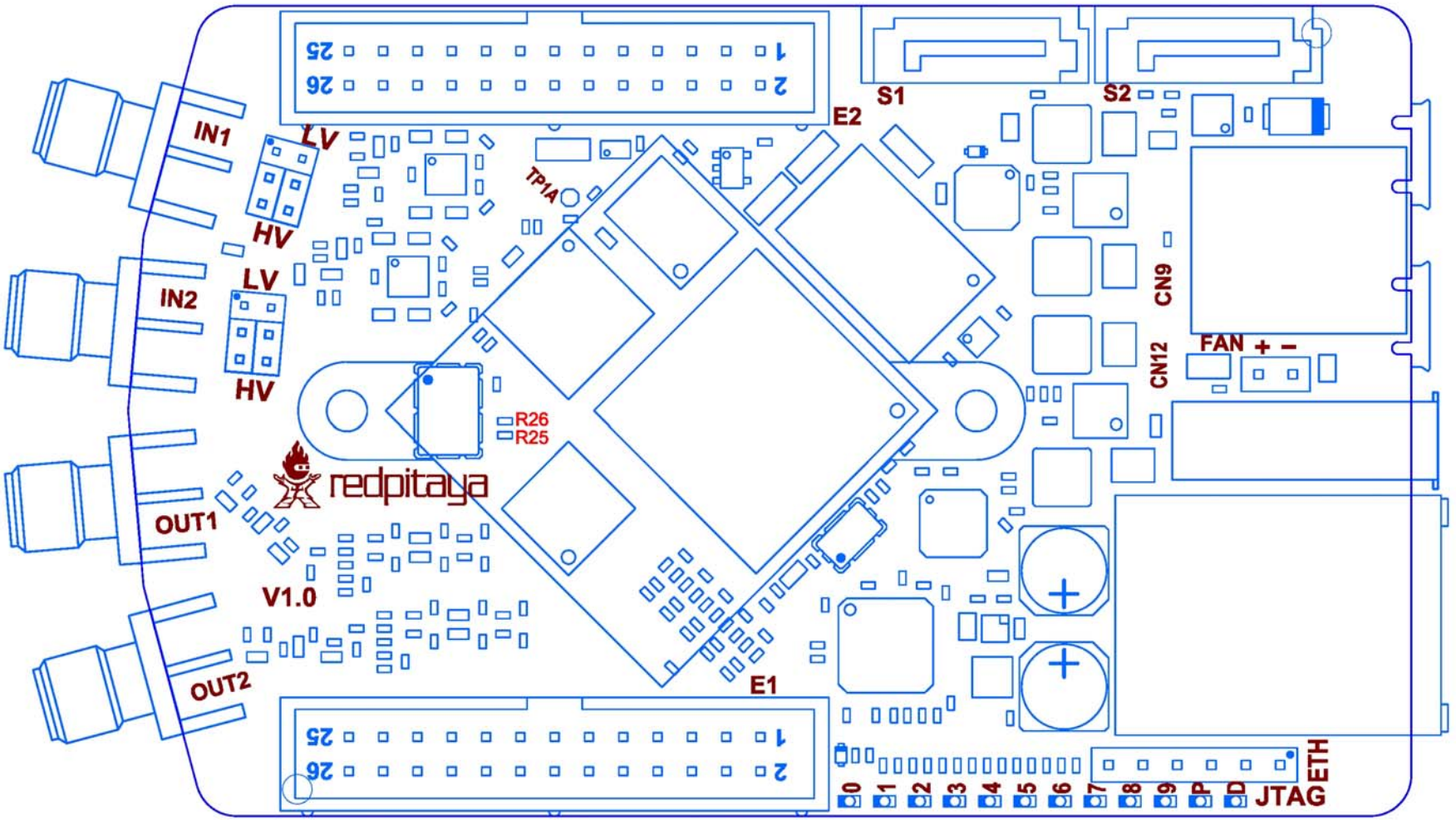
Note: number next to port symbol indicates the sheet where the signal is connected

Designer: B.B., B.R., Z.L.	Document:	Red_Pitaya_Schematics_v1.0.1	Sheet 6 of 9
Drawn By: Z.L.	Modif. Date:	6.3.2014	SCHEMATIC
Approved By: R.U.	Print Date:	6.3.2014	Size: A4 H

LED, Power, Fan, Serial I/O, JTAG, testpoints

redpitaya

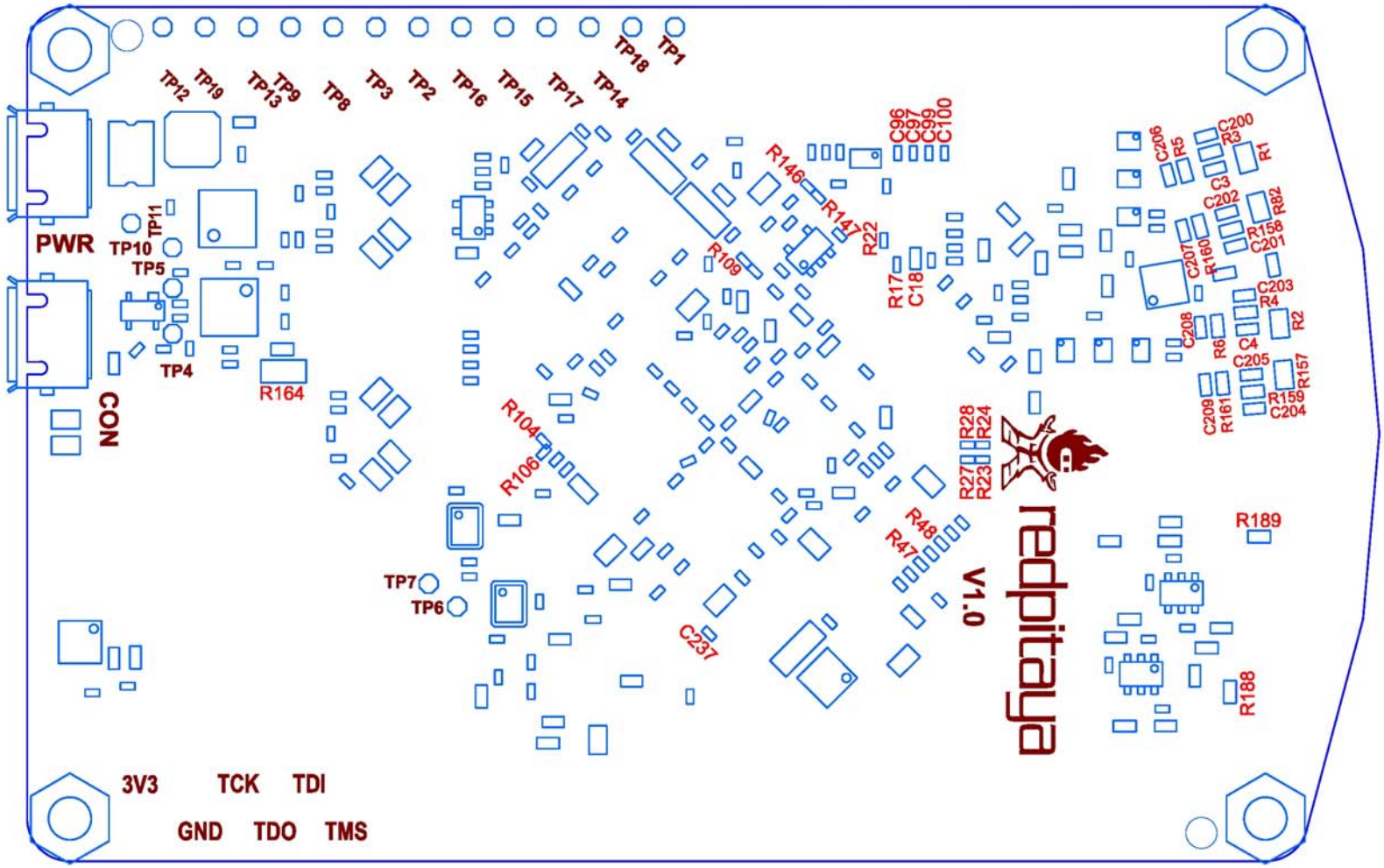

U1D XC7Z010-1CLG400C
PS_CLK_500 E7
PS_POR_B_500 C7
PS_SRST_B_501 B10
PS_MIO_VREF_501 E11
VCCO_MIO0_500 B6 D7
VCCO_MIO1_501 A13 B16 D12 E15
PS_MIO0_500 E6
PS_MIO1_500 A7
PS_MIO2_500 B8
PS_MIO3_500 D6
PS_MIO4_500 B7
PS_MIO5_500 A6
PS_MIO6_500 A5
PS_MIO7_500 D8
PS_MIO8_500 D5
PS_MIO9_500 B5
PS_MIO10_500 E9
PS_MIO11_500 C6
PS_MIO12_500 D9
PS_MIO13_500 E8
PS_MIO14_500 C5
PS_MIO15_500 C8
PS_MIO16_501 A19
PS_MIO17_501 E14
PS_MIO18_501 B18
PS_MIO19_501 D10
PS_MIO20_501 A17
PS_MIO21_501 F14
PS_MIO22_501 B17
PS_MIO23_501 D11
PS_MIO24_501 A16
PS_MIO25_501 F15
PS_MIO26_501 A15
PS_MIO27_501 D13
PS_MIO28_501 C16
PS_MIO29_501 C13
PS_MIO30_501 C15
PS_MIO31_501 E16
PS_MIO32_501 A14
PS_MIO33_501 D15
PS_MIO34_501 A12
PS_MIO35_501 F12
PS_MIO36_501 A11
PS_MIO37_501 A10
PS_MIO38_501 E13
PS_MIO39_501 C18
PS_MIO40_501 D14
PS_MIO41_501 C17
PS_MIO42_501 E12
PS_MIO43_501 A9
PS_MIO44_501 F13
PS_MIO45_501 B15
PS_MIO46_501 D16
PS_MIO47_501 B14
PS_MIO48_501 B12
PS_MIO49_501 C12
PS_MIO50_501 B13
PS_MIO51_501 B9
PS_MIO52_501 C10
PS_MIO53_501 C11
PS_CLK 7
PS_POR# 6, 7
PS_SRST# 6
+2V5D
R191 1k0
R192 1k0
C247 10nF
+3V3D
LED8 6
SFSPI_CS# 7
SFSPI_IO0 7
SFSPI_IO1 7
SFSPI_IO2 7
SFSPI_IO3 7
SFSPI_SCK 7
Out only
LED9 6, 7
PS_MIO08 5, 7 (TxD1)
PS_MIO09 5 (RxD1)
PS_MIO10 5 (SPI1_MOSI)
PS_MIO11 5 (SPI1_MISO)
PS_MIO12 5 (SPI1_SCK)
PS_MIO13 5 (SPI1_CS#)
(alternative ZYNQ function)
RX_D0 7
TX_D0 7
ETH_TXCLK 7
ETH_TXD0 7
ETH_TXD1 7
ETH_TXD2 7
ETH_TXD3 7
ETH_TXCTL 7
ETH_RXCLK 7
ETH_RXD0 7
ETH_RXD1 7
ETH_RXD2 7
ETH_RXD3 7
ETH_RXCTL 7
USB_D4 7
USB_DIR 7
USB_STP 7
USB_NXT 7
USB_D0 7
USB_D1 7
USB_D2 7
USB_D3 7
USB_CLK 7
USB_D5 7
USB_D6 7
USB_D7 7
SDIO_CLK 7
SDIO_CMD 7
SDIO_DAT0 7
SDIO_DAT1 7
SDIO_DAT2 7
SDIO_DAT3 7
SDIO_SDDET 7
SDIO_WP 7
USB_RESB 7
USB_FLG 7
ETH_MDC 7
ETH_MDIO 7
Level translator 2,5V/3,3V
I2C0_SDA 5, 7
I2C0_SCL 5, 7
Power-up Zynq initialization
+3V3D
SFSPI_IO0 7
R147 22k0
R146 22k0
JTAG SELECTION
MIO2=0 ARM+FPGA
MIO2=1 FPGA only
SFSPI_IO2 7
R109 22k0
MIO4=1 BOOT SDIO
MIO4=0 BOOT QSPI
SDIO_SDDET 7
SFSPI_SCK 7
R106 22k0
R104 22k0
MIO6=1 PLL bypassed
MIO6=0 PLL used
Do not connect external pull-up on MIO08!
RA10 22k
MIO8=0 5, 7 PS_MIO08
MIO5=1 7 SFSPI_IO3
MIO3=0 7 SFSPI_IO1
7 SFSPI_CS#
MIO7=0 6, 7 LED9
R156 22k0
MIO7=0 FPGA MIO0Vcc=3,3V
MIO8=0 FPGA MIO1Vcc=2,5V
SYSTEM CLOCK 33.33MHz
PS_CLK 7
SYSTEM EEPROM
5, 7 I2C0_SCL
5, 7 I2C0_SDA
OPTIONAL DESIGN FLASH
7 SFSPI_CS#
7 SFSPI_SCK
7 SFSPI_IO0
7 SFSPI_IO1
7 SFSPI_IO2
7 SFSPI_IO3
+1V5D
ZYNQ page 502 DDR3 CONTROLLER
DDR3 MEMORY 4Gb 16bit interface
ETH_TXD0 7
ETH_TXD1 7
ETH_TXD2 7
ETH_TXD3 7
ETH_TXCLK 7
ETH_TXCTL 7
ETH_RXD0 7
ETH_RXD1 7
ETH_RXD2 7
ETH_RXD3 7
ETH_RXCLK 7
ETH_RXCTL 7
ETH_MDC 7
ETH_MDIO 7
PS_POR# 6, 7
+2V5D
ETHERNET PHY 10/100/1000
+3V3D
CN13
TRAFFIC
ETH
LINK
RJ45 shielded
RX_D0 7
TX_D0 7
USB CONSOLE
CN11
VCC
D-
D+
ID
GND
SHIELD
CON
µ USB B type
CN_SHIELD
USB_FLG 7
USB_D0 7
USB_D1 7
USB_D2 7
USB_D3 7
USB_D4 7
USB_D5 7
USB_D6 7
USB_D7 7
USB_NXT 7
USB_STP 7
USB_DIR 7
USB_CLK 7
USB_RESB 7
USB OTG
+5VUSB
CN12
USB OTG
USB A type
+2V5D
+5VD
µ SD memory card
SDIO_DAT0 7
SDIO_DAT1 7
SDIO_DAT2 7
SDIO_DAT3 7
SDIO_CMD 7
SDIO_CLK 7
SD CARD INTERFACE
+3V3D
+2V5D
SDIO_SDDET 7
SDIO_WP 7
RSV1/DAT2
CS#/DAT3
DI/CMD
Vdd
SCLK
GND
DO/DAT0
RSV2/DAT1
SW1
SW2
ON=card IN
SH1
push in, push out
Note: number next to port symbol indicates the sheet where the signal is connected
Designer: B.B., B.R., Z.L.
Drawn By: Z.L.
Approved By: R.U.
Document: Red_Pitaya_Schematics_v1.0.1
Modif. Date: 6.3.2014
Print Date: 6.3.2014
Sheet 7 of 9
SCHEMATIC
Size: A4 H
Zynq PS bank500 and 501, Ethernet, Console, USB, memory
redpitaya



Designer:	B.B., B.R., Z.L.	Document:	Red_Pitaya_Schematics_v1.0.1	Sheet 8 of 9	
Drawn By:	Z.L.	Modif. Date:	6.3.2014	SCHEMATIC	
Approved By:	R.U.	Print Date:	6.3.2014	Size: A4 H	

Top Assembly

redpitaya



Designer:	B.B., B.R., Z.L.	Document:	Red_Pitaya_Schematics_v1.0.1	Sheet 9 of 9	
Drawn By:	Z.L.	Modif. Date:	6.3.2014	SCHEMATIC	
Approved By:	R.U.	Print Date:	6.3.2014	Size: A4 H	

Bottom Assembly

redpitaya