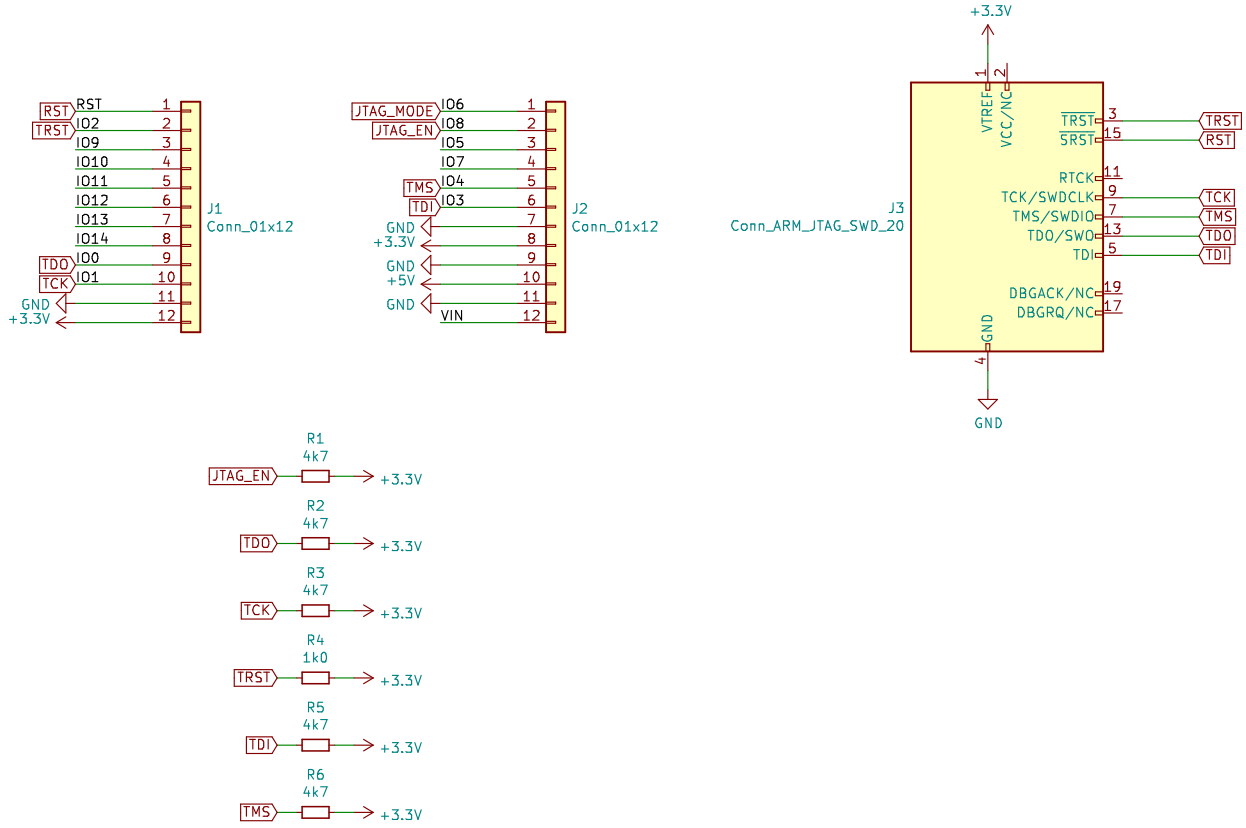

Pin	Default state	Low level	High level
IO2/REFCLK_FREQ_STATUS	Pull down	40MHz (Default)	24MHz
IO6/JTAG_MODE	Pull down	Normal function mode (Default)	DFT Test mode
IO8/JTAG_ENABLE	Pull down	Ordinary IO (Default)	JTAG enable

Leave R4 open for 40MHz clock frequency

koendv

Sheet: /

File: hi3861-jtag.sch

Title: Hi3861 JTAG SWD Connector

Size: A4	Date: 2022-02-16	Rev:
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