國立清華大學 電機工程學系
105 學年度第一學期
EE-6250 超大型積體電路測試 VLSI Testing
Homework #3 (佔學期總成績 10 分)
(每人一組) Due on Jan. 19, 2017

1. Consider a printed-circuit board with two ICs, A and B. There are a set of 4 interconnects going from IC A to IC B.
   (a) (50%) Write a synthesizable Verilog module to model the behavior of this printed-circuit board with the IEEE-1149.1 boundary scan test standard inserted in each IC. Note that, each IC is now represented by a Verilog sub-module.
   (b) (50%) Write a testbench (representing a host controller driving this printed-circuit board). Try to apply all 16 possible patterns through the interconnect set between IC A and B and see if you can get the correct response back to the host controller (via the boundary scan test channel). Show all 16 responses as a table.

Note: 繳交資料: (1) Combine your answers to the above questions (a)-(b) into a single PDF file. (2) Append to the above combined file your source Verilog code. (3) Attach a cover page with your 系所，中英文姓名，學號等資訊 before submitting your all-in-one file to our【清華大學-數位學習系統】(http://lms.nthu.edu.tw).