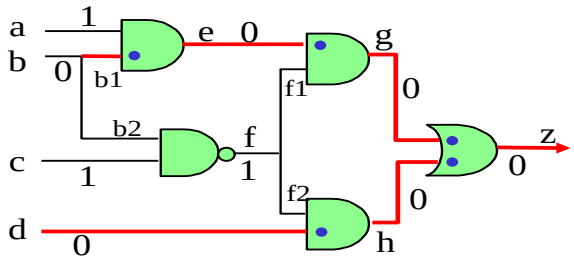
國立清華大學 電機工程學系(碩博士班)
105 學年度 第一學期
EE6250 超大型積體電路測試 — 期中考題 (Nov. 17, 2016)

1. (20%) Answer the following questions.
   (a) What are the variables *Y* and *T* in the following popularly used *defect-level estimation formula*: $DL = 1 - Y^{(1-T)}$ (5%)
   Y: yield, T: fault coverage
   (b) In a test procedure of an IC, one test item is to test for the tolerance of *±4KV under Human Body Mode*. What kind of test is this test item out of the following options: humidity test, mechanical test, ESD test, UV test, and salt mist test? (5%)
   ESD test. ESD means electrostatic discharge.
   (c) The *IDDQ test*, which tests for the IDDQ current of an IC, is sometimes considered as the "*canary in a coal-mine*". What does IDDQ mean anyway? Explain it in one sentence. (5%)
   Quiescent current at VDD pin. IDDQ could detect some un-modeled defects.
   (d) For a combinational circuit with *n* signal lines, there will be in total 2*n* single stuck-at faults. What is the total *number of multiple stuck-at faults*? (5%)
   3^k-1(means all conditions minus fault-free condition)
2. (20%) Answer the following questions.
   (a) There are *two basic requirements to test a stuck-at fault* in an IC by structural ATPG. The first is to *activate the fault*. What is the second? Explain briefly the second requirement in one or two sentences. (5%)
   Propagate the fault: we need to propagate the fault to the output, after activating the fault. Then we could observe the fault.
   (b) Is it true that a combinational *undetectable stuck-at fault* a redundant fault, meaning that we can simply replace the stuck-at line with its stuck-at value without changing the functionality and thereby simplifying the circuit? (5%)
   Yes, the fault is redundant and won't affect the result of output.
   (c) There are two *major improvement techniques of FAN algorithm* over PODEM for combinational test pattern generation. One is using the head-lines as the pseudo-PIs for value assignment. Name the second? (5%)
   Second one is using multiple backtrace procedure.
   (d) In the *9-valued D-algorithm* for ATPG, logic symbol '0/u' actually corresponds to two 5-valued symbols. One of them is '0'. What is the other? (5%)
   D'
3. (15%) Consider the technique of critical-path tracing for fault simulation.
   (a) What is the definition of *sensitive input*? (5%)
   The value of sensitive input changes value of the gate output.
   (b) Mark the *critical lines* of the circuit below based on the simulation results in response to an

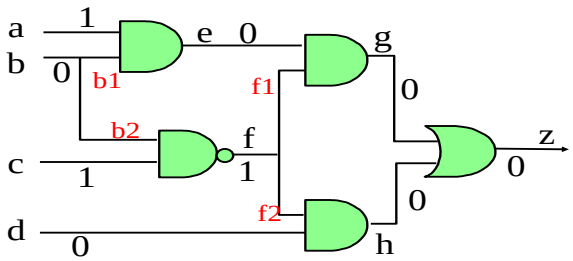
input vector (a,b,c,d)=(1,0,1,0). Note that the critical-path tracing traverses the circuit from the outputs towards the inputs and stops whenever a stem is encountered. (5%)



(c) Derive the set of detected faults and the set of undetected faults by the given input vector using only the information derived in (b). Follow the branch notations as shown in the figure. The faults on primary inputs should also be considered. (5%)

detected faults = v = {b1/1, e/1, g/1, d/1, h/1, z/1}

undetected faults = v'



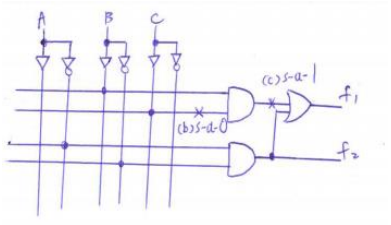
4. (15%) Consider a PLA design as shown in the figure below.

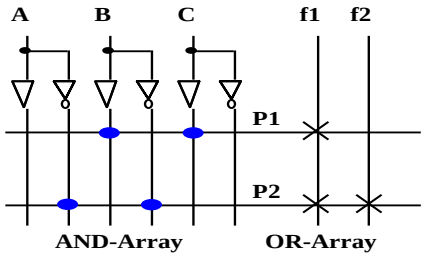
(a) Derive the fault-free two-level AND-OR logic model for this PLA.

f1 = BC + A'B', f2 = A'C'

(b) Considering that there is a *missing cross-point* fault between input variable *C* and product line P_1, derive its equivalent stuck-at fault model. (Note: you only need to mark the stuck-at fault location and the stuck-at value in the fault-free model) (5%)

(c) Considering that there is a *missing cross-point* fault between product line P_1 and output line f_1, derive its equivalent stuck-at fault model. (Note: Again, you only need to mark the stuck-at fault location and the stuck-at value in the fault-free model) (5%)





5. (15%) Consider the backtrace across a NOR gate in PODEM algorithm. If the inputs of this NOR gates are {*x*1, *x*2, *x*3} with the following controllability probabilities: {CY0(*x*1) = 0.1,

CY1($x1$) = 0.9}, {CY0($x2$) = 0.5, CY1($x2$) = 0.5}, and {CY0($x3$) = 0.8, CY1($x3$) = 0.2}.

(a) What is the controlling value at the input of an NOR gate? (5%)

The controlling value of NOR is 1.

(b) If the objective is to set the NOR gate's output to logic '0', then which one of its inputs should be selected for the backtrace? (5%)

It is several solutions, so we need to choose the easiest one. X1 should be selected, because of highest controllability of 1.

(c) If the objective is to set the NOR gate's output to logic '1', then which one of its inputs should be selected for the backtrace? (5%)

It is several unsolved problems, so we need to choose the hardest one firstly. X1 should be resolve, because of the lowest controllability of 0.

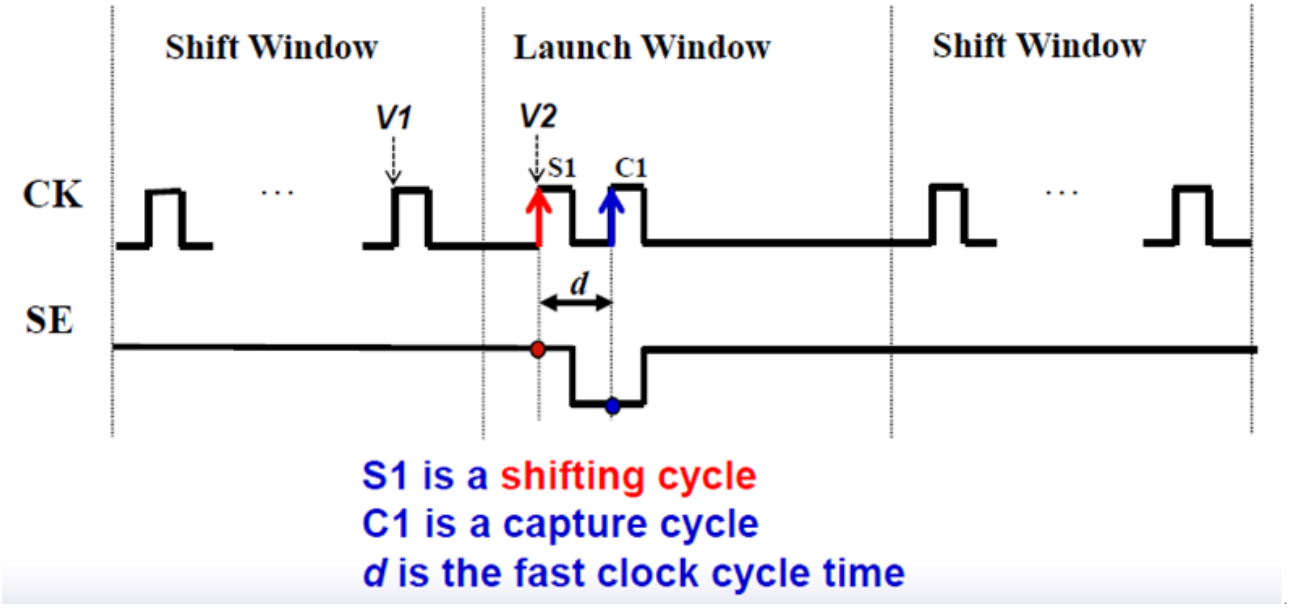
6. (15%) Consider the transition fault testing in a scan test environment. It requires a 2-pattern test, namely (v1, v2). The entire test application takes three stages: (1) scan-in v1, (2) lauch-v2-and-capture, (3) scan-out response vector.

(a) There are two types of test application, LoS and LoC. Show the complete names of these two acronyms. (5%)

launch of shifting

launch of capture

(b) Show the waveforms of scan clock (TCK) and scan control signal (SE) during the 2nd stage, i.e., the stage that launches v2 and capture response, if LoS test method is used. (5%)



(c) If LoS is used, and v1: (y1, y2, y3) = (1, 0, 0), where y1, y2, and y3 are three PPI's. Let SI is stable at '0', **derive v2**, assuming the scan chain order from input to output is SI→y3→y2→y1. (5%)

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