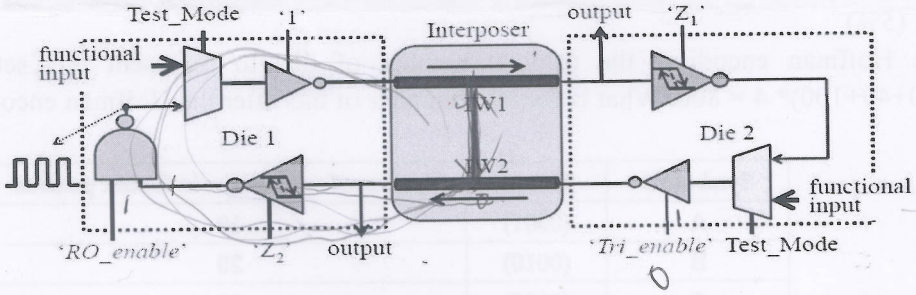
5. (10%) Suppose we have 7 random signals produced by a **Linear Feedback Shift Register** (LFSR), denoted as $\{x_1, x_2, x_3, x_4, x_5, x_6, x_7\}$. Show a logic circuit that can use these 7 signals to produce a *weighted random signal* with a signal-1 probability of 9/32 using only two AND gates and one OR gate.

6. (10%) Answer the following questions about **pulse-vanishing test** for an interconnect.
   (a) A *double-pulsed signal* is transmitted from a test controller to each launch cell at the driver of an interconnect (which is then locally converted to a *test pulse* to be launched into the interconnect by a toggle flip-flop). Why can't we just transmit the test pulse from the test controller to the launch cells directly? (5%)
   (b) Draw a *basic capture cell* placed at the output of the receiver of an interconnect under test. (Hint: it consists of only one FF, assumed to be initialized to '0' before a test session). (5%)

7. (10%) Consider the following problems related to **VOT-based oscillation test**.
   (a) Draw the transistor schematic of the Schmitt-Trigger inverter discussed in class. (5%)
   (b) A Schmitt-Trigger inverter has a hysteresis effect. What nice property of this effect can be useful in the approximation of the transition time of the inverter's input signal? (5%)

8. (10%) Consider the following **VOT-based oscillation test** for two high-speed interconnects, IW1 and IW2.
   (a) Set (*RO_enable*, *Tri_enable*) to (1, 1) and measure three oscillation periods, namely T_{REF} (Z_1=0, Z_2=0), T_{ST1} (Z_1=1, Z_2=0), and T_{ST2} (Z_1=0, Z_2=1). From these three oscillation periods, a metric almost linearly proportional to the delay across interconnect IW1 can be derived. Show the formula of this metric. (5%)
   (b) What values should be applied to signals *RO_enable* and *Tri_enable* when a test session for detecting the *intra-RO bridging fault* is performed? (5%)



9. (10%) Consider the **scan chain diagnosis** using signal profiling technique for a scan chain consisting of 6-flip-flops, (F_1, F_2, F_3, F_4, F_5, F_6), where the Scan-Input pin drives F_1, and F_6 is the Scan-Out pin.
   (a) One simulated fault-free image is (F_1,F_2,F_3,F_4,F_5,F_6) = (0,1,1,1,1,1), and its corresponding observed image of the failing chip is (F_1,F_2,F_3,F_4,F_5,F_6) = (1,0,0,1,1,1). Compute the difference image. (5%)
   (b) Consider 5 fault-free images and their corresponding observed images as shown in the table below. Which flip-flop will be considered as the fault location, assuming there is only one fault? (Note: the fault is not necessary a stuck-at fault, and could be intermittent). (5%)

Image index	Fault-free image (F1, F2, F3, F4, F5, F6)	Observed image of a failing chip (F1, F2, F3, F4, F5, F6)
1	(100111)	(011111)
2	(000100)	(111100)
3	(010101)	(101101)
4	(110000)	(110000)
5	(100110)	(011110)