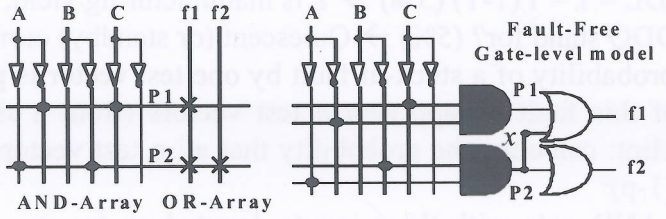
expression for output signal f1, (Note: denote the name of this faulty signal as f1-faulty? (5%) → f1-faulty = C + AB'

(c) On the left-hand side of the figure, if there is a missing cross-point fault at the cross-point of (horizontal) product line P2 and (vertical) output line f1, then what stuck-at fault is this fault equivalent to on the circuit model on the right-hand-side? (Note: you have to specify the signal name and the stuck-at value). (5%) → x stuck-at-0



5. (15%) Answer the following questions about *test time*.
   (a) Why is test time an essential issue in VLSI testing? (5%) → Test time is a major factor of testing cost
   (b) Consider the full-scan methodology for a circuit with 99 flip-flops. A combinational ATPG program produces 123 vectors to fully test the logic. Compute the minimum number of clock cycles needed to apply these vectors, assuming that the system clock and test clock are the same and there is only one scan chain. (Note: the scan-in operation and scan-out operation are assumed to be overlapped whenever applicable. In this calculation, we also ignore the cycles for applying the PI sub-vectors and the cycles for observing the PO sub-vectors.) (10%) → 123*(99+1) + 99 = 12399

6. (15%) Consider the transition fault testing in a scan test environment. It requires a 2-pattern test, namely (v1, v2). The entire test application takes three stages: (1) scan-in v1, (2) lauch-v2-and-capture, (3) scan-out response vector.
   (a) There are two types of test application, LoS and LoC. Show the complete names of these two acronyms. (5%)
   (b) Show the waveforms of scan clock (TCK) and scan control signal (SE) during the 2nd stage, i.e., the stage that launches v2 and capture response, if LoS test method is used. (5%) → See lecture notes in Chapter 6
   (c) If LoS is used, and v1: (y1, y2, y3) = (1, 0, 0), where y1, y2, and y3 are three PPI's. Let SI is stable at '0', **derive v2**, assuming the scan chain order from input to output is SI→y3→y2→y1. (5%) → v2: (y1, y2, y3) = (0, 0, 0)