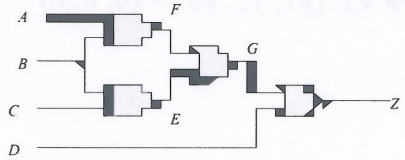
國立清華大學 電機工程學系(碩博士班)
103 學年度 第一學期
EE6250 超大型積體電路測試 — 期中考題 (Nov. 26, 2014)

1. (20%) Answer the following questions.
   (a) What are the variables Y and T in the following popularly used estimation formula for defect level: DL = 1 – Y(1-T) (5%) → Y is manufacturing yield, and T is fault coverage
   (b) What does IDDQ stand for? (5%) → Quiescent (or standby) current through a VDD pin.
   (c) A detection probability of a stuck-at fault by one test vector is p, then what is the detection probability of this fault by applying *n* test vectors (from a statistical point of view like STAFAN). (Hint: calculate the probability that all n test vectors fail to detect a fault first). (5%) → $1-(1-p)^n$
   (d) Consider an AND gate with three inputs denoted as $\{x_1, x_2, x_3\}$ and output f. Compute Boolean difference df/dx_1 as a Boolean expression in terms of $\{x_2, x_3\}$. (5%) → $x_2 \& x_3$

2. (25%) Answer the following questions.
   (a) For a two-input NOR gate, C = (A+B)', is it true that C-stuck-at-1 fault dominates A stuck-at-0 fault? (5%) → Yes, C-sa-1 dominates A-sa-0
   (b) In D-algorithm, if we have seen a fault effect at an output, what extra condition is needed in order to indicate a successful test vector generation? (5%) → J-frontier is empty
   (c) In a 9-valued D-algorithm for ATPG, logic symbol '1/u' corresponds to a set of two logic symbols used in a 5-valued D-algorithm. One of them is '1'. What is the other? (5%) → (1/0) or D
   (d) Consider a two-input NAND-gate, Z = (AB)'. If CC0(A), CC1(A), CC0(B), CC1(B) are 3, 6, 10, and 1, respectively, by SCOAP (Sandia Controllability and Observability Analysis Program). If observability of Z, denoted as CO(Z), is 5, then, what is CO(A). (5%) → (5+1)+1 = 7
   (e) There are two *major improvement techniques of FAN algorithm* over PODEM for combinational test pattern generation. One is using the head-lines as the pseudo-PIs for value assignment. Name the second? (5%) → Multiple backtrace

3. (10%) Derive a test vector for *G stuck-at-1 fault* in the circuit shown below. → (A, B, C, D) = (1, 1, 1, 0)



4. (15%) Consider the fault modeling of a PLA with the symbolic schematic shown below. Note that product line P2 has two branches, the one driving output line f1 is particularly called x (as shown in the figure below).
   (a) Derive the fault-free Boolean function for output signal f1 of this PLA in the Sum-of-Product (SoP) form (5%). → f1 = A'C + AB'
   (b) On the left-hand side of the figure, if there is a missing cross-point fault at the cross-point of (vertical) input line A' and (horizontal) product line P1, then what is the faulty Boolean