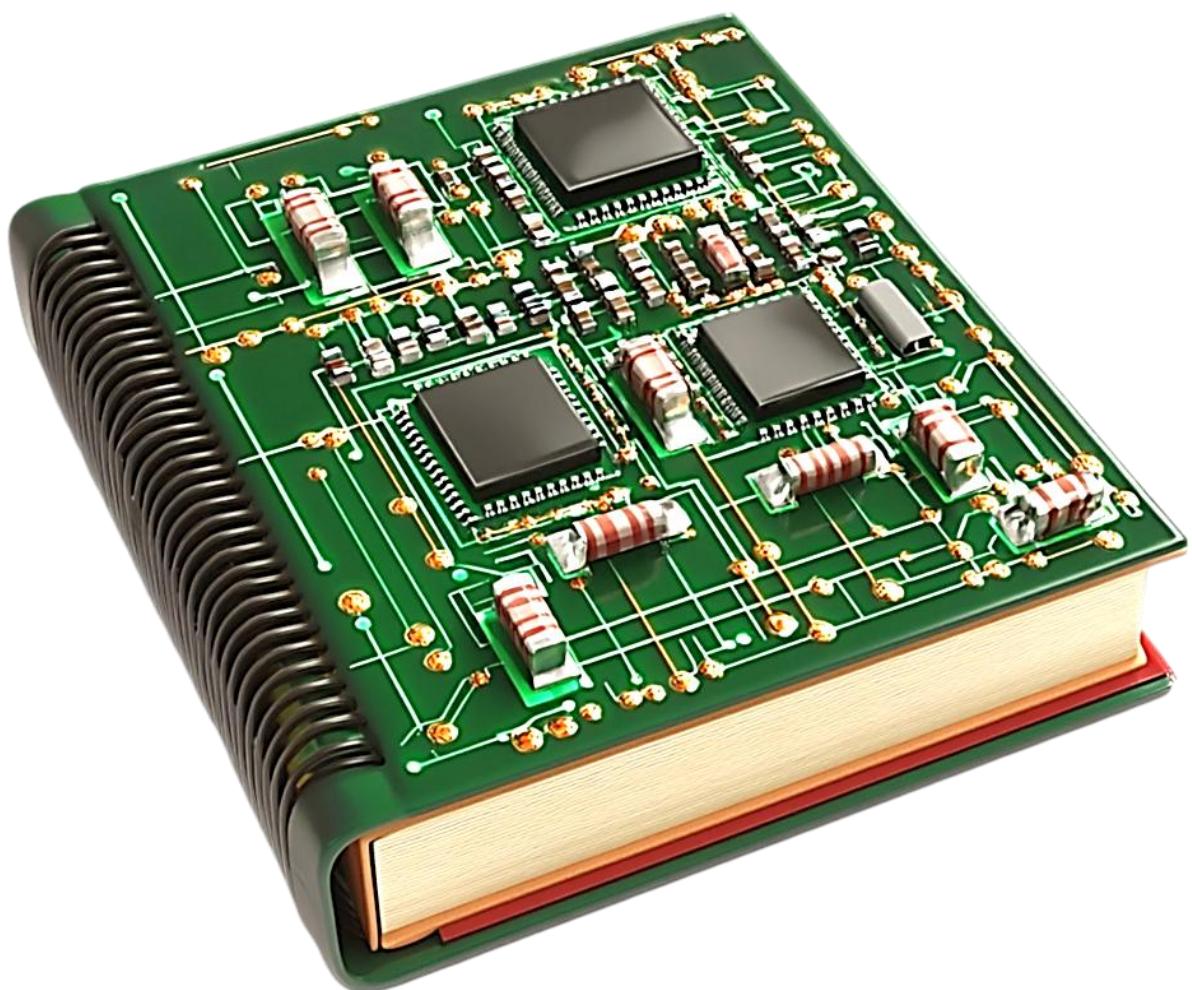


Hardware Engineer's Guide

# PCB DESIGN

*By Shimi Cohen*



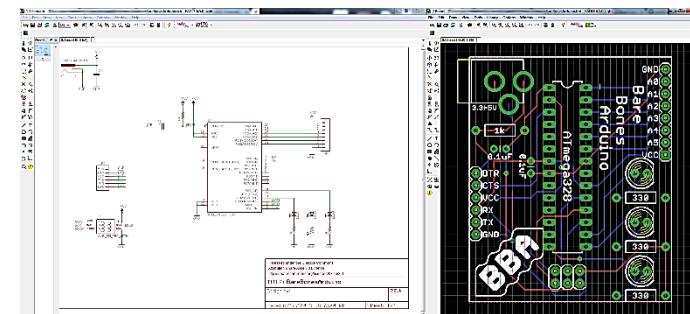
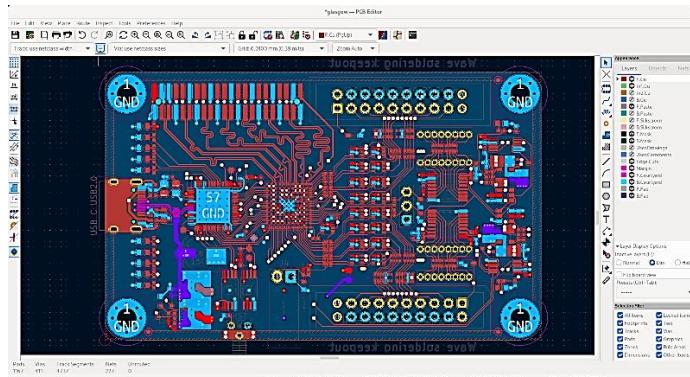
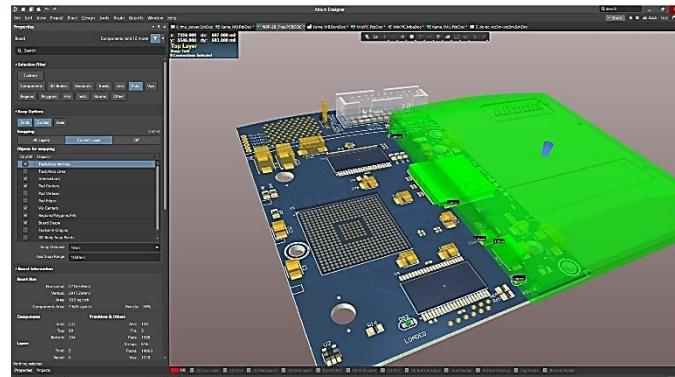
# 1. FUNDAMENTALS OF PCB DESIGN

PCB design transforms electrical schematics into manufacturable circuit boards. Modern design requires understanding both electrical theory and manufacturing constraints.

## 1.1 MODERN CAD TOOLS

Most Popular Tools used today:

NAME	MANUFACTURER	STRONGEST FEATURE
ALLEGRO	CADENCE	ADVANCED ROUTING FOR HIGH-SPEED
ALTIUM	ALTIUM	ALL-IN-ONE ENVIRONMENT
PADS	SIEMENS	STRONG SIGNAL INTEGRITY ANALYSIS
EAGLE	AUTODESK	INTEGRATION WITH FUSION 360
KICAD	OPEN SOURCE	FREE, OPEN-SOURCE



## 1.2 INDUSTRY STANDARDS

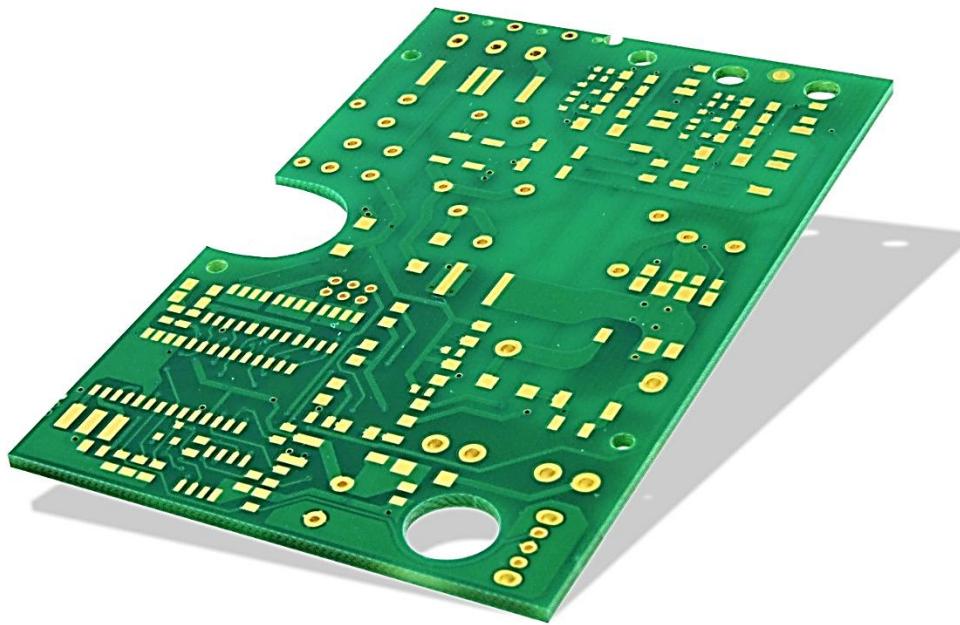
Critical standards governing PCB design:

STANDARD	TITLE
<b>IPC-2221</b>	GENERIC STANDARD ON PRINTED BOARD DESIGN
<b>IPC-2222</b>	DESIGN STANDARD FOR RIGID ORGANIC PRINTED BOARDS
<b>IPC-6012</b>	QUAL AND PERF SPEC FOR RIGID PRINTED BOARDS
<b>IPC-A-610</b>	ACCEPTABILITY OF ELECTRONIC ASSEMBLIES
<b>IPC-2226</b>	DESIGN STANDARD FOR HIGH DENSITY INTERCONNECT (HDI)
<b>IPC-4101</b>	SPEC FOR BASE MATERIALS FOR RIGID PRINTED BOARDS
<b>IPC-6013</b>	QUAL AND PERF SPEC FOR FLEXIBLE PRINTED BOARDS
<b>IPC-2152</b>	CURRENT CARRYING CAPACITY IN PRINTED BOARD DESIGN
<b>UL 796</b>	SAFETY FOR PRINTED-WIRING BOARDS
<b>IPC-7351</b>	GENERIC REQUIREMENTS FOR SURFACE MOUNT DESIGN

## 1.3 CORE MATERIAL & SUBSTRATE

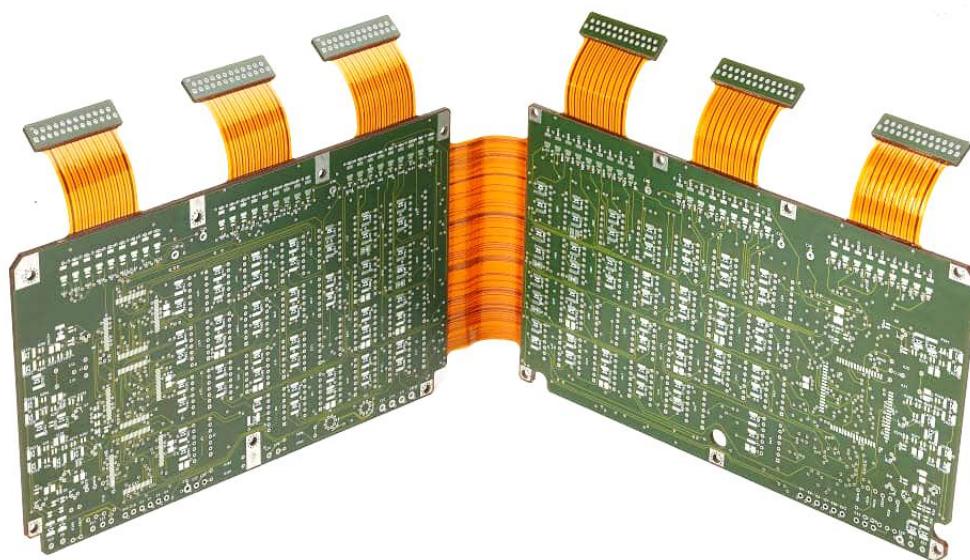
### FR-4

A fiberglass-reinforced epoxy laminate, widely used for its balance of cost, mechanical strength, and thermal resistance (up to ~140°C). It is chemically resistant, easy to manufacture, and suitable for most applications.



### POLYIMIDE

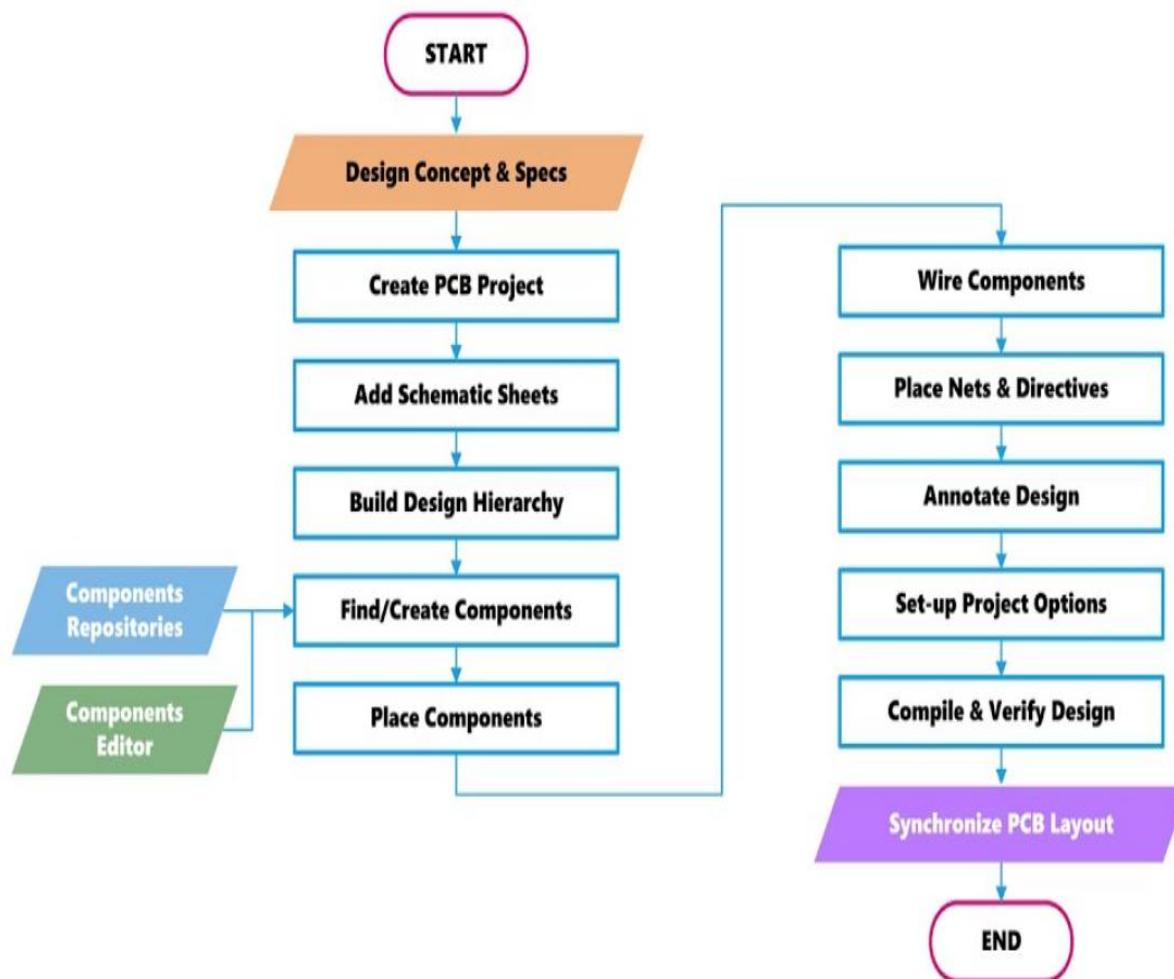
Offers superior flexibility and high-temperature endurance (up to 260°C or more), making it ideal for flexible circuits and harsh environments. Polyimide has a lower dielectric constant and excellent chemical resistance but is more expensive.



## 1.4 DESIGN WORKFLOW

### **PCB DESIGN PROCESS:**

1. **Schematic** Creation Draw the circuit diagram in PCB design software.
2. **Placement** Place electronic components on the board layout.
3. **Routing** Connect components with copper traces
4. **DRC** Run automated checks
5. **Gerbers** Export files Generation (Gerber, drill, etc.)
6. **Production** Manufacturing PCB
7. **Assembly** Pick and Place (PCBA)



## 2. DESIGN PREPARATION

Effective PCB design begins with thorough preparation and analysis.

### 2.1 SCHEMATIC ANALYSIS

#### **CRITICAL SCHEMATIC REVIEW ELEMENTS:**

- Net connectivity - Verify all connections are intentional
- Power requirements - Identify supply voltages and currents
- Signal types - Classify analog, digital, and power nets
- Critical paths - Locate timing-sensitive connections

### 2.2 COMPONENT SELECTION

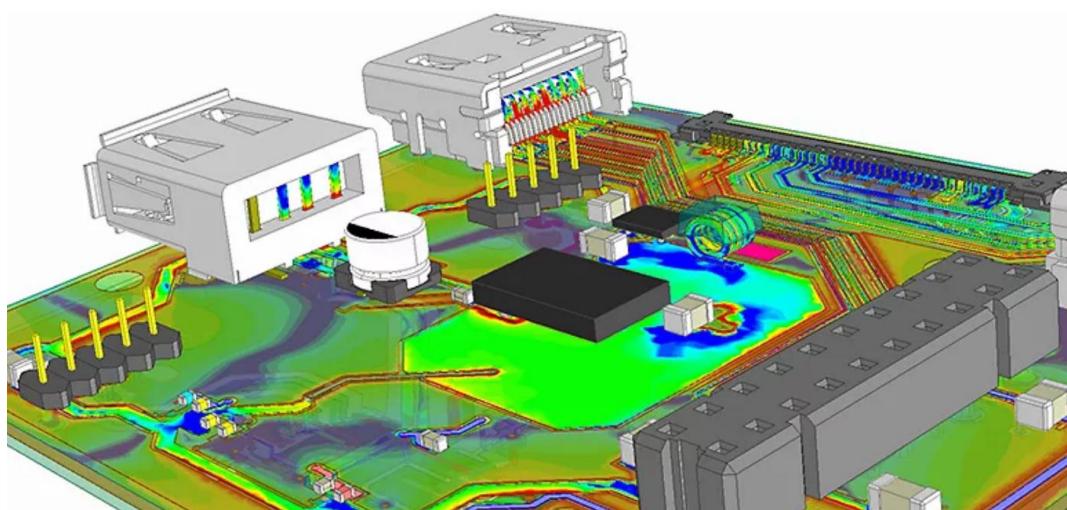
Package considerations for layout:

PACKAGE	PITCH	LAYOUT DIFFICULTY	THERMAL PERFORMANCE
SOIC	1.27MM	LOW	GOOD
QFP	0.8MM	MEDIUM	FAIR
BGA	0.5-1.0MM	HIGH	EXCELLENT
QFN	0.5MM	MEDIUM	EXCELLENT

### 2.3 BOARD PLANNING

#### **ESSENTIAL PLANNING STEPS:**

- Board outline - Define mechanical constraints (DXF)
- Layer count - Determine based on routing density
- Component groups - Organize by function (power, analog, digital)
- Connector placement - Position for system integration



# 3. PHYSICAL DESIGN PARAMETERS

Physical design parameters directly impact electrical performance.

## 3.1 MEASUREMENT

PCB design uses both imperial and metric units:

PARAMETER	IMPERIAL	METRIC	APPLICATION
DRILL SIZES	MILS/INCHES	MILLIMETERS	VIA AND HOLE SIZING
TRACE WIDTH	MILS	MICRONS	FINE PITCH ROUTING
COMPONENT PITCH	MILS	MILLIMETERS	PACKAGE DIMENSIONS



UNIT	DEFINITION	RATIO TO OTHER UNITS
MIL	1/1000 INCH (0.001 INCH)	1 MIL = 0.0254 MM = 25.4 $\mu$ M
MM	1/1000 METER	1 MM = 39.37 MILS
INCH	STANDARD IMPERIAL UNIT	1 INCH = 25.4 MM = 1000 MILS
$\mu$ M	1/1,000,000 METER (0.001 MM)	1 $\mu$ M = 0.03937 MIL = 0.001 MM

## 3.2 TRACE GEOMETRY

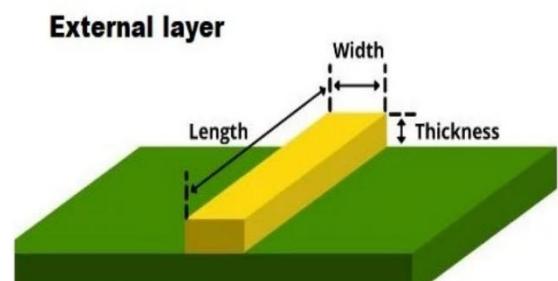
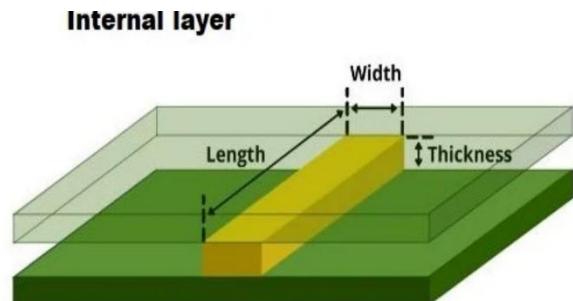
Standard trace specifications:

### MINIMUM TRACE WIDTHS BY LAYER:

- Outer layers - 0.1mm (4 mil) typical
- Inner layers - 0.075mm (3 mil) typical
- High current - Calculate based on IPC-2221

### TRACE SPACING REQUIREMENTS:

- Same net - No minimum spacing
- Different nets - 0.1mm (4 mil) minimum
- High voltage - Per IPC-2221 voltage tables



### 3.3 TRACE CURRENT CALCULATIONS

Calculate trace width for current carrying capacity:

#### IPC-2221 FORMULA:

- $\text{Area} = (\text{Current} / (k \times (\text{Temp Rise})^b))^{\frac{1}{c}}$
- Where k, b, c are constants based on layer type

#### COMMON APPLICATIONS:

- Signal traces - 0.1-0.2mm width adequate
- Power traces - 0.5-2.0mm typical
- High current - Use copper pours or multiple vias

#### EXAMPLE:

12V, 2A power supply requires 0.8mm trace width for 10°C temperature rise on outer layer.

### 3.4 VIA SIZING

#### MINIMUM SIZE:

Determined by PCB manufacturer capabilities, typically 0.2–0.3 mm drill diameter.

#### ASPECT RATIO:

Ensure via depth-to-diameter ratio supports reliable plating (commonly  $\leq 8:1$ ).

#### CURRENT CAPACITY:

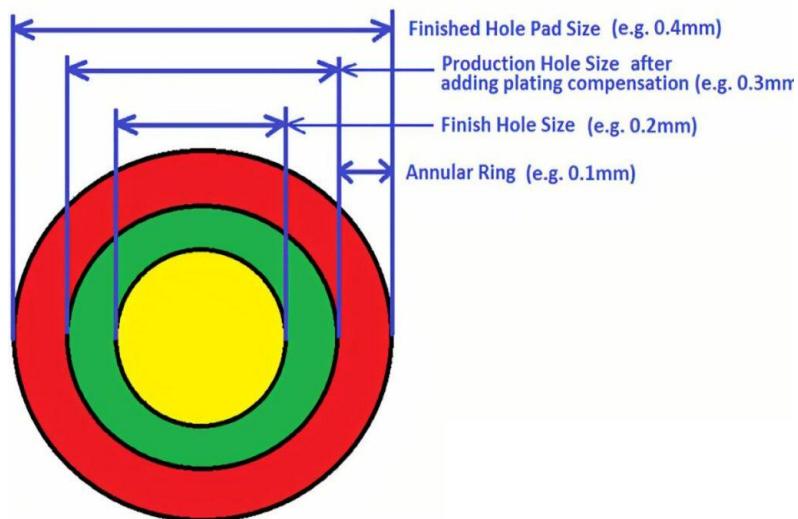
Select via size based on required current (multiple vias for high-current paths).

#### SIGNAL INTEGRITY:

Avoid placing vias in high-speed signal paths unless necessary, minimize stubs.

#### CLEARANCE:

Maintain adequate spacing between vias and other features to prevent



# 4. COMPONENT INTEGRATION

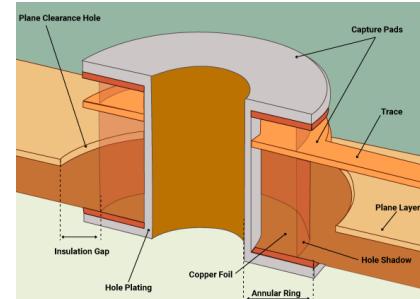
Proper component integration ensures reliable manufacturing and assembly.

## 4.1 PAD DESIGN

Pad geometry affects soldering reliability:

### **STANDARD PAD EXTENSIONS:**

- SOIC packages - 0.05mm extension beyond lead
- QFP packages - 0.1mm extension for fine pitch
- BGA packages - Pad diameter 80% of ball diameter

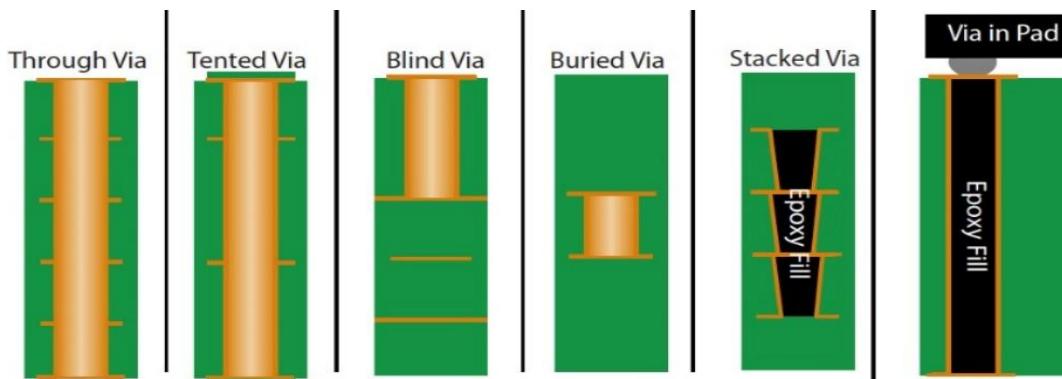


### **PAD SHAPES:**

- Round - Standard for through-hole
- Oval - Wave soldering applications
- Rectangle - Surface mount devices
- Thermal - Heat dissipation requirements

## 4.2 VIA IMPLEMENTATION

- Standard Via: Drilled through all layers
- Micro Via: Very small, laser-drilled
- Blind Via: Connects outer layer to one or more inner layers.
- Buried Via: Located entirely within inner layers



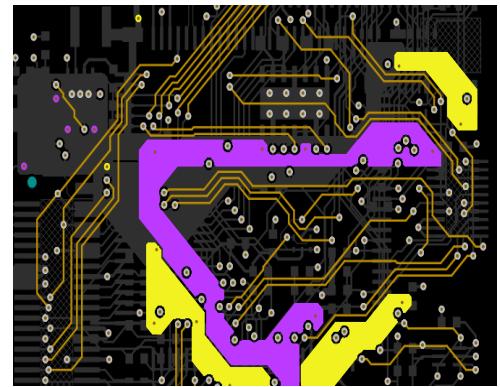
### **VIA PLACEMENT GUIDELINES:**

- Signal vias - Minimize length for high-speed signals
- Power vias - Multiple vias for current distribution
- Thermal vias - Under heat-generating components

## 4.3 COPPER FILLS (POLYGON)

### COPPER FILLS PROVIDE:

- Ground planes - Low impedance return paths
- Power distribution - Reduced resistance
- EMI shielding - Noise reduction
- Thermal management - Heat spreading

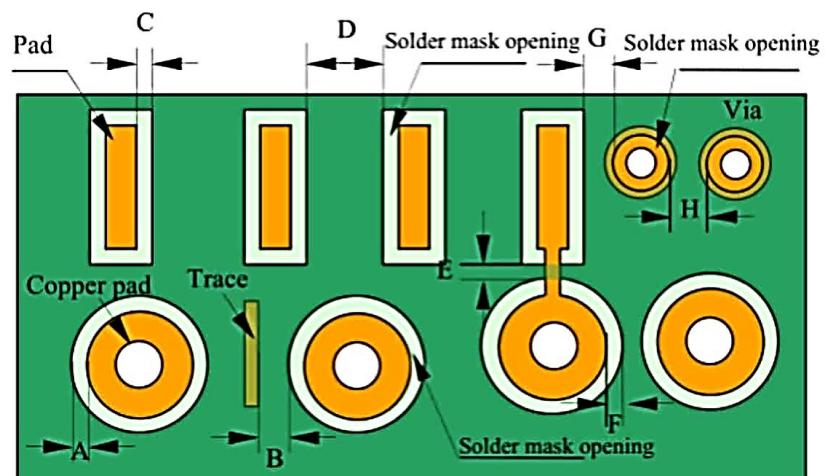
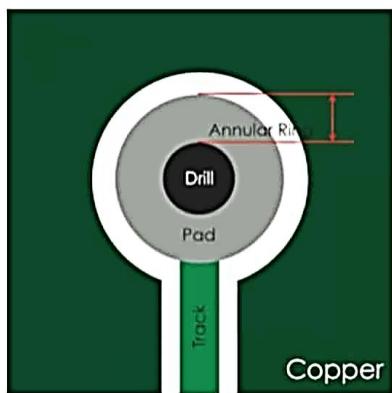


### FILL STRATEGIES:

- Solid fills - Maximum copper coverage
- Hatched fills - Reduced copper stress
- Thermal relief - Soldering accessibility

## 4.4 OTHER BOARD FEATURES

<b>COPPER TRACES</b>	CONDUCTIVE PATHS
<b>SUBSTRATE</b>	THE CORE MATERIAL (LIKE FR-4)
<b>SOLDER MASK</b>	PROTECTIVE COATING TO PREVENT SHORTS
<b>SILKSCREEN</b>	PRINTED MARKINGS FOR LABELS, REFDES.
<b>COMPONENTS</b>	PHYSICAL ELECTRONIC PARTS
<b>TEST POINTS</b>	DESIGNATED TESTING SPOTS
<b>MOUNTING HOLES</b>	MECHANICALLY SECURING THE PCB



# 5. DESIGN RULES AND CONSTRAINTS

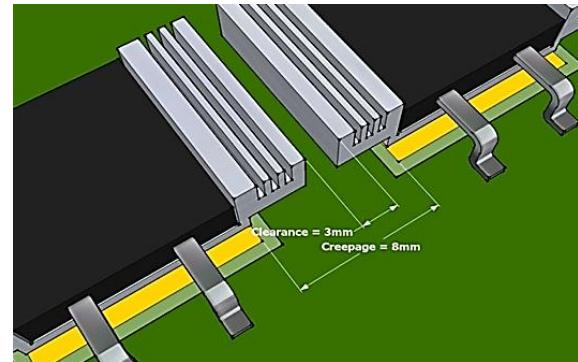
Design rules ensure manufacturability and electrical performance.

## 5.1 CLEARANCE REQUIREMENTS

Critical clearances for reliable operation:

### **ELECTRICAL CLEARANCES:**

- Trace to trace - 0.1mm minimum
- Via to trace - 0.05mm minimum
- Pad to pad - 0.1mm minimum
- High voltage - Per safety standards



### **MECHANICAL CLEARANCES:**

- Board edge - 0.5mm keep-out zone
- Mounting holes - 1.0mm clearance
- Connectors - Mating clearance required

	All	Route	Via	Through	SMD	Plane	Drill	LVH
Route	0.15							
Via	0.15	0.30						
Through	0.25	0.25	0.25					
SMD	0.25	0.25	0.25	0.25				
Plane	0.25	0.25	0.25	0.25	0.25			
Drill	1.00	0.50	0.50	0.50	0.50	0.50		
LVH	0.35	0.35	0.35	0.35	0.35	0.50	0.50	
Board	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00

Non-Electric Objects on Electric Layer Clearance

Non-Electric Objects: 0.30

## 5.2 DRC IMPLEMENTATION

Design Rule Check categories:

### **ELECTRICAL RULES:**

- Connectivity verification
- Net class constraints
- Power integrity checks

### **PHYSICAL RULES:**

- Minimum trace width
- Via size verification
- Clearance validation

### **MANUFACTURING RULES:**

- Drill size limitations
- Aspect ratio constraints
- Solder mask requirements

## 5.3 ROUTING CONSTRAINTS

Define rules for how traces are routed on the PCB, including minimum and maximum trace widths, controlled impedance requirements, differential pair routing, and maximum trace lengths. These constraints ensure signal integrity, manufacturability, and compliance with electrical performance requirements.

## 5.4 MANUFACTURING CONSTRAINTS

Set limitations based on your PCB fabricator's capabilities, such as minimum drill sizes, annular ring sizes, copper-to-edge clearances, and stack-up requirements. These rules ensure the design can be reliably and cost-effectively manufactured, avoiding costly redesigns and production delays.

# 6. LAYOUT STRATEGIES

Strategic layout approach determines design success and efficiency.

## 6.1 COMPONENT PLACEMENT

Systematic placement methodology:

### **PHASE 1 - CRITICAL COMPONENTS:**

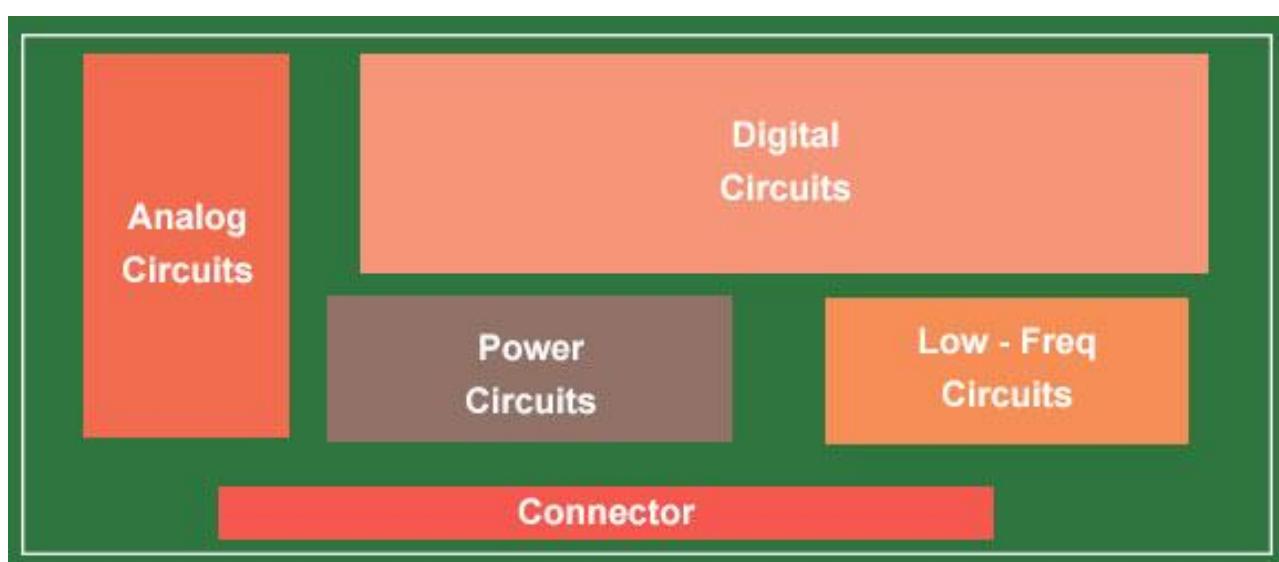
- Connectors at board edges
- Crystal oscillators near processors
- Power regulators for thermal management
- High-current components with thermal relief

### **PHASE 2 - FUNCTIONAL GROUPS:**

- Analog circuits isolated from digital switching
- Power supply components grouped
- Decoupling capacitors near power pins
- Test points accessible

### **PHASE 3 - OPTIMIZATION:**

- Minimize trace lengths for high-speed signals
- Balance component density
- Consider mechanical constraints
- Plan for thermal management



## 6.2 MANUAL ROUTING

Strategic routing approach:

### **PRIORITY ORDER:**

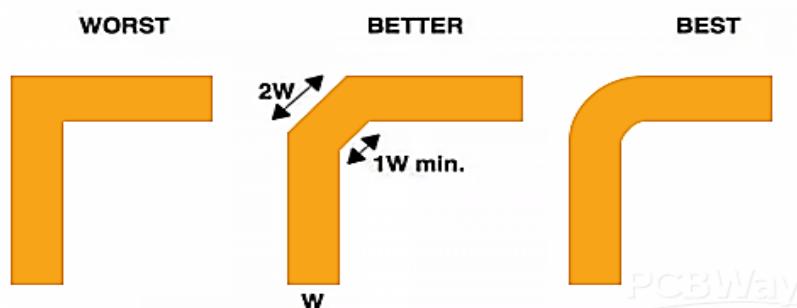
1. **Power and ground** - Establish solid references
2. **Clock signals** - Minimize skew and noise
3. **Critical analog** - Avoid digital noise coupling
4. **High-speed digital** - Control impedance and timing
5. **General I/O** - Fill remaining connections

### **ROUTING TECHNIQUES:**

- 45-degree angles - Minimize signal reflection
- Constant width - Maintain impedance control
- Via minimization - Reduce signal disruption
- Layer transitions - Plan for signal integrity

Routing by case:

THEORY	ROUTING TECHNIQUE	REASON
<b>HIGH SPEED</b>	MINIMIZE SHARP CORNERS	REDUCES REFLECTIONS & EMI
	USE GRADUAL CURVES	
	CONTROL LENGTH	
<b>POWER</b>	USE WIDE TRACES	ENSURES LOW RESISTANCE
	MULTIPLE VIAS	
	SOLID COPPER PLANES	
<b>DIFFERENTIAL</b>	ROUTE PARALLEL	MAINTAINS SIGNAL INTEGRITY
	EQUAL-LENGTH	
	COUPLED TRACE PAIRS	
<b>ANALOG</b>	ISOLATE FROM DIGITAL	MINIMIZES NOISE
	USE GUARD TRACES	
	AVOID LOOPS	
<b>RF</b>	SHORT DIRECT PATHS	PREVENTS REFLECTION & LOSS
	CONTROLLED IMPEDANCE	
	AVOID STUBS (ANTENNA)	



## 6.3 LAYER MANAGEMENT

Effective layer utilization:

### **TWO-LAYER BOARDS:**

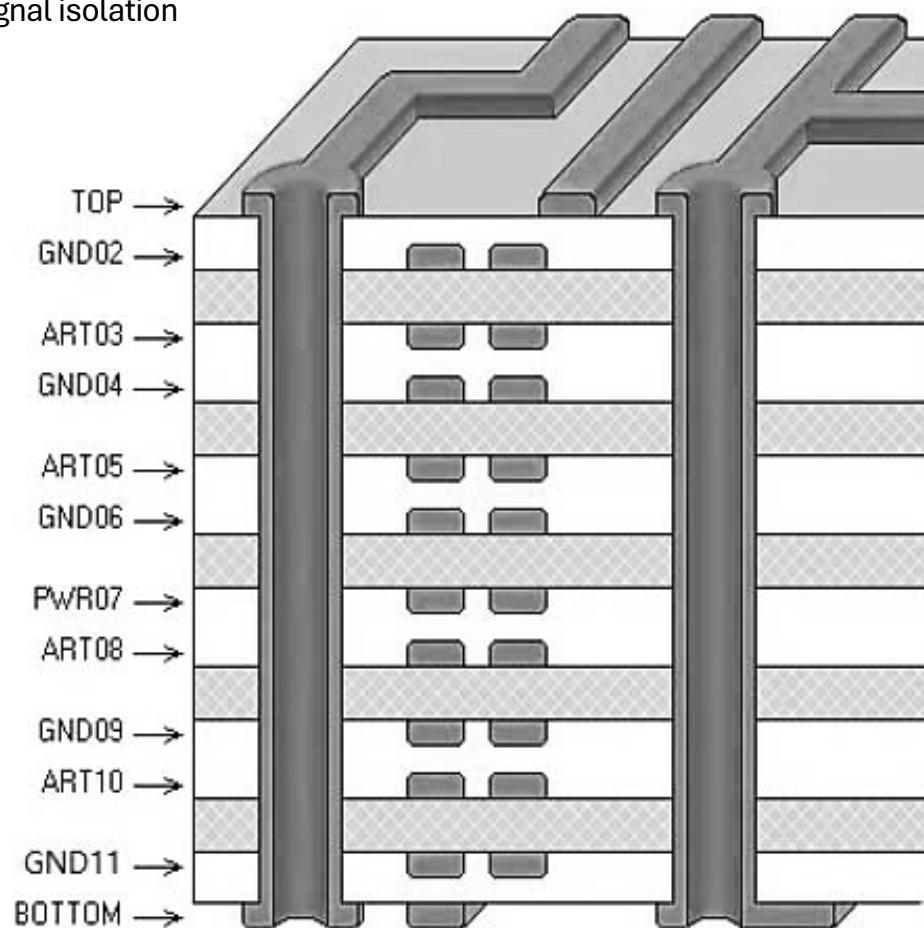
- Component side for horizontal routing
- Solder side for vertical routing
- Ground plane sections where possible

### **FOUR-LAYER BOARDS:**

- Layer 1: Component placement and routing
- Layer 2: Ground plane
- Layer 3: Power plane
- Layer 4: Routing and components

### **SIX-LAYER AND BEYOND:**

- Dedicated signal layers
- Multiple power planes
- Controlled impedance requirements
- High-speed signal isolation



## 6.4 LAYER CONSIDERATIONS

### **STANDARD THICKNESS:**

Most common thickness 1.57mm for 2-layer and some mid-layer counts.

Multilayer builds often range from 2.36–4.75 mm but can be customized

### **LAYER COUNT CONSTRAINTS:**

More layers increase overall thickness and complexity.

Internal dielectric thickness (core/prepreg) must meet minimums for reliability and manufacturability. IPC-6012 requires ~2.5mil for class 3 (recommended 3-4mil)

### **ODD VS. EVEN LAYERS:**

Odd-numbered layer counts (e.g., 9, 11) are possible but less common due to manufacturing and lamination constraints.

Even-numbered layers are standard for symmetry, cost, and reliability.

### **COMPONENT SIDE AND BOTTOM:**

Components can be placed on both sides (top and bottom).

Some high-density designs use micro-vias and buried/blind vias for inter-layer routing.

### **POTENTIAL PROBLEMS IN MULTILAYER (10+):**

- Increased risk of registration errors between layers.
- Thermal management and warping become more critical.
- Signal integrity challenges (crosstalk, impedance control).
- Higher manufacturing cost and longer lead times.
- Complex stack-up management and increased risk of delamination.

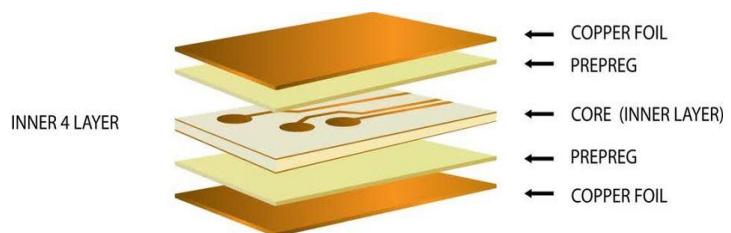
# 7. MANUFACTURING

## 7.1 FABRICATION LAYERS

Essential manufacturing layers:

### COPPER LAYERS:

- Signal & power distribution
- Controlled impedance
- Current carrying capacity



### SOLDER MASK:

- Many colors available
- 0.1mm minimum feature size
- Reg. tolerance  $\pm 0.075\text{mm}$

### SILKSCREEN:

- RefDes and values
- Polarity markings and pin 1
- Assembly instructions
- Company logos (revision)

### DRILL FILES:

- Through-hole specifications
- Via definitions
- Slot and cutout requirements



## 7.2 ASSEMBLY REQUIREMENTS

Design for assembly guidelines:

### **COMPONENT ORIENTATION:**

- Consistent polarized component alignment
- IC pin 1 indicators clearly marked
- Similar components in same orientation

### **SILKSCREEN:**

- Each component with its own RefDes (when possible)
- Minimum 50mil to be seen
- Avoid silk beneath components placement

### **FIDUCIAL MARKINGS:**

- Minimum 3 fiducials for automated assembly
- 1mm diameter copper circles
- Clear of solder mask
- Positioned for maximum accuracy

### **TEST POINT ACCESS:**

- 1.27mm minimum spacing
- 0.5mm minimum diameter
- Accessible from single side preferred

### **COMPONENT OCCUPANCY**

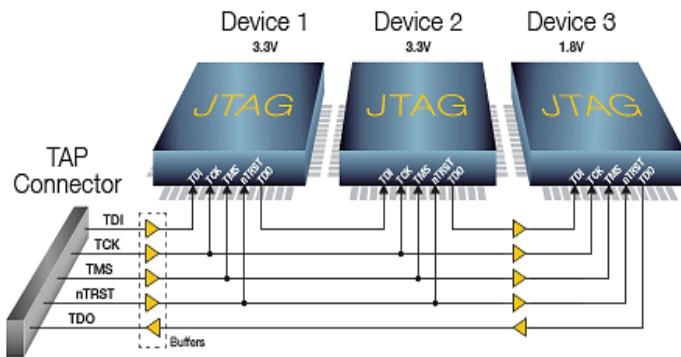
- Try to avoid over 70% occupancy
- High density design (mobile) increase the risks such as thermal and integrity
- Assembly access becomes challenging in HDI design

## 7.3 TESTING PROVISIONS

Built-in test capabilities:

### IN-CIRCUIT TESTING:

- Test point accessibility
- Fixture probe clearances
- Component value verification



### BOUNDARY SCAN:

- JTAG connectivity for digital circuits
- Test access port implementation
- Scan chain continuity

### FUNCTIONAL TESTING:

- Power supply verification
- Signal integrity checks
- Performance validation

### AUTOMATED OPTICAL INSPECTION (AOI):

- Component placement accuracy
- Solder joint quality inspection
- Polarity and orientation verification

### BURN-IN TESTING:

- Extended operation under stress conditions
- Early failure detection
- Reliability assessment under load



# 8. HIGH SPEED & POWER

## 8.2 HIGH-SPEED CONSIDERATIONS

Critical parameters for high-frequency design:

### **TRANSMISSION LINE EFFECTS:**

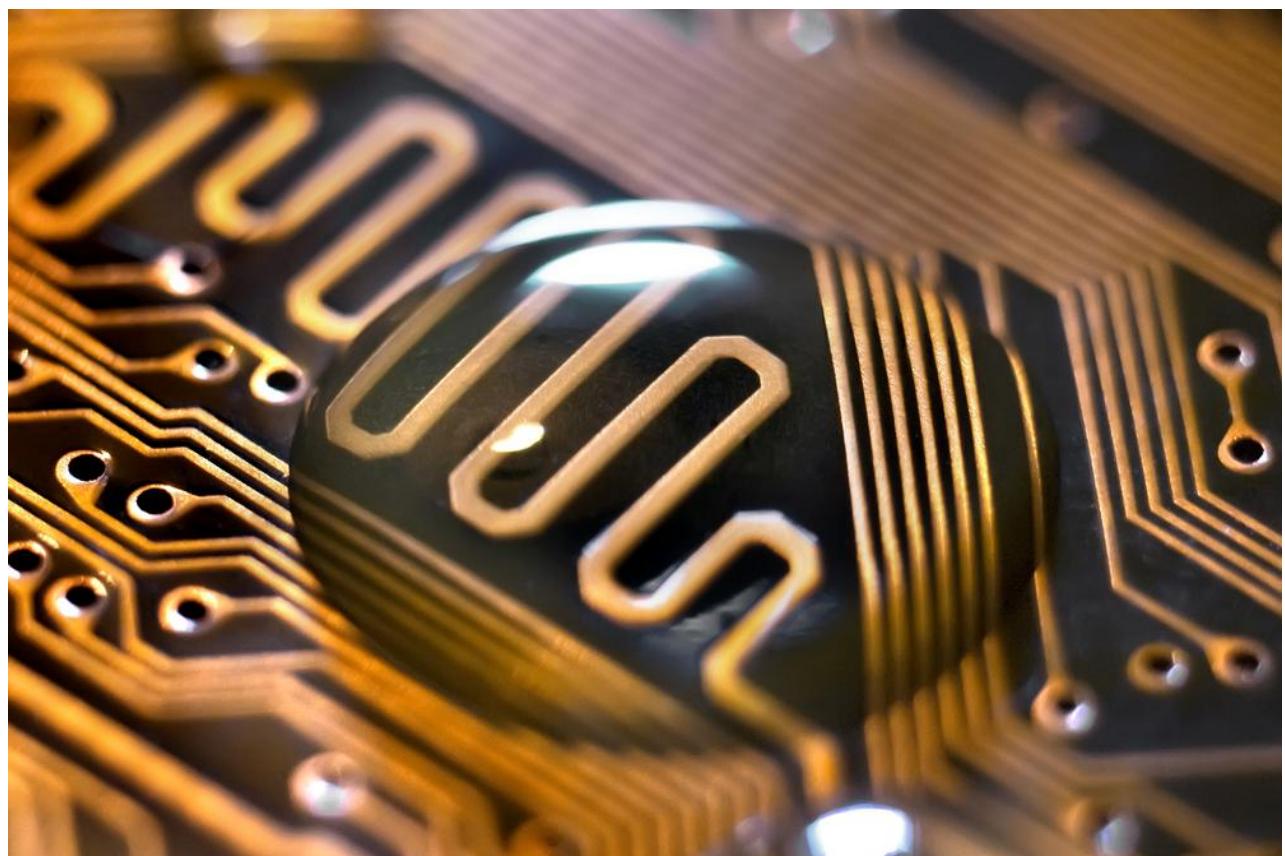
- Controlled impedance ( $50\Omega$  single-ended,  $100\Omega$  differential)
- Trace length matching for clock distributions
- Via stub elimination for frequencies  $>1\text{GHz}$
- Ground plane continuity for return paths

### **SIGNAL INTEGRITY TECHNIQUES:**

- Differential pair routing for high-speed data
- Guard traces for sensitive analog signals
- Termination networks for signal quality
- Power supply decoupling strategies

### **EXAMPLE:**

DDR4 memory interface requires matched trace lengths within 0.1mm and controlled  $100\Omega$  differential impedance for data signals.



## 8.3 POWER DISTRIBUTION

Robust power delivery systems:

### **POWER PLANE DESIGN:**

- Minimum 0.5oz copper weight for power planes
- Multiple via connections for current distribution
- Decoupling capacitor placement optimization
- Thermal management integration

### **BYPASS CAPACITOR STRATEGY:**

- High-frequency ceramics ( $0.1\mu F$ ) at each IC
- Medium-frequency tantalums ( $10\mu F$ ) per circuit section
- Low-frequency electrolytics ( $100\mu F+$ ) at power input
- ESR and ESL considerations for effectiveness

### **CURRENT DENSITY MANAGEMENT:**

- Maximum  $35A/mm^2$  for external copper layers
- Maximum  $17.5A/mm^2$  for internal copper layers
- Thermal rise calculations per IPC-2221
- Hot spot identification and mitigation

### **VOLTAGE REGULATION AND DISTRIBUTION:**

- Voltage regulator selection for stability and efficiency
- Distributed regulation for localized supply needs
- Feedback loop compensation for transient response
- Load regulation and line regulation specifications

### **GROUNDING AND RETURN PATH OPTIMIZATION:**

- Solid ground planes for low impedance returns
- Minimized ground loops for noise reduction
- Ground stitching vias for multi-layer continuity
- Segregation of analog and digital ground domains

# 9. SIGNAL INTEGRITY

Signal integrity ensures reliable data transmission in high-speed digital circuits.

## 9.1 TRANSMISSION LINE THEORY

### **BASIC TRANSMISSION LINE PARAMETERS:**

- Characteristic impedance -  $Z_0 = \sqrt{L/C}$
- Propagation delay - Critical for timing analysis
- Rise time effects - Signals behave as transmission lines when trace length  $> \lambda/10$

### **COMMON IMPEDANCE TARGETS:**

- Single-ended  $50\Omega \pm 10\%$  General digital
- Differential  $100\Omega \pm 10\%$  High-speed data
- Coaxial  $75\Omega \pm 5\%$  Video signals
- LVDS  $100\Omega \pm 5\%$  Display interfaces

## 9.2 CROSSTALK ANALYSIS

### **CROSSTALK MECHANISMS:**

- Capacitive coupling - Dominant in high-impedance circuits
- Inductive coupling - Significant in high-current switching
- Common impedance - Shared return paths

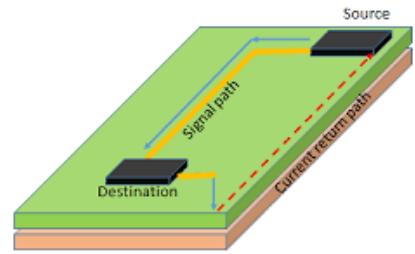
### **MITIGATION TECHNIQUES:**

- Increased spacing (3W rule minimum)
- Orthogonal routing between layers
- Differential signaling for critical nets

## 9.3 RETURN PATH MANAGEMENT

### GROUND PLANE CONTINUITY:

- Unbroken reference planes for high-speed signals
- Via stitching across plane splits
- Minimum 0.1mm via spacing for effective stitching

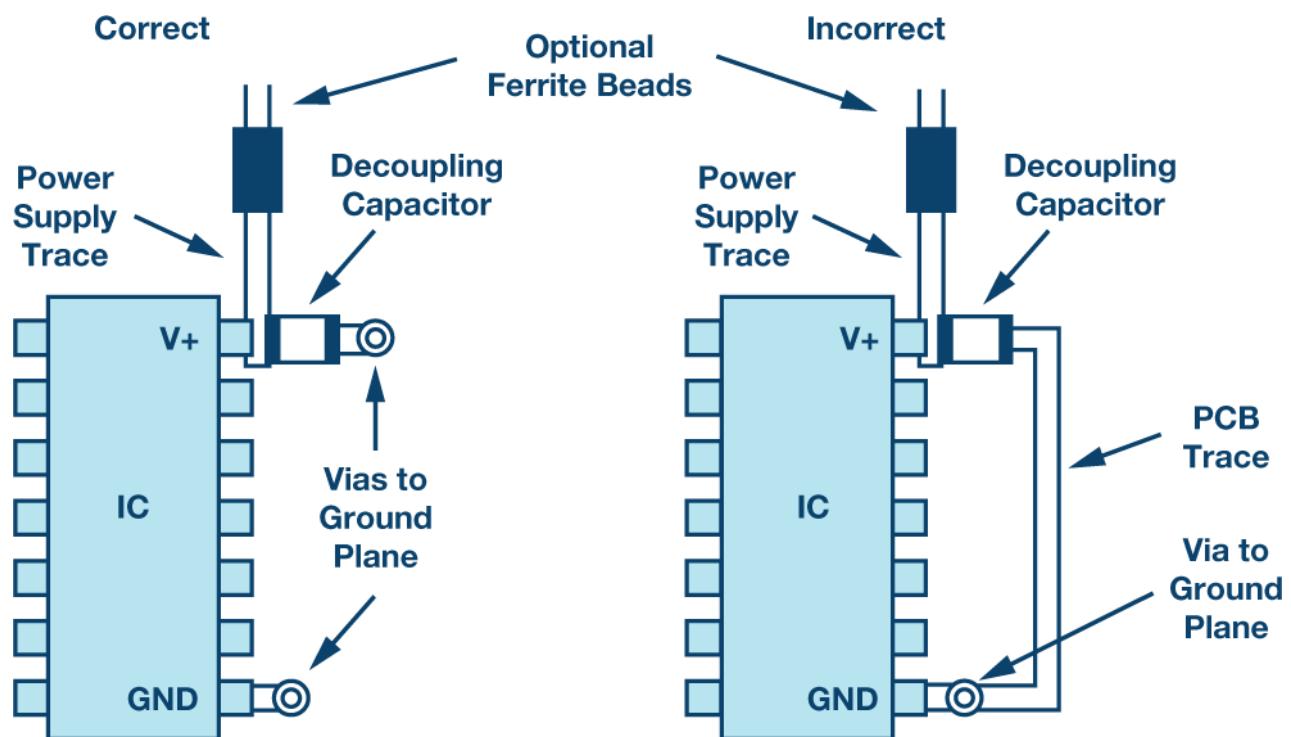


### LAYER TRANSITIONS:

- Reference plane changes require return vias
- Via placement within 200 mils of signal via
- Shortest possible via stubs

### POWER SUPPLY DECOUPLING:

- Multiple capacitor values for broadband filtering
- Placement within 5mm of power pins
- Low ESL capacitors for high-frequency performance



# 10.THERMAL MANAGEMENT

Effective thermal design prevents component failure and ensures reliable operation.

## 10.1 HEAT TRANSFER PRINCIPLES

### **THERMAL RESISTANCE CALCULATION:**

- $R_{th} = \Delta T / P$  (°C/W)
- Junction-to-ambient path analysis
- Multiple heat transfer paths in parallel

### **EFFICIENCY DESIGN CONSIDERATIONS**

- Conduction High PCB copper Thermal vias, pours
- Convection Medium Air-Cooling Component spacing
- Radiation Low High temperature Surface emissivity

## 10.2 THERMAL VIA DESIGN

### **VIA ARRAY CALCULATIONS:**

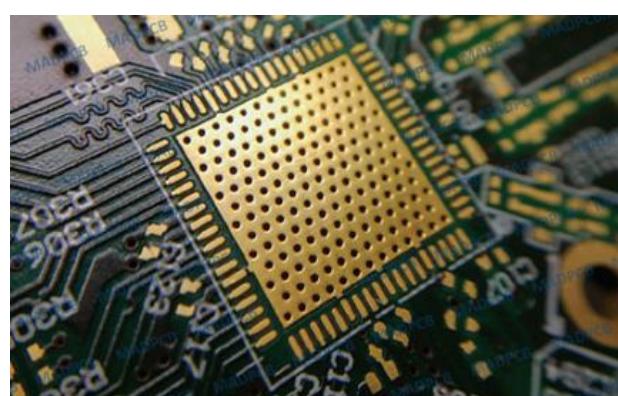
- Thermal resistance per via -  $R_{th} = 70\text{°C/W}$  typical
- Via spacing - 1.2mm maximum for effective heat spreading
- Fill options - Solid copper, thermal epoxy, or air-filled

### **THERMAL VIA SPECIFICATIONS:**

- Drill diameter - 0.2-0.3mm standard
- Plating thickness - 25μm minimum
- Aspect ratio - <6:1 for reliable plating

### **EXAMPLE CALCULATION:**

Power dissipation 5W (20°C rise) - Needs minimum 14 thermal vias of 0.2mm under IC.



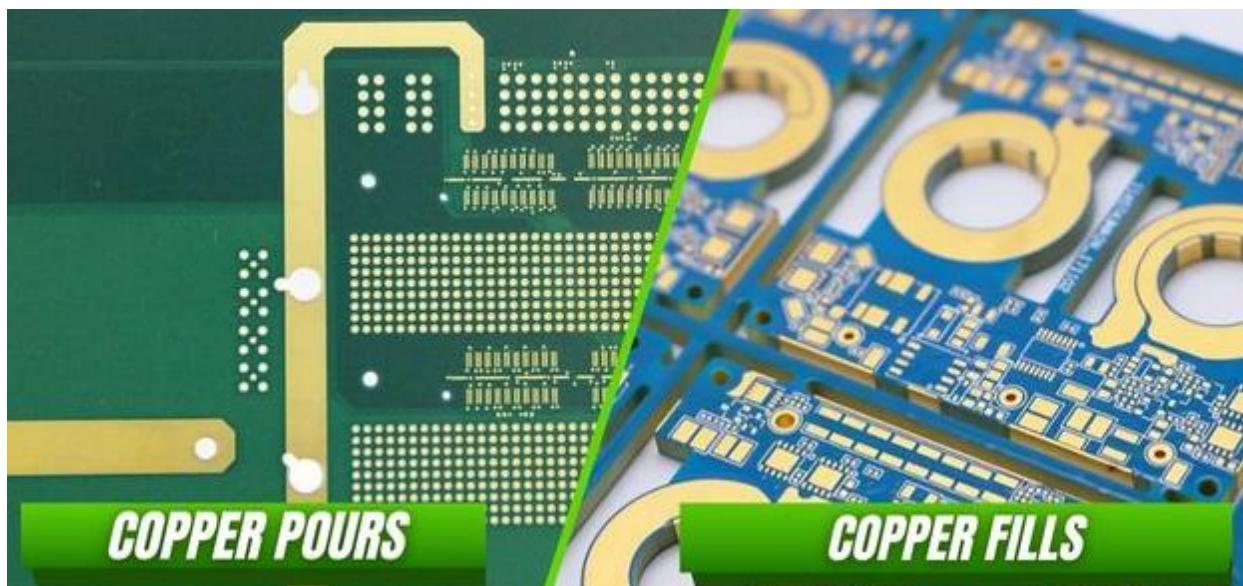
## 10.3 COPPER POUR STRATEGIES

### **HEAT SPREADING TECHNIQUES:**

- Solid copper pours under high-power components
- Thermal spoke connections to maintain solderability
- Multi-layer thermal vias for vertical heat transfer

### **COPPER THERMAL PERFORMANCE**

- Low-power digital 0.5oz (17µm) Basic heat spreading
- Power management 1.0oz (35µm) Standard thermal design
- High-power analog 2.0oz (70µm) Enhanced heat dissipation
- Power electronics 3.0oz+ (105µm+) Maximum thermal capacity



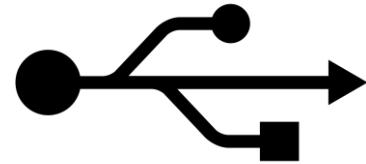
# 11. HIGH-SPEED PROTOCOLS

Contemporary digital interfaces require specific design considerations.

## 11.1 USB DESIGN GUIDELINES

### USB 2.0 REQUIREMENTS:

- Differential impedance -  $90\Omega \pm 15\%$
- Trace length matching -  $\pm 0.1\text{mm}$
- Maximum trace length - 1500mm
- Common mode choke placement



### USB 3.0/3.1 CONSIDERATIONS:

- SuperSpeed differential pairs -  $90\Omega \pm 7\Omega$
- Tighter length matching -  $\pm 50\mu\text{m}$
- Via minimization in signal path
- Enhanced shielding requirements

### DESIGN SPECIFIC CONSIDERATION

- USB 2.0 : 480 Mbps  $\pm 0.1\text{mm}$  EMI filtering
- USB 3.0 : 5 Gbps  $\pm 50\mu\text{m}$  Separate SS pairs
- USB 3.1 : 10 Gbps  $\pm 25\mu\text{m}$  Advanced SI analysis
- USB4.0 : 40 Gbps  $\pm 12\mu\text{m}$  Strict via control

## 11.2 PCIE IMPLEMENTATION

### PCIE GEN3 DESIGN RULES:

- Differential impedance -  $85\Omega \pm 7\Omega$
- Intra-pair skew - <5ps (0.8mm)
- Inter-pair skew - <100ps (15mm)
- Reference clock requirements



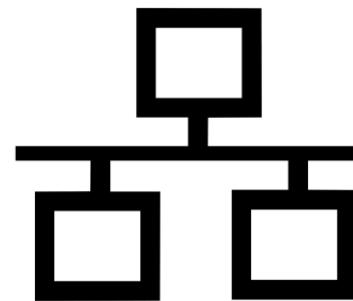
### SIGNAL INTEGRITY REQUIREMENTS:

- Via stub elimination above 8GHz
- Continuous reference planes
- AC coupling capacitor placement
- Spread spectrum clock compatibility

## 11.3 ETHERNET DESIGN

### **GIGABIT ETHERNET SPECIFICATIONS:**

- Differential impedance -  $100\Omega \pm 10\%$
- All four pairs length matched within 50mm
- Minimum bend radius -  $2 \times$  trace width
- Magnetic isolation requirements



### **10 GIGABIT CONSIDERATIONS:**

- Tighter impedance control -  $100\Omega \pm 5\%$
- Enhanced crosstalk management
- Backplane loss budgeting
- Advanced equalization support

## 1.4 DDR MEMORY INTERFACE DESIGN

### **DDR4/DDR5 DESIGN RULES:**

- Single-ended impedance:  $40-60\Omega \pm 10\%$
- Differential clock pairs:  $100\Omega \pm 7\Omega$
- Data groups:  $\pm 5$  mils (0.127mm)
- Address/ctrl to clock:  $\pm 25$  mils (0.635mm)



### **SIGNAL INTEGRITY REQUIREMENTS:**

- Strict reference planes: Continuous GND under data groups
- Via count limitation:  $\le 2$  vias per net
- On-die termination (ODT) tuning
- $< 30mV$  noise on VDDQ
- Dedicated power islands for VPP/VDDQ

PROTOCOL	SPEED[MBPS]	KEY CONSTRAINT	CRITICAL FOCUS
DDR3	800–2133	LENGTH SKEW < 50 MILS	T-BRANCH TOPOLOGY
DDR4	1600–3200	DATA STROBE $\pm 10\text{PS}$	CA/CS FLY-BY
DDR5	3200–6400	DQ/DQS $\pm 0.5\text{PS}$	FEEDBACK EQUAL

# 12. FLEXIBLE AND RIGID-FLEX

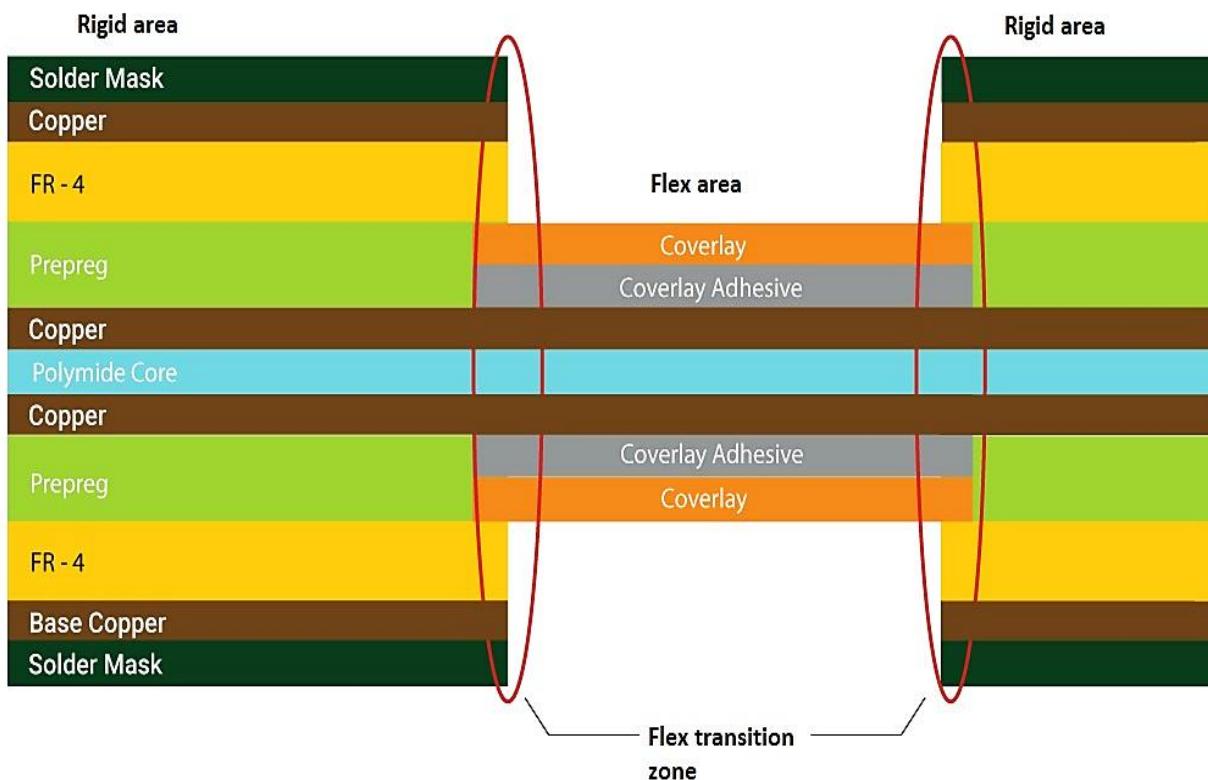
## 12.1 FLEXIBLE CIRCUIT FUNDAMENTALS

### **RECOMMENDED MATERIAL:**

- Polyimide base - Standard flexibility
- LCP (Liquid Crystal Polymer) - High-frequency applications

Thickness considerations:

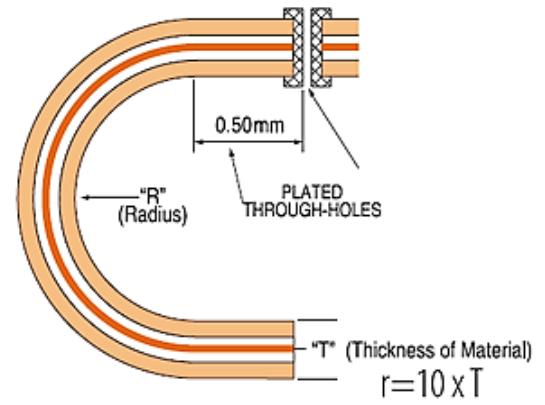
LAYER COUNT	THICKNESS	BEND RADIUS
1-LAYER	0.05-0.1MM	5x THICKNESS
2-LAYER	0.1-0.2MM	10x THICKNESS
4-LAYER	0.2-0.4MM	15x THICKNESS
6+ LAYER	0.4MM	+20x THICKNESS



## 12.2 BEND RADIUS CALCULATIONS

### DYNAMIC FLEXING REQUIREMENTS:

- Minimum bend radius -  $6 \times$  total thickness
- Stress relief design - Teardrop transitions
- Conductor routing - Perpendicular to bend axis



### STATIC BEND APPLICATIONS:

- One-time installation bending
- Minimum radius -  $3 \times$  total thickness
- Stiffener placement for support

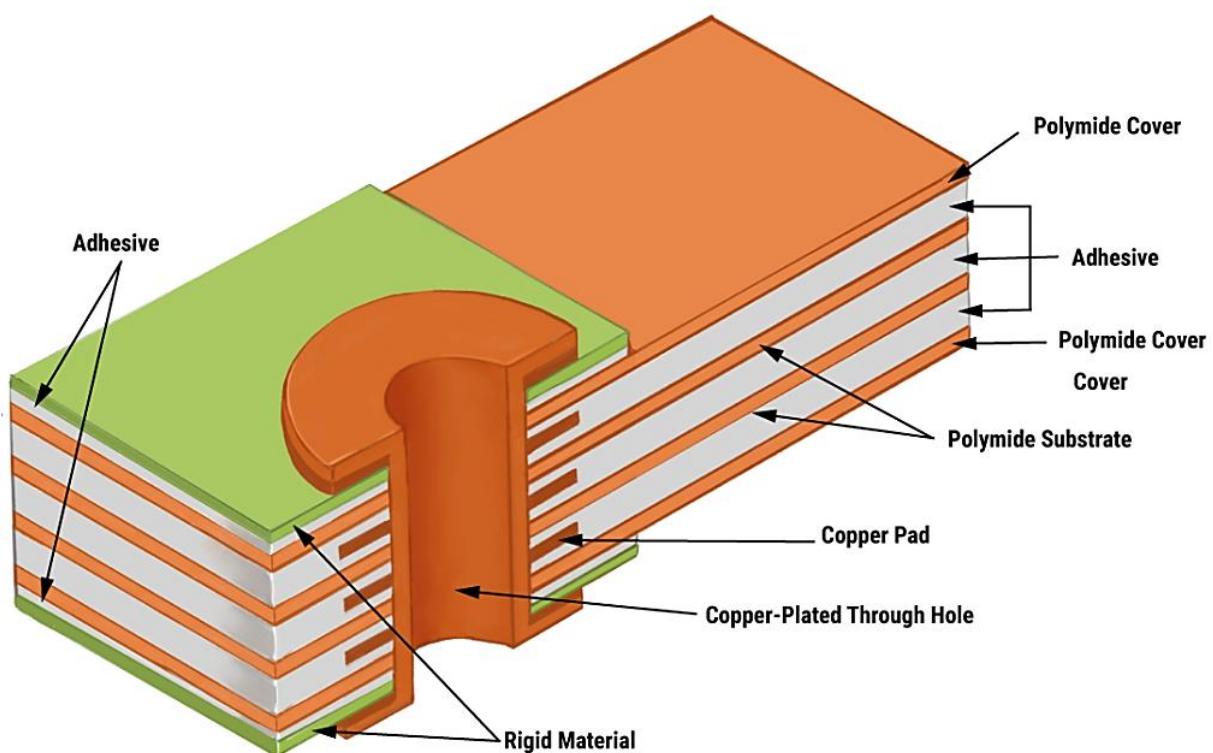
## 12.3 RIGID-FLEX TRANSITION DESIGN

### STACK-UP CONSIDERATIONS:

- Layer transitions in rigid sections only
- Via placement restrictions in flex zones
- Controlled impedance through transitions

### MANUFACTURING CONSTRAINTS:

- Minimum rigid section - 6mm width
- Flex section entry angle -  $<45^\circ$
- Stiffener overlap requirements - 1mm minimum



# 13. COMPONENT GUIDELINES

Different component types require specialized layout considerations.

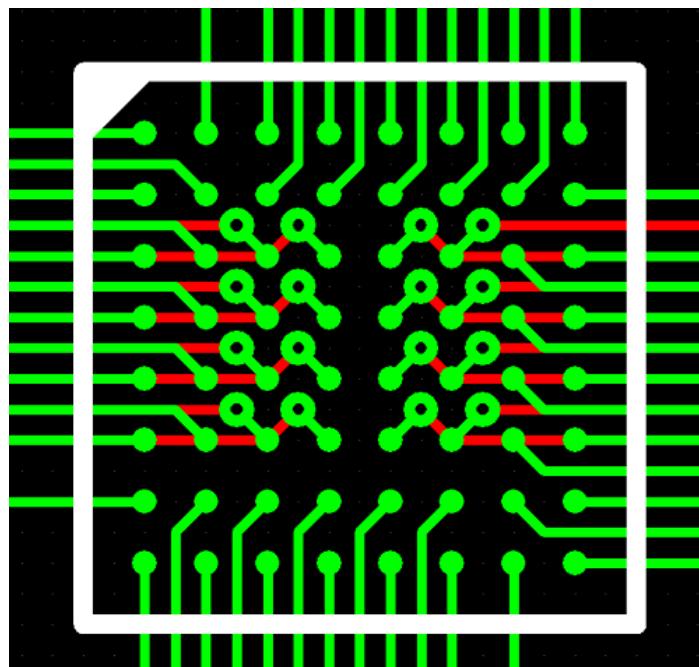
## 13.1 BGA ESCAPE ROUTING

### **VIA-IN-PAD TECHNIQUE:**

- Micro vias for high-density BGAs
- Via filling requirements for assembly
- Pad size reduction considerations

### **ESCAPE ROUTING STRATEGIES:**

BGA PITCH	VIA SIZE	ESCAPE	REQ. LAYERS
1.0MM	0.1MM	DIRECT ESCAPE	2 LAYERS
0.8MM	0.1MM	VIA-IN-PAD	4 LAYERS
0.5MM	0.08MM	MICRO VIA ONLY	6+ LAYERS
0.4MM	0.08MM	HDI TECHNOLOGY	8+ LAYERS



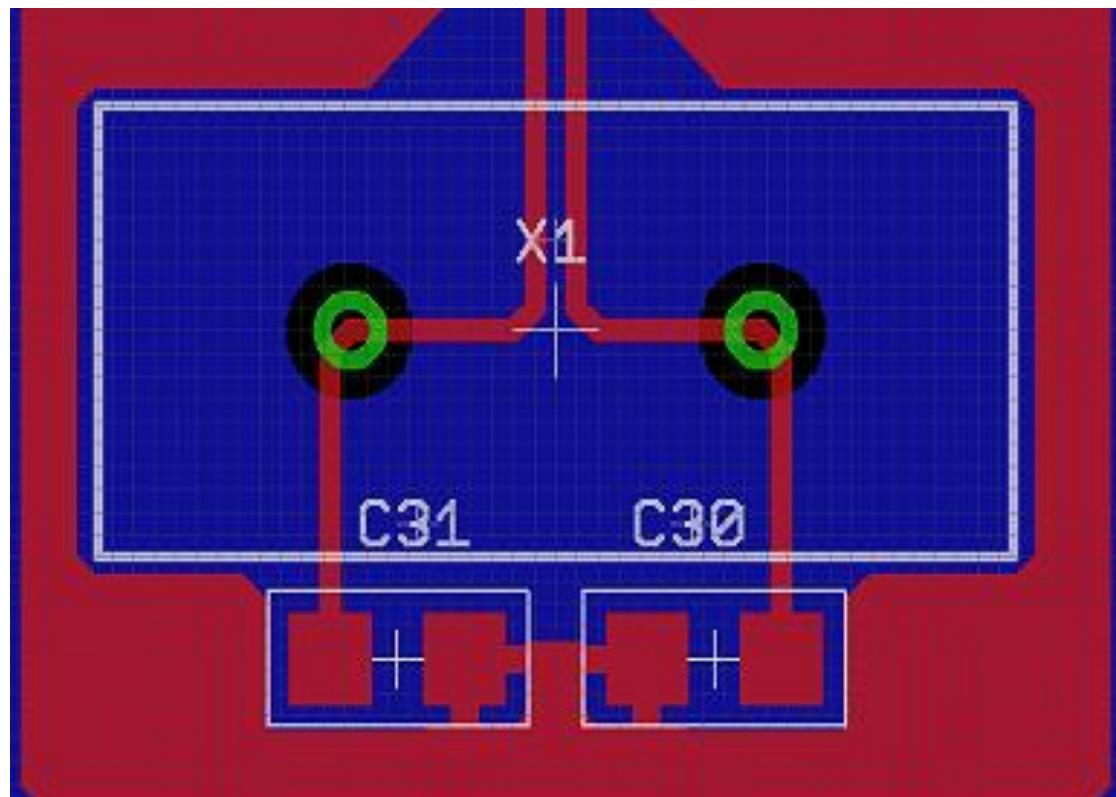
## 13.2 CRYSTAL OSCILLATOR LAYOUT

### **CRITICAL DESIGN ELEMENTS:**

- Ground guard ring around crystal
- Minimum trace length to IC pins
- Load capacitor placement - <5mm from crystal
- Keep-out zones for switching signals

### **FREQUENCY-SPECIFIC CONSIDERATIONS:**

- Low frequency (<10MHz) - Standard layout rules
- Medium frequency (10-100MHz) - Guard rings essential
- High frequency (>100MHz) - Dedicated ground plane



## 13.3 SWITCH-MODE POWER SUPPLY LAYOUT

### **COMPONENT PLACEMENT PRIORITY:**

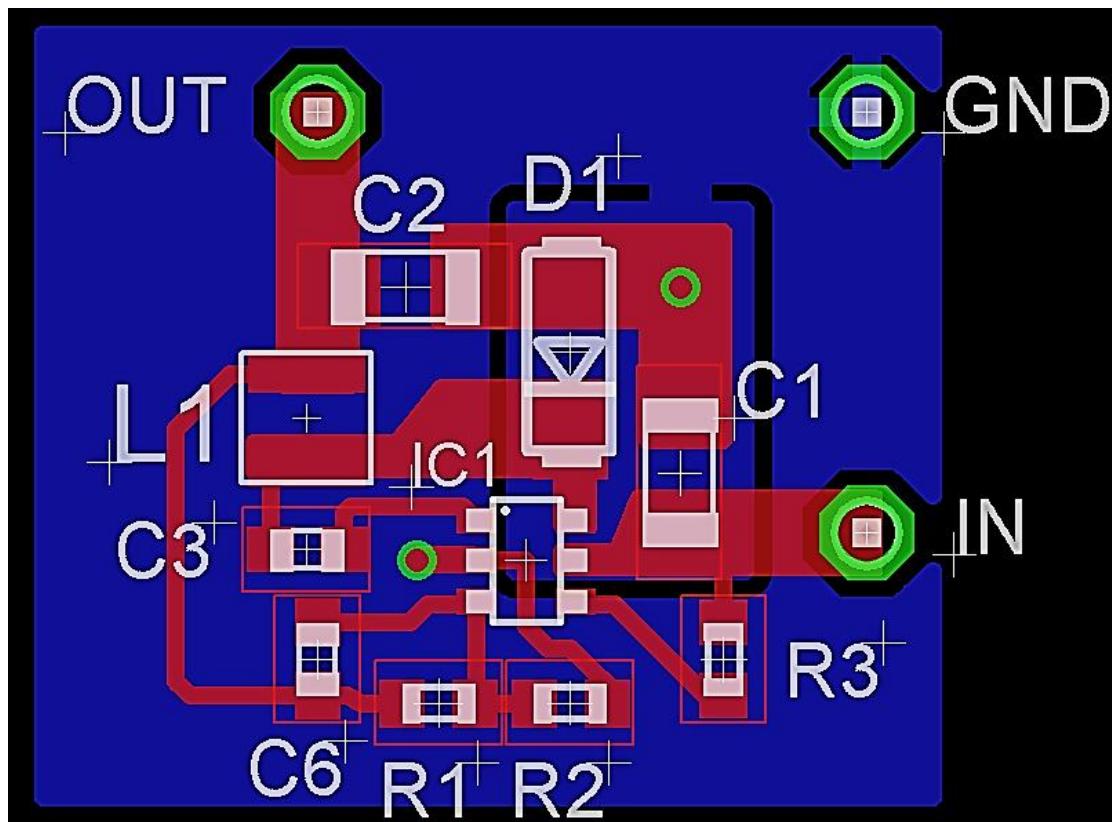
1. Input and output capacitors closest to switching IC
2. Inductor placement for minimal loop area
3. Feedback network routing away from switching nodes
4. Thermal management for switching components

### **CRITICAL ROUTING GUIDELINES:**

- Minimize switching loop area
- Separate analog and power grounds
- Star ground connection point
- Input/output filtering isolation

### **EXAMPLE LAYOUT:**

Buck converter requires  $<25\text{mm}^2$  switching loop area for acceptable EMI performance at 1MHz switching frequency.



## 13.4 CONNECTOR DESIGN INTEGRATION

### **HIGH-SPEED CONNECTOR REQUIREMENTS:**

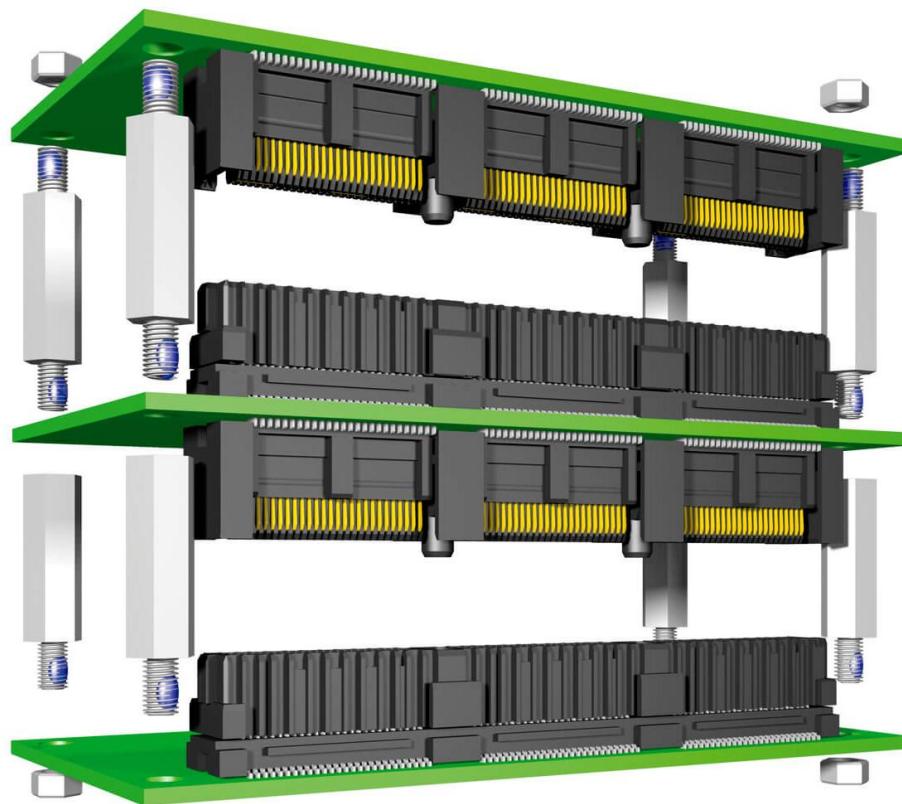
- Controlled impedance through connector
- Via placement for signal transitions
- Ground plane continuity
- EMI shielding considerations

### **POWER CONNECTOR DESIGN:**

- Current density calculations
- Multiple pin paralleling
- Thermal management integration
- Contact resistance minimization

### **MECHANICAL CONSIDERATIONS:**

- Stress relief design
- Board edge reinforcement
- Connector keep-out zones
- Assembly accessibility requirements



# 14. DESIGN VERIFICATION

## 14.1 FINAL DESIGN VERIFICATION CHECKLIST

- [ ] DRC passes with zero violations
- [ ] Netlist verification against schematic
- [ ] Component placement review for assembly
- [ ] Thermal analysis for power dissipation
- [ ] Signal integrity simulation for critical nets
- [ ] Mechanical fit verification with enclosure
- [ ] Manufacturing file generation and review

## 14.2 MANUFACTURING DELIVERABLES

- Gerber files
- Excellon drill files
- Pick and place files
- Bill of materials with manufacturer part numbers
- Assembly drawings with component orientations
- Fabrication notes with special requirements

## 14.3 QUALITY METRICS

- First-pass manufacturing yield >95%
- Assembly time optimization
- Test coverage maximization
- Field failure rate minimization



# 15. PANELIZATION

Panelization combines multiple PCBs into a single manufacturing panel to optimize production efficiency, reduce costs, and improve handling during assembly processes.

## 15.1 PANELIZATION FUNDAMENTALS

### **DEFINITION AND PURPOSE:**

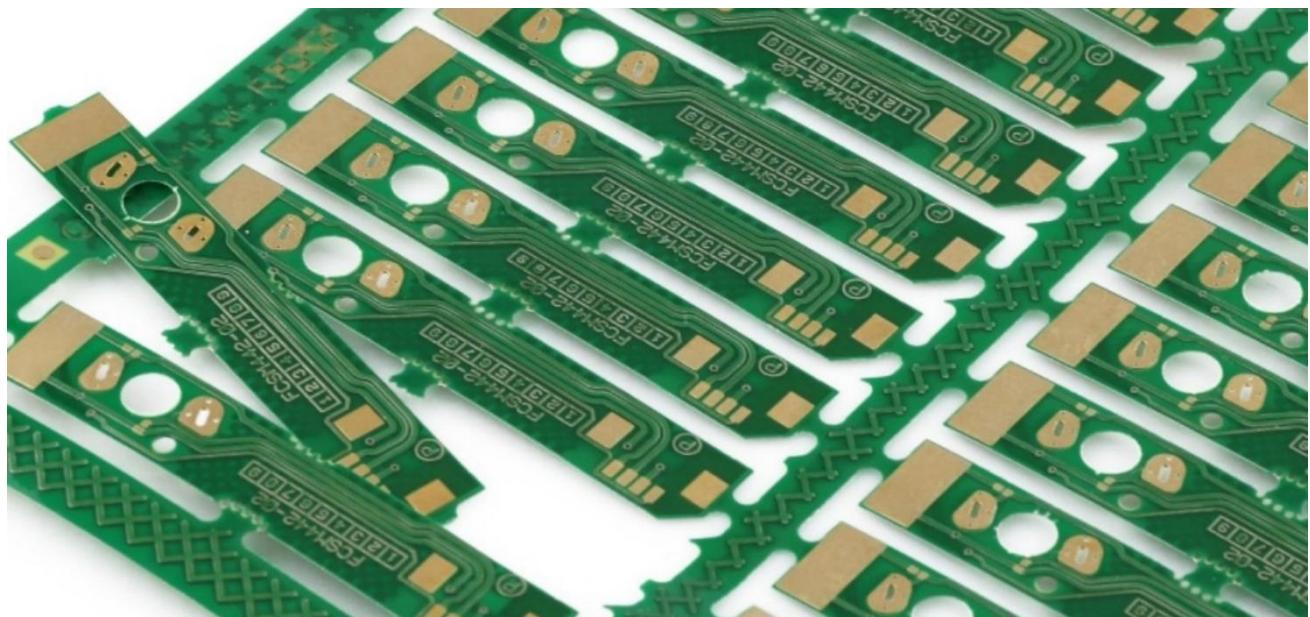
Panelization is the process of arranging multiple PCB copies on a single production panel for efficient manufacturing and assembly. This technique maximizes material utilization while maintaining manufacturability.

### **PRIMARY BENEFITS:**

- Cost reduction - Shared setup costs across multiple units
- Manufacturing efficiency - Batch processing advantages
- Handling improvement - larger panels easier to process
- Yield optimization - better material utilization ratios

### **STANDARD PANEL SIZES:**

PANEL SIZE	DIMENSIONS	TYPICAL APPLICATION
SMALL	50MM × 80MM	PROTOTYPE RUNS
MEDIUM	100MM × 80MM	PRODUCTION BATCHES
STANDARD	100MM × 160MM	HIGH-VOLUME MANUFACTURING
LARGE	160MM × 100MM	INDUSTRIAL APPLICATIONS



## 15.2 PANEL LAYOUT STRATEGIES

### **ARRAY CONFIGURATION:**

Strategic arrangement maximizes panel utilization:

Single Design Arrays:

- 1×2 arrangement - Simple doubling for small boards
- 2×2 configuration - Standard four-up panelization
- 3×3 layout - Nine-up for very small designs
- Custom arrays - Optimized for specific board dimensions

### **MIXED DESIGN PANELS:**

- Product family grouping - Related designs together
- Complementary sizing - Different boards filling panel space
- Test board inclusion - Quality control samples integrated

### **SPACING REQUIREMENTS:**

Critical clearances between boards:

- Minimum separation - 2.0mm between board edges
- Routing channels - 3.0mm for mechanical separation
- V-groove spacing - 0.5mm additional for scoring depth
- Tab connections - 1.5-3.0mm width depending on board thickness

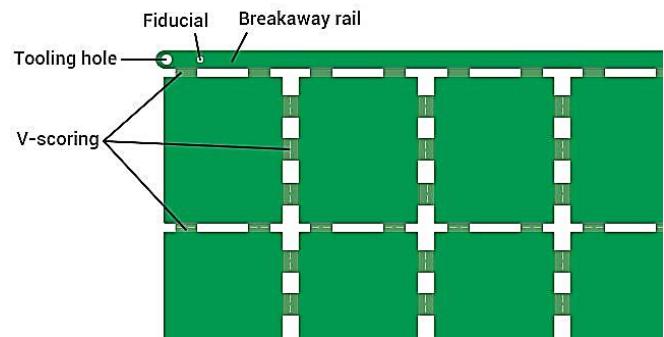
## 15.3 SEPARATION METHODS

### V-SCORING (V-GROOVE):

Most cost-effective separation method:

Design Requirements:

- **Straight line separation**
- **Optimal Board thickness** - 0.8-3.2mm
- **Minimum score depth** - 1/3 of board thickness
- **Edge distance** - Minimum 0.5mm from components



Advantages and Limitations:

- **Pros** - Low cost, clean separation, high-speed process
- **Cons** - Straight lines only, board stress during separation

### TAB ROUTING:

Flexible separation using small connecting tabs:

Tab Design Parameters:

- **Tab width** - 1.5-3.0mm typical
- **Tab thickness** - Full board thickness maintained
- **Tab quantity** - 3-6 tabs per board perimeter
- **Tab placement** - Avoid component areas and stress points

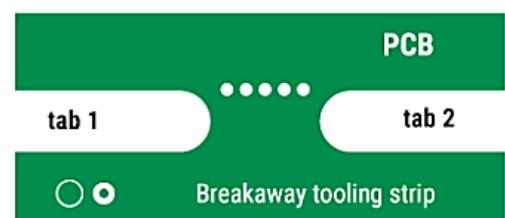
Tab Positioning Guidelines:

- **Corner placement** - Maximum structural support
- **Edge centering** - Balanced stress distribution
- **Component avoidance** - Minimum 2.0mm clearance
- **Stress relief** - Rounded tab connections preferred

### MOUSE BITES (PERFORATED TABS):

Alternative tab method using small drill holes:

- **Hole diameter** - 0.5mm typical
- **Hole spacing** - 0.5-1.0mm on centers
- **Perforation length** - 2-4mm typical
- **Break strength** - Easily separated by hand



## 15.4 ADVANCED PANELIZATION TECHNIQUES

### **FLEX-RIGID PANEL DESIGN:**

Special considerations for flexible circuits:

- **Stiffener coordination** - Support during assembly
- **Bend relief integration** - Stress management in panels
- **Separation planning** - Avoid damage to flex sections
- **Handling fixtures** - Custom tooling requirements

### **HDI PANELIZATION:**

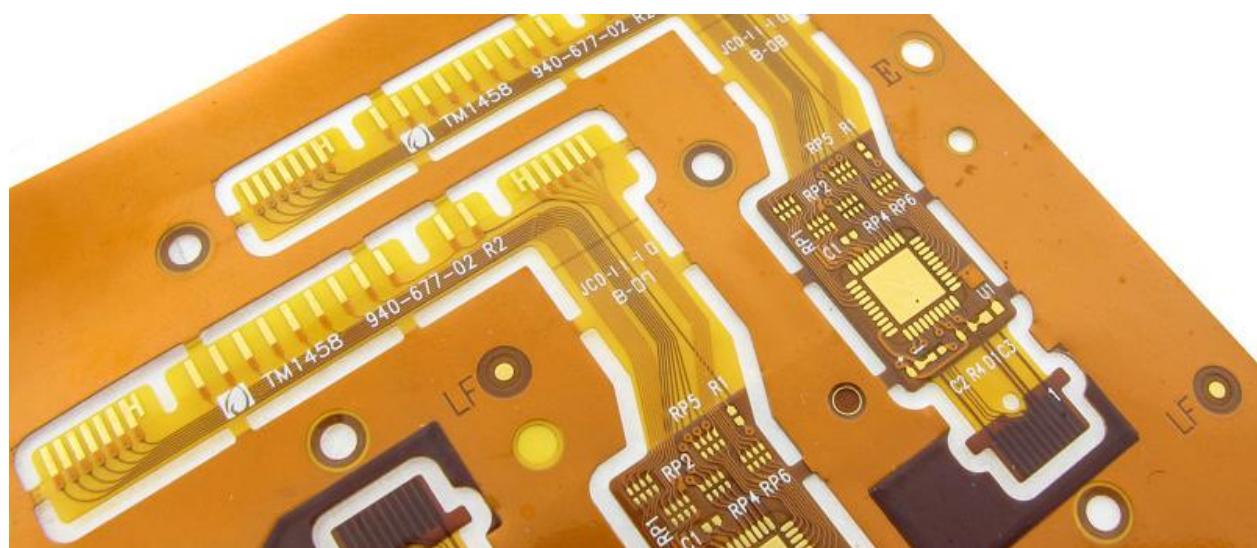
High Density Interconnect considerations:

- **Micro-via alignment** - Registration across panel
- **Sequential lamination** - Process step coordination
- **Yield optimization** - Defect isolation strategies
- **Test accessibility** - Probing considerations for dense designs

### **MIXED TECHNOLOGY PANELS:**

Combining different board types:

- **Thickness matching** - Assembly line compatibility
- **Material compatibility** - Thermal expansion coordination
- **Process optimization** - Shared manufacturing steps
- **Quality segregation** - Different test requirements



# 16.FREE ONLINE TOOLS

## SATURN PCB TOOLKIT

<https://saturnpcb.com/saturn-pcb-toolkit/>

Comprehensive freeware resource for PCB-related calculations including current capacity of traces, via current, differential pairs and much more.

## JLCPCB IMPEDANCE CALCULATOR

<https://jlcpbc.com/pcb-impedance-calculator>

Computes track width values and recommended stack-ups from user-input values of board layer, thickness, copper weight, target impedance, trace spacing, and impedance trace to copper gap.

## PCBWAY IMPEDANCE CALCULATOR

[https://www.pcbway.com/pcb\\_prototype/impedance\\_calculator.html](https://www.pcbway.com/pcb_prototype/impedance_calculator.html)

Calculate the approximate impedance of your PCB / high frequency circuit board

## PCBWAY TRACE WIDTH CALCULATOR

[https://www.pcbway.com/pcb\\_prototype/trace-width-calculator.html](https://www.pcbway.com/pcb_prototype/trace-width-calculator.html)

Based on formulas from IPC-2221, estimates the width of copper PCB boards and traces required under given current while maintaining temperature rise limits.

## SIERRA CIRCUITS PCB TOOLS SUITE

<https://www.protoexpress.com/tools/>

Comprehensive suite including impedance calculator using 2D numerical solution of Maxwell's equations, via calculators, power distribution analyzers, and signal integrity tools.

## ADVANCEDPCB TRACE WIDTH CALCULATOR

<https://www.advancedpcb.com/en-us/tools/trace-width-calculator/>

Find the ideal trace width for PCB designs, ensuring optimal performance and reliability in circuit boards.

# SUMMARY

Professional PCB design integrates electrical engineering principles with manufacturing realities. Success requires systematic approach from schematic analysis through manufacturing handoff.

## KEY SUCCESS FACTORS

- Thorough preparation and component selection
- Strategic layer planning and routing
- Manufacturing constraint consideration
- Comprehensive design verification
- Clear documentation and communication

## CONTINUOUS IMPROVEMENT

- Design review feedback incorporation
- Manufacturing yield optimization
- Assembly process refinement
- Field performance monitoring

## NEXT STEPS

- Apply these techniques to actual projects
- Develop design rule libraries for common applications
- Build relationships with manufacturing partners
- Stay current with evolving technologies and standards

Thank  
you!