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Design For Manufacturability

ASSEMBLY
selection, inspection, responses, levels, footprint, ground, sensitivity, modes, orientation, heat, protection, mod, pin, modes, timing, modes, simulation, digi-key, simulation, resistors, integrity, blocks, clock, mouse, depanelization, components, reflow, source, part, unit, electrical, handling, emi, corner, active, standards, capability, hand, circuits, panelization, signal, please, manufacturing, testing, placement, double-check, time, operating, sourcing, market, obsolescence.

Components
capacitors, floating, standard, yield, number, multi-sourcing, termination, environmental, distributor, place, reset, debug, assessment, logic, qfn, pick, functional, lead, mount, stencil, nodes, nmd, range, rrd, impedance, distribution, team, e-series, compatible, sink, fmea, types, temperature, thermal, safety, emc, parts.

POWER
component, failure, compliance, validation, trace, annotations, imone, integration, soldering, timer, package, supply, bom, standard, rework, esd, ipc, pcb, npi, reach, approved, inventory, surface, worst, rules, verification, prototype, naming, can, test, cases, and, matching, derating, interface, high, mixed, moisture, decoupling, digital, via, cost, management, schematic, analog, process, drawing, clearance, layout, vendor, drawing, swd, anal, via, rohs, lispice, overcurrent, carlo, reliability, risk, chair, uart.

By Shimi Cohen

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TIP 1 : Standard Components

1.1 THE E-SERIES STANDARDS

Component value standardization reduces inventory complexity and procurement risk.

Why This Matters:

Non-standard values increase lead times, minimum order quantities, and total cost of ownership.

Buyers maintain larger safety stock for standard values, ensuring availability during shortages.

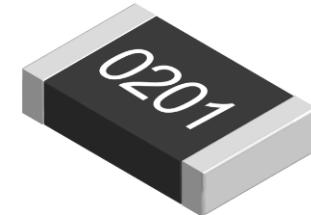
Resistor Accuracy Factors:

Parameters that Determine the accuracy

Factor	Effect on Accuracy	Notes
Manufacturing Process	Sets base precision	Metal/thin film → tighter control
Material Stability	Impacts long-term drift	Metal/foil resistors have low drift
Temperature Coefficient	resistance vs. temp.	Expressed in ppm/°C
Trim & Laser Calibration	Fine-tunes resistance	Tighter tolerances

Quick Tolerance Reference

Series	Tolerance	Typical Tech	Common Use
E6	±20%	Carbon composition	Power or non-critical loads
E12	±10%	Carbon film	General purpose
E24	±5%	Metal film	Most analog/digital designs
E48	±2%	Metal film / thin film	More precise analog
E96	±1% or better	Thin film / foil	Precision measurement



Series	Standard Values
E6 (±20%)	1.0, 1.5, 2.2, 3.3, 4.7, 6.8
E12 (±10%)	1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2
E24 (±5%)	1.00, 1.02, 1.05, 1.07, 1.10, 1.13, 1.15, 1.18, 1.21, 1.24, 1.27, 1.30, 1.33, 1.37, 1.40, 1.43, 1.47, 1.50, 1.54, 1.58, 1.62, 1.65, 1.69, 1.74
E48 (±2%)	1.00, 1.02, 1.05, 1.07, 1.10, 1.13, 1.15, 1.18, 1.21, 1.24, 1.27, 1.30, 1.33, 1.37, 1.40, 1.43, 1.47, 1.50, 1.54, 1.58, 1.62, 1.65, 1.69, 1.74, 1.78, 1.82, 1.87, 1.91, 1.96, 2.00, 2.05, 2.10, 2.15, 2.21, 2.26, 2.32, 2.37, 2.43, 2.49, 2.55, 2.61, 2.67, 2.74, 2.80, 2.87, 2.94, 3.01, 3.09
E96 (±1%)	1.00, 1.02, 1.05, 1.07, 1.10, 1.13, 1.15, 1.18, 1.21, 1.24, 1.27, 1.30, 1.33, 1.37, 1.40, 1.43, 1.47, 1.50, 1.54, 1.58, 1.62, 1.65, 1.69, 1.74, 1.78, 1.82, 1.87, 1.91, 1.96, 2.00, 2.05, 2.10, 2.15, 2.21, 2.26, 2.32, 2.37, 2.43, 2.49, 2.55, 2.61, 2.67, 2.74, 2.80, 2.87, 2.94, 3.01, 3.09, 3.16, 3.24, 3.32, 3.40, 3.48, 3.57, 3.65, 3.74, 3.83, 3.92, 4.02, 4.12, 4.22, 4.32, 4.42, 4.53, 4.64, 4.75, 4.87, 4.99, 5.11, 5.23, 5.36, 5.49, 5.62, 5.76, 5.90, 6.04, 6.19, 6.34, 6.49, 6.65, 6.81, 6.98, 7.15, 7.32, 7.50, 7.68, 7.87, 8.06, 8.25, 8.45, 8.66, 8.87, 9.09, 9.31, 9.53, 9.76

TIP 2 : Avoid Obsoletes/NRND

2.1 COMPONENT LIFECYCLE MANAGEMENT

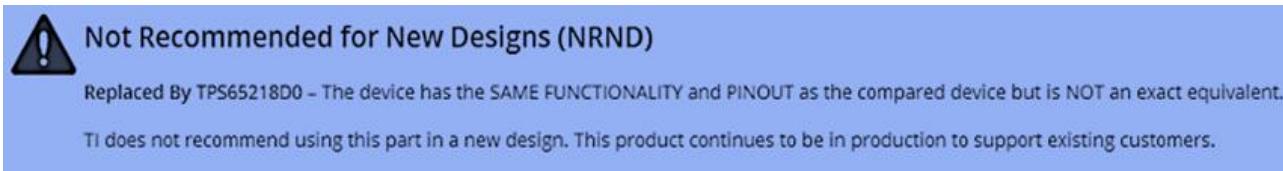
Single-source dependencies create supply chain fragility.

Why This Matters:

Component obsolescence forces expensive redesigns during production. Single-source parts give suppliers pricing power and eliminate fallback options during allocation.

Lifecycle Stages:

- Active: Full production, recommended for new designs
- NRND (Not Recommended for New Designs): Available but production ending
- Obsolete: Production ceased, last-time-buy only
- Allocated: Limited supply, requires factory authorization



2.2 MULTI-SOURCING STRATEGY

Critical Component Criteria:

- ICs with >\$5 unit cost
- Components with >6-month lead time
- Parts representing >10% of total BOM cost

Second-Source Requirements:

- Pin-compatible footprint and pinout
- Electrical specifications within ±10% of primary part
- Same communication protocol (SPI, I²C, etc.)
- Available from different manufacturer

Implementation:

1. Search parametric tables for alternates during initial selection
2. Design circuits with sufficient margin to accommodate alternate specs
3. Qualify second source during DVT phase
4. Document both manufacturers in approved vendor list (AVL)

2.3 OBSOLESCENCE MONITORING

Proactive Checks:

- Review manufacturer PCNs (Product Change Notifications) quarterly
- Subscribe to distributor lifecycle alerts (Digi-Key, Mouser, Arrow)
- Monitor lead times—sudden increases signal allocation risk



TIP 3 : Common Package Types

3.1 STANDARD PACKAGE SELECTION

Assembly equipment and process optimization favor standard footprints.

Why This Matters:

Exotic packages require custom stencils, specialized nozzles, and manual placement.

Standard packages leverage existing assembly line configuration, reducing NRE and improving yield.

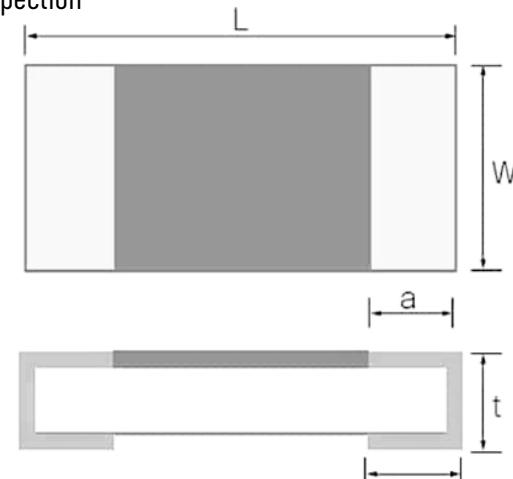
Recommended Passives:

- 0603 (1608 metric): Minimum size for automated placement
- 0805 (2012 metric): Best balance of cost and reliability
- 1206 (3216 metric): High-power resistors, polarized capacitors

Recommended ICs:

- SOIC-8/16: Wide availability, hand-solderable for rework
- TSSOP: Higher density, still compatible with standard equipment
- QFN: Thermal performance, use $\geq 0.5\text{mm}$ pitch
- BGA: High I/O count, use $\geq 0.8\text{mm}$ pitch, requires X-ray inspection

Code	Len. (mm)	Wid.(mm)	Power (W)
01005	0.4	0.2	1/40 (0.025)
0201	0.6	0.3	1/20 (0.05)
0402	1.0	0.5	1/16 (0.062)
0603	1.6	0.8	1/10 (0.10)
1005	2.0	1.25	1/8 (0.125)
1608	3.2	1.6	1/4 (0.25)
2012	3.2	2.5	1/2 (0.5)



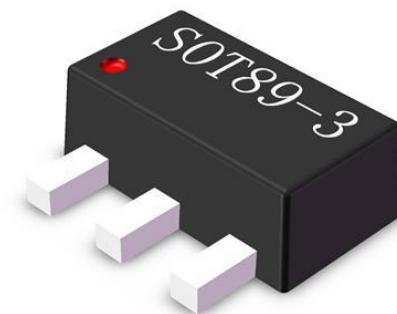
3.2 PACKAGE SELECTION CRITERIA

Avoid:

- Chip-scale packages (CSP) with $<0.4\text{mm}$ pitch
- Custom footprints requiring CAD library creation
- Packages with single-source assembly vendors
- Ultra-fine-pitch BGAs without design justification

When Specialty Packages Are Necessary:

- Consult CM (contract manufacturer) during part selection
- Verify equipment capability and yield history
- Allocate budget for custom tooling



TIP 4 : Complete BOM

4.1 BOM SYNCHRONIZATION

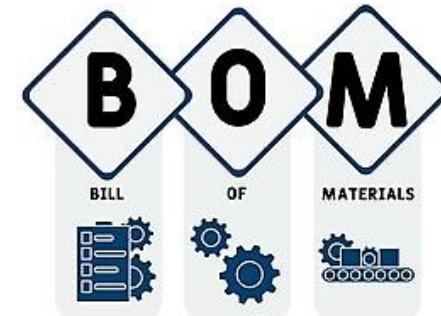
The bill of materials is the contract between engineering and manufacturing.

Why This Matters:

BOM errors cause production delays, incorrect parts procurement, and assembly rework. A single missing MPN can halt a production run.

Required BOM Fields:

- Reference Designator: Matches schematic annotation
- Manufacturer: Exact legal entity name
- Complete manufacturer part number
- Description: Functional description, not marketing copy
- Quantity: Per-board count, verified against schematic
- DNP Flag: Do-not-populate status with revision applicability



4.2 P/N SPEC BEST PRACTICES

Resistor Example (Incorrect):

- MPN: RC0805
- Problem: Missing resistance value, tolerance, power rating

Resistor Example (Correct):

- MPN: RC0805FR-0710KL
- Decodes to: 0805, 1%, 10kΩ, 0.125W

Capacitor Specification:

Must include voltage rating, dielectric type, and tolerance.

- MPN: GRM21BR61E106KA73L
- Decodes to: 0805, X5R, 10µF, 25V, ±10%

C	R	C	W	0	6	0	3	5	6	2	R	F	K	E	C		
MODEL			VALUE			TOLERANCE			TCR			PACKAGING			SPECIAL		
CRCW0402			R = Decimal			T = ± 1.0 %			K = ± 100 ppm/K			EA, EB,			Up to 2 digits		
CRCW0603			K = Thousand			J = ± 5.0 %			N = ± 200 ppm/K			EC, ED,					
CRCW0805			M = Million			Z = Jumper			O = Jumper			EE, EF,					
CRCW1206			0000 = Jumper									EG, EH,					
CRCW1210												EI, EL,					
CRCW1218												EK					
CRCW2010																	
CRCW2512																	

4.3 BOM VERIFICATION PROCESS

Pre-Release Checklist:

1. Run schematic → BOM export and compare line-by-line
2. Verify every MPN exists in distributor databases (Digi-Key, Mouser)
3. Confirm reference designators match PCB layout
4. Cross-check DNP components against assembly notes
5. Validate quantity field against schematic component count

TIP 5 : Panel Programming

5.1 PROGRAMMING ARCHITECTURE

In-panel programming reduces test time and improves throughput.

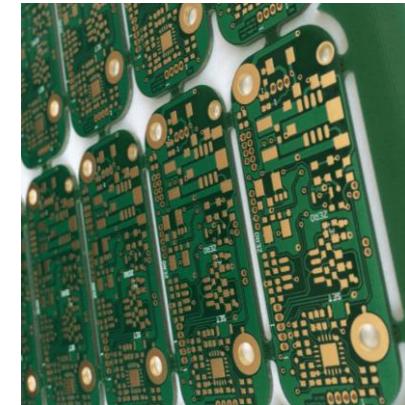
Why This Matters:

Depanelizing before programming requires handling individual boards, increasing touch time and breakage risk.

Panel programming enables simultaneous multi-board flashing.

Design Requirements:

- Dedicated programming connector on each board instance
- Test points accessible from panel top side
- Power input accepts panel-level voltage distribution
- No mechanical interference with panel rails or tooling holes



5.2 INTERFACE SELECTION

Recommended Interfaces:

- MCU programming: SWD (ARM Cortex), JTAG (general-purpose)
- Flash memory: SPI, I²C (for configuration data)
- FPGA: JTAG chain with boundary scan

Connector Strategy:

- Tag-Connect pogo-pin footprints: No installed connector, saves BOM cost
- 0.1" header: Install for prototypes, DNP for production
- Spring-loaded test points: Requires fixture but no board real estate

5.3 IMPLEMENTATION GUIDELINES

Power Considerations:

1. Programming interface draws 50–200mA during flash write
2. Design panel power distribution for N × programming current
3. Include bulk capacitance (100µF minimum) per board for current spikes

ARM 10-Pin Connector		ARM 20-Pin Connector	
VCC	1	2	SWDIO
GND	3	4	SWCLK
GND	5	6	SWO
N/U	7	8	N/U
GND	9	10	RESET
		VCC	1
		N/U	2
		N/U	4 GND
		N/U	6 GND
		SWDIO	7
		SWCLK	9
		SWO	11
		RESET	13
		NIC	15
		NIC	17
		NIC	19
		VCC (optional)	
		GND	

Signal Integrity:

- Use series termination (22–47Ω) on programming lines if panel trace >6 inches
- Include pull-up resistors on bidirectional programming signals
- Add ESD protection if programming connector exposed in final product

Tools:

- Gang programmers: BK Precision, Data I/O
- Fixture design: Spring-loaded pogo pins (Mill-Max, Harwin)

NPI Coordination:

Provide panel programming instructions including: voltage levels, baud rates, flash algorithms, and expected programming duration.

TIP 6 :Voltage Headroom

6.1 DERATING PHILOSOPHY

Operating components below maximum ratings extends reliability.

Why This Matters:

Components operated at maximum ratings experience accelerated aging. Voltage stress, temperature cycling, and manufacturing tolerances compound to cause premature failures.

Industry Standards:

- Military (MIL-HDBK-217): 50% voltage derating
- Commercial/Industrial: 20-30% voltage derating
- Consumer products: 10-20% voltage derating (minimum)



6.2 DERATING IMPLEMENTATION

Capacitor Voltage Selection:

Rail Voltage	Rated Voltage (20% Derate)	Rated Voltage (30% Derate)
3.3V	6.3V minimum	6.3V minimum
5V	10V minimum	10V minimum
12V	25V minimum	25V minimum
24V	50V minimum	50V minimum

Voltage Rail (V)	Rated Voltage of Cap (V)	
	Tantalum	OxiCap®
3.3	6.3	4
5	10	6.3
8	16	10
10	ca.	20
12	50 %	25
15	35	-
>24	Series Combination	-

Resistor Power Derating:

Semiconductor Voltage Margins:

- MOSFETs: V_{DS} rating $\geq 1.5 \times$ maximum applied voltage
- Diodes: PIV (peak inverse voltage) $\geq 1.3 \times$ maximum reverse voltage
- Voltage regulators: Input voltage rating $\geq 1.2 \times$ maximum supply

6.3 TOLERANCE STACKING

Input Voltage Range Analysis:

- Nominal input: $12V \pm 10\% = 10.8V$ to $13.2V$
- Transient overvoltage: Add 10% margin = $14.5V$ maximum
- Component selection: Choose $20V$ rated parts minimum

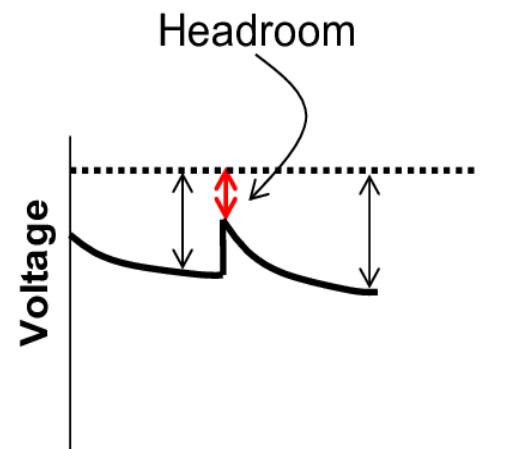
Temperature Impact:

Capacitor voltage derating must account for temperature coefficient.

X5R and X7R ceramics lose capacitance at temperature extremes.

Failure Modes:

- Under-voltage: Capacitor operates correctly
- Over-voltage: Dielectric breakdown
- Result: Always derate to prevent field failures



TIP 7 : Avoid Marginal Designs

7.1 TIMING MARGIN REQUIREMENTS

Digital circuits require setup and hold time margin for reliable operation.

Why This Matters:

Marginal timing creates intermittent failures that manifest only under specific conditions: temperature extremes, voltage sag, or component tolerance stacking.

Setup Time:

Data must be stable before clock edge. Minimum 20% margin above datasheet specification.

Hold Time:

Data must remain stable after clock edge. Minimum 20% margin above datasheet specification.

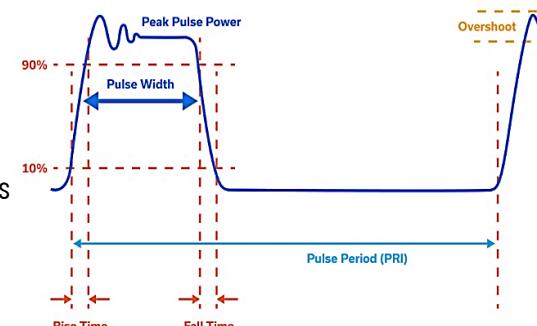
Propagation Delay:

Account for worst-case logic delays, trace delays, and clock skew.

7.2 TIMING BUDGET CALCULATION

Example: SPI Interface at 10 MHz

1. Clock period: 100ns
2. Master setup time required: 10ns (datasheet)
3. Trace delay: 2ns (estimated)
4. Design margin: $20\% \times (100\text{ns}) = 20\text{ns}$
5. Available data valid window: $100\text{ns} - 10\text{ns} - 2\text{ns} - 20\text{ns} = 68\text{ns}$



Margin Verification:

- Best case: Fast process, high voltage, cold temperature
- Worst case: Slow process, low voltage, hot temperature
- Design must meet timing in worst case with 20% additional margin

7.3 COMMON TIMING PITFALLS

Clock Domain Crossing:

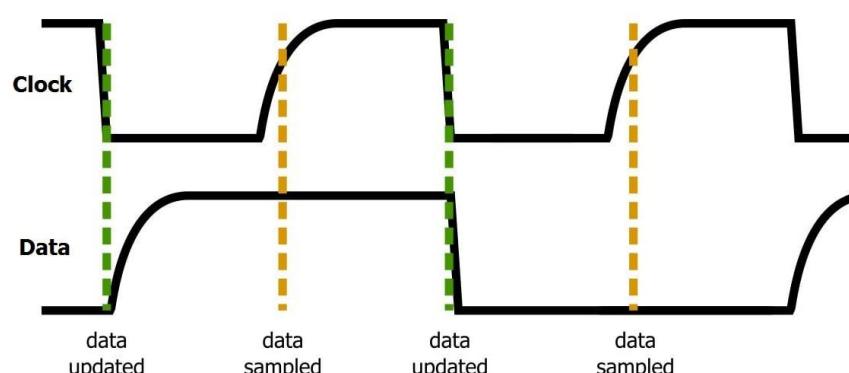
Use synchronizers (two flip-flop stages minimum) when crossing clock domains.

Metastability:

Occurs when setup/hold violated. Synchronizers reduce but don't eliminate risk.

Asynchronous Inputs:

External signals (buttons, sensors) must be synchronized to system clock.



TIP 8 : Match I/O Logic Levels

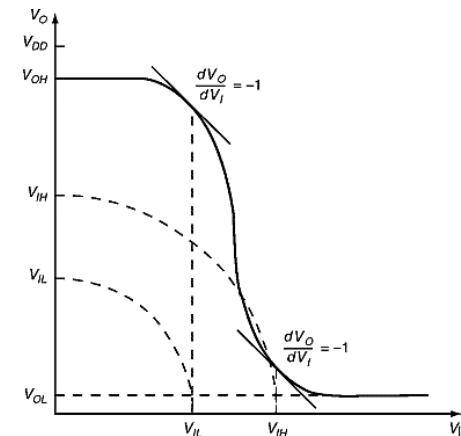
8.1 LOGIC LEVEL COMPATIBILITY

Interfacing devices with different logic levels requires careful analysis.

Why This Matters: Driving 3.3V logic with 5V output can cause latch-up or permanent damage. Insufficient voltage swing causes bit errors and intermittent communication failures.

Standard Logic Levels:

- 5V CMOS: $V_{IH} = 3.5V$, $V_{IL} = 1.5V$
- 3.3V CMOS: $V_{IH} = 2.0V$, $V_{IL} = 0.8V$
- 2.5V CMOS: $V_{IH} = 1.7V$, $V_{IL} = 0.7V$
- 1.8V CMOS: $V_{IH} = 1.17V$, $V_{IL} = 0.63V$



8.2 INTERFACE STRATEGIES

Direct Connection (Same Voltage):

Acceptable when both devices operate at identical voltage rails.

5V Tolerant Inputs:

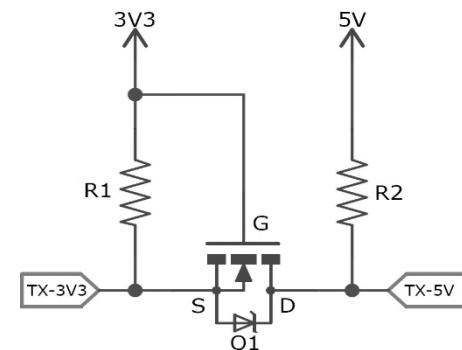
Many 3.3V devices accept 5V inputs. Verify datasheet "5V tolerant" specification explicitly.

Voltage Divider:

Simple resistive divider for unidirectional, low-speed signals only. Not suitable for bidirectional or high-speed interfaces.

Level Shifters:

Type	Directionality	Speed	Example IC
Unidirectional buffer	One-way	<100 MHz	74LVC1T45
Bidirectional buffer	Two-way	<100 MHz	TXS0108E
Open-drain	Two-way	<10 MHz	I ² C native



8.3 DESIGN GUIDELINES

I²C Buses:

Use pull-up resistors to lower voltage rail (typically 3.3V). Higher voltage devices must have 5V-tolerant I²C pins.

SPI Buses:

Requires level translation on MOSI, MISO, SCK, and CS lines. Use bidirectional or separate unidirectional buffers.

UART:

Straightforward level shifting on TX and RX lines. Flow control signals (RTS/CTS) also require translation.

Design Rule:

Never rely on clamping diodes for level shifting. This injects current into power rails and can cause latch-up.

Verification:

Measure signal levels with oscilloscope during initial power-on. Verify V_{IH} and V_{IL} margins meet datasheet requirements plus 20% margin.

TIP 9 : IC Solutions VS Discrete

9.1 INTEGRATION BENEFITS

Integrated circuits reduce part count and improve reliability.

Why This Matters:

Each additional component introduces failure modes, requires PCB real estate, increases assembly cost, and adds tolerance stacking complexity.

Integration Opportunities:

- Power management: Use PMICs (power management ICs) instead of discrete regulators
- Interface circuits: Integrated USB-to-UART bridges vs. discrete transistor level shifters
- Motor drivers: H-bridge ICs vs. discrete MOSFETs and gate drivers
- Amplifier chains: Instrumentation amplifier ICs vs. discrete op-amp networks

9.2 TRADE-OFF ANALYSIS

Discrete Advantages:

- Lower BOM cost for high-volume production
- Flexibility to optimize individual stages
- Easier to source during component shortages



Integrated Advantages:

- Reduced design complexity and validation time
- Smaller board footprint
- Matched components within IC (better temperature tracking)
- Lower assembly cost (fewer placements)

9.3 SELECTION STRATEGY

Use Integrated Solution When:

1. Production volume <50,000 units annually
2. Time-to-market critical (6-month design cycle)
3. Board space constrained
4. Thermal management benefits from fewer components
5. Reliability requirements favor reduced part count



Use Discrete Solution When:

1. Cost sensitivity extreme (consumer electronics)
2. Production volume >100,000 units annually
3. Custom performance requirements exceed available ICs
4. Supply chain requires multi-sourcing flexibility

Example:

LED Driver Comparison

Approach	Part Count	BOM Cost	Design Time
Discrete (MOSFET, resistors, PWM)	8	\$0.35	2 weeks
Integrated (LED driver IC)	1	\$0.75	2 days

TIP 10 : Reset and Watchdog Circuits

10.1 RESET CIRCUIT FUNDAMENTALS

Every processor-based system requires reliable reset generation to ensure deterministic startup.

Why This Matters:

Processors power-up in unknown states. Without proper reset, program counters point to random addresses, peripherals remain unconfigured, and systems exhibit unreliable behavior. Reset circuits guarantee clean initialization.

Reset Types:

- Power-on Reset (POR): Occurs when power first applied
- Manual Reset: User-initiated via button or command
- Brownout Reset: Triggered by supply voltage sag
- Watchdog Reset: Automatic recovery from software hang



Reset Timing Requirements:

- Minimum pulse width: 100ns to 10ms depending on device
- De-assert timing: Must wait for clocks and power to stabilize
- Setup time: Reset must be stable before first clock edge

10.2 RESET CIRCUIT TOPOLOGIES

RC Reset (Simple but Problematic):

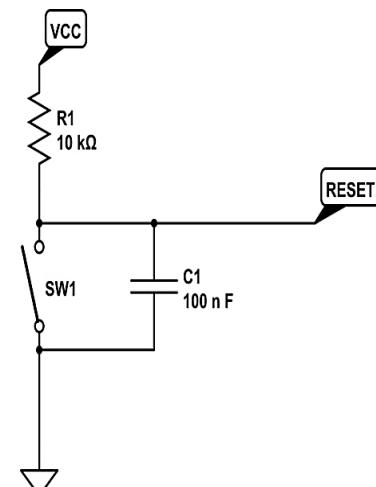
Basic RC network generates reset pulse during power-up.

Problems:

- Poor tolerance ($\pm 20\%$ timing variation)
- Sensitive to power supply ramp rate
- No brownout protection
- No manual reset capability

When acceptable:

- Cost-critical designs (<\$0.10 budget)
- Single-rail systems with fast power ramp
- Non-critical applications tolerating occasional bad startup

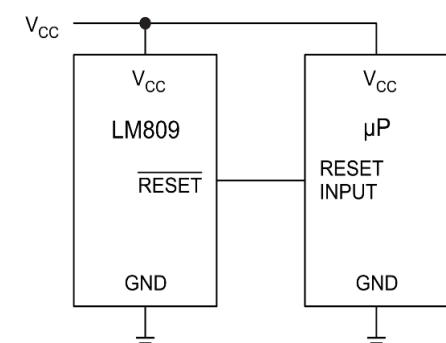


Dedicated Reset IC (Recommended):

Modern reset supervisors provide accurate, reliable reset generation.

Essential Features:

- Precise voltage threshold monitoring
- Guaranteed reset pulse duration
- Manual reset input
- Watchdog timer integration (optional)



10.3 WATCHDOG TIMER IMPLEMENTATION

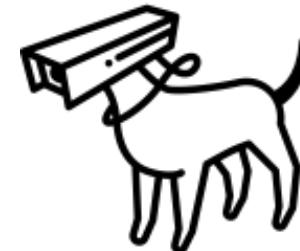
Watchdog timers automatically reset system when software fails to execute correctly.

Why This Matters:

Software hangs occur from infinite loops, corrupted stack pointers, and unexpected interrupts. Watchdog timers provide autonomous recovery without human intervention, critical for unattended or remote systems.

Operating Principle:

1. Software periodically "kicks" watchdog (writes to register)
2. Hardware timer counts down from preset value
3. If timer reaches zero: system reset triggered
4. Proper execution prevents timeout



Watchdog Timeout Selection:

Application Type Timeout Range Rationale

Fast control loops	10-100ms	Catch real-time failures quickly
General embedded	500ms-2s	Balance responsiveness vs. false triggers
Slow processes	5-60s	Allow long operations (flash writes)

MCU Watchdog:

Most modern MCU include integrated watchdog.

Advantages:

- No external components
- Fast response
- Integrated with sleep modes

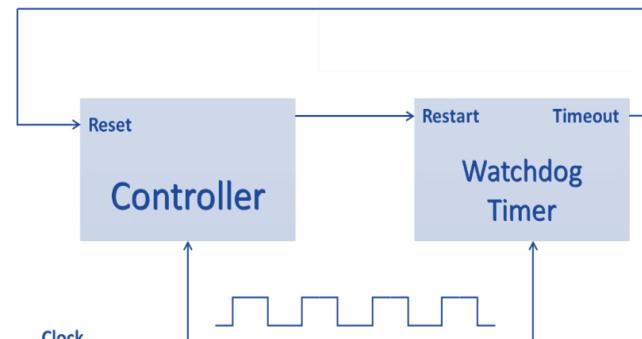
Limitations:

- Cannot detect clock failure
- Disabled by debugger
- Software can accidentally disable

Configuration example (typical):

```
// Enable watchdog with 1 second timeout
WDOG_Configure(TIMEOUT_1SEC, ENABLE);

// In main loop:
while(1){
    WDOG_Kick(); // Reset timer
    // Application code
}
```



TIP 11 : Include Interfaces

11.1 DEBUG INTERFACE REQUIREMENTS

Every processor-based design needs accessible debug and programming interfaces.

Why This Matters:

Debug ports enable firmware development, production programming, field diagnostics, and failure analysis. Omitting debug access forces expensive workarounds or redesigns.

Essential Interfaces:

- UART: Universal asynchronous serial for debug messages and console access
- SWD: Serial Wire Debug for ARM Cortex-M processors (2-wire: SWDIO, SWCLK)
- JTAG: Joint Test Action Group for complex processors and FPGAs (4-wire minimum)

11.2 INTERFACE IMPLEMENTATION

UART Configuration:

- Voltage levels: Match processor I/O voltage (typically 3.3V)
- Baud rate: Default to 115200 bps, support up to 921600 bps
- Connector: 0.1" header with GND, TX, RX pins minimum
- Protection: Series resistors (100Ω) for ESD protection



SWD Configuration:

- Pin assignment: SWDIO, SWCLK, GND, optional RESET
- Pull-up resistors: 10kΩ on SWDIO and SWCLK
- Connector: Tag-Connect TC2030 or 0.05" header
- Keep traces <3 inches to avoid signal integrity issues



JTAG Configuration:

- Pin assignment: TDI, TDO, TCK, TMS, GND, optional RESET and RTCK
- Pull-up resistors: 10kΩ on TDI, TMS, RESET
- Connector: Standard 20-pin 0.1" header (ARM standard)



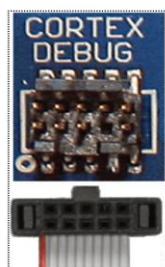
11.3 DESIGN GUIDELINES

Accessibility:

Position connectors on board edge or top surface. Avoid placing under mechanical assemblies or shields.

Production Use:

- Debug ports enable production testing without custom fixtures
- Boot mode selection: Use resistor straps or unpopulated jumpers
- Firmware version readback: Essential for traceability



10-pin JTAG/SWD Connector

VCC	1	□ □	2 SDWIO / TMS
GND	3	□ □	4 SWDCLK / TCLK
GND	5	□ □	6 SWO / TDO
KEY	7	□	8 NC / TDI
GNDDetect	9	□ □	10 nRESET

TIP 12 : Connector Placement

12.1 CONNECTOR TYPE SELECTION

Board-to-Board Connectors:

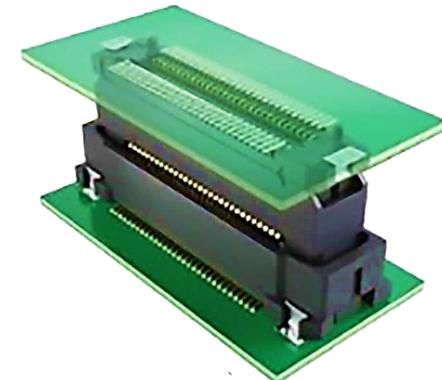
Stack-Height Connectors Used for parallel PCB mounting.

Common types:

- 0.1" (2.54mm) header: General purpose, hand-solderable
- High-density (0.5-1.27mm pitch): Space constrained applications
- Mezzanine: Robust mechanical retention, 6-20mm stack height

Selection guidelines:

- Use keyed connectors to prevent reverse insertion
- Specify gold plating for signal contacts (minimum 30 μ " flash)
- Verify maximum current per row (internal pins derate)



Recommended series:

Application	Series	Pitch	Current/Pin
General I/O	Samtec SSQ/ESQ	2.54mm	3A
High-speed	Samtec Razor Beam	0.635mm	1A
Power + signal	Molex MicroFit	3.0mm	5A

Wire-to-Board Connectors:

Crimp-Style Connectors - Industry standard for field-replaceable connections.

Popular families:

- Molex MiniFit Jr: 3.0mm pitch, 2-24 circuits, 13A per circuit
- JST XH: 2.5mm pitch, 2-16 circuits, 3A per circuit
- Phoenix Contact: Pluggable terminal blocks, 15A typical

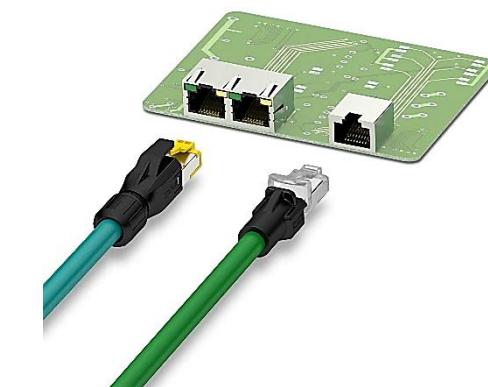


Design considerations:

- Specify housing color for voltage coding (red=power, black=GND, white=signal)
- Provide strain relief via housing retention or cable clamp
- Use polarized housings to prevent miswiring

Crimp vs. IDC:

- Crimp: More reliable, production-friendly, requires tooling
- IDC: Lower setup cost, suitable for prototypes, <100 units



I/O Connectors:

USB, Ethernet, HDMI, etc.

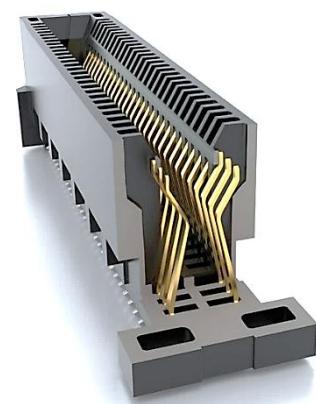
Design requirements:

- Use connectors with datasheets specifying retention force
- Verify PCB thickness compatibility (1.6mm standard)
- Include mounting holes for mechanical support on high-insertion-force connectors

12.2 CONTACT PLATING AND MATERIALS

Plating Options:

Plating	Applications	Durability
Tin	Low-cost, general purpose	10-100 cycles
Gold flash (30μ")	Signal contacts	100-500 cycles
Gold (50μ")	High-reliability	500-1,000 cycles
Palladium-nickel	High-temperature, harsh environments	1,000+ cycles



Application Guidelines:

Power contacts:

- Tin plating acceptable for high-current contacts
- Larger contact area compensates for higher resistance
- Verify temperature rise at maximum current

Signal contacts:

- Gold plating required for low-level signals (<1V, <100mA)
- Prevents oxide formation causing high resistance
- Critical for analog, high-impedance circuits

Harsh environments:

- Consider sealed/IP-rated connectors
- Use palladium-nickel or gold over nickel plating
- Specify conformal coating compatible with mating cycles



12.3 MECHANICAL PLACEMENT STRATEGY

Orientation Rules:

1. Face all connectors outward toward board edges
2. Avoid placing connectors under components requiring rework access
3. Maintain >0.25" clearance from adjacent tall components
4. Position keying features visible to operator

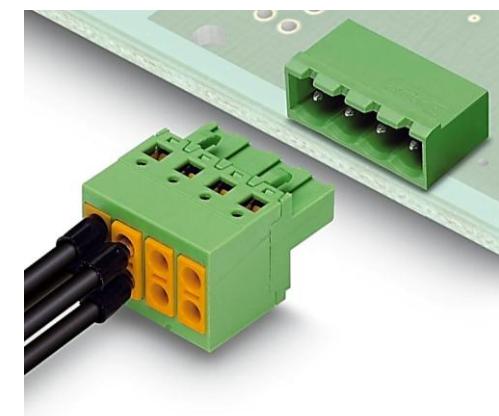
Panel Assembly:

- Ensure connector clearance from panel rails and tooling holes
- Verify mating cable/connector can access all panel positions

Stress Relief and Retention:

Through-hole vs. SMT:

Mounting	Advantages	When to Use
Through-hole	Mechanical strength	Pull force, I/O connectors
SMT	Lower assembly cost	Board-to-Board, low-stress
Hybrid	Best of both	High-reliability SMT



Retention Features:

- Use connectors with positive locking (latches, screws)
- Add mounting holes adjacent to large connectors
- Specify housing standoff height matching PCB thickness
- Consider adhesive or epoxy for potting in vibration environments

TIP 13 : Avoid Floating Nodes

13.1 FLOATING NODE HAZARDS

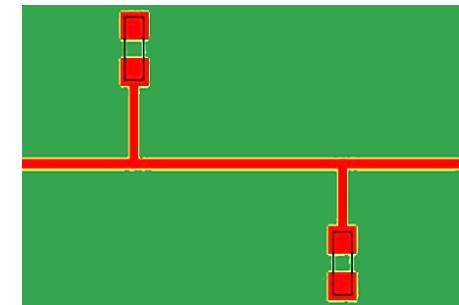
Unconnected pins and unterminated signals create unpredictable behavior.

Why This Matters:

Floating nodes act as antennas, picking up electromagnetic interference. Logic inputs float to intermediate voltages, causing excessive current draw and erratic operation.

Common Floating Node Sources:

- Unused IC inputs
- Disabled interface signals
- Optional features left unconnected
- Test points with no pull-up/pull-down



13.2 TERMINATION STRATEGY

Digital Logic Inputs:

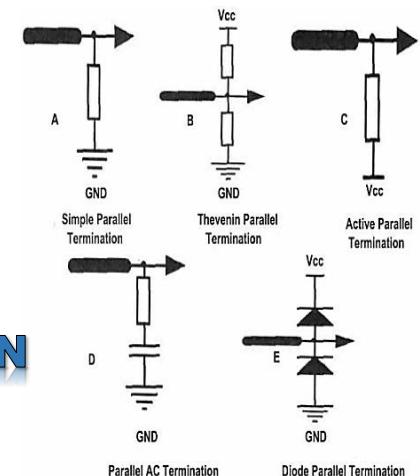
- CMOS inputs: Tie unused inputs to GND or V_{CC} via 10kΩ resistor
- TTL inputs: Tie unused inputs to V_{CC} via 1kΩ resistor (current sourcing)
- Never leave floating: Even unused inputs draw current when floating

Analog Inputs:

- Unused op-amp inputs: Tie to mid-rail or ground depending on application
- Unused ADC channels: Connect to GND via 100kΩ resistor
- Comparator inputs: Always terminate to defined voltage

Bidirectional I/O:

- GPIO pins: Configure as output driving low, or input with pull-down
- I²C/SPI unused chip selects: Pull high (de-selected state)
- Tri-state buses: Use keeper circuits or weak pull-ups



13.3 INTERFACE-SPECIFIC TERMINATION

USB Data Lines:

USB ports require termination per USB specification.

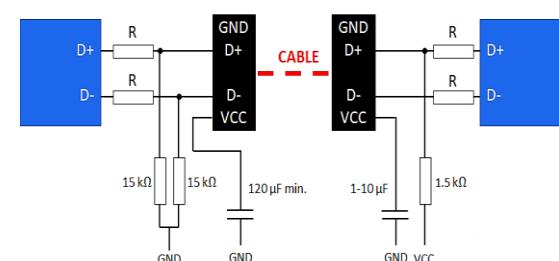
- USB 2.0: 15kΩ pull-down on D+ and D-
- USB device: Pull-up on D+ or D- indicates speed

Ethernet:

Ethernet pairs require 75Ω termination to chassis ground via 0.01μF cap.

LVDS Interfaces:

Unused LVDS receivers require 100Ω differential termination.



TIP 14 : Use Simulation

14.1 SIMULATION BENEFITS

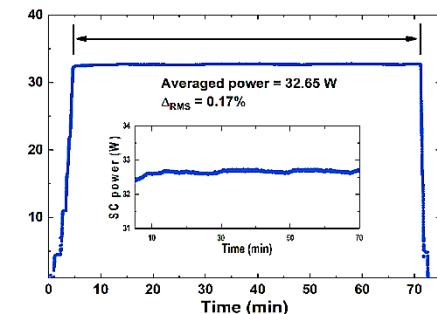
SPICE simulation catches design flaws before hardware fabrication.

Why This Matters:

Simulation identifies issues in hours rather than weeks, compressing development schedules and reducing NRE.

Simulation Capabilities:

- AC frequency response
- Transient analysis (time domain)
- Parameter sweeps and sensitivity analysis
- Worst-case simulation



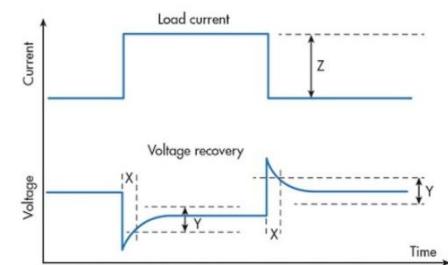
14.2 CIRCUIT SIMULATION

Power Supply Design:

- Stability analysis: Phase and gain margin in control loop
- Load transient response: Output voltage regulation during current steps
- Startup behavior: Inrush current and soft-start sequencing

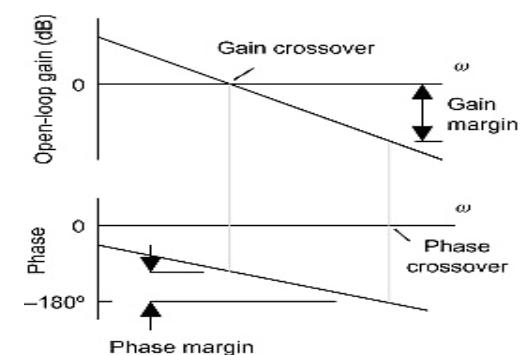
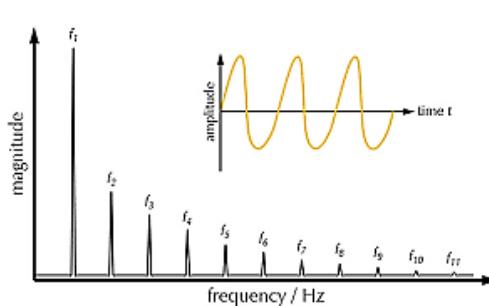
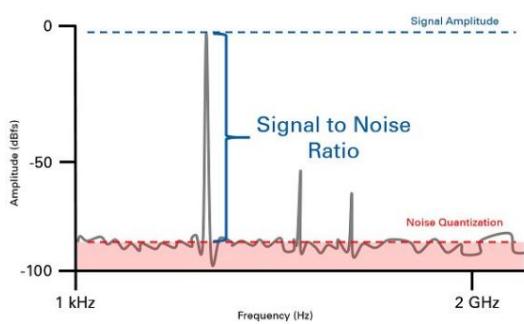
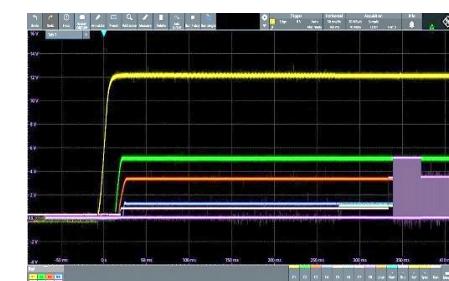
Analog Signal Chains:

- Gain and phase accuracy across frequency range
- Total harmonic distortion (THD) at maximum signal level
- Noise analysis and SNR calculation



High-Speed Digital:

- Signal integrity: Rise time, overshoot, ringing
- Impedance matching and reflections
- Setup and hold time verification



14.3 SIMULATION TOOLS



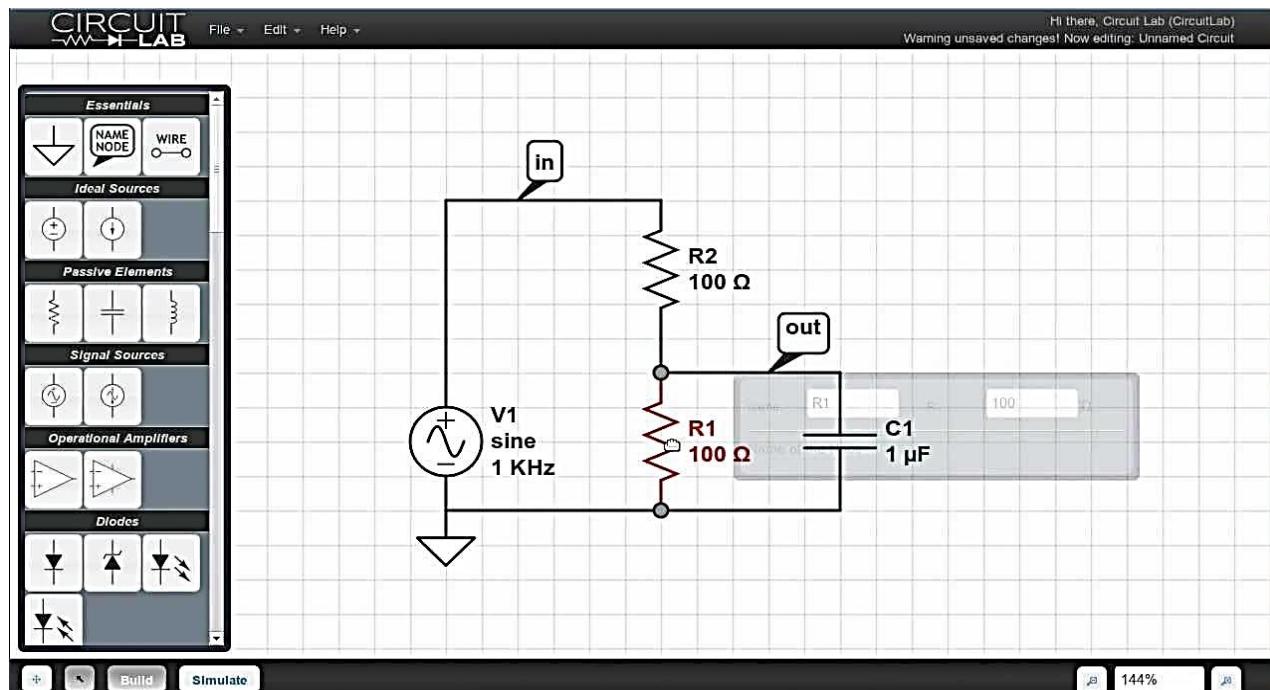
Free/Low-Cost Tools:

- LTspice: Industry-standard, extensive component library
- TINA-TI: Texas Instruments specific, includes reference designs
- Micro-Cap: Full-featured, free for up to 50 components
- CircuitLab: Advanced Design, easy to use.



Professional Tools:

- Cadence PSpice: Industry standard with advanced analysis
- Keysight ADS: RF and high-speed digital emphasis
- ANSYS HFSS: Electromagnetic simulation for complex structures



14.4 SIMULATION WORKFLOW

Component Models:

1. Use manufacturer SPICE models when available (most accurate)
2. Use generic models for initial architecture exploration
3. Validate critical paths with manufacturer models before release

Analysis Sequence:

1. DC analysis: Verify bias points and quiescent currents
2. AC analysis: Verify frequency response meets requirements
3. Transient analysis: Verify time-domain behavior under realistic signals
4. Sensitivity analysis: Identify critical component tolerances

Validation:

Simulate all analog circuits and switched-mode power supplies before prototyping. Digital circuits require simulation only for high-speed interfaces (>50 MHz).

TIP 15 : Preliminary Testing

15.1 PRE-CERTIFICATION PLANNING

Design decisions impact regulatory testing outcomes and certification timelines.

Why This Matters:

Test failures discovered during formal certification require expensive redesigns and delay product launch. Planning for test requirements during design phase prevents costly surprises.

Common Test Standards:

Safety Standards

- IEC 61010-1 (Measurement, Control, and Lab Equipment)
- UL/CSA equivalents as applicable
- Focus: creepage/clearance, isolation, protective grounding, fusing.

EMC / EMI Compliance

- IEC / EN 61000-6-x (Generic EMC standards)
- CISPR 32 / EN 55032 (Emissions for multimedia equipment)
- CISPR 24 / EN 55024 (Immunity)
- FCC Part 15 (for U.S. markets)
- Focus: layout for emissions control, shielding, grounding, filtering.

Environmental & Material Compliance

- RoHS (Restriction of Hazardous Substances)
- REACH (Substance registration & restriction)
- WEEE (Waste / recycling marking)
- Focus: component sourcing, labeling, documentation.

Electrical & Power Interface

- IEC 60950 / IEC 62368 (for external power inputs)
- IEC 60335 (if household appliance context)
- Focus: connector safety, inrush, fuses, protective earth.

Wireless & Connectivity (if relevant)

- ETSI EN 300 328 / FCC Part 15 Subpart C (Wi-Fi/Bluetooth)
- EN 301 489 (EMC for RF devices)
- Focus: antenna placement, ground plane isolation, coexistence.



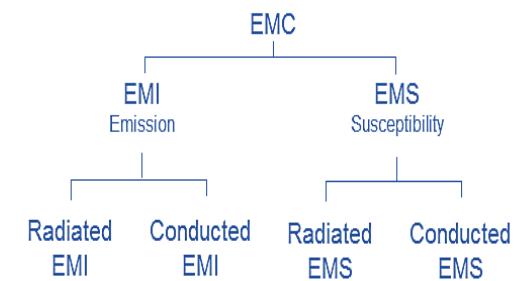
15.2 DESIGN FOR EMC COMPLIANCE

Emissions Reduction:

- Clock frequency selection: Avoid frequencies near regulatory limits (e.g., FM radio band)
- Spread-spectrum clocking: Reduces peak emissions by 10-15 dB
- Ferrite beads: Place on high-speed signals at board edge
- Decoupling capacitors: Use 0.1µF close to IC power pins

Immunity Enhancement:

- ESD protection: TVS diodes on all external interfaces
- Input filtering: Common-mode chokes on power and data lines
- Chassis grounding: Low-impedance connection to enclosure



15.3 SAFETY DESIGN CONSIDERATIONS

Spacing Requirements:

Primary to secondary isolation requires minimum creepage and clearance distances per voltage rating.

Voltage (AC/DC) Creepage Distance Clearance Distance

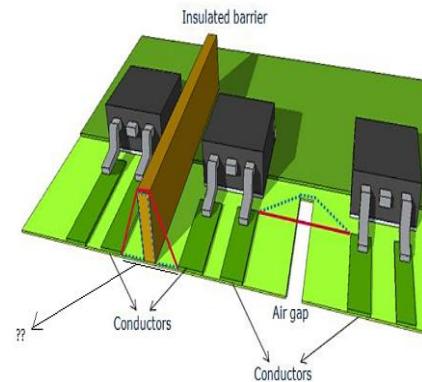
50V	0.5mm	0.4mm
150V	1.5mm	1.0mm
300V	3.2mm	2.0mm

Component Selection:

- Use safety-rated capacitors (X/Y rated) across isolation barriers
- Select transformers with UL/VDE approval for isolation applications
- Specify appropriate insulation rating for wiring and PCB material

Protective Features:

- Overcurrent protection: Fuses or electronic current limiting
- Overvoltage protection: MOVs or TVS diodes on AC inputs
- Thermal protection: Thermal fuses or temperature monitoring



15.4 TEST PREPARATION CHECKLIST

Before Prototype:

1. Review applicable standards for target markets
2. Design in protection circuits and filtering
3. Allocate board space for EMC components (may add during debug)
4. Select components with appropriate safety certifications

During Development:

1. Perform pre-compliance testing with near-field probes
2. Identify emission hotspots and iteration solutions
3. Validate protection circuits with ESD simulator
4. Document test results and design changes

Before Certification:

1. Complete internal testing to verify likely pass
2. Prepare test documentation and technical files
3. Select accredited test lab
4. Budget 2-4 weeks for formal testing plus 1-2 weeks for failures

Tools:

- Pre-compliance testing: Tekbox TBOH01 near-field probe set
- ESD simulation: Noiseken ESS-2000, Keytek MiniZap
- Design guides: TI EMI Troubleshooting Cookbook, Analog Devices EMI/EMC Design Guide

TIP 16 : Consistent Naming

16.1 NAMING CONVENTION BENEFITS

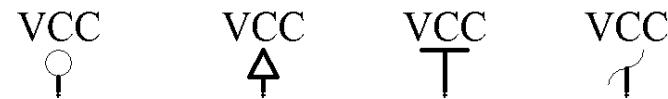
Standardized net names improve schematic readability and reduce design errors.

Why This Matters:

Inconsistent naming causes confusion during design reviews, complicates troubleshooting, and increases risk of connecting incompatible voltage domains.

Voltage Net Examples:

- VCC_IN: System Input Voltage
- VCC_3V3: Main 3.3V supply
- VCCA_5V: 5V analog supply
- VCC_1V8: 1.8V processor core supply
- GND: Ground (single ground net preferred)
- AGND: Analog ground (only if isolated from digital ground)



16.2 IMPLEMENTATION GUIDELINES

Voltage Designation:

- Use decimal notation with V separator: 3V3, 5V0, 12V0
- Avoid ambiguous names like VDD, VCC without voltage (legacy designs)
- Include voltage even if single rail to maintain consistency

Domain Specification:

Add functional suffix when multiple rails at same voltage exist:

- VCC_3V3_IO: I/O supply
- VCC_3V3_CORE: Core logic supply
- VCC_3V3_PHY: Physical layer interface supply



Ground Naming:

- Prefer single GND net for most designs
- Use AGND only when analog ground truly isolated with single-point connection
- PGND: Power ground for high-current paths (optional, document connection to GND)

16.3 DOCUMENTATION REQUIREMENTS

Schematic Title Block:

Include power rail summary listing all supplies with voltage range and maximum current.

Net Class Definition:

Assign power nets to appropriate classes for layout tool.

Net Name	Voltage	Max Current	Trace Width Min
VCC_12V	12V ±5%	2.5A	20 mil
VCC_5V	5V ±5%	1.0A	15 mil
VCC_3V3	3.3V ±3%	500mA	10 mil

TIP 17 : Functional Blocks

17.1 HIERARCHICAL SCHEMATIC

Hierarchical design with clear functional boundaries improves maintainability.

Why This Matters:

Well-organized diagrams accelerate design reviews, simplify troubleshooting, and enable design reuse. Poor organization causes errors and extends development time.

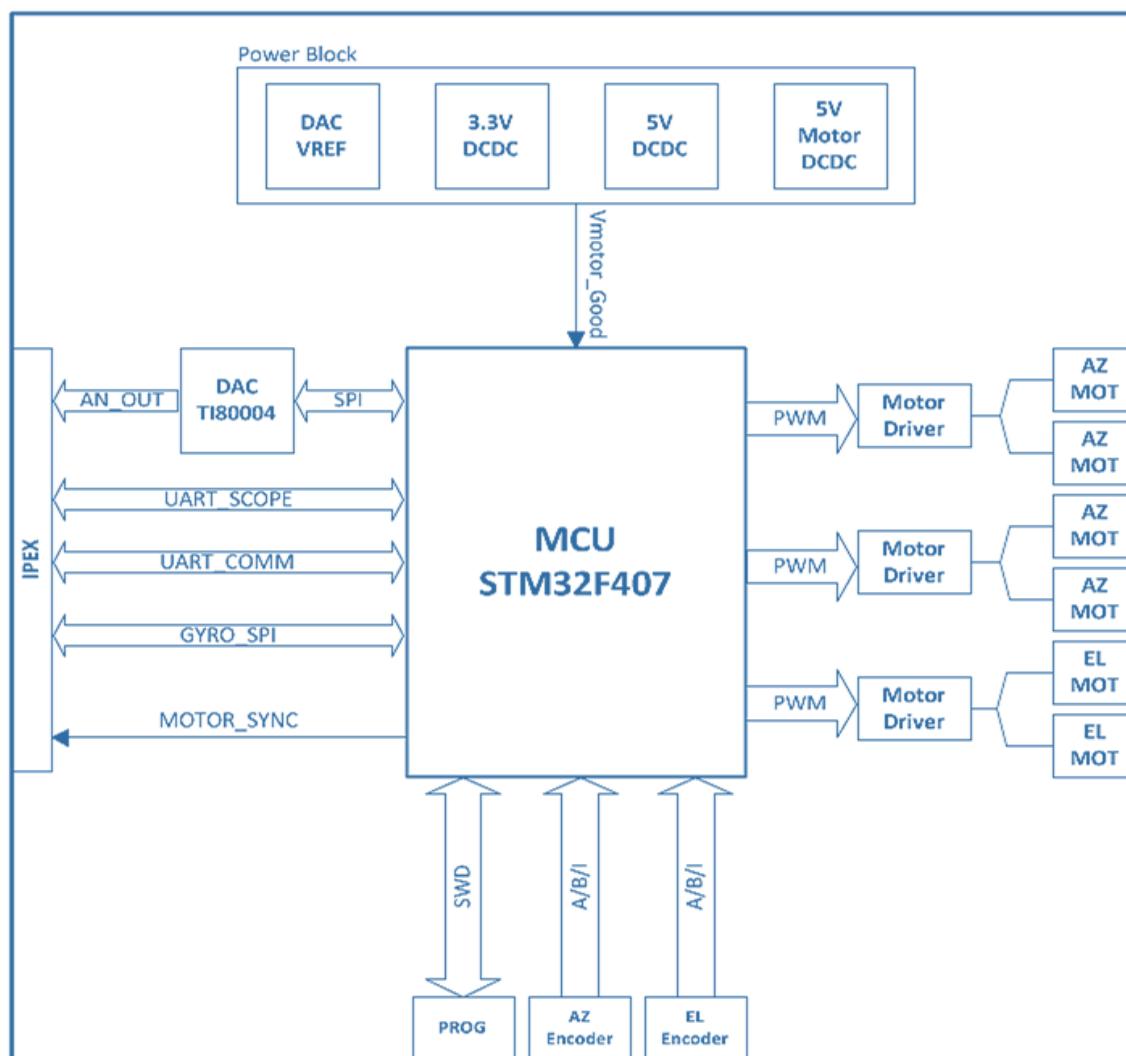
Hierarchical Structure:

- Top-level: Block diagram showing major functional units
- Second-level: Detailed schematics for each functional block
- Third-level: Complex sub-circuits warranting separate sheets

Functional Block Categories:

- Power supply: All regulators and power distribution
- Processor core: CPU, memory, clock generation
- Communication interfaces: UART, SPI, I²C, Ethernet, USB
- Analog front-end: Sensors, signal conditioning, ADC
- Output drivers: Relays, motor drivers, high-current switches

Simplifying Diagram:



17.2 POWER DIAGRAMS

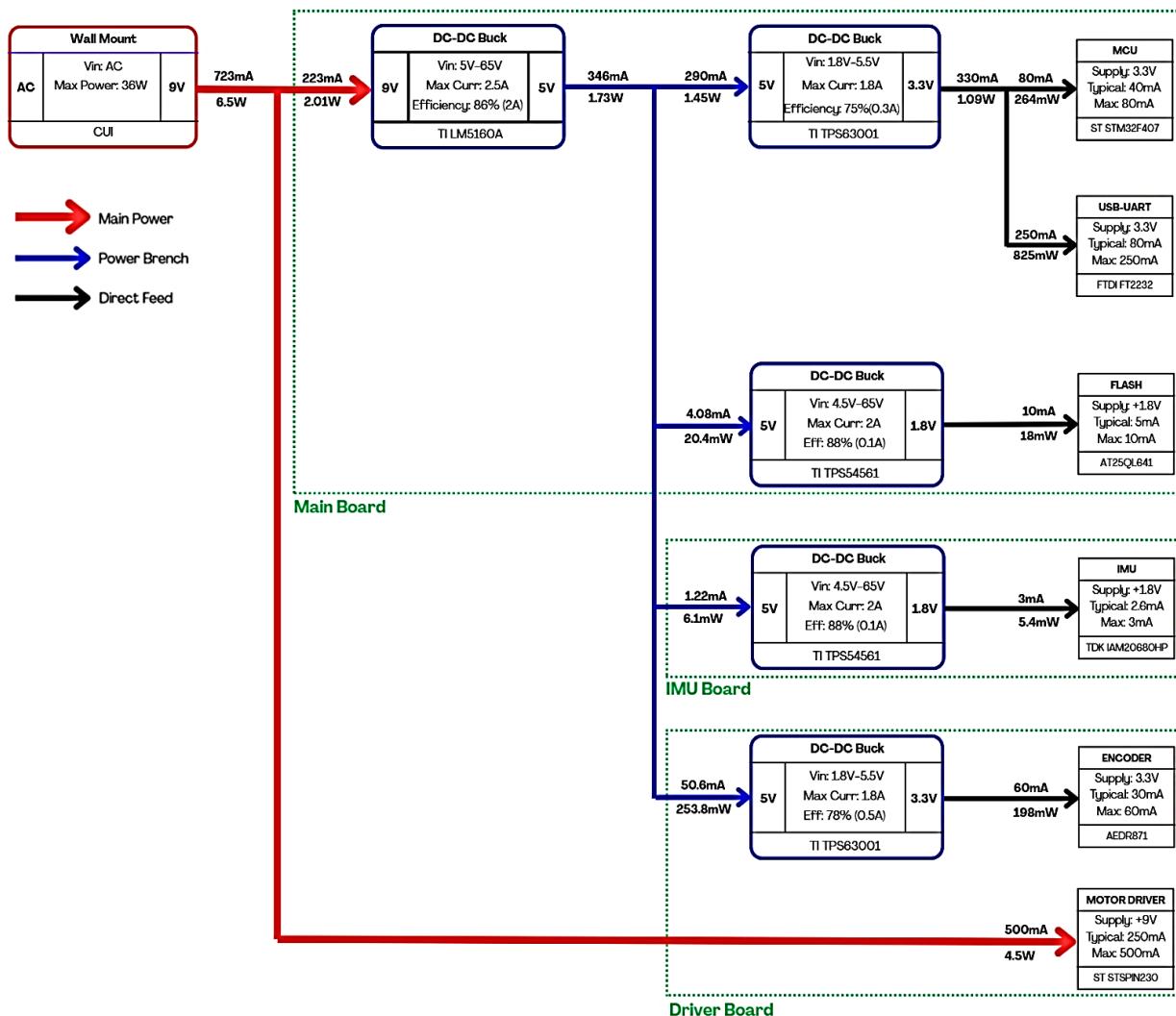
Defines how all voltage rails, regulators, and domains connect within the system.

It's a key DFM artifact – bridging schematic intent, layout strategy, and test planning.

A clear power diagram ensures consistent voltage hierarchy, simplifies review, and prevents costly re-spins.

Why Power Diagrams Matter (DFM Perspective)

- Clarifies voltage hierarchy and regulation order.
- Enables current flow validation early in design.
- Reduces risk of cross-domain shorts or miswiring.
- Guides PCB layer stack and copper thickness choices.
- Improves test coverage for power sequencing and monitoring.



17.3 ANNOTATION AND COMMENTS

Required Annotations:

- Test points: Label with signal name and expected voltage/waveform
- Configuration options: Document resistor straps and jumper settings
- Critical timing: Note setup/hold requirements at interface boundaries
- Power consumption: Indicate current draw for each block

Comment Blocks:

Include on each schematic sheet:

- Sheet purpose and function
- Key specifications (voltage, current, frequency)
- Special design considerations
- Reference to relevant datasheet sections

17.4 DESIGN REVIEW FACILITATION

Review Checklist:

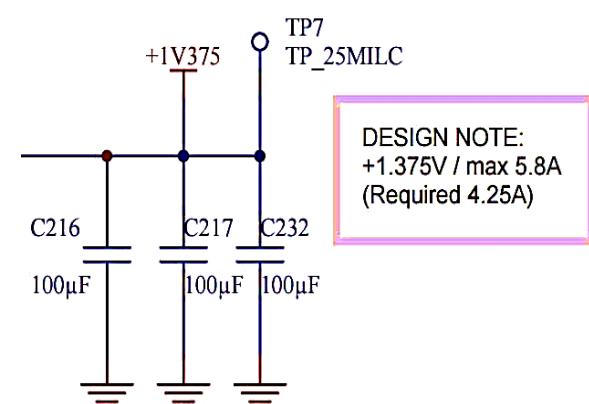
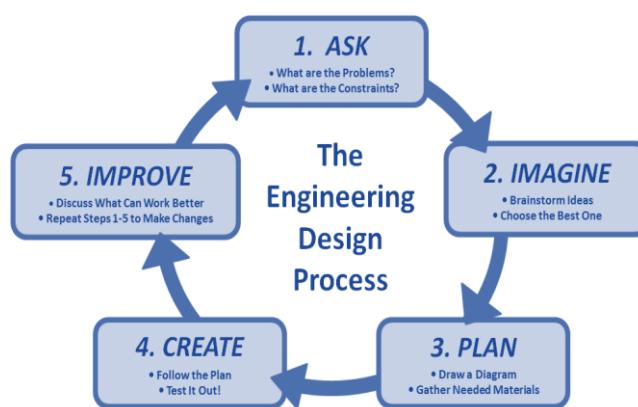
1. Each functional block clearly defined and labeled
2. Signal flow logical and easy to follow
3. Inter-sheet connections clearly marked
4. All components have reference designators
5. Critical signals annotated with specifications

Tools:

- Altium: Room-based design with folder structure
- KiCad: Hierarchical sheets with inheritance
- OrCAD: Multi-sheet design with global symbols

Design Rule:

Schematic should be understandable by engineer unfamiliar with design within 30 minutes. If review requires constant clarification, organization needs improvement.



TIP 18 : Monte Carlo Analysis

18.1 STATISTICAL ANALYSIS REQUIREMENTS

Monte Carlo simulation evaluates circuit performance across component tolerance distributions.

Why This Matters:

Worst-case analysis assumes all components simultaneously at extreme values—statistically unlikely. Monte Carlo provides realistic yield prediction and identifies critical tolerances.

Analysis Types:

- Worst-case: All components at tolerance extremes (pessimistic)
- RSS (root sum square): Statistical combination assuming normal distribution
- Monte Carlo: Random sampling from tolerance distributions (most accurate)

When to Run Monte Carlo:

- Analog circuits with multiple tolerance contributors
- Precision measurement circuits
- Circuits with tight output specifications
- High-volume production (>10,000 units) where yield matters

18.2 SIMULATION SETUP

Component Tolerance Specification:

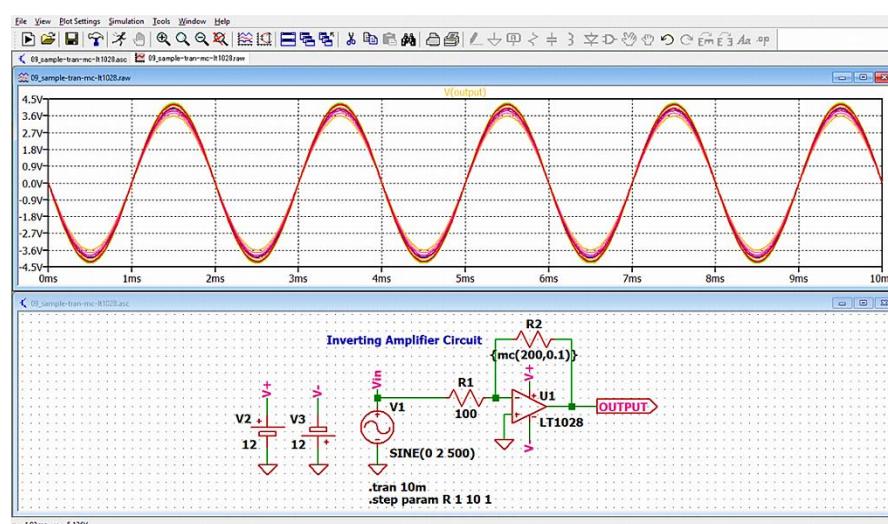
- Resistors: $\pm 1\%$, $\pm 5\%$ per E-series selection
- Capacitors: $\pm 5\%$, $\pm 10\%$, $\pm 20\%$ plus voltage and temperature coefficients
- Transistors: hFE variations, VBE spread
- Op-amps: Input offset voltage, bias current

Distribution Types:

- Gaussian (normal): Most components follow this distribution
- Uniform: Conservative assumption when distribution unknown
- Truncated Gaussian: Gaussian limited to $\pm 3\sigma$ (realistic manufacturing)

Sample Size:

- 1,000 iterations minimum for initial analysis
- 10,000 iterations for accurate yield prediction
- More samples improve confidence but increase simulation time



18.3 RESULTS INTERPRETATION

Yield Calculation: Percentage of simulation runs meeting all specifications.

- Target: $\geq 99.7\%$ yield (3σ process capability)
- Acceptable: 99% yield with screening or adjustment
- Unacceptable: $< 95\%$ yield indicates redesign needed

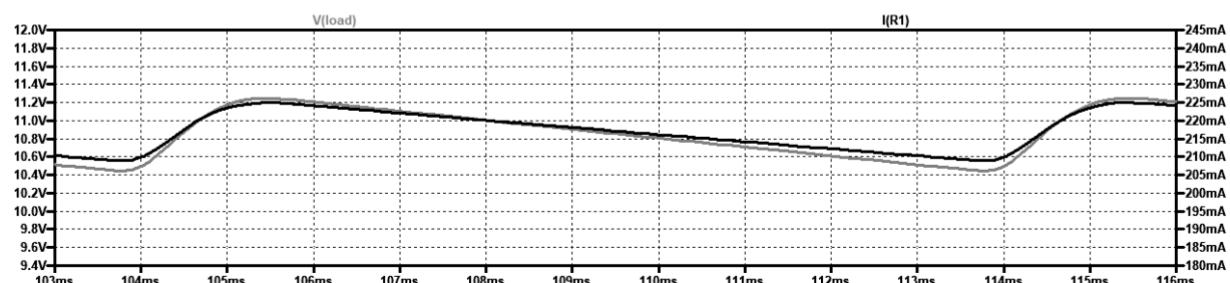
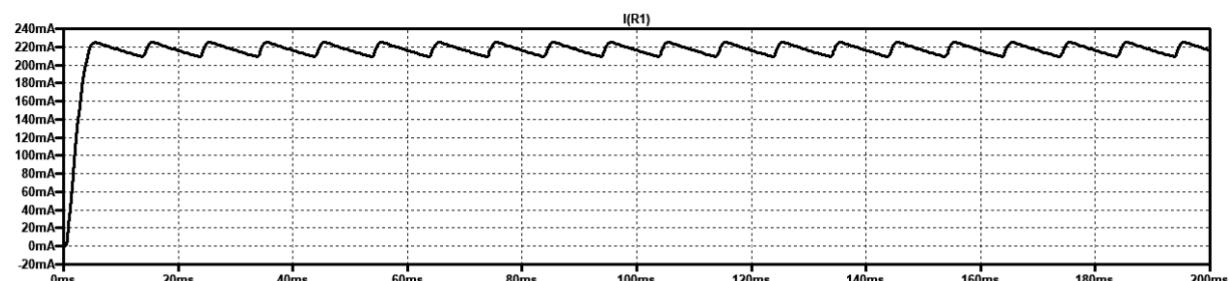
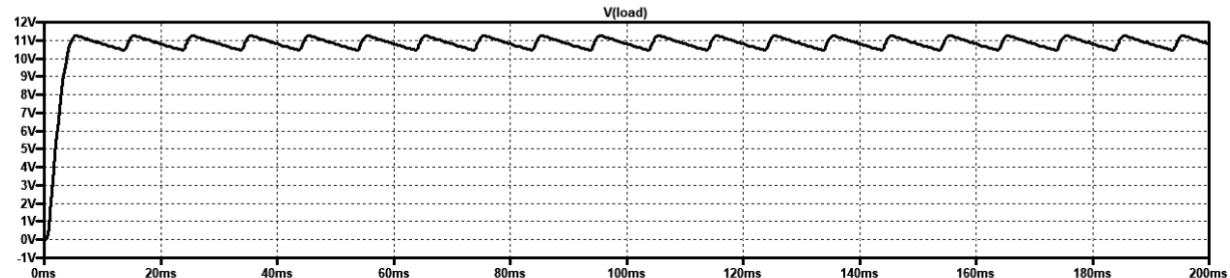
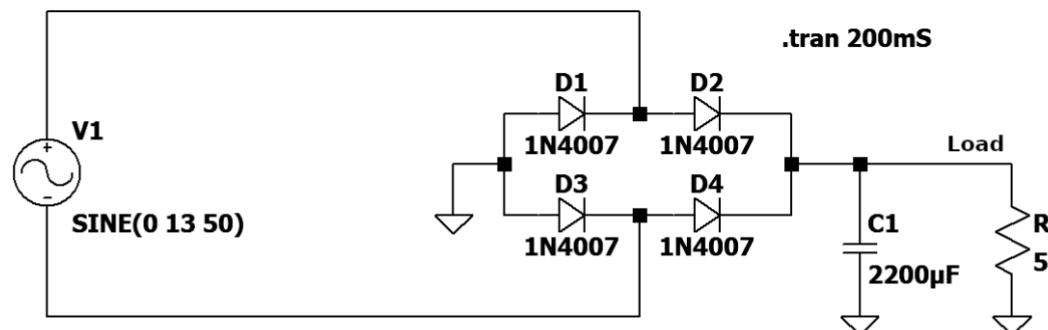
Sensitivity Analysis: Identify which component tolerances contribute most to output variation.

- Focus tightening tolerance specifications on high-sensitivity components
- Relaxing non-critical tolerances reduces BOM cost

Example Results:

Circuit Parameter Nominal 3σ Spread Yield

Gain	10.0 V/V	± 0.8 V/V	99.5%
Offset	0 mV	± 15 mV	98.2%
Bandwidth	100 kHz	± 12 kHz	99.9%



18.4 DESIGN OPTIMIZATION

Iterative Process:

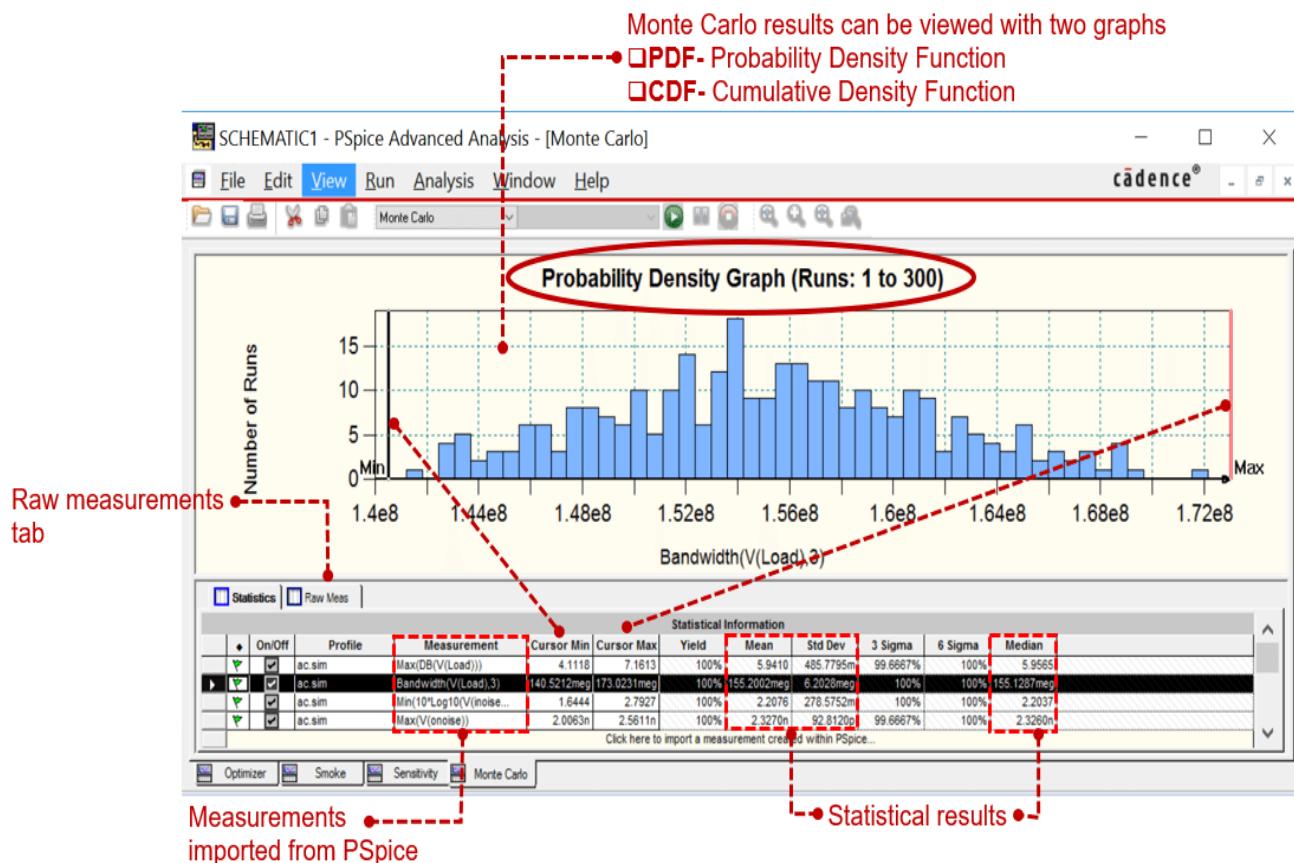
1. Run initial Monte Carlo with standard tolerances
2. Identify yield limiters from sensitivity analysis
3. Tighten critical component tolerances or add adjustment capability
4. Re-run simulation to verify improved yield

Adjustment Options:

- Trimming: Adjustable components or parameters calibrated during production
- Selection: Measure and bin components, use matched sets
- Calibration: Software correction using stored calibration constants

Tools:

- LTspice: Built-in Monte Carlo with .step param command
- TINA-TI: Monte Carlo analysis with statistical reporting
- Python + PySpice: Custom Monte Carlo with advanced statistics



TIP 19 : FMEA and DFM Checks

19.1 DFM REVIEW PROCESS

Design Stage Reviews:

- Concept: Architecture and component selection
- Schematic: Circuit implementation and interfaces
- Pre-layout: Component placement strategy
- Pre-release: Final verification against DFM checklist

Review Participants:

- Design engineer: Circuit functionality and specifications
- Manufacturing engineer: Assembly and test considerations
- Quality engineer: Reliability and failure analysis
- Supply chain: Component availability and cost



19.2 FAILURE MODE AND EFFECTS ANALYSIS

FMEA systematically identifies potential failure modes and their impact.

Why This Matters:

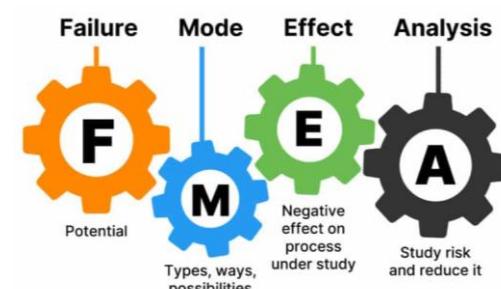
Catching failure modes during design costs hours of engineering time. Discovering failures in production costs thousands per incident. Field failures cost reputation and customer relationships.

FMEA Process:

1. List all components and subsystems
2. Identify potential failure modes for each
3. Assess severity, occurrence probability, and detection difficulty
4. Calculate risk priority number
5. Prioritize mitigation efforts on highest RPN items

Common Failure Modes:

- Open circuits: Resistor failure, connector disconnect
- Short circuits: Capacitor breakdown, solder bridges
- Parametric drift: Component aging, temperature effects
- Stuck-at faults: Digital logic failures
- Intermittent faults: Cold joints, vibration-induced opens



Process Step/Input	Potential Failure Mode	Potential Failure Effects	SEVERITY	Potential Causes	OCCURRENCE	Current Controls	DETECTION	RPN	Action Recommended	Resp.	Actions Taken	SEVERITY	OCCURRENCE	DETECTION	RPN
									What controls and procedures exist that prevent the cause or the Failure Mode?	What are the actions for reducing the occurrence of the cause or improving detection?	What are the completed action taken with the recalculated RPN?				
What is the process step and input under investigation?	In what ways does the Key Input go wrong?	What is the impact on the Key Output Variables (Customer Requirements)?													

19.3 DFM CHECKLIST CATEGORIES

Component Selection:

- All components active lifecycle status
- Dual-source availability verified
- Package types compatible with assembly equipment
- Lead times <12 weeks for all components

Circuit Design:

- Adequate voltage and current margins
- Protection circuits on all external interfaces
- Debug access and test points included
- Firmware update mechanism implemented

Documentation:

- BOM complete and accurate
- Schematic organized and annotated
- Assembly notes clear and complete
- Test specifications defined



19.4 RISK MITIGATION STRATEGIES

Design Redundancy:

- Parallel components for critical functions (increased reliability)
- Watchdog timers for processor lockup recovery
- Redundant power supplies for high-availability systems

Protection Circuits:

- Overvoltage: Zener diodes, TVS diodes, MOVs
- Overcurrent: Fuses, electronic current limiting, PPTC devices
- ESD: TVS diodes on external interfaces
- Reverse polarity: Series diode or MOSFET protection

Fault Detection:

- Built-in self-test (BIST) at power-on
- Continuous monitoring of critical parameters
- Error logging for failure analysis

RPN Range Priority Action Required

1-50	Low	Monitor, no immediate action
51-100	Medium	Mitigation recommended
101-200	High	Mitigation required before release
>200	Critical	Redesign necessary

Severity Probability	1	2	3	4	5
1	Low	Low	Low	Low	Moderate
2	Low	Low	Low	Moderate	High
3	Low	Low	Moderate	Moderate	High
4	Low	Moderate	Moderate	High	Unacceptable
5	Moderate	Moderate	High	Unacceptable	Unacceptable

Tools:

- FMEA software: ReliaSoft XFMEA, IQS FMEA
- Checklists: IPC-2221/2222 design standards
- Review templates: Company-specific design review forms

TIP 20 : Involve NPI Team

20.1 EARLY NPI ENGAGEMENT

New Product Introduction (NPI) engineers optimize designs for manufacturing.

Why This Matters:

Manufacturing challenges discovered late require expensive ECOs (engineering change orders). Early NPI involvement catches issues during design phase when changes cost hours, not weeks.

NPI Team Expertise:

- Assembly process capabilities and limitations
- Test fixture and programming requirements
- Component handling and moisture sensitivity
- Manufacturing yield optimization

Engagement Timeline:

- Concept phase: Review architecture and component strategy
- Schematic phase: Validate component selection and test approach
- Pre-prototype: Review assembly documentation and test plan
- Post-prototype: Participate in build review and PFMEA



20.2 DESIGN FOR ASSEMBLY (DFA)

Component Orientation:

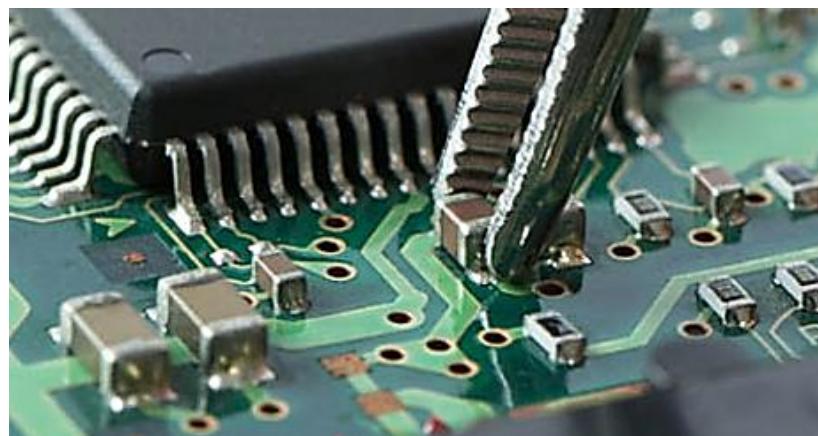
- Align polarized components in consistent direction
- Orient ICs with pin 1 indicators toward same corner
- Place connectors on board edges when possible

Component Spacing:

- Minimum 0.5mm between adjacent components
- Clearance for pick-and-place nozzles and inspection cameras
- Access to test points without obstruction

Tooling Considerations:

- Panel design: Allow fiducials and tooling holes per CM requirements
- Support locations: Prevent board flexing during assembly
- Depanelization: V-score or routed tabs with break-away design



20.4 MANUFACTURING DOCUMENTATION

Assembly Drawings:

- Component placement views with reference designators
- Polarity indicators and orientation marks
- Special handling instructions (ESD sensitive, press-fit connectors)

Test Procedures:

- Step-by-step functional test sequence
- Expected measurements and pass/fail criteria
- Troubleshooting guide for common failures

Work Instructions:

- Panel programming procedure with hex file location
- Calibration procedure with adjustment points
- Final inspection checklist

NPI Handoff Package:

1. Complete schematic and BOM
2. Assembly drawings and work instructions
3. Test specifications and procedures
4. Firmware with version control
5. Known issues and work-arounds
6. Yield targets and acceptance criteria



Appendix A: Tools

DESIGN TOOLS

Schematic Capture:

- Altium Designer: Professional, comprehensive
- KiCad: Open-source, community support
- OrCAD Capture: Industry standard, enterprise

Simulation:

- LTspice: Free, extensive model library
- TINA-TI: Texas Instruments specific
- Cadence PSpice: Professional analysis

Component Search:

- Octopart: Parametric search, lifecycle data
- Digi-Key: Large inventory, excellent filters
- Mouser: Alternative sourcing, good stock



REFERENCE MATERIALS

Design Standards:

- IPC-2221: Generic PCB design standard
- MIL-HDBK-217: Reliability prediction
- IEC 60950-1: Safety of IT equipment

Application Notes:

- Texas Instruments: Power, analog, embedded
- Analog Devices: Precision analog design
- Infineon: Power electronics, automotive
- " by Marty Brown

INDUSTRY ORGANIZATIONS

Standards Bodies:

- IPC: PCB design and assembly standards
- IEEE: Electrical engineering standards
- UL: Safety certification

Professional Development:

- IPC training and certification programs
- IEEE conferences and publications
- Local engineering society chapters

Appendix B: Glossary

- AOI:** Automated Optical Inspection - visual inspection using cameras and image processing
- AVL:** Approved Vendor List - qualified suppliers for components
- BOM:** Bill of Materials - complete list of components and quantities
- CM:** Contract Manufacturer - external company providing manufacturing services
- DFA:** Design for Assembly - optimizing design for manufacturing processes
- DFM:** Design for Manufacturing - broader term including assembly, test, and cost
- DNP:** Do Not Populate - components on BOM but not installed in certain configurations
- DVT:** Design Verification Test - prototype testing phase before production
- ECO:** Engineering Change Order - formal design modification process
- EMC:** Electromagnetic Compatibility - emissions and immunity requirements
- EMI:** Electromagnetic Interference - unwanted electromagnetic emissions
- ESD:** Electrostatic Discharge - static electricity discharge causing component damage
- FMEA:** Failure Mode and Effects Analysis - systematic reliability assessment
- MOQ:** Minimum Order Quantity - smallest purchase quantity from supplier
- MPN:** Manufacturer Part Number - unique identifier for specific component
- NPI:** New Product Introduction - process of transitioning design to production
- NRND:** Not Recommended for New Designs - component approaching end-of-life
- PCN:** Product Change Notification - manufacturer notice of component changes
- PFMEA:** Process Failure Mode and Effects Analysis - manufacturing process risk assessment
- PMIC:** Power Management IC - integrated voltage regulation and sequencing
- RPN:** Risk Priority Number - FMEA metric combining severity, occurrence, and detection
- TVS:** Transient Voltage Suppressor - protection device for voltage spikes