

# POWER DESIGN



By Bargunan Ponnusamy

# 1. POWER FUNDAMENTALS

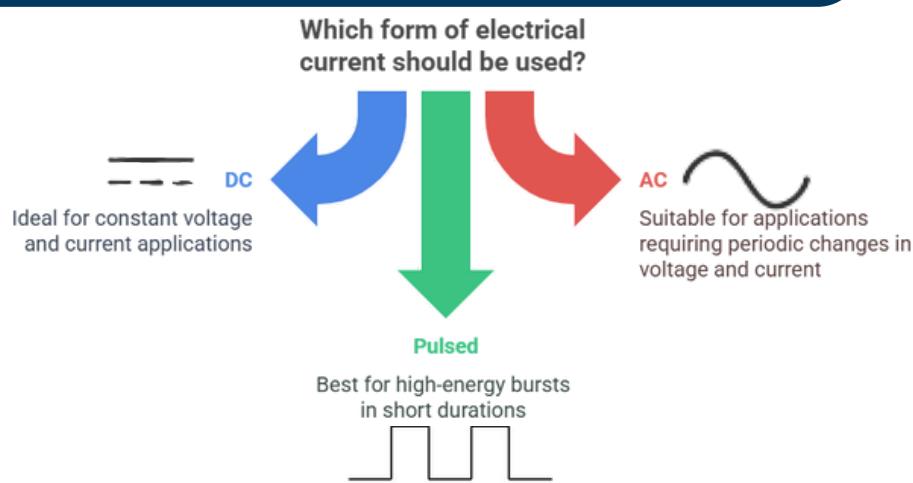
## What is a Power Supply?

A power supply is an essential component in electronic devices that converts incoming electrical power into the appropriate voltage, current, and frequency needed by the device. As you begin your journey in power supply design, it's crucial to understand its fundamental role in electronics.

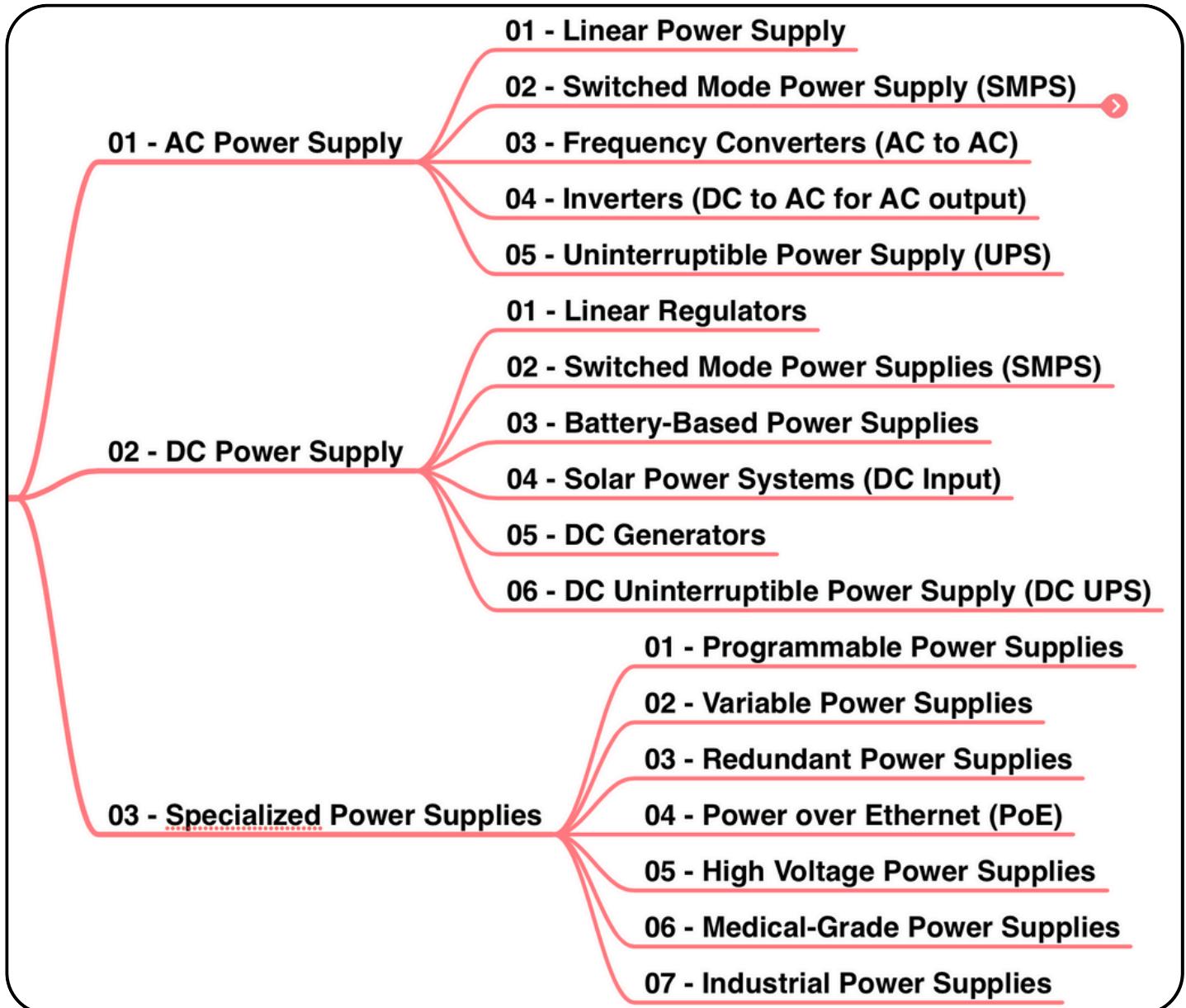
## Key Concepts

- **Power** = Voltage × Current ( $P = V \times I$ )
- **Power Consumption:**
  - **Static power consumption:** Power consumed when the circuit is idle
  - **Dynamic power consumption:** Power consumed during switching activity
- **Power density:** Power-handling capability per unit volume ( $\text{W/cm}^3$ )
- **Power efficiency:** Output power divided by input power (%)
- **Power factor:** Ratio of real power to apparent power
- **Power integrity:** Ability to deliver clean power to all components

## Different forms



# **TYPES OF POWER SUPPLY**



# AC POWER SUPPLY

An AC Power Supply is a power source that provides Alternating Current (AC) output, typically derived from an AC mains input. It either supplies AC directly to a load or converts AC to a regulated DC voltage using various internal power conversion topologies.

## Key Characteristics:

- **Input:** Alternating Current (AC) from mains (typically 50 Hz or 60 Hz).
- **Output:** Can be either AC (variable or controlled) or DC (regulated).
- **Voltage Levels:** Commonly handles input ranges like 85V – 264V AC.

## Types of AC Power Supplies

### 1. Linear Power Supply (AC-DC)

- Converts AC mains to low voltage DC using a step-down transformer, rectifier, and linear regulator.
- Provides clean, low-noise power.
- Example: Laboratory bench power supply.

### 2. Switched Mode Power Supply (SMPS) (AC-DC)

- Converts AC mains to DC using high-frequency switching circuits for efficient power conversion.
- **Types:**
  - **Isolated:** Flyback, Forward, Half-Bridge, Full-Bridge.
  - **Non-Isolated:** Buck, Boost, Buck-Boost, Charge Pump.
- Example: Laptop chargers, industrial power supplies.

### 3. Uninterruptible Power Supply (UPS)

- Provides backup AC power using batteries during mains failure.
- **Types:** Offline, Online, Line-Interactive.
- **Example:** Data centers, medical equipment.

# AC POWER SUPPLY

## 4. Frequency Converters (AC-AC)

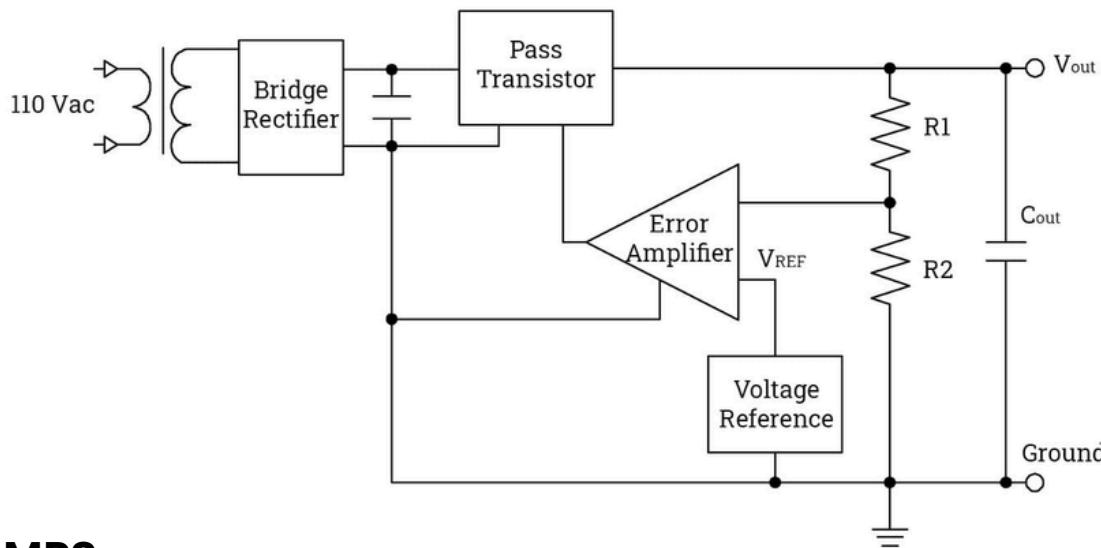
- Converts AC power from one frequency to another.
- **Example:** Equipment running on 60 Hz power in a 50 Hz country.

## 5. Inverters (DC-AC)

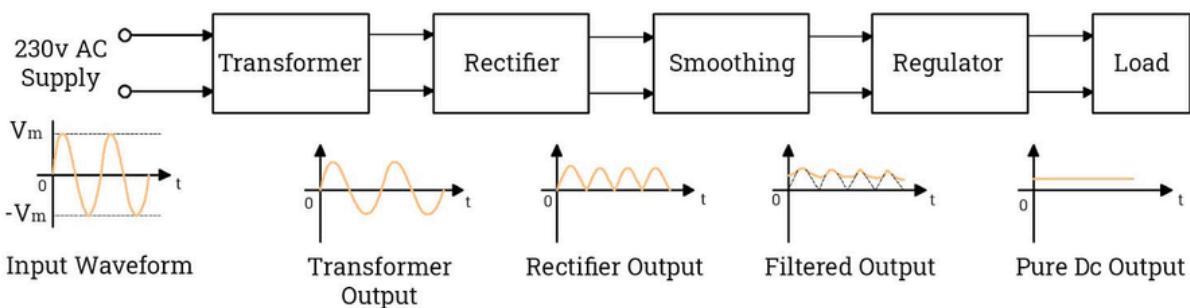
- Converts DC (from batteries or solar panels) into AC power.
- **Types:** Sine wave, modified sine wave, square wave.
- **Example:** Solar inverters, off-grid backup systems.

## Block Diagram of Typical AC-DC Power Supply

### Linear AC/DC Power Supply



### SMPs



## Advantages of AC Power Supplies

- Can efficiently deliver power over long distances (AC transmission benefits).
- Supports a wide range of input voltages (universal input).
- Available in both low and high-power configurations.
- Supports battery backup and failsafe designs via UPS integration.

# AC POWER SUPPLY

## Disadvantages

- Requires complex filtering for EMI suppression in SMPS.
- Can involve higher design complexity in switching topologies.
- Linear power supplies are large and less efficient due to low-frequency transformers.

## Real-World Applications

- **Consumer Electronics:** TVs, mobile chargers, laptops.
- **Industrial Equipment:** Power supplies for automation controllers.
- **Data Centers:** Redundant AC power supplies and UPS systems.
- **Medical Devices:** Clean, isolated AC power sources.
- **Renewable Energy:** Inverters in solar power plants.

## Types of DC Power Supplies

A DC Power Supply provides a direct current (DC) voltage output to power electronic circuits, devices, and systems. It typically takes input from:

- AC Mains (through conversion)
- Batteries
- Solar panels
- DC Generators

## Key Characteristics

- **Input:** AC, battery, solar, or direct DC bus.
- **Output:** Regulated DC voltage.
- **Voltage Levels:** Can range from millivolts to kilovolts depending on application.

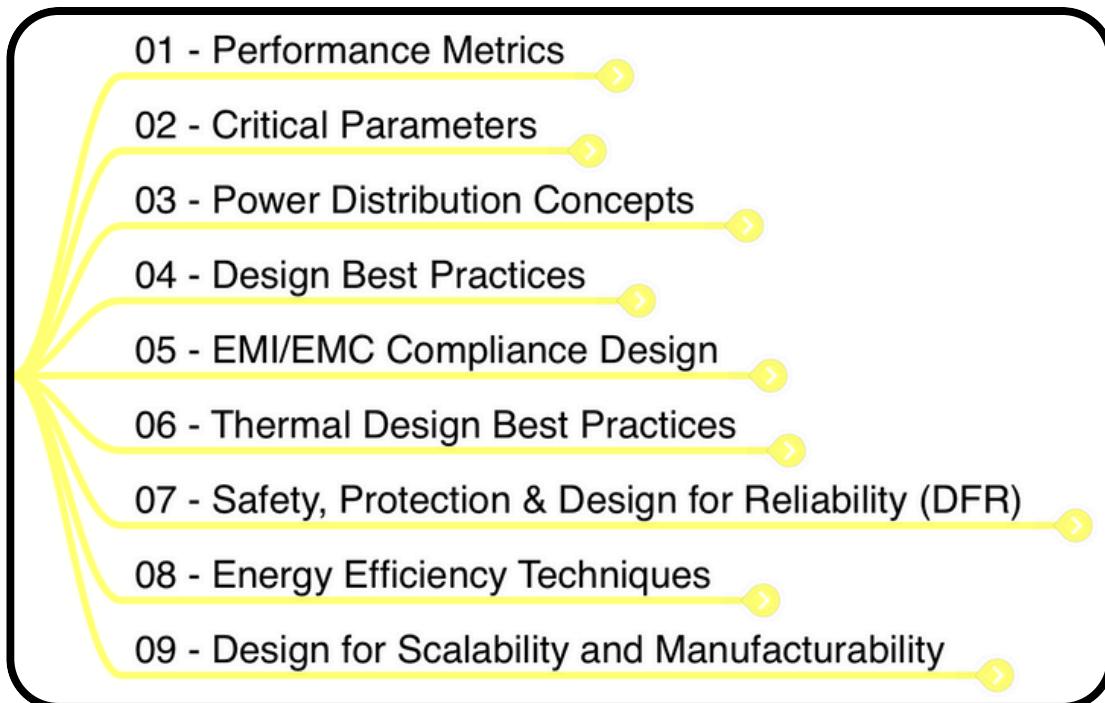
## Real-World Applications

- **Consumer Electronics:** Smartphones, laptops.
- **Automotive:** ECU power supplies, infotainment.
- **Industrial:** DC bus systems, process control.
- **Renewable Energy:** Solar microgrids, battery charging.
- **Telecommunications:** Base station power supplies.

# DESIGN CONCEPTS

Before diving into detailed architectures or topologies, a solid grasp of fundamental design concepts is essential. These principles guide how

- Provide the foundation for reliable and efficient power system design.
- Ensure optimal performance under varying load and environmental conditions.
- Address critical aspects like protection, EMI/EMC, and thermal behavior early in the design phase.
- Help in designing systems that are scalable, manufacturable, and compliant with standards.
- Bridge the gap between theoretical requirements and real-world implementation.



# 01 – PERFORMANCE METRICS

01 - High Efficiency	85 - 95%
02 - Low Standby Power	<100mW
03 - Tight Regulation	+/-1-3%
04 - Fast Transient Response	<100us

## 1. High Efficiency (85% – 95%)

Efficiency measures how much of the input power is converted to useful output power.

$$\text{Efficiency } (\eta) = \left( \frac{P_{out}}{P_{in}} \right) \times 100\%$$

If a power supply outputs 90W but draws 100W from the input:

$$\eta = \left( \frac{90}{100} \right) \times 100\% = 90\%$$

- Higher efficiency = less heat, better thermal performance.
- Critical for battery-operated and thermally-constrained systems.

## 2. Low Standby Power (< 100 mW)

Power consumed when the system is powered but not actively delivering output.

- Saves energy during idle periods.
- Complies with energy standards (e.g., <0.1W standby for many ENERGY STAR products).
- Important for IoT, smart appliances, always-on electronics.

No specific formula, but measured in watts (W) using:

$$P_{standby} = V_{input} \times I_{standby}$$

# 01 – PERFORMANCE METRICS

## 3. Tight Regulation ( $\pm 1\%$ to $\pm 3\%$ )

Voltage regulation ensures output voltage remains stable despite:

- Changes in input voltage (Line Regulation)
- Changes in output current (Load Regulation)

**Formulas:**

$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \times 100\%$$

$$\text{Load Regulation} = \frac{V_{no\ load} - V_{full\ load}}{V_{full\ load}} \times 100\%$$

**Why it matters:**

- Keeps microcontrollers, analog sensors, and communication circuits stable.
- Ensures **system accuracy and reliability** under load variations.

## 4. Fast Transient Response (< 100 $\mu\text{s}$ )

Time taken for output voltage to recover to steady-state after a sudden load change.

**Formula (Inductive Load):**

$$\tau = \frac{L}{R}$$

( $\tau$  is the time constant – relevant when modeling response time using L and R.)

**Also modeled using:**

$$V(t) = V_{final} + (V_{initial} - V_{final}) \cdot e^{-\frac{t}{\tau}}$$

**Why it matters:**

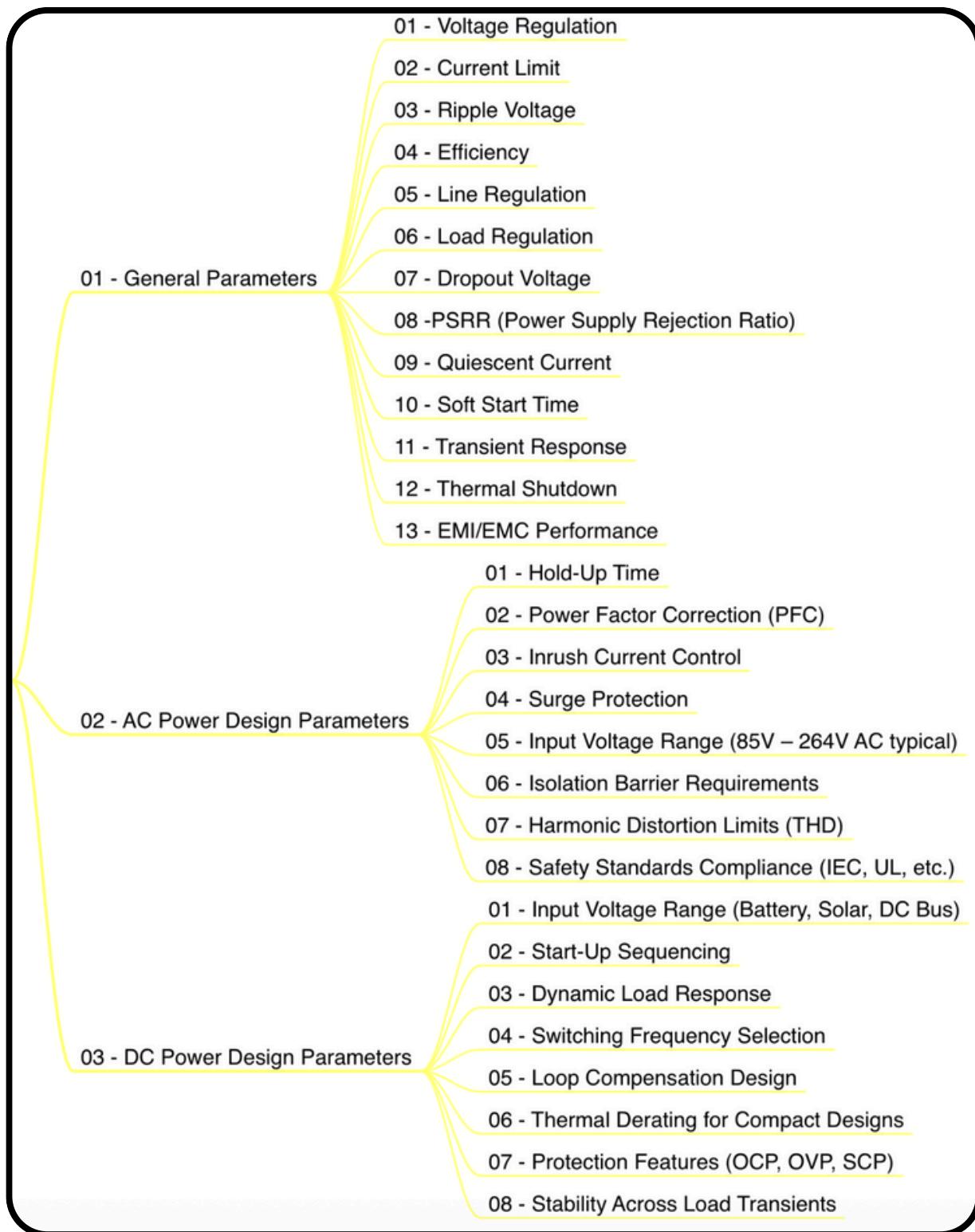
- Prevents system instability and voltage undershoots/overshoots.
- Especially important in high-speed digital circuits (CPUs, FPGAs).

**Tip:**

Good PCB layout, sufficient output capacitance, and fast feedback loops help achieve <100 $\mu\text{s}$  transient response.

## 02 – CRITICAL PARAMETERS

Every reliable power system begins with careful attention to critical design parameters. These include essential metrics like voltage regulation, efficiency, ripple, and protection mechanisms that directly affect performance and safety. Whether dealing with AC or DC input sources, these parameters ensure that the power supply remains stable, responsive, and compliant under real-world operating conditions.



# GENERAL PARAMETERS

## Voltage Regulation

Ability of the power supply to maintain a constant output voltage despite input voltage or load current changes.

### Types:

- **Line Regulation:** Change in output due to input variation.
- **Load Regulation:** Change in output due to load variation.

$$\text{Line Regulation} = \frac{V_{\text{out max}} - V_{\text{out min}}}{V_{\text{nominal}}} \times 100\%$$

$$\text{Load Regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{full load}}} \times 100\%$$

## Current Limit

The maximum output current the power supply can deliver before entering protection or shutdown mode.

- **Why It Matters:** Prevents damage to components and wiring during overcurrent or short-circuit events.
- **Related Protection:** Often integrated into OCP (Overcurrent Protection).

## Ripple Voltage

Small residual AC voltage present on the DC output due to incomplete suppression of switching or rectification.

### Formula (Peak-to-Peak):

$$V_{\text{ripple}} = I_{\text{load}} \times \frac{\text{ESR}}{fC}$$

- ESR: Equivalent Series Resistance
- f: Frequency
- C: Output capacitance

**Target:** Typically < 1–2% of output voltage for most designs.

# GENERAL PARAMETERS

## Dropout Voltage

The minimum difference between input and output voltage required to maintain regulation (primarily in LDOs).

$$V_{dropout} = V_{IN\ min} - V_{OUT\ nominal}$$

Low dropout is essential for **battery-powered or low-headroom** applications.

## PSRR (Power Supply Rejection Ratio)

Ability of the regulator to suppress variations or noise in the input voltage from reaching the output.

$$PSRR(dB) = 20 \cdot \log\left(\frac{\Delta V_{in}}{\Delta V_{out}}\right)$$

**Higher PSRR** is better, especially for analog and RF circuits.

## Quiescent Current

Quiescent Current ( $I_q$ ) is the amount of current a power supply or regulator consumes internally when there is no load (or very light load) on the output.

It's the baseline operating current needed for internal control circuitry (like error amplifiers, reference voltages, comparators, etc.) to function.

**How to Estimate  $I_q$  Losses (in sleep mode):**

$$P_{Iq} = V_{in} \times I_q$$

Example if  $V_{in}=3.3V$  &  $I_q=2\mu A$

$$P_{Iq} = 3.3V \times 2\mu A = 6.6\mu W$$

**Importance:** Low  $I_q$  is critical for battery-powered and low-power systems.

**Tip:**

Always check  $I_q$  on the regulator's datasheet if your device:

- Enters sleep/standby frequently
- Is powered by coin cell, AA battery, or supercap
- Targets low average power consumption (e.g.,  $<10 \mu W$  total system idle)

# GENERAL PARAMETERS

## Soft Start Time

Soft Start Time refers to the controlled, gradual ramp-up of a power supply's output voltage when it is first turned on.

Instead of instantly applying full voltage (which can cause large inrush currents), soft start limits the rate of voltage increase, thereby protecting both the power supply and the load.

### Why Soft Start Is Important:

- Prevents inrush current that can damage capacitors, MOSFETs, or connectors.
- Reduces stress on power components and extends lifespan.
- Avoids voltage overshoot that might violate load tolerances.
- Ensures sequencing coordination when multiple rails power a system (e.g., MCU + analog).

### Typical Control Method:

- Internal or external capacitor charges slowly, controlling the gate of pass element (like a MOSFET).
- Controlled by a soft-start pin or programmable timing.

### Soft Start Time Formula (approx):

$$\text{Soft Start Time } (T_{ss}) = \frac{C_{ss} V_{ref}}{I_{ss}}$$

Where

$T_{ss}$  = Soft start time (seconds)

$C_{ss}$  = External soft – start capacitor (farads)

$V_{ref}$  = Reference voltage (typically 0.6V to 1.2V)

Ex: if  $C_{ss} = 0.1\mu F$ ,  $V_{ref} = 0.6V$ ,  $I_{ss} = 5\mu A$ ,

$$\text{Soft Start Time } (T_{ss}) = \frac{0.1 \times 10^{-6} \times 0.6}{5 \times 10^{-6}} = 12ms$$

$I_{ss}$  = Internal soft – start charging current ( $\mu A$ )

### Tip:

When powering high-capacitance or sensitive loads, increase soft-start time to reduce inrush and improve system stability.

# GENERAL PARAMETERS

## Thermal Shutdown

Thermal Shutdown is a built-in protection mechanism in power supplies and voltage regulators that **automatically disables the output** when the internal temperature exceeds a safe limit.

It prevents **permanent damage** due to overheating.

### How it Works:

- The IC contains an internal temperature sensor.
- If the die temperature exceeds the thermal shutdown threshold (typically 150°C–180°C), the regulator or converter shuts down.
- The device automatically restarts when the temperature drops below the hysteresis threshold (often 20–30°C lower).

### Why Thermal Shutdown Is Important:

- Protects the device from thermal runaway and failure.
- Acts as a last-resort protection, especially when:
  - Cooling is insufficient
  - Heat sink design is inadequate
  - Ambient temperature is high
  - Load exceeds safe power dissipation

### Power Dissipation and Temperature Rise (for design estimation):

$$P_D = (V_{in} - V_{out}) \times I_{out}$$

$P_D$  = Power dissipated in the regular

$$\Delta T = P_D \times \theta_{JA}$$

$\theta_{JA}$  = Thermal resistance junction – to – ambient (°C/W)

### Tip to Avoid Thermal Shutdown:

- Keep power dissipation low using efficient regulation (e.g., switchers over LDOs).
- Use adequate copper area or thermal vias to improve heat dissipation.
- Maintain proper ventilation or forced airflow.
- Avoid placing hot components close together on PCB.
- Check  $\theta_{JA}$  and ambient temperature during design review.

# GENERAL PARAMETERS

## EMI/EMC Performance

EMI & EMC refer to how a power supply behaves in the presence of or as a source of electromagnetic noise.

- EMI: Unwanted noise a device generates.
- EMC: A device's ability to function properly in a noisy environment without causing or being affected by interference.

### Why EMI/EMC Performance Is Important:

- Poor EMI can interfere with nearby sensitive circuits (e.g., audio, RF, sensors).
- Failing EMC standards can block product certification (e.g., FCC, CISPR, IEC, EN).
- High EMI can trigger functional errors or false triggering in digital systems.

### Main EMI Sources in Power Supplies:

Type	Source Example	Frequency Range
Conducted EMI	High di/dt switching edges in SMPS	< 30 MHz
Radiated EMI	PCB traces, cables acting as antennas	30 MHz – 1 GHz+

### Typical EMI Standards:

Standard	Description
CISPR 22/32	Radiated & conducted emissions for IT
EN 55011/55032	EMI for industrial and multimedia equipment
FCC Part 15	EMI compliance in the US
IEC 61000-4-x	Immunity tests (ESD, surge, EFT, etc.)

### Related Formula: Radiated Emissions Estimation

$$E = \frac{I \times l \times f^2}{r}$$

Where

- E: Emitted electric field
- I: Current in loop
- l: Loop length
- f: Frequency
- r: Distance from loop

# GENERAL PARAMETERS

## Design Guidelines to Improve EMI/EMC Performance:

- **Use Input and Output Filtering**
  - Add LC filters or ferrite beads on power input/output lines.
  - Ferrite beads: High-frequency noise suppression
  - $\pi$ -filters: High attenuation, compact
  - Use common-mode chokes for differential noise suppression.
- **Minimize High-Frequency Loop Areas**
  - Keep the switch node and high  $di/dt$  paths short and tight. Keep high  $dV/dt$  loops small:  $< 1\text{in}^2$
  - Minimize parasitic inductance using solid ground planes.
  - Minimize common impedance path
  - Shield high-frequency sources
- **Control Switching Transitions**
  - Use gate resistors or soft switching to reduce  $dV/dt$  and  $di/dt$ .
- **Shielding and Enclosures**
  - Use grounded metal shields or cages for high-noise circuits.
- **Proper Grounding**
  - Single-point grounding strategy for analog/digital separation.
  - Avoid ground loops.
- **Snubber Circuits and Damping**
  - RC snubbers across switching devices reduce high-frequency ringing.
- **Board stack-up recommendations:**
  - Signal-Ground-Power-Signal: Good for 4-layer
  - Signal-Ground-Signal-Power-Signal-Ground-Signal: Better for 6+ layers

## Real-World Example:

A buck converter switching at 500kHz can generate EMI that causes a nearby audio amplifier to buzz. Adding an input LC filter, shortening the switch node trace, and adding a grounded shield resolved the issue and passed CISPR 22.

# AC POWER DESIGN PARAMETERS

## Hold-Up Time

Hold-up time is the duration a power supply can maintain its output voltage within regulation limits after the input AC power is lost (e.g., due to a brief brownout or disconnection).

It is typically defined until the output falls below the minimum allowed voltage for the load.

### Why it matters:

- Prevents system reset or malfunction during short power interruptions.
- Critical in:
  - Telecom/Networking
  - Industrial Automation
  - Medical Devices
- Ensures enough energy is stored in the bulk input capacitor to ride through line dropouts or switching transients.

### Where It Happens:

- In AC-DC power supplies, just after the input rectifier and before the switching stage, there's a bulk capacitor that stores energy.
- When AC input drops, this capacitor discharges, keeping the system alive briefly.

### Typical Specification:

- 10–20 milliseconds is common.
- Telecom standard:  $\geq 10$  ms at full load.

$$t_{hold-up} = \frac{1}{2} \times \frac{C_{bulk} \times (V_{initial}^2 - V_{min}^2)}{P_{load}}$$

$t_{hold-up}$  = Hold-up time(s)

$C_{bulk}$  = Bulk cap value(F)

$V_{initial}$  = Initial Cap Voltage(V)

$V_{min}$  = Minimum Voltage before shutdown(V)

$P_{load}$  = Output power(W)

### For Design Example:

You want 10ms hold-up for a 50W power supply:

$$C_{bulk} = 470\mu F$$

$$V_{initial} = 375V$$

$$V_{min} = 300V$$

$$t_{hold-up} = \frac{1}{2} \times \frac{400 \times 10^{-6} \times (375^2 - 300^2)}{50} \approx 10.5ms$$

# AC POWER DESIGN PARAMETERS

## Power Factor Correction (PFC)

PFC is the process of improving the power factor of a power supply so that it draws current in phase with the voltage and with a waveform shape that closely resembles a sine wave.

A high power factor means the power drawn from the AC source is used more efficiently, reducing wasted energy and minimizing stress on the power grid.

$$PF = \frac{P_{real}}{P_{apparent}}$$

- Real Power : Power actually consumed (in Watts)
- Apparent Power : Product of RMS voltage and RMS current (in VA)

### Why Poor Power Factor Is a Problem:

- Draws higher input current for the same power → increases conductor losses
- Produces harmonic distortion → affects other equipment
- Causes voltage drops in power distribution lines
- Fails compliance with international standards (EN61000-3-2)

### PFC Techniques:

#### 1. Passive PFC

- Uses inductors, capacitors, and sometimes ferrites to filter and correct current.
- Simple, low-cost, but typically achieves PF ~ 0.6–0.8.
- Suitable for <75W designs or where compliance isn't strict.

#### 2. Active PFC

- Uses a boost converter and control IC to shape input current into a sine wave.
- Achieves PF ≥ 0.95 (even at 20–100% load).
- Required for >75W power supplies in most regions.
- May be single-stage or dual-stage (boost + isolated DC/DC).

Power Factor Type	Value	Characteristics
Ideal PF	1	Voltage and current are perfectly in phase
Lagging PF	< 1	Current lags (inductive loads)
Leading PF	< 1	Current leads (capacitive loads)

# AC POWER DESIGN PARAMETERS

## Inrush Current Control

Inrush current is the initial surge of current drawn by a power supply when first powered ON, primarily due to charging bulk input capacitors. In AC power supplies, this can be 10x–30x higher than the normal operating current lasting a few milliseconds.

### Why Inrush Current Matters

- Can trip circuit breakers or blow input fuses.
- Causes voltage dips that affect other systems on the same power line.
- Stresses rectifier diodes and other front-end components.
- Leads to EMI spikes, potentially failing EMC compliance.

### Common Inrush Control Methods:

#### 1. NTC Thermistor (Passive)

- High resistance at startup, drops as it heats up.
- Simple and cheap, but limited performance.
- Requires cool-down before re-powering.

#### 2. Relay + Precharge Resistor

- At power-on, current flows through a power resistor.
- After capacitors charge, a relay bypasses the resistor.
- Better for medium to high-power systems (>100W).

#### 3. Active Inrush Current Limiter (IC-based)

- Uses MOSFET + controller to monitor voltage and control turn-on.
- Compact, efficient, repeatable.
- Examples: LTC4350, LM5069, TPS2490

### Best Practices:

Method	Use Case	Notes
NTC Thermistor	<150W, simple systems	Cheap, but slow recovery
Relay + Resistor	150W–1kW+ designs	Reliable, higher BOM
Active Controller IC	High-reliability designs	Compact, feature-rich

# AC POWER DESIGN PARAMETERS

## Formula:

$$I_{inrush} = \frac{V_{AC\ peak}}{R_{limiting\ path}}$$

Where,  $V_{AC\ peak} = V_{RMS} \times \sqrt{2}$

$R_{limiting\ path}$  is minimal if no control is present

## Design Example:

230V AC  $\Rightarrow V_{peak} \approx 325V$

Capacitor initially at 0V

Without resistance, the current can be >50A, damaging components

For a 300W SMPS with a 400V, 220 $\mu$ F input cap:

- *Without limiting:*

$$I = \frac{325V}{0.5\Omega} = 650A \text{ (theoretical peak)}$$

- *With a 10Ω NTC, inrush becomes:*

$$I = \frac{325V}{10\Omega} = 32.5A$$

Better, but still high – so larger designs add a relay bypass.

# AC POWER DESIGN PARAMETERS

## Surge Protection

Surge protection is the implementation of circuit techniques or components to suppress high-voltage transients that can occur on power lines. These transients—also called surges or spikes—can be caused by:

- Lightning strikes (direct or nearby)
- Switching of inductive loads (motors, relays)
- Grid disturbances or brownouts
- Electrostatic discharge (ESD) or electromagnetic interference (EMI) events

### Why Surge Protection is Critical:

- Prevents damage to sensitive semiconductors (MOSFETs, ICs)
- Improves reliability and electrical safety
- Helps comply with international EMC/safety standards (IEC 61000-4-5)
- Protects against catastrophic failure in industrial or field-deployed systems

### How Surge Protection Works:

Most surge protection devices act as voltage-dependent switches:

- At normal voltage → high impedance → circuit unaffected
- At overvoltage (surge) → device clamps or redirects energy → protects load

### Common Surge Protection Devices:

Component	Function	Where Used
MOV (Metal Oxide Varistor)	Clamps high voltage surges to safe levels	AC mains lines, DC bus
TVS Diode	Fast-acting clamping; ideal for ESD and EFT	Low-voltage I/O, power rails
GDT (Gas Discharge Tube)	Diverts surge to ground via ionization	High-energy surge entry
Spark Gap	Passive surge path (usually PCB-integrated)	Telecom, outdoor systems
Common-Mode Choke	Suppresses differential/common-mode surges	AC input filtering stage

# AC POWER DESIGN PARAMETERS

## Input Voltage Range (85V – 264V AC Typical)

The input voltage range of a power supply defines the acceptable AC voltage window over which the power supply operates reliably & within specification. A typical universal AC input range is: 85V(min) to 264V(max) AC.

### Why It Matters:

- Ensures power supply works globally across voltage standards
- Allows for tolerance to input fluctuations, brownouts, or unstable grids
- Protects downstream electronics from input under/over-voltage faults

### Input Range Design Considerations:

Parameter	Design Concern
Low-end voltage (85V)	Must deliver full rated power without dropout
High-end voltage (264V)	Must withstand higher stress on input components
Startup behavior	Should reliably power on from minimum voltage
Efficiency variance	May vary across input voltages – consider universal efficiency
Switching frequency	Some topologies adjust frequency based on input voltage

### Rectified DC Bus Calculation:

$$V_{DC\ Bus} = V_{RMS} \times \sqrt{2} \text{ (minus diode drops)}$$

AC Input (V)	DC Bus (after bridge)
85V AC	≈ 120V DC
230V AC	≈ 325V DC
264V AC	≈ 373V DC

### Best Practices:

- Always derate input capacitors and FETs above the max expected DC bus
- Consider wide input voltage range topologies:
  - Flyback (wide-range)
  - PFC Boost + LLC or Buck (multi-stage)
- Include input undervoltage lockout (UVLO) to prevent brownout malfunction

# AC POWER DESIGN PARAMETERS

## Isolation Barrier Requirements

An isolation barrier in a power supply refers to the electrical separation between the high-voltage input side (typically AC mains) and the low-voltage output side (e.g., 5V, 12V DC). This barrier protects users and sensitive circuits from dangerous voltages, ensuring both safety and signal integrity.

### Why Isolation Is Needed:

- Safety:** Prevents high-voltage shocks from reaching the user or low-voltage circuits.
- Regulatory compliance:** Mandatory for medical, industrial, and consumer electronics.
- Noise immunity:** Breaks ground loops, blocks conducted noise.
- Functional integrity:** Allows different circuit domains to communicate safely.

### Applications That Require Isolation:

Application	Isolation Required?
AC-DC adapters	<input checked="" type="checkbox"/> Yes
USB chargers	<input checked="" type="checkbox"/> Yes
LED drivers (mains-based)	<input checked="" type="checkbox"/> Yes
Battery chargers	<input checked="" type="checkbox"/> Often
DC-DC converters (non-isolated)	<input type="checkbox"/> No

### Key Isolation Components:

Component	Function
Transformer	Primary mechanism for galvanic isolation
Optocoupler	Isolates feedback/control signal
Digital Isolator	High-speed isolated communication
Photovoltaic Driver	For gate driving across isolation

# AC POWER DESIGN PARAMETERS

## Isolation Design Requirements:

Parameter	Description
Isolation Voltage	Max withstand voltage between input/output (e.g., 3kV)
Creepage Distance	Distance across PCB surface between isolated domains
Clearance Distance	Air gap between conductive elements
Insulation Type	Basic, Supplementary, Reinforced

## Typical Isolation Ratings:

Application	Isolation Voltage (rms)	Creepage (mm)	Standard
Consumer (Class II)	3kV–4kV	≥ 5 mm	IEC 62368-1
Medical (Patient)	≥ 5kV	≥ 8 mm	IEC 60601-1
Industrial	2.5kV–4kV	≥ 6.4 mm	IEC 61010-1

## Insulation Types:

Type	Description
Basic	One level of protection (minimum legal requirement)
Supplementary	Additional protection to support Basic insulation
Reinforced	Single insulation system providing the same protection as Double insulation

## Best Practices:

- Use transformers with appropriate isolation test ratings
- Place optocouplers with proper spacing from high-voltage traces
- Enforce creepage and clearance rules in PCB layout (use slots if needed)
- Choose reinforced insulation for Class II appliances (no protective earth)
- Apply safety margins above the minimum spec (e.g., 4kV instead of 3kV)

# AC POWER DESIGN PARAMETERS

## Harmonic Distortion Limits (THD)

In AC power systems, harmonic distortion refers to the presence of undesired frequencies (multiples of the fundamental 50/60Hz AC line frequency) in the input current waveform. These are typically caused by non-linear loads such as power supplies, LED drivers, and motor controllers.

$$THD(\text{Total Harmonic Distortion}) = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \dots + I_n^2}}{I_1}$$

$I_1$  =Fundamental current at 50/60 Hz

$I_2 + I_3 + I_4 + \dots + I_n$  Harmonic currents at higher frequencies

- Expressed in %: Lower THD = cleaner, more sinusoidal waveform
- Typical Acceptable Limit: THD < 10% for power supplies (depending on application)

### Why Harmonics Are a Problem:

- Pollutes the power grid
- Increases heating in transformers and neutral conductors
- Causes voltage distortion and equipment malfunction
- Reduces system efficiency
- Can interfere with communication and sensitive circuits

### How to Reduce Harmonic Distortion:

Method	How It Helps
Power Factor Correction (PFC)	Shapes input current to follow voltage sinusoid
Input EMI Filters	Attenuates high-frequency components
Soft switching topologies	Reduce switching noise and harmonics
Proper layout & grounding	Avoids parasitic resonances

### Regulatory Compliance Standards:

Standard	Description
EN61000-3-2	Limits harmonic emissions in AC-powered equipment
IEC 61000-3-12	Harmonics for high-current equipment (>16A/phase)
IEEE 519	Harmonic control in industrial systems

# AC POWER DESIGN PARAMETERS

## Safety Standards Compliance

Safety standards define regulations and guidelines that ensure an electrical product is safe for users and equipment. These standards cover shock protection, fire prevention, insulation, creepage/clearance distances, grounding, and isolation. Compliance is mandatory for commercial and industrial power supply products.

### Why Safety Compliance Matters:

- Ensures user safety from electric shock, fire, and over-temperature
- Legally required for certification and market access (CE, UL, FCC, etc.)
- Guarantees product quality and reliability
- Prevents recalls, lawsuits, or import bans

### Key Safety Standards by Region and Purpose:

Standard	Governing Body	Purpose	Region
IEC 62368-1	IEC	Audio/video, IT, telecom power supplies	Global
IEC 60601-1	IEC	Medical equipment	Global
IEC 61010-1	IEC	Industrial, lab, measurement instruments	Global
UL 62368-1	UL (NRTL)	North American equivalent of IEC 62368-1	USA/Canada
EN 62368-1	CENELEC	European version (CE marking)	Europe
CSA C22.2	CSA	Canadian electrical safety	Canada
GB standards	CCC	Chinese safety requirements	China

### What Safety Standards Typically Cover:

Category	Details
Creepage & Clearance	Minimum distances between live and accessible parts
Insulation Type	Basic, Supplementary, or Reinforced
Protective Earth	Connection integrity for Class I appliances
Touch Current Limits	How much current can reach user-accessible surfaces
Temperature Rise	Maximum allowable heating under full load
Flame Retardance	Flammability class of plastics, PCBs (e.g., UL94V-0)
Dielectric Strength	Withstand voltage test between input and output (e.g., 3kV)

# DC POWER DESIGN PARAMETERS

## 01. Input Voltage Range

The input voltage range refers to the span of voltages over which a DC power supply or converter can reliably operate and regulate its output voltage.

### Common Sources & Typical Voltage Ranges:

Source Type	Typical Voltage Range
Single Li-ion Battery	3.0V – 4.2V
Automotive Battery	9V – 16V (12V nominal)
Solar Panel	9V – 18V (for single panel)
DC Bus (Industrial)	24V, 48V, 110V, 380V

### Design Considerations:

- **Wide Input Range Support:**
  - Especially important in systems with unstable supply (e.g., solar, automotive).
  - Boost or buck-boost converters often used in such cases.
- **Undervoltage Lockout (UVLO):** Prevents operation at voltages too low for safe regulation.
- **Oversupply Protection (OVP):** Prevents damage from accidental high voltage inputs.
- **Efficiency at Extremes:** Converter must remain efficient across the full voltage range.

### Design Tip:

Always consider worst-case input voltage (min & max) and load condition when choosing regulators or converters.

# DC POWER DESIGN PARAMETERS

## 02. Start-Up Sequencing

Start-up sequencing is the controlled, timed activation of power rails in a specific order to ensure that multivoltage systems (like FPGAs, MCUs, ASICs, DDR memory) power up safely and predictably.

### Sequencing requirements:

- FPGA/ASIC core vs. I/O voltages
- Analog supplies
- Bus interfaces
- Clock/PLL power

### Why Start-Up Sequencing Matters:

- Prevents latch-up or damage to devices requiring specific voltage rail activation order.
- Ensures that core voltage, I/O voltage, and analog power come up in a defined sequence.
- Avoids inrush current surges when all supplies turn on simultaneously.
- Crucial for reliable booting in complex systems.

### Common Use Cases:

Common Use Cases System	Power-Up Sequence
FPGA	Vcore → Vaux → Vio
DDR Memory	VDD → VTT → VREF
Microcontroller + Sensor	Vcore → Vanalog → VIO

### Techniques for Sequencing

- **Passive Delay with RC Circuits:** Simple delay per rail using RC and enable pin. Suitable for low-cost designs.
- **Power Management ICs (PMICs):** Advanced sequencing using PMIC with multiple rails and programmable timing.
- **Digital Control via GPIOs:** MCU GPIO enables each power stage with programmable delay.

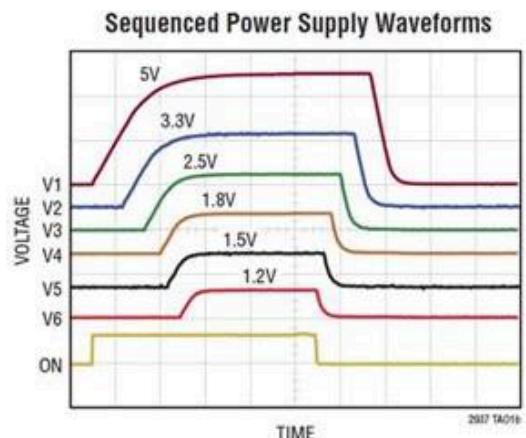
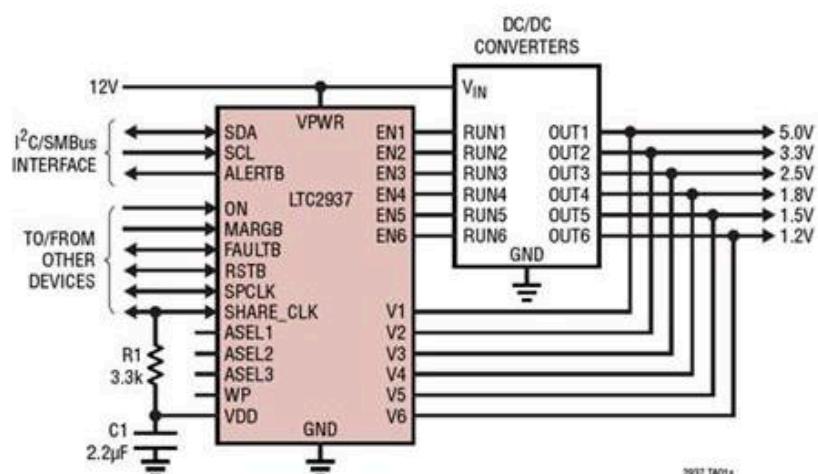
# DC POWER DESIGN PARAMETERS

## Key Parameters:

Parameter	Description
Delay Time	Time between activating successive rails
Rise Time Matching	Ensuring similar slew rate for critical rails
Enable Thresholds	Voltage level to trigger rail activation

## Monitoring requirements:

- Power-good signals
- Reset generation
- Voltage supervision
- Fault detection



## Best Practices

- Always check IC datasheets for recommended rail-up/down sequence.
- Use Power-Good (PG) or Enable pins to coordinate supply stages.
- For shutdown sequencing, reverse the order unless otherwise specified

# DC POWER DESIGN PARAMETERS

## 03. Dynamic Load Response

Dynamic Load Response refers to a power supply's ability to maintain output voltage within acceptable limits when the load changes rapidly (e.g., a processor switching between sleep and active modes).

### Why It Matters

- Critical for digital circuits, processors, FPGAs, and ASICs that switch current loads quickly.
- Prevents voltage dips or overshoots that can cause system instability, data loss, or hardware resets.
- Improves system robustness, especially under burst-mode or pulse-load conditions.

### Performance Goals:

Parameter	Typical Range
Voltage Deviation ( $\Delta V$ )	$\pm 3\%$ to $\pm 5\%$ of $V_{out}$
Response Time (settling)	<100 $\mu s$ (fast systems)
Load Step Size	50% to 100% of $I_{out}$

### Key Factors Affecting Dynamic Response:

- **Output Capacitance ( $C_{out}$ ):** More capacitance = better damping of sudden load changes.
- **Control Loop Bandwidth:** Faster control loop  $\rightarrow$  faster compensation.
- **ESR of Output Capacitors:** Affects overshoot/undershoot behavior. Lower ESR = tighter response.
- **PCB Layout:** Short return paths & minimized parasitic inductance

$$\Delta I = \frac{\Delta V \times ESR}{1 - e^{\left(\frac{-t}{RC}\right)}}$$

$\Delta V$  = Transient voltage deviation

$\Delta I$  = Change in load current

ESR = equivalent series resistance of capacitor

$t$  = response time

$R, C$  = output stage resistance and capacitance

### Design Tips:

- Use multiple ceramic capacitors close to the load.
- Combine low-ESR ceramics (for fast transient) with bulk capacitors (for sustained load).
- Increase control loop bandwidth but avoid instability (watch phase margin).
- Minimize inductive trace lengths in high-current paths.

# DC POWER DESIGN PARAMETERS

## 04. Switching Frequency Selection

Switching frequency is the rate at which a DC-DC converter's switching elements (usually MOSFETs) turn on and off. It directly impacts efficiency, component size, EMI behavior, and thermal performance.

### Why It Matters

Parameter	Effect of Higher Frequency
Inductor size	↓ Smaller due to faster energy transfer
Output capacitor size	↓ Smaller capacitance required
Efficiency	↓ May decrease due to switching losses
EMI	↑ Increased EMI noise above 1 MHz
Transient response	↑ Improved (faster response to load changes)

### Important Considerations:

**1. Switching Losses:** Power lost in turning the MOSFET on/off:

$$P_{switch} = \frac{1}{2}VIt_{sw}f_{sw}$$

**2. Conduction vs. Switching Losses**

- Lower frequencies: More conduction losses, less switching losses
- Higher frequencies: Opposite behavior

**3. Magnetics Design**

- Higher frequencies = smaller inductors but higher core losses
- Must choose ferrite cores optimized for selected frequency

**4. EMI Management**

- High-frequency switching increases EMI harmonics
- Requires proper shielding, layout, snubbers, and filters

### Selection Guidelines

- **Battery-powered or portable systems:** Choose high frequencies (1–2 MHz) for smaller size
- **Industrial or thermally-constrained:** Use mid-range (~500 kHz) to balance losses and size
- **Noise-sensitive (e.g., RF, analog):** Opt for lower frequencies to reduce EMI

# DC POWER DESIGN PARAMETERS

## 05. Loop Compensation Design

Loop compensation is the process of designing the feedback control loop in a DC-DC converter to ensure stable, responsive, and accurate regulation of output voltage under varying conditions.

It's essential in switching regulators where feedback is used to control the PWM duty cycle to maintain the output voltage.

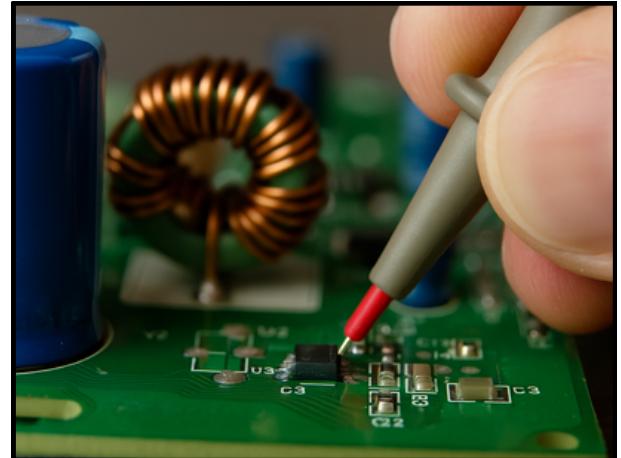
### Why It Matters

#### Without proper loop compensation:

- Output may oscillate (unstable)
- Poor load or line regulation
- Slow transient response
- Risk of runaway conditions or converter failure

#### Proper compensation ensures:

- Stability
- Fast response
- Good phase margin ( $\geq 45^\circ$ )
- Predictable behavior under transients



### Key Concepts:

Term	Description
Loop Gain ( $T$ )	Gain from input to output in the closed-loop system
Bandwidth	Frequency at which gain = 1 (0 dB), defines response speed
Phase Margin	Phase angle at crossover frequency (target: $\geq 45^\circ$ )
Gain Margin	Additional gain required to make the loop unstable

### Compensation Types

Type	Use Case	Features
Type I	LDOs, basic regulators	One pole (slow, low bandwidth)
Type II	Buck converters	One pole + one zero
Type III	Voltage-mode, current-mode SMPS	Two poles + two zeros (complex loads)

# DC POWER DESIGN PARAMETERS

## Design Steps:

1. Identify Power Stage Transfer Function ( $G(s)$ )
2. Depends on topology (buck, boost) and passive components.
3. Select Compensation Network ( $C(s)$ )
4. Choose RC components in error amplifier or external network.
5. Plot Bode Plot (Gain/Phase vs Frequency)
6. Use simulation tools or analytical models.
7. Adjust Components
8. Tune zeros/poles for:
  - Crossover frequency (typically 1/10 of switching frequency)
  - $\geq 45^\circ$  phase margin
  - 10 dB gain margin

## Key Formulas:

Power stage output pole (For Buck converter):  $f_{p1} = \frac{1}{2\pi R_{load} C_{out}}$

ESR Zero:  $f_{z1} = \frac{1}{2\pi R_{ESR} C_{out}}$

Compensation Zero (Type II):  $f_z = \frac{1}{2\pi R_C C_C}$

Where,

$R_{load}$  = Load Resistance

$C_{out}$  = Output Capacitance

$R_{ESR}$  = ESR of capacitor

$R_C C_C$  = Compensation network values

## Practical Tips

- Use ceramic capacitors for consistent ESR and predictable zeros
- Design for wide load variation (light to heavy)
- Always verify compensation under real PCB conditions

# DC POWER DESIGN PARAMETERS

## 06. Thermal Derating for Compact Designs

Thermal derating is the practice of reducing the electrical load or current rating of components as temperature rises – especially in compact or enclosed designs – to maintain reliability, prevent failure, and meet longevity targets.

### Why It Matters

- Compact designs limit airflow and increase power density, causing:
  - Higher ambient and internal temperatures
  - Reduced heat dissipation
  - Accelerated component aging
- Derating ensures components operate below their absolute maximum ratings under actual use conditions, not just in ideal lab environments.

### Key Impacts of Thermal Derating:

Component	Temperature Effect
Capacitors	Reduced capacitance and life above 85°C or 105°C
Inductors	Core saturation increases with heat
MOSFETs	Higher R <sub>d(on)</sub> → more conduction loss
Diodes	Forward voltage drops → thermal runaway risk
ICs	Junction temperature rise may cause shutdown or drift

### Thermal Formula:

$$T_j = T_a + (R_{0JA} \times P_d)$$

$T_j$  = Junction Temperature (°C)

$T_a$  = Ambient Temperature (°C)

$R_{0JA}$  = Junction – to – ambient thermal resistance (°C/W)

$P_d$  = Power dissipated (W)

**Goal:** Keep  $T_j$  below the maximum rated temperature (usually ~125°C for ICs, 150°C for power devices)

### Derating Examples:

Component	Rated @ 25°C	Max Temp	Derating Strategy
MOSFET	10A	125°C	Use 6A max current @
LDO Regulator	1A	125°C	Limit to 0.6–0.8A with
Ceramic Cap	100µF	105°C	May drop to 60–70µF at
Aluminum Cap	1000 hr @ 105°C	–	Derated to 4000–8000

# DC POWER DESIGN PARAMETERS

## Best Practices:

- Use larger copper pours under heat-generating components
- Add thermal vias to spread heat to internal layers
- Place heat-sensitive components away from hot zones
- Use components rated above expected operating temps
- Apply derating charts from datasheets (e.g., output current vs. temperature)

## Real-World Example::

A 3A switching regulator in a 5x5mm QFN package has:

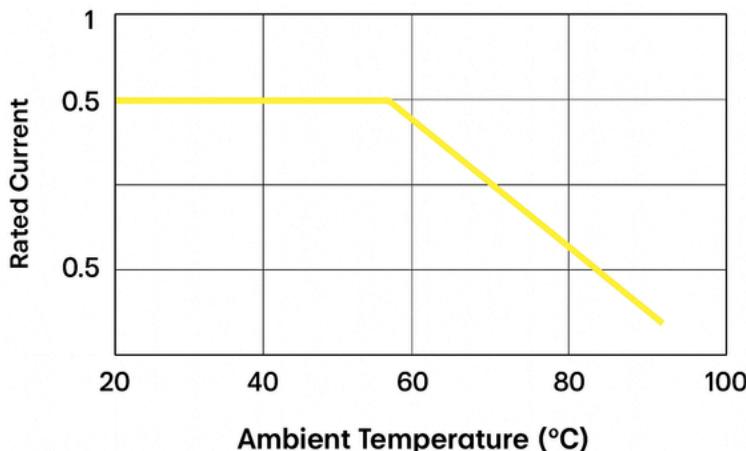
$$T_a = 45^\circ C$$

$$R_{0JA} = 40^\circ C/W$$

$$T_i = 45^\circ C + (40^\circ C/W \times 1.2W) = 93^\circ C$$

$$P_d = 1.2W$$

If maximum  $T_j=125^\circ C$ , it's safe – but any ambient rise requires derating.



## Flat Region (Safe Operating Zone):

- From room temperature (say  $25^\circ C$ ) to a specific threshold (e.g.,  $60^\circ C$ ), the device operates at full rated capacity.
- In this range, no derating is needed.

## Derating Slope:

- After this threshold, the output capability drops linearly.
- This drop is due to increased internal temperature caused by poor heat dissipation in compact designs.

## Cutoff Point:

- Beyond a certain temperature (e.g.,  $85^\circ C$  or  $105^\circ C$ ), the component may shut down (thermal protection), or the manufacturer recommends no operation.

# DC POWER DESIGN PARAMETERS

## 07. Protection Features

Protection features are essential in DC power supply design to safeguard the system, load, and the power source from faults like excessive current, voltage spikes, or short circuits. These protections improve system reliability, prevent damage, and ensure user safety.

### OCP – Over-Current Protection

Prevents damage caused by **excessive load current** which could overheat or damage the power supply or the load.

#### How it works:

- Monitors output current continuously.
- If current exceeds the preset threshold, the output is:
  - Clamped (constant current limiting), or
  - Shut down (latch-off or hiccup mode).

#### Common Setting:

- Set slightly above the maximum rated current (e.g., for a 5A rail, OCP at 6A).

### OVP – Over-Voltage Protection

Prevents damage due to **unexpected high output voltages**, which could destroy sensitive components.

#### Causes:

- Faulty feedback loop
- Failure of regulation circuitry

#### How it works:

- Monitors output voltage.
- If voltage rises above a safe limit, output is:
  - Clamped using crowbar circuits or zener clamps, or
  - Turned off instantly.

#### Common Setting:

- 10–15% above nominal output voltage (e.g., for a 5V supply, OVP triggers at ~5.5–5.75V).

# DC POWER DESIGN PARAMETERS

## SCP – Short Circuit Protection

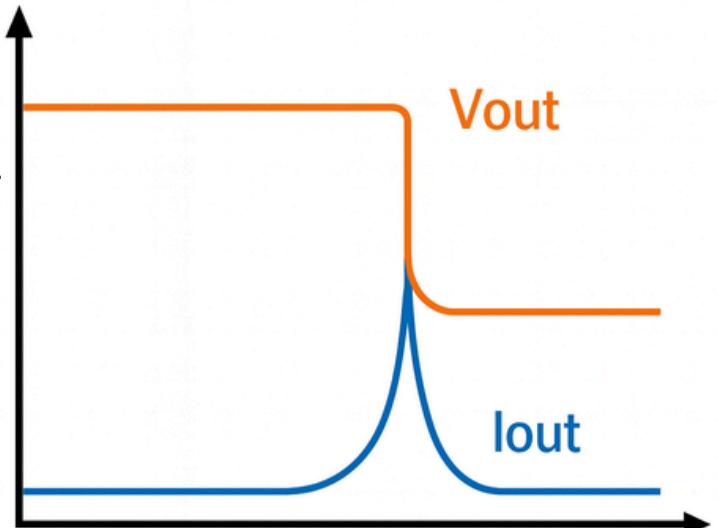
Activates when output terminals are directly shorted ( $V_{out} \approx 0V$ ), drawing excessive current.

### How it works:

- Instant current rise is detected.
- Controller:
  - Cuts off the output (latch-off), or
  - Tries to restart in intervals (hiccup mode) until short is cleared.

### Importance:

- Prevents power source overheating
- Avoids burnt traces or blown components



## Common Implementation Modes

Mode	Behavior
Hiccup Mode	Shuts down temporarily, tries restarting at intervals
Latch-Off Mode	Shuts down until power is recycled or reset is applied
Foldback Mode	Gradually reduces output current as output voltage falls (used in OCP)

### Design Tip:

When designing or selecting a DC power supply, always verify:

- OCP trip point and response time
- OVP clamping accuracy
- SCP behavior (especially in compact or sensitive systems)

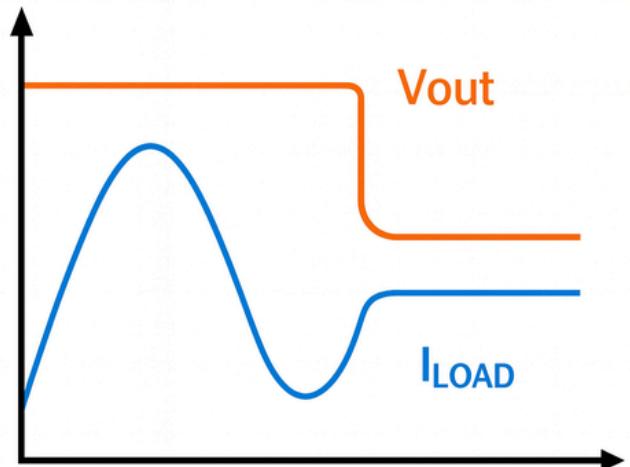
## 08. Stability Across Load Transients

Stability across load transients refers to a power supply's ability to maintain output voltage within acceptable limits when the load changes rapidly – without oscillation, overshoot, or undershoot that could cause malfunction or damage.

This is critical in digital systems where processors, FPGAs, or peripherals frequently switch between low and high current modes (sleep to active state).

### Why It Matters

- Prevents voltage overshoot (which can exceed component ratings)
- Avoids undershoot (which can cause logic failures or resets)
- Maintains system reliability, data integrity, and signal timing
- Essential for low-voltage high-speed logic (e.g., 1.2V, 3.3V rails)



### Key Challenges

Factor	Effect During Load Transients
High loop gain	Can lead to instability if not compensated well
Slow feedback loop	Causes delayed response to fast load steps
Poor PCB layout	Induces parasitic inductance and voltage noise
Insufficient decoupling	Causes ripple and bounce in power rail

### Performance Goals:

Parameter	Target Value
Output voltage deviation	< $\pm 5\%$ of nominal
Settling time	< 100 $\mu s$
No oscillations	$\geq 45^\circ$ phase margin in control loop

# DC POWER DESIGN PARAMETERS

## Formula (Simplified Voltage Deviation)

$\Delta V$  = Voltage deviation

$\Delta I$  = Load step current

ESR = Equivalent series resistance of output cap

C = Output capacitance

$t_{response}$  = Time taken for loop to respond

## Techniques to Improve Stability

- **Control Loop Compensation**
  - Tune error amplifier and compensation network (Type II / III)
  - Ensure phase and gain margins are within safe limits
- **Fast Feedback Path**
  - Use low-latency control loops or digital controllers (e.g., D-CAP, COT)
- **Output Capacitor Selection**
  - Use low-ESR capacitors for high-frequency response
  - Mix bulk (e.g., tantalum) and ceramic capacitors
- **Current Sensing & Peak Control**
  - Use accurate current sensing for peak current mode control
- **Minimized Parasitics**
  - Compact power/ground loop
  - Place caps close to IC pins

## Example Scenario:

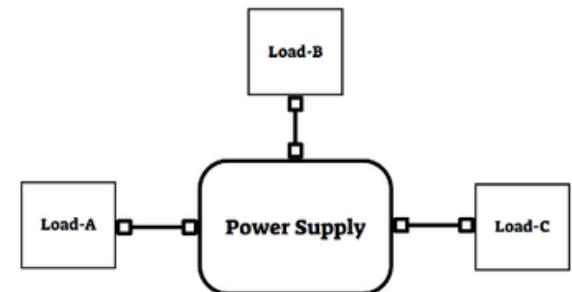
- **System:**
  - 1.2V rail supplying a processor
  - Load step: 1A → 4A in 1 μs
  - Allowable deviation: ±60 mV
- **Solution:**
  - Use 3×22μF ceramic caps with ESR = 3mΩ
  - Design loop with 80 kHz bandwidth
  - Verify transient performance using oscilloscope or power supply simulator

# 03. POWER DISTRIBUTION CONCEPTS

- 01 - Star Topology
- 02 - Daisy Chain
- 03 - Multi-Layer Approach
- 04 - Distributed Architecture

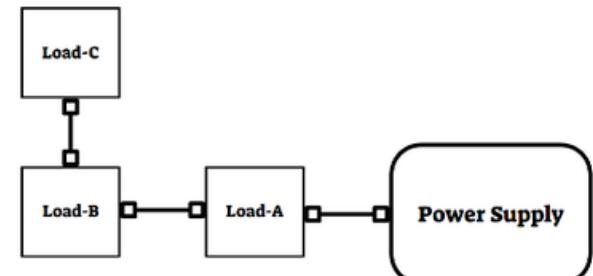
## Star topology

- **Description:** Single power source
- **Advantages:** Minimal interaction between loads
- **Disadvantages:** More copper, higher resistance, Noise



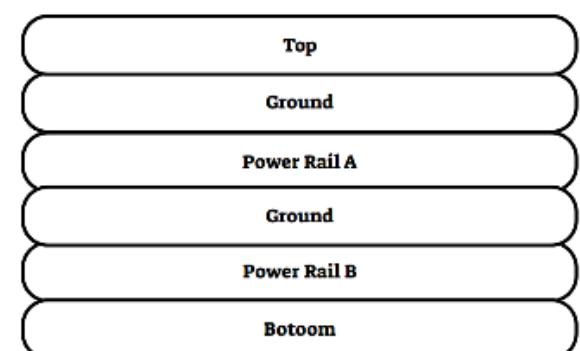
## Daisy chain

- **Description:** Power connects to load then to next one
- **Advantages:** Simpler routing
- **Disadvantages:** Voltage drops accumulate along chain



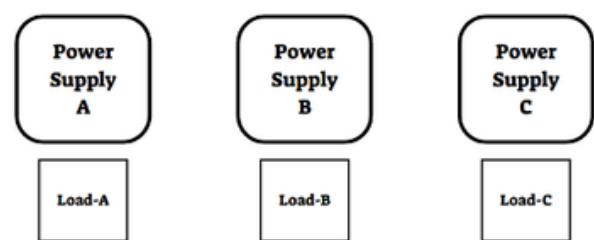
## Multi-layer approach

- **Description:** Dedicated power planes in PCB
- **Advantages:** Low impedance, excellent current handling
- **Disadvantages:** Increased complexity and cost



## Distributed architecture

- **Description:** Multiple power sources near loads
- **Advantages:** Reduced distribution losses
- **Disadvantages:** Coordination complexity, components



# 04. DESIGN BEST PRACTICES

- 01 - Soft-Start Sequencing
- 02 - Dynamic Load Handling
- 03 - Current Sharing in Multi-Phase Designs
- 04 - Thermal Management in Compact Layouts
- 05 - Feedback Loop Stability
- 06 - Component Selection and Derating
- 07 - Efficiency Optimization

## 01 – Soft-Start Sequencing

Soft-start sequencing is a controlled method to gradually ramp up the output voltage of a power supply during startup. This avoids sudden inrush currents that can damage components, trip protection circuits, or create voltage dips.

### Why It's Important:

- Prevents inrush current through large output capacitors
- Avoids overstressing power FETs or the load
- Reduces EMI caused by sudden voltage application
- Enables proper sequencing between multiple power rails

### How It Works:

Most power ICs have a soft-start (ss) pin. Connecting a capacitor ( $C_{SS}$ ) to this pin sets the startup ramp time.

$$T_{SS} = \frac{C_{SS} \times 0.6}{I_{SS}}$$

$T_{SS}$  = Soft start time

$C_{SS}$  = Soft start capacitor value

$I_{SS}$  = Internal current source (usually in  $\mu A$ )

### Design Tips:

- Use larger soft-start capacitors for slower, gentler ramps (e.g.,  $1\mu F \rightarrow$  several ms).
- Some controllers support tracking or sequencing, allowing multiple supplies to start in order.
- A typical startup time: 1 ms to 10 ms, depending on load sensitivity.

# 04. DESIGN BEST PRACTICES

## 02 – Dynamic Load Handling

Dynamic Load Handling refers to the power supply's ability to maintain a stable output voltage when the load changes rapidly — such as sudden increases or decreases in current demand from the connected circuitry.

### Why It's Important:

- In real-world applications (e.g., processors, FPGAs, RF systems), loads are rarely static.
- Sudden current demands can cause voltage dips (undershoot) or overshoots, affecting system stability.
- Poor dynamic response can lead to malfunction, timing errors, or even hardware damage.

### Key Parameters:

- **Transient Response Time ( $t_{tr}$ ):** Time taken for the output voltage to recover to within a specified error band (e.g.,  $\pm 5\%$ ) after a step change in load.
- **Voltage Deviation ( $\Delta V$ ):** The amount by which the voltage dips or overshoots during the transient.

$$\Delta V = \frac{I_{STEP}}{C_{OUT}} \times \Delta t$$

$I_{STEP}$  = Change in load current

$C_{OUT}$  = Output Capacitance

$\Delta t$  = Time during which the loop hasn't fully responded

This equation highlights that larger output capacitance helps absorb current surges, reducing voltage dip.

### Design Guidelines:

- Use low ESR capacitors (e.g., ceramic) for faster response.
- Ensure fast feedback compensation in the control loop.
- Use bulk capacitance to buffer high-current transients.
- Consider pre-bias startup and tracking if dealing with multiple rails.

### Example:

- If a 3.3V regulator supplies a load that jumps from 0.5A to 2A in 1 $\mu$ s, with 100 $\mu$ F output capacitance:

$$\Delta V = \frac{1.5}{100 \times 10^{-6}} \times 1 \times 10^{-6} = 15mV$$

→ A manageable dip, assuming good loop compensation.

## 04. DESIGN BEST PRACTICES

### 03 – Current Sharing in Multi-Phase Designs

Current sharing in multi-phase designs refers to the distribution of load current equally across multiple parallel power stages (phases) to improve thermal management, reduce stress on individual components, and enhance overall efficiency.

#### Why It's Important:

- Reduces current through a single inductor or FET, allowing smaller, more efficient components.
- Minimizes thermal hotspots on the PCB by spreading the heat.
- Improves dynamic response, since multiple phases can respond collectively to sudden load changes.
- Reduces input and output ripple currents through phase interleaving.

#### Where It's Used:

- High-power CPUs, GPUs, FPGAs
- Telecom and server power systems
- High-performance voltage regulators (e.g., VCORE rails)

#### Two Common Methods:

##### 1. Passive Current Sharing

- Relies on matching component tolerances (inductors, resistors)
- Simple but less accurate, prone to imbalance

##### 2. Active Current Sharing

- Uses dedicated controllers or digital feedback loops
- Monitors and adjusts each phase to balance current precisely

#### Key Design Parameters:

- **Current imbalance (%)**: Acceptable tolerance between phases (typically <10%)
- **Inductor DCR or current sense resistor matching**: Ensures accurate sensing for feedback
- **Phase Interleaving**: Phases are time-shifted to reduce overall ripple

$$I_{\text{Total}} = I_1 + I_2 + \dots + I_n \quad \text{where ideally} \quad I_1 = I_2 = \dots = I_n$$

#### Example:

- A 60A core rail uses a 4-phase buck converter:
- Each phase ideally handles 15A
- If not balanced, one phase might overheat or trigger protection earlier
- Active current sharing IC ensures automatic load balance

# 04. DESIGN BEST PRACTICES

## 04 – Thermal Management in Compact Layouts

In compact electronic systems, thermal management becomes critically important due to high power density and limited airflow. If not handled properly, excess heat can degrade performance, shorten component life, or cause thermal shutdowns.

### Why It's Important:

- Prevents thermal runaway in power-dense circuits
- Maintains regulation accuracy of power supplies
- Ensures long-term reliability and reduces MTBF (Mean Time Between Failures)
- Complies with thermal derating guidelines from component datasheets

### Techniques for Thermal Management:

#### 1. Use of Thermal Vias:

- Vias under power ICs (e.g., MOSFETs, regulators) transfer heat to internal or bottom copper layers.
- Ensures heat spreads across multiple layers.

#### 2. Wider Copper Traces & Copper Pours:

- Use thick, wide copper planes connected to heat-generating pads.
- Create thermal "islands" to distribute heat evenly.

#### 3. Heatsinks and Thermal Pads:

- Attach small passive heatsinks to high-power components.
- Use thermal pads for direct heat conduction to chassis.

#### 4. Component Placement Optimization:

- Keep heat-generating components (like FETs, inductors) spaced to prevent hot spots.
- Avoid clustering power devices near sensitive analog ICs.

#### 5. Board Layer Stack-Up:

- Use 4+ layer stack-ups with inner ground planes for heat spreading.
- Place power traces on outer layers for better heat dissipation.

#### 6. Airflow Considerations:

- Orient heat-generating components along natural airflow paths.
- Add vents or use forced air (fans) if needed.

#### 7. Thermal Interface Materials (TIM):

- Use between components and heat spreaders/heatsinks to improve contact and conduction.

$$T_j = \text{Junction Temperature} (\text{°C})$$

$$T_a = \text{Ambient Temperature} (\text{°C})$$

$$R_{0JA} = \text{Junction - to - ambient thermal resistance} (\text{°C/W})$$

$$P_d = \text{Power dissipated (W)}$$

# 04. DESIGN BEST PRACTICES

## 05 – Feedback Loop Stability

Feedback loop stability is a crucial aspect of power supply design that ensures your voltage regulator or converter responds accurately and predictably to changes in load or input voltage without oscillation or sluggish response.

### Why It's Important:

- Maintains output voltage regulation during dynamic load or line changes.
- Prevents oscillations and system instability.
- Ensures fast and controlled transient response.
- Critical for DC-DC converters, LDOs, and SMPS.

### Key Concepts:

#### 1. Loop Gain ( $A \times \beta$ ):

- Product of open-loop gain ( $A$ ) and feedback factor ( $\beta$ ).
- Must be  $< 1$  at  $180^\circ$  phase shift to avoid instability.

#### 2. Phase Margin (PM):

- Angle by which the phase is greater than  $-180^\circ$  when gain crosses 0 dB.
- Recommended:  $\geq 45^\circ$  for good stability.

#### 3. Gain Margin (GM):

- Amount by which the gain is below 0 dB when phase is  $-180^\circ$ .
- Recommended:  $\geq 10$  dB.

#### 4. Bode Plot Analysis:

- Gain vs. Frequency and Phase vs. Frequency are plotted.
- Used to evaluate loop response and margins.

### Types of feedback:

- **Voltage mode:** Simpler, faster response
- **Current mode:** Better line regulation, inherent current limiting

### Loop compensation methods:

- **Type I:** Single pole compensation
- **Type II:** Zero-pole pair compensation
- **Type III:** Two zero-pole pairs

### Stability Design Example Formula:

$$f_c \approx \frac{1}{2\pi R_c C_c}$$

## 04. DESIGN BEST PRACTICES

### Stability Parameters:

- **Phase margin:** 45–60° minimum
- **Gain margin:** >10dB
- **Crossover Frequency (fc):** Where gain crosses 0 dB. Should be 1/10th to 1/5 of the switching frequency.
- **Compensation Pole/Zero Placement:** Design compensation networks (Type I/II/III) using resistors and capacitors to shape loop response.

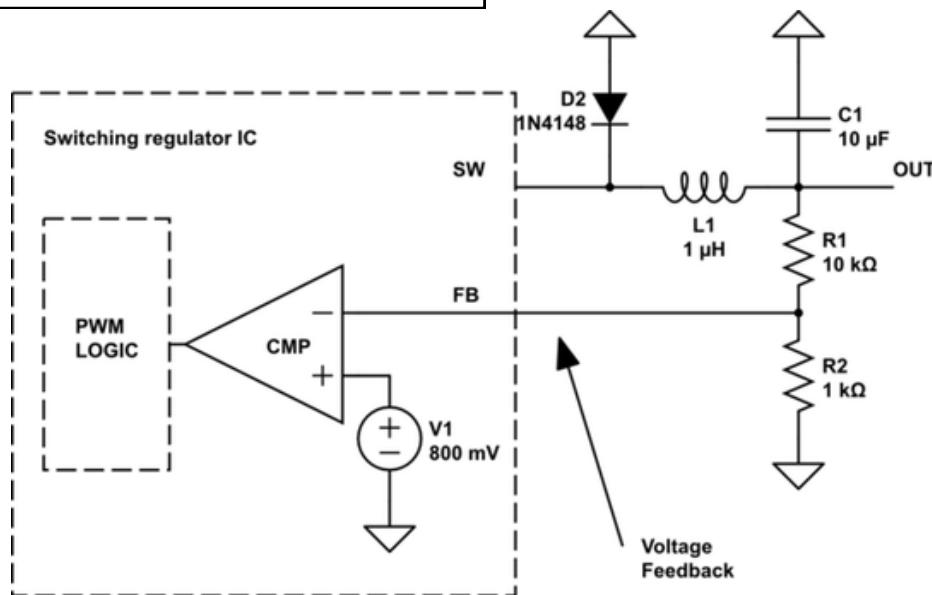
### Best Practices:

- Always verify loop stability with Bode plots.
- Leave adequate margin for component tolerances and temperature variations.
- Match compensation to the output filter characteristics (L and C values).

### Example: From TI's TPS5xxxx Family:

This circuit uses a voltage divider ( $R_1, R_2$ ) to provide feedback to the error amplifier (FB pin), which compares it with an internal reference (800 mV). The regulator adjusts the PWM to maintain a stable output voltage using the equation:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB}$$



ensuring accurate closed-loop control.

# 04. DESIGN BEST PRACTICES

## 06 – Component Selection and Derating

Component selection and derating is the process of choosing components that exceed the system's maximum expected electrical, thermal, and mechanical stress, then operating them below their rated limits to improve reliability, lifespan, and performance.

### Why It's Important:

- Reduces risk of failure due to over-voltage, over-current, over-temperature, etc.
- Improves long-term reliability in harsh or high-temperature environments.
- Supports Design for Reliability (DFR) and compliance with safety standards.
- Helps handle component tolerances, aging, and manufacturing variations.

### Common Derating Guidelines (Typical Values):

Comp Type	Parameter	Derating (%)	Example
Capacitors	Voltage	50–70%	10V part used for 5V application
Inductors	Current	20–30%	4A rated used at max 3A
Resistors	Power Dissipation	50%	1W resistor used at $\leq 0.5W$
MOSFETs	V <sub>ds</sub> and I <sub>d</sub>	20–30%	100V part used for 70–80V
Diodes	Reverse Voltage/Current	25–50%	1A diode used at $\leq 0.5A$
Connectors	Current	50–80%	5A connector used at $\leq 3A$

### How to Select Components:

- **Understand Operating Conditions:** Voltage, current, frequency, temperature, mechanical shock
- **Add Safety Margins:** Apply derating factors to rated specs
- Check Environmental Factors: Vibration, altitude, humidity, corrosive atmosphere
- **Review Datasheets Thoroughly:** Look for thermal resistance, reliability curves, and safe operating areas
- **Use Application Notes and Manufacturer Guides:** Many vendors like Murata, Vishay, TI provide derating charts

## 04. DESIGN BEST PRACTICES

### Power switches (MOSFETs/BJTs):

- RDS(on) vs. gate charge tradeoff
- Thermal resistance
- Max Current

### Inductors:

- Saturation current rating
- DCR (DC resistance)
- Core material (ferrite vs. powder iron)
- Physical size vs. efficiency

### Capacitors by type:

Cap Type	ESR	ESL	Capacitance	Cost
Ceramic	Very low	Low	Small–Medium	Low
Aluminum	Medium	High	Large	Low
Polymer	Low	Medium	Medium–Large	Medium
Tantalum	Medium	Medium	Medium	Medium

### Diodes:

- Forward voltage drop
- Reverse recovery time
- Thermal considerations
- Schottky vs. ultrafast recovery

### Design Tips:

- Always consider temperature derating along with electrical stress
- For mission-critical systems (medical, automotive, aerospace), follow mil-spec or IPC guidelines
- Apply component derating early in design, not as a late fix

## 04. DESIGN BEST PRACTICES

### 07 – Efficiency Optimization

Efficiency Optimization is crucial in power supply design to reduce power loss, manage heat, extend battery life, and meet regulatory standards. High-efficiency designs deliver more power to the load while minimizing the energy wasted in conversion and regulation.

#### Why It's Important:

- Minimizes Heat Generation: Reduces the need for large heatsinks and improves reliability.
- Extends Battery Life: Especially critical in portable and IoT devices.
- Improves Overall System Performance: Lower thermal stress improves component longevity.
- Meets Regulatory Requirements: Efficiency standards like ENERGY STAR, DOE, etc.

#### Key Methods for Optimization:

- **Select High-Efficiency Topologies:**
  - Prefer switch-mode designs (e.g., buck, boost) over linear regulators when dropout and ripple tolerance allow.
  - Use synchronous converters to reduce diode losses.
- **Minimize Switching and Conduction Losses:**
  - Use MOSFETs with low  $R_{DS(on)}$  and fast switching characteristics.
  - Choose appropriate switching frequency to balance size and loss.
- **Optimize Inductor and Capacitor Selection:**
  - Choose components with low ESR and core losses.
  - Ensure minimal DCR (DC Resistance) for inductors.
- **Use Proper Gate Drive Techniques:**
  - Avoid under- or over-driving power MOSFETs to reduce transition losses.
- **Enable Power-Saving Modes:**
  - Use burst mode, skip mode, or pulse-frequency modulation (PFM) in light-load conditions.
- **Layout Considerations:**
  - Reduce trace resistance and loop areas for switching paths.
  - Optimize thermal dissipation for less power wasted as heat.
- **Synchronous rectification:** Replace diodes with MOSFETs
- **Variable frequency operation:** Reduce switching at light loads
- **Gate drive optimization:** Match driver strength to MOSFET

## 04. DESIGN BEST PRACTICES

$$\text{Efficiency } (\eta) = \left( \frac{P_{out}}{P_{in}} \right) \times 100\%$$

### Loss mechanisms:

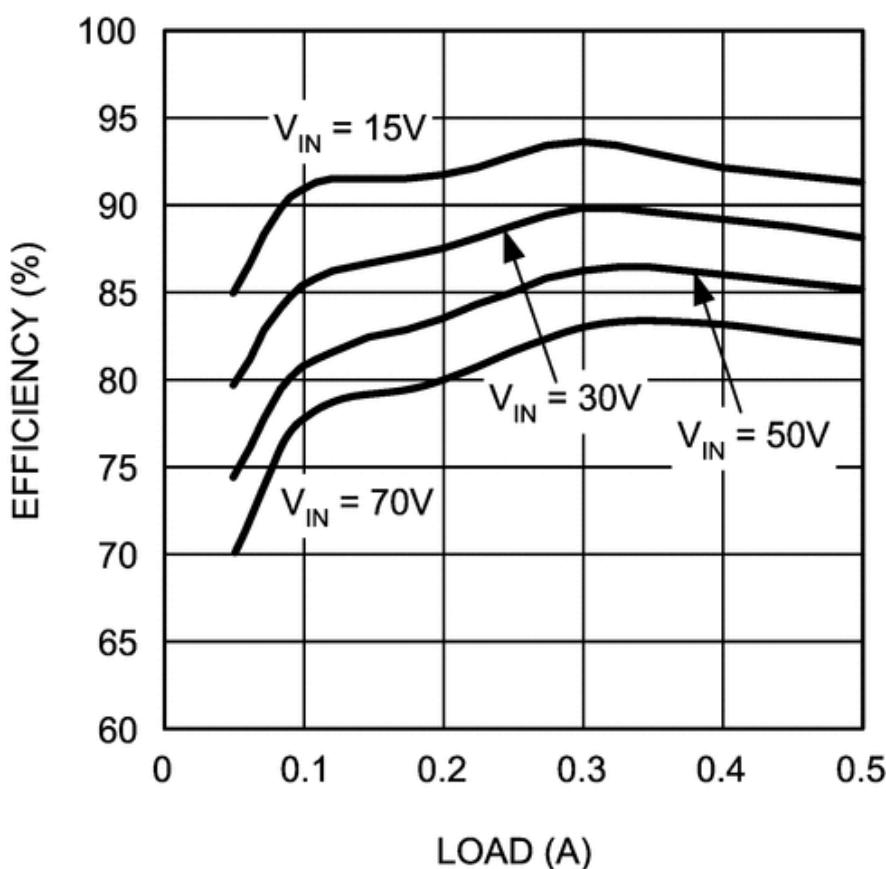
- **Conduction losses:**  $I^2R$  losses in switches, inductors
- **Switching losses:**  $CV^2f$  losses during transitions.

### Impact of switching frequency:

- **Higher frequency:** Smaller components, higher switching losses
- **Lower frequency:** Larger components, lower switching losses
- Optimal range depends on application

### Select Proper Regulator:

- Power supply efficiency drops low currents.
- Select a regulator that delivers peak efficiency within your app operating range. In this case, optimal efficiency occurs around 300 mA with input voltage below 15 V



# 05. EMI/EMC COMPLIANCE DESIGN

- 01 - PCB Layout for Minimum Loop Area
- 02 - Proper Grounding and Shielding
- 03 - Input/Output Filtering Techniques
- 04 - Return Path Control
- 05 - Adherence to CISPR and IEC EMC Standards

Designing for EMI and EMC is crucial to ensure that a power supply does not emit noise that interferes with other systems, and it must also tolerate noise from external sources.

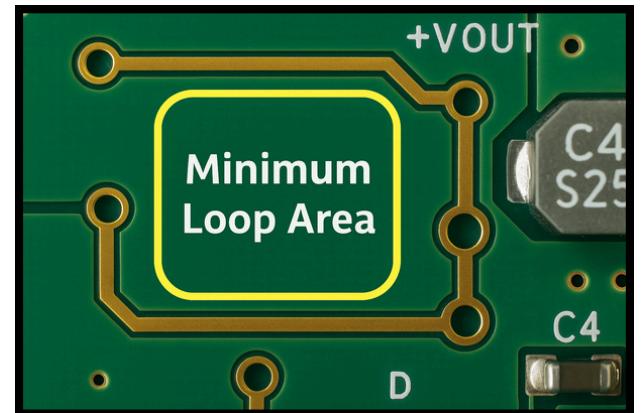
## 01 – PCB Layout for Minimum Loop Area

**Why it matters:** High-frequency switching currents form loops that can radiate EMI.

**Best Practice:** Minimize loop area between high  $di/dt$  paths (e.g., switch node, input cap, MOSFET).

### Tips:

- Place input capacitor close to high-side switch.
- Route return paths directly under signal paths.



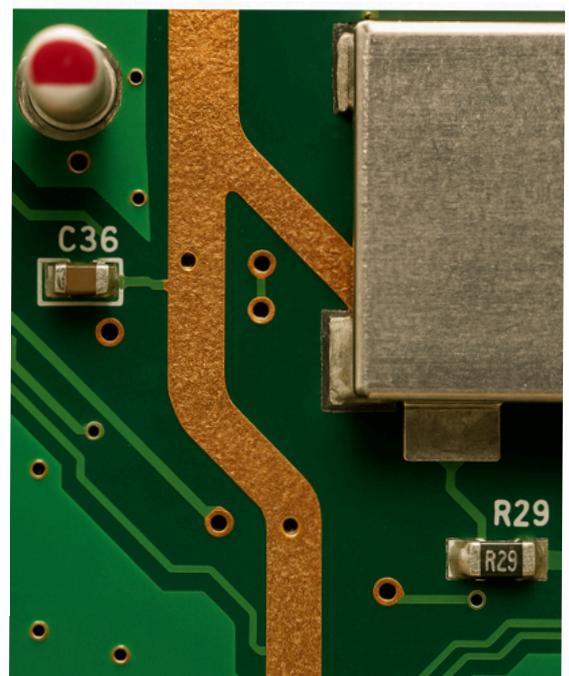
## 02 – Proper Grounding and Shielding

**Objective:** Prevent conducted and radiated emissions.

### Grounding Types:

- Single-point ground: Good for low-frequency analog circuits.
- Multi-point ground: Suitable for high-frequency designs.

**Shielding:** Use grounded copper planes or metal enclosures to isolate EMI-sensitive areas.



# 05. EMI/EMC COMPLIANCE DESIGN

## 03 – Input/Output Filtering Techniques

**Purpose:** Attenuate high-frequency noise from power supply and external cables.

### Techniques:

- LC filters at input/output.
- Common-mode chokes to suppress differential/radiated noise.
- Ferrite beads to block high-frequency EMI.

## 04 – Return Path Control

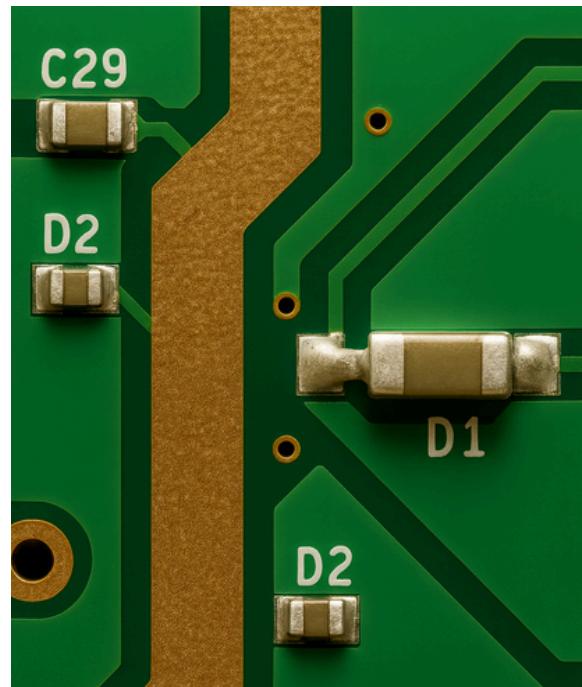
**Key Idea:** Signal currents seek the lowest impedance return path.

### Design Goal:

Ensure return paths are:

- Wide and continuous (on solid planes).
- Avoid split planes under high-speed or switching nodes.

**Helps reduce:** Ground bounce, loop inductance, and radiated emissions.



## 05 – Adherence to CISPR and IEC EMC Standards

### Common Standards:

- CISPR 22 / CISPR 32: Emission requirements for IT and multimedia equipment.
- IEC 61000 series: Immunity standards (e.g., ESD, EFT, surge).

### Design Strategy:

- Perform EMI pre-compliance testing.
- Use shielded enclosures, EMI gaskets, and filtering connectors when needed.

# 06. THERMAL DESIGN BEST PRACTICES

- 01 - Copper Pour and Thermal Vias
- 02 - PCB as Heatsink
- 03 - Hot Spot Mitigation
- 04 - Natural Convection Spacing

Effective thermal design in power electronics ensures reliable performance, longevity, and safety. Heat must be efficiently conducted away from power-dissipating components to maintain optimal operating conditions.

## 01 – Copper Pour and Thermal Vias

### Copper Pour:

- Use wide copper planes around heat-generating components.
- Helps spread and dissipate heat laterally.

### Thermal Vias:

- Provide vertical heat conduction from top to inner/bottom layers.
- Typically filled or tented in high-density boards.
- 10mil filled via reduces thermal resistance by ~15%
- Optimum placement: directly under thermal pad
- Array patterns outperform single large vias

### Formula Reference:

- Thermal conductivity of copper:  $k_{\text{Cu}} \approx 385 \text{ W/m}\cdot\text{K}$
- Resistance through vias:  $R_{\text{th}} = \frac{t}{k \cdot A}$  (t is via height, A is cross-sectional area.)

## 02 – PCB as Heatsink

**Strategy:** Use thick copper layers and large ground planes to act as a passive heatsink.

**Benefit:** Reduces need for external heatsinks in compact designs.

**Note:** 2 oz or 3 oz copper increases conduction but impacts cost and etching accuracy.

### PCB as "Heatsink":

- 1oz copper, 1in<sup>2</sup> area ≈ 70°C/W
- 2oz copper, 1in<sup>2</sup> area ≈ 35°C/W
- 4oz copper, 1in<sup>2</sup> area ≈ 18°C/W

# 06. THERMAL DESIGN BEST PRACTICES

## 03 – Hot Spot Mitigation

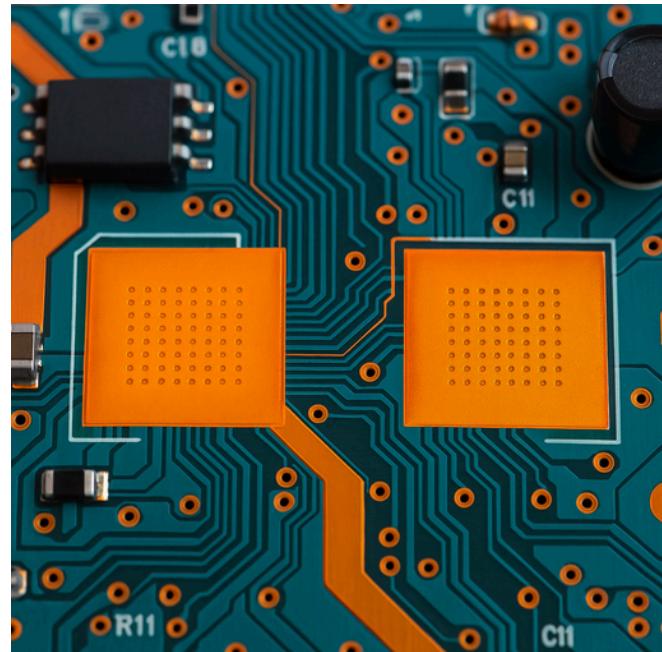
**Objective:** Prevent localized overheating that leads to failure.

### Best Practices:

- Distribute power components evenly.
- Use thermal interface materials (TIMs) for heat-spreading ICs.
- Avoid stacking multiple heat sources near each other.

## 02 – PCB as Heatsink

**Definition:** Natural airflow between components allows passive cooling without fans.



### Guidelines:

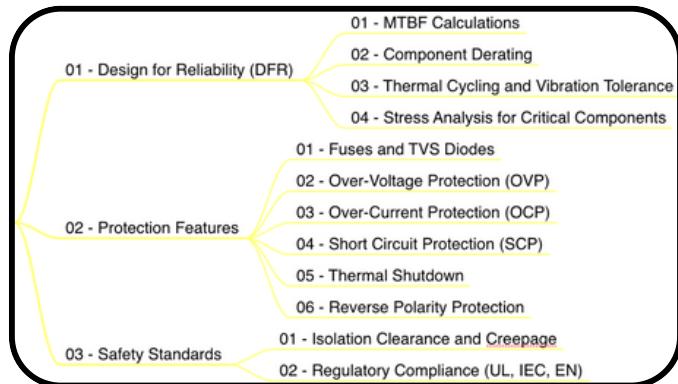
- Maintain 2–3 mm spacing between hot components.
- Orient heat sources vertically when possible (chimney effect).
- Leave air gaps around high-power devices.

### Thermal resistance chain:

- Junction-to-case ( $\theta_{JC}$ ): 1–5°C/W for power devices
- Case-to-heatsink ( $\theta_{CS}$ ): Depends on interface material
- Heatsink-to-ambient ( $\theta_{SA}$ ): 1–30°C/W based on size/airflow

## 07. SAFETY, PROTECTION & DESIGN FOR RELIABILITY (DFR)

Designing robust power systems requires not just performance optimization but ensuring safety, long-term reliability, and protection against abnormal events. This block addresses both proactive and reactive design strategies.



### Design for Reliability (DFR)

Design for Reliability focuses on ensuring that a power supply operates safely, consistently, and over the intended lifecycle of the product, even under harsh or varying environmental conditions.

#### 1. MTBF Calculations (Mean Time Between Failures):

- It quantifies the expected reliability of a system.
- Higher MTBF indicates better reliability.

$$\text{MTBF} = \frac{\text{Total Operational Time}}{\text{Number of Failures}}$$

#### 2. Component Derating:

- Operating components below their maximum rated limits (voltage, current, temperature) to extend lifespan and reduce failure rates.
- Example: Using a 50 V capacitor in a 24 V circuit for safety margin.

#### 3. Thermal Cycling and Vibration Tolerance:

- Designs must withstand repeated thermal expansion and mechanical stress.
- Includes selecting components with strong solder joints and using conformal coating or mechanical reinforcement where needed.

#### 4. Stress Analysis for Critical Components:

- Identifies components under electrical, thermal, or mechanical stress.
- Uses simulation or margin testing to ensure long-term performance.

# 07. PROTECTION FEATURES

## 01. Fuses and TVS Diodes

### 1. Fuses (Overcurrent Protection):

Fuses protect circuits by interrupting the current path when the current exceeds a safe predefined threshold.

**How it works:** A thin wire inside the fuse melts when excessive current flows, breaking the circuit.

**Types of Fuses:** Fast-Blow Fuses – respond quickly to short circuits.

- Slow-Blow (Time Delay) Fuses – tolerate brief overcurrent (e.g., inrush current).

**Placement:** Usually placed at the power input line.

**Reset:** Fuses are one-time protection devices (unless a resettable PTC is used).

**Formula (for selection):**

$$I_{rated} = I_{load} \times 1.25$$

Choose a fuse rated 25% above the normal operating current to avoid nuisance tripping.

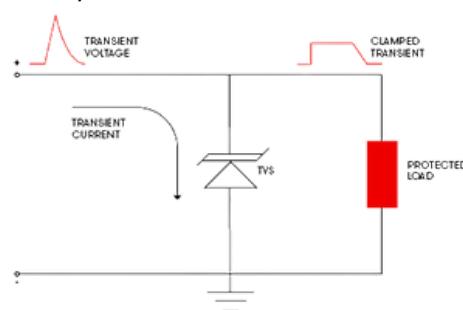


### 2. TVS Diodes (Surge & ESD Protection):

TVS diodes clamp voltage spikes from transients like ESD, lightning, or inductive switching.

- **How it works:** When voltage exceeds the breakdown voltage of the TVS, it turns on and shunts the excess energy to ground.
- **Response time:** Extremely fast (<1 ns), ideal for ESD and EFT (Electrical Fast Transient) protection.
- **Placement:** Across input/output lines, near connectors or sensitive components.
- **Key Parameters:**

- Breakdown Voltage (VBR)
- Clamping Voltage (VC)
- Peak Pulse Current (IPP)



## 07. PROTECTION FEATURES

### 02. Over-Voltage Protection (OVP)

Over-Voltage Protection (OVP) is a safety feature used to prevent damage to sensitive electronic components when the output voltage exceeds a defined safe level.

- OVP detects if the output voltage rises above a preset threshold.
- It responds by disabling, clamping, or shutting down the power supply to protect the load.
- Essential in protecting ICs, microcontrollers, and communication interfaces.

Type	Functionality
Latch-Off	Powers down permanently until user reset or power cycle.
Auto-Restart	Automatically retries after fault is cleared.
Crowbar Circuit	Uses a thyristor/SCR to short the output and blow a fuse.
Voltage Clamp	Uses a Zener or TVS diode to clamp voltage to a safe limit.

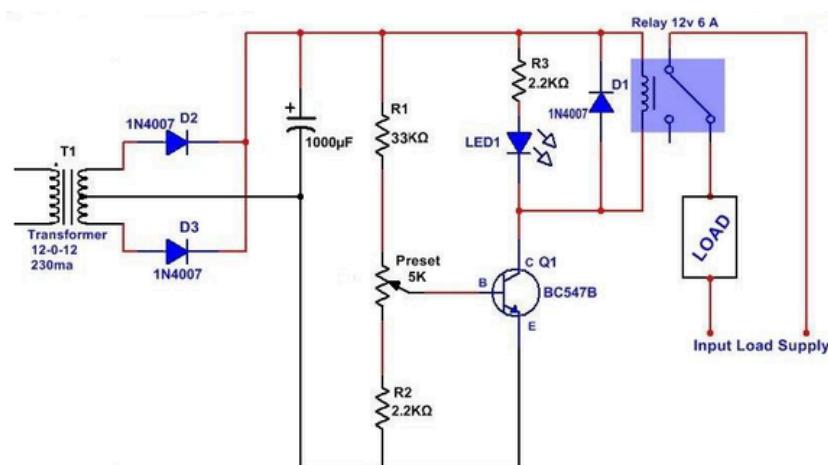
#### Typical Implementation:

- A voltage divider senses the output voltage.
- The sensed value is compared with an internal reference voltage.
- When:  $V_{out} > V_{OVP\_threshold}$  The comparator output activates the shutdown logic  $\text{o}_V_{out} > V_{OVP\_threshold}$  nbar.
- To calculate resistor values for a voltage divider that triggers OVP:

$$V_{OVP} = V_{ref} \times \left( 1 + \frac{R1}{R2} \right)$$

#### Application Use Cases:

- Power rails for microprocessors or FPGAs
- Battery-operated devices (Li-ion protection)
- Power adapters and chargers
- Telecom and automotive supplies



## 07. PROTECTION FEATURES

### 03. Over-Current Protection (OCP)

Over-Current Protection (OCP) is a critical safety feature in power supplies designed to prevent excessive current from damaging components or wiring.

- OCP limits the maximum output current a power supply can deliver.
- If the output current exceeds the predefined limit, the supply reduces or shuts off the output to prevent damage.

#### OCP Response Modes:

Mode	Behavior
Current limiting	Linear reduction of output
Latch-off	Power supply shuts down permanently until manually reset.
Auto-restart / Hiccup	Tries to restart after a delay if the fault persists.
Foldback	Reduces output current to a safe value rather than shutting off.
Constant Current	Maintains constant current even as output voltage drops (used in LED drivers).
Cycle-by-cycle limiting	Pulse-by-pulse control

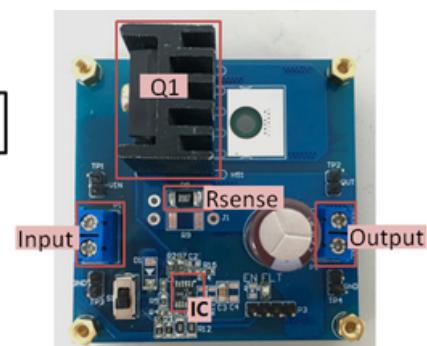
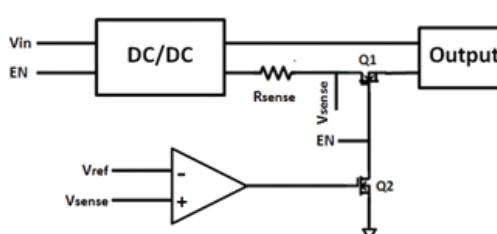
#### Typical Implementation:

- Sense resistor ( $R_{sense}$ ) placed in the current path.
- The voltage across  $R_{sense}$  is compared against a reference.
- If:  $V_{sense} = I_{out} \times R_{sense} > V_{ref}$  Then the protection mechanism activates.
- Example: Suppose the desired current limit is 2A and reference voltage is 100 mV.

$$R_{sense} = \frac{V_{ref}}{I_{limit}} = \frac{0.1}{2} = 0.05 \Omega$$

#### Where It's Used:

- DC-DC converters
- Battery charging circuits
- Motor drivers
- LED power supplies



## 07. PROTECTION FEATURES

### 04. Short Circuit Protection (SCP)

SCP is a critical feature in power supplies that detects and prevents damage when the output is shorted (i.e., the load resistance approaches zero ohms).

- SCP is designed to quickly detect a direct short between output and ground (or between power rails).
- It then limits current or shuts down the power supply, preventing:
  - Component overheating
  - Trace/bond wire damage
  - Fire or safety hazards

#### Typical SCP Strategies:

Method	Action Taken
Latch-off	Disables output until power cycle or reset.
Auto-retry	Periodically checks if short has cleared.
Foldback Current Limit	Reduces current significantly during a short.
Constant Current Mode	Maintains max current regardless of output drop.

#### Basic Implementation:

- SCP usually shares the current sense resistor with Over-Current Protection (OCP).
- When:  $I_{load} \geq I_{SCP}$  The protection logic triggers and disables the switch or output stage.

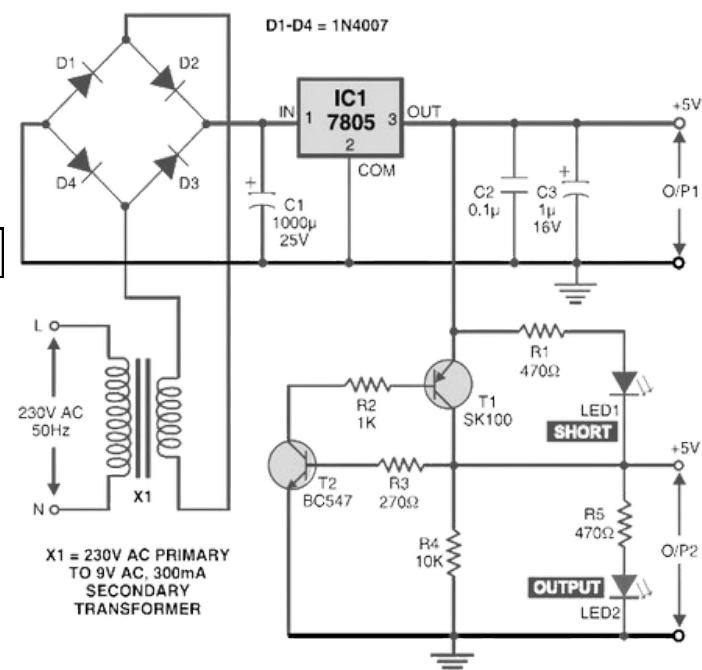
#### Foldback Current Limiting Formula:

- Some designs use a foldback curve to reduce current during short:

$$I_{OUT} = I_{NOM} \times \left( \frac{V_{OUT}}{V_{NOM}} \right) \quad \text{As } V_{OUT} \rightarrow 0, I_{OUT} \rightarrow 0$$

#### Why SCP is Important:

- Prevents catastrophic failure during:
  - Solder bridges
  - Misconnected loads
  - Faulty cables or connectors
- Essential for compliance with safety standards like UL, IEC, and EN.



## 07. PROTECTION FEATURES

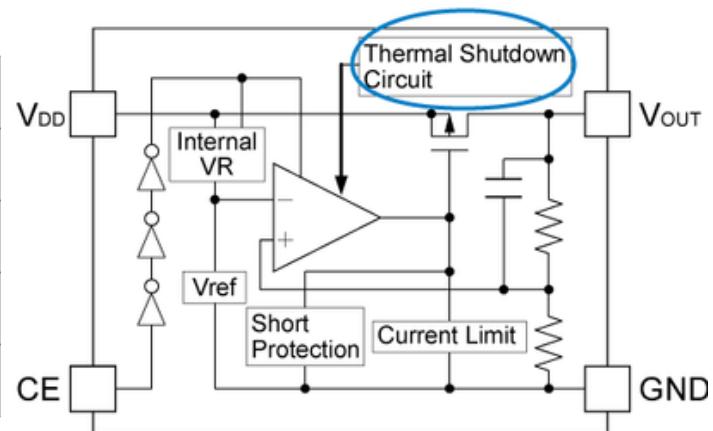
### 05. Thermal Shutdown

Thermal Shutdown is an essential protection mechanism in power supply and IC design that prevents damage due to overheating. When internal temperatures exceed a predefined safe threshold, the circuit automatically shuts down or throttles until the temperature returns to normal.

- A built-in temperature sensor monitors the junction temperature of the IC or power component.
- If the temperature rises above a set limit (typically 150°C to 180°C), the system:
  - Disables switching or output
  - Alerts the controller (in PMICs)
  - Waits for cooling before auto-restart (optional)

#### Typical Behavior

Event	Temperature Range
Normal Operation	< 125°C
Thermal Warning	~125°C – 140°C
Thermal Shutdown	~150°C – 180°C
Auto-Restart (if enabled)	~120°C – 140°C

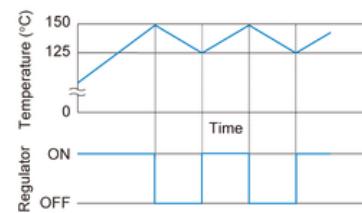
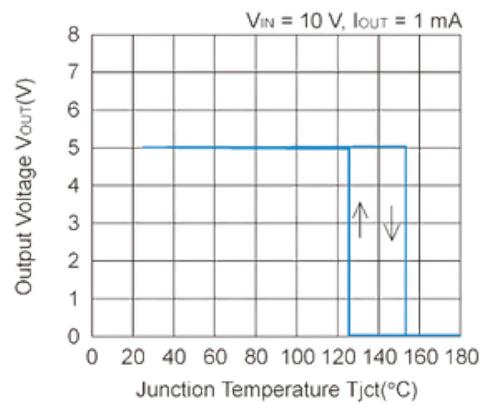


#### How It's Implemented:

- Internal thermal sense circuits in regulators or controllers.
- Shutdown signal disables gate drivers or disables internal power stages.
- In microcontrollers or digital PMICs, it can trigger interrupts or safe states.

#### Why Thermal Shutdown is Critical:

- Prevents permanent damage to semiconductors and passives.
- Protects against:
  - Poor airflow
  - Excessive load
  - Ambient temperature rise
  - Blocked heatsinks or enclosure faults
- Enhances MTBF and long-term system reliability.



## 07. PROTECTION FEATURES

### 06. Reverse Polarity Protection

Reverse Polarity Protection is a design safeguard that prevents damage when the input power connections are accidentally reversed — a common issue in battery-powered or connector-based systems.

- It blocks or redirects current when the power supply's positive and negative terminals are swapped.
- Protects sensitive circuits from reverse voltage, which could otherwise cause:
  - IC burnout
  - Component destruction
  - System malfunction

#### Common Implementation Methods:

Method	Description	Pros	Cons
Series Diode (e.g., 1N4007)	A simple diode in series with input power.	Very simple, low cost	Power loss due to voltage drop (~0.7V for Si)
Schottky Diode	Lower forward voltage drop than silicon diodes (~0.3–0.5V).	Higher efficiency	Limited reverse voltage rating
P-Channel MOSFET	MOSFET in series or reverse direction to block current flow.	Low loss, efficient	Needs gate biasing circuit
Ideal Diode Controller + FET	Uses IC to mimic diode behavior with near-zero loss.	Best performance	Higher cost and complexity

#### Series Diode Example:

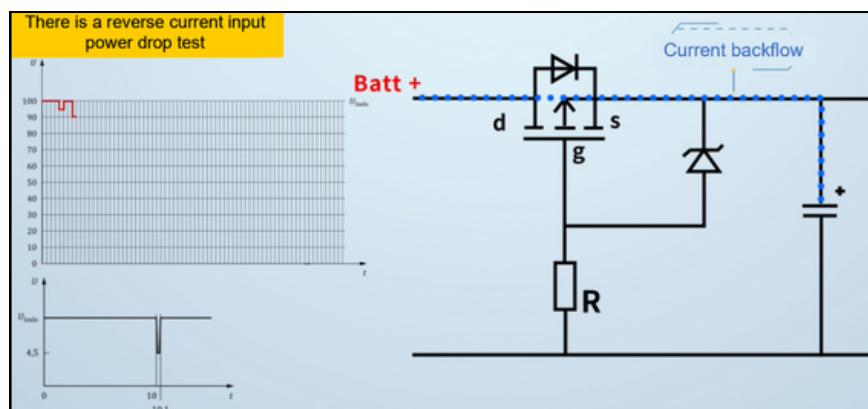
If using a diode like 1N5819:

$$V_{in} = 12V, \quad V_{forward\_drop} \approx 0.3V$$

$$V_{available\_to\_circuit} = 11.7V$$

#### Why It's Important:

- Prevents costly mistakes during installation or battery insertion.
- Mandatory for:
  - Field-deployable systems
  - Consumer electronics
  - Battery-powered or automotive applications



# 08. ENERGY EFFICIENCY TECHNIQUES

These techniques aim to reduce power consumption, increase battery life, and enhance sustainability in both portable and embedded systems.

- 01 - Power Saving Modes for Standby/Idle Conditions
- 02 - Light Load Efficiency Optimization
- 03 - Adaptive Switching Frequency
- 04 - Input Voltage Range Adaptability for Energy Harvesting

## 01 – Power Saving Modes for Standby/Idle Conditions

- Uses low-power or sleep states in microcontrollers and power ICs.
- Example: Enable shutdown mode ( $<1 \mu\text{A}$ ) when no load is active.
- Impact: Extends battery life during inactive periods.

## 02 – Light Load Efficiency Optimization

- Switch-mode converters often perform poorly at low loads.
- Techniques like:
  - Pulse Frequency Modulation (PFM)
  - Burst Mode operation
- These reduce switching losses under light load.

## 03 – Adaptive Switching Frequency

- Switching frequency is adjusted based on load condition:
  - **High load:** Higher frequency for fast response.
  - **Light load:** Lower frequency for reduced losses.
- Improves efficiency across wide load ranges.

## 04 – Input Voltage Range Adaptability for Energy Harvesting

- Efficiently accepts wide or fluctuating input voltages from:
  - Solar panels
  - Piezoelectric/thermoelectric sources
- Enables maximum power point tracking (MPPT) and low start-up voltages.

# 09. DESIGN FOR SCALABILITY & MANUFACTURABILITY

## 01 – Modular Power Architecture:

- Use independent or pluggable power modules for different subsystems.
- Makes power distribution flexible and simplifies system upgrades or modifications.
- Example: Using DC-DC converter modules for each FPGA, SoC, or memory domain.

## 02 – Multi-Voltage Compatibility:

- Ensure the power system supports a wide range of voltage rails (e.g., 1.0V, 1.2V, 3.3V, 5V, 12V).
- Helps integrate diverse components (analog, digital, memory, RF) without major redesign.
- Common in systems with mixed-signal or multi-core processors.

## 03 – Stackable Supply Options:

- Use identical power modules that can be paralleled to increase load capacity.
- Enhances current capability and allows load sharing.
- Often used in high-performance FPGAs, GPUs, and industrial power systems.

## 04 – BOM and DFM Optimization:

- Choose components that are cost-effective and readily available.
- Optimize for Design for Manufacturability (DFM): select parts with good solderability, consistent package types, and minimum variants.
- Avoid components with long lead times or EOL (End-of-Life) status.

## 05 – Component Placement for Automated Assembly:

- Align components in a uniform orientation (e.g., polarity marks in same direction).
- Maintain clearance for pick-and-place machines and reflow ovens.
- Group related components (e.g., decoupling capacitors near ICs) for both function and ease of inspection.

## 06 – PCB Trace Width and Spacing for Manufacturability:

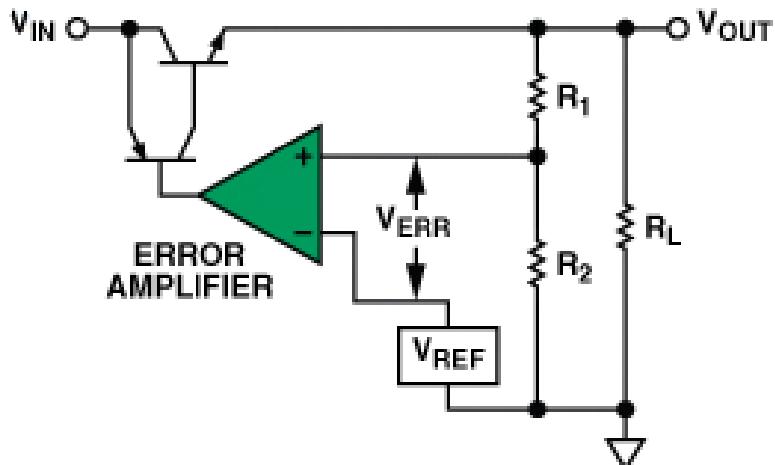
- Use IPC-2221/IPC-2152 standards for trace width vs. current.
- Maintain spacing to prevent solder bridging and improve yield.
- Consider minimum manufacturable width/space from your PCB vendor (e.g., 4/4 mil or 6/6 mil).

# LINEAR REGULATORS (LDO)

A Linear Regulator, specifically a Low Dropout Regulator (LDO), is a simple and widely used DC voltage regulator that maintains a steady output voltage even when the input voltage is just slightly higher than the output.

## Basic Operation:

An NPN or PMOS transistor operates as a variable resistor in series with the load. The output voltage is controlled by comparing a scaled-down version of the output to a reference voltage using an error amplifier.



Voltage Regulation Equation:

$$V_{OUT} = V_{REF} \left( 1 + \frac{R_1}{R_2} \right)$$

## Key Characteristics:

- **Low Dropout Voltage:**

- The minimum difference between input and output voltage can be as low as 100 mV – 500 mV, enabling efficient regulation even with tight voltage margins.

- **Simple Design:**

- Requires minimal external components (just a few capacitors).

- **Low Noise:**

- Excellent for sensitive analog and RF circuits (e.g., ADCs, DACs, audio circuits).

## Advantages:

- Ultra-low output noise: Suitable for RF, audio, and precision analog.
- No switching spikes or EMI: Simplifies PCB layout and filtering.
- Simple implementation: Minimal components needed.
- Fast transient response: Typically 1–5  $\mu$ s.
- Excellent PSRR: Superior noise rejection from supply rail.
- Cost-effective: Particularly at low currents.

# LINEAR REGULATORS (LDO)

## Disadvantages:

- Low efficiency with large voltage drop:
- Dropout Voltage limits operation when VIN is close to VOUT.
- High thermal dissipation:

$$(\eta) = \left( \frac{P_{out}}{P_{in}} \right) \times 100\%$$

$$P_D = (V_{in} - V_{out}) \times I_{out}$$
$$\Delta T = P_D \times \theta_{JA}$$

## Applications:

- Analog/RF loads (op-amps, ADCs, DACs)
- Post-regulation stage after a noisy switcher
- Battery-powered systems (smartphones, wearables)
- Low-IQ standby regulators for MCU/SoC cores
- Noise-sensitive loads in medical or industrial control

## Additional Key Design Considerations:

- **Dropout Definition:** Minimum headroom between input and output required for regulation. “Low-dropout” designs operate even at 100 mV above output.
- **Thermal Shutdown:** Most LDOs include thermal protection (~150–170°C).
- **Reverse Current Protection:** Required when multiple sources are tied to VOUT.
- **Capacitor Requirements:** LDOs need output capacitors (typically 1–10  $\mu$ F) with low ESR for stability. Some require specific ESR ranges.

Parameter	Typical Range
Dropout Voltage	100 mV – 1.5 V
Quiescent Current (IQ)	15 $\mu$ A – 5 mA
Load Regulation	0.01% – 0.5%
Line Regulation	0.02% – 0.5%/V
PSRR @ 100 Hz	60 – 100 dB
Output Noise	< 100 $\mu$ V RMS
Stability Cap Range	1 $\mu$ F to 10 $\mu$ F (typical)

# BUCK CONVERTERS

A Buck Converter is a type of DC-DC switching regulator that steps down a higher input voltage to a lower output voltage while maintaining high efficiency. It operates by rapidly switching a transistor on and off and using an inductor and capacitor to filter and smooth the output.

## Working Principle

A Buck Converter uses the principle of energy storage in an inductor during the ON phase and energy transfer to the load during the OFF phase.

## Operating Modes:

### 1. Switch ON:

- The transistor (MOSFET) connects input voltage  $V_{IN}$  to the inductor.
- Inductor current increases, storing energy as a magnetic field.
- The output capacitor is charged and supplies current to the load.

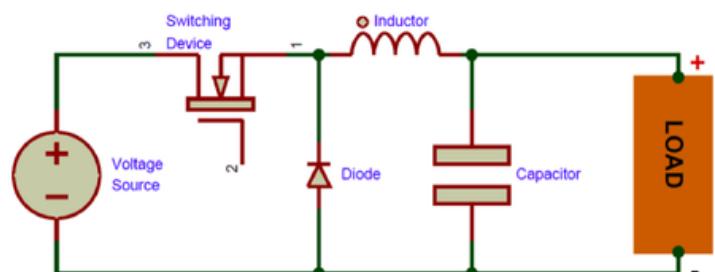
### 2. Switch OFF:

- The transistor turns off.
- The inductor releases its stored energy to the load via the freewheeling diode.
- Inductor current flows through the diode, maintaining current continuity.

## Key Equation:

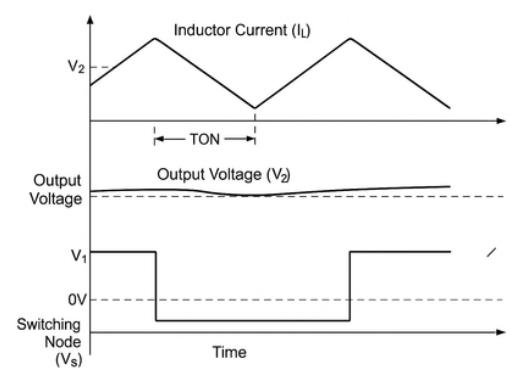
The steady-state output voltage is directly proportional to the input voltage and duty cycle:

$$V_{OUT} = D \times V_{IN}$$
$$\text{Duty Cycle (D)} = \frac{T_{ON}}{T_{ON}+T_{OFF}}$$



## Waveforms

- **Inductor Current ( $I_L$ ):** Ramps up during ON time, ramps down during OFF time
- **Output Voltage ( $V_o$ ):** Nearly constant with small ripple
- **Switching Node ( $V_{sx}$ ):** Square waveform oscillating between 0V and  $V_{IN}$



# BUCK CONVERTERS

## Advantages:

- **High efficiency:** Typically 85–95%, especially at medium and high loads
- **Compact size:** Operates at high frequency, reducing passive component size
- **Lower heat dissipation:** Less power wasted than LDOs
- **Wide operating voltage range:** Flexible for various applications

## Disadvantages

- Generates EMI and noise due to switching
- Requires complex design: compensation network, layout care, filtering
- May produce output ripple if not filtered properly
- Minimum load required for continuous conduction mode

## Component Selection

Component	Function	Design Tip
Inductor (L)	Energy storage, current smoothing	Choose for ~30–40% current ripple
Capacitor (Cout)	Filters output voltage ripple	Low-ESR ceramic types preferred
MOSFET	Main switch	Low R_DS(ON) for higher efficiency
Diode	Freewheeling current path (or use synchronous MOSFET)	Fast recovery, low forward voltage
Controller IC	Controls PWM and regulates voltage	Includes feedback and compensation

## Formulas:

- **Inductor Value (Continuous mode):**

$$L = \frac{(V_{IN} - V_{OUT}) \cdot D}{f_{SW} \cdot \Delta I_L}$$

- **Output Capacitor (for ripple voltage):**

$$C_{OUT} = \frac{\Delta I_L}{8 \cdot f_{SW} \cdot \Delta V_{OUT}}$$

Where:

- $f_{SW}$ : Switching frequency (e.g., 100kHz – 2MHz)
- $\Delta I_L$ : Inductor current ripple
- $\Delta V_{OUT}$ : Output voltage ripple

# BUCK CONVERTERS

## Modes of Operation

- **Continuous Conduction Mode (CCM)**
  - Inductor current never falls to zero – more efficient, steady
- **Discontinuous Conduction Mode (DCM)**
  - Inductor current drops to zero – lower load, simpler control
- **Pulse-skipping:**
  - Cycles skipped at light loads for efficiency
- **Synchronous Buck Converter**
  - Replaces diode with a second MOSFET – improves efficiency, especially at low output voltages

## Applications

- Voltage regulators for CPUs, GPUs, FPGAs
- USB and battery-powered systems
- Industrial and telecom systems
- Embedded and automotive electronics
- Power supply modules in IoT devices

## Performance Summary

Parameter	Typical Value
Efficiency	85–95%
Output Voltage Accuracy	±1–3%
Switching Frequency	100 kHz – 2 MHz
Output Ripple	<50 mV
Output Current Capability	Up to 20A (multi-phase)
Load Transient Response	<50 µs

# BOOST CONVERTERS

A Boost Converter is a type of DC-DC converter that steps up (increases) the input voltage to a higher output voltage while reducing current. It's widely used when the supply voltage is lower than what the load requires.

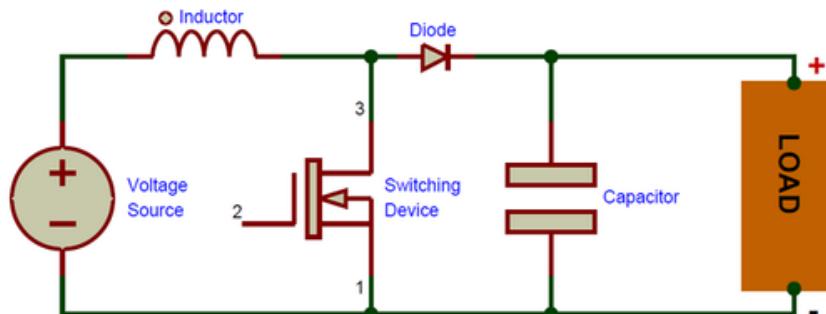
## Operating Phases:

### 1. Switch ON (Charging phase):

- The switch closes.
- Input current flows through the inductor and switch.
- The inductor stores energy in the form of a magnetic field.
- The diode is reverse-biased; the load is powered by the capacitor.

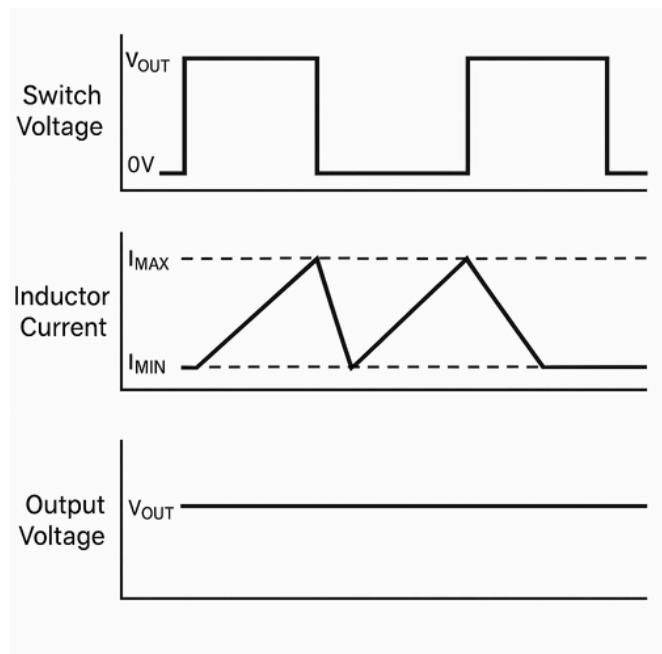
### 2. Switch OFF (Discharging phase):

- The switch opens.
- The magnetic field in the inductor collapses.
- Inductor polarity reverses, forward-biasing the diode.
- Inductor adds to input voltage, pushing energy into the output capacitor and load.



## Waveforms

- **Inductor Current:** Triangle wave during continuous conduction mode (CCM).
- **Switch Voltage:** Pulses from 0V (ON) to output voltage (OFF).
- **Output Voltage:** Constant (regulated), higher than input.



# BOOST CONVERTERS

## Key Formulas

- **Output Voltage:**

$$V_{OUT} = \frac{V_{IN}}{1 - D}$$

Where  $D$  = Duty Cycle ( $0 < D < 1$ )

Where:

- **Inductor Selection:**

$$L = \frac{V_{IN} \cdot D}{f \cdot \Delta I_L}$$

- $f$ : switching frequency
- $\Delta I_L$ : desired inductor ripple current

- **Capacitor selection:**

$$C = \frac{I_{OUT} \cdot D}{f \cdot \Delta V_{OUT}}$$

## Advantages

- Step-up voltage from lower input
- High efficiency (up to 95%)
- Simple and compact

## Disadvantages

- Output voltage always greater than input (no step-down)
- Ripple current and voltage at output
- Requires careful component selection for stability

## Applications

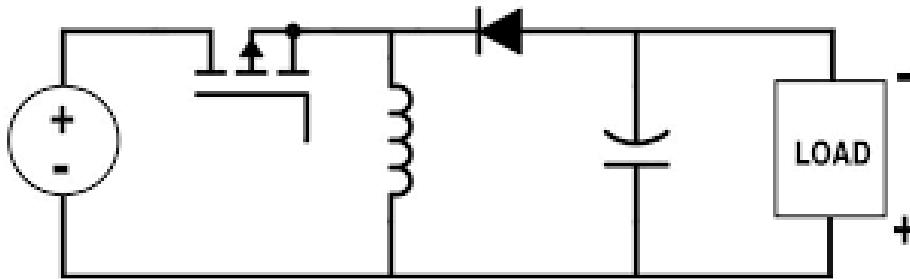
- Battery-powered devices (e.g., powering 5V logic from 3.3V batteries)
- Powering sensors or actuators in IoT systems
- Solar charge controllers
- Automotive electronics (boosting 12V to 24V)

# BUCK-BOOST CONVERTERS

A Buck-Boost Converter is a type of DC-DC converter that can step up or step down the input voltage depending on the duty cycle. It's widely used when the output voltage needs to be higher or lower than the input voltage.

## Inverting Buck-Boost Converter

The Inverting Buck-Boost Converter is a non-isolated DC-DC converter that inverts the polarity of the input voltage and regulates it to a higher or lower magnitude based on the duty cycle.



## Basic Operation

- **Switch ON:** The inductor is connected directly to the input. Energy is stored in the inductor's magnetic field. The diode is reverse-biased, so the load is supplied only by the capacitor.
- **Switch OFF:** The inductor's stored energy is released. Current flows through the diode to the load and capacitor, but with negative polarity at the output.

Phase	Switch	Diode	Inductor Action	Load Supply
ON (Ton)	Closed	Off	Charging from Vin	From Cap
OFF (Toff)	Open	On	Discharging to Vout	From L + Cap

## Key Formula:

$$V_{OUT} = -\frac{D}{1-D} \cdot V_{IN}$$

Where:

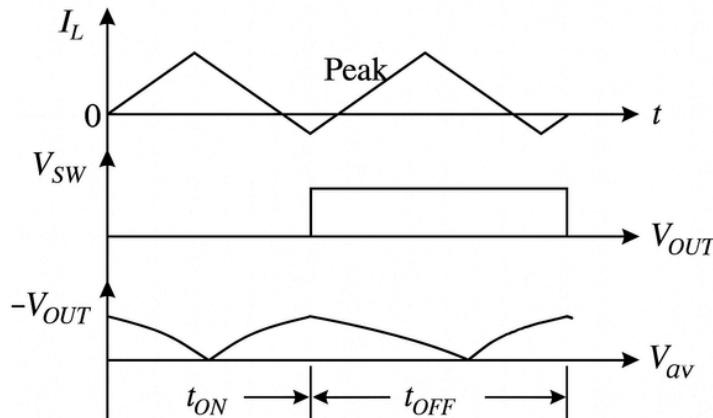
- $V_{OUT}$ : Negative output voltage
- $V_{IN}$ : Positive input voltage
- $D$ : Duty cycle (0 to 1)

This shows how the output voltage is **inverted and scaled**.

# BUCK-BOOST CONVERTERS

## Waveforms Overview

- Inductor Current: Sawtooth waveform
- Switch Voltage: Square wave (0 to  $V_{in}$ )
- Output Voltage: DC (negative) with ripple



Waveforms of inverting buck-boost converter

## Advantages

- Can generate negative voltages from a positive input.
- Supports both step-up and step-down conversion.
- Simple structure with only one inductor and one switch.

## Disadvantages

- Output is inverted (negative).
- Higher ripple current and voltage.
- Efficiency is usually lower compared to buck or boost converters.

## Applications

- Op-amp negative bias supply
- Analog signal processing circuits
- Audio and sensor circuits needing negative rails
- Bipolar power supplies
- Industrial systems with  $\pm$  power rails

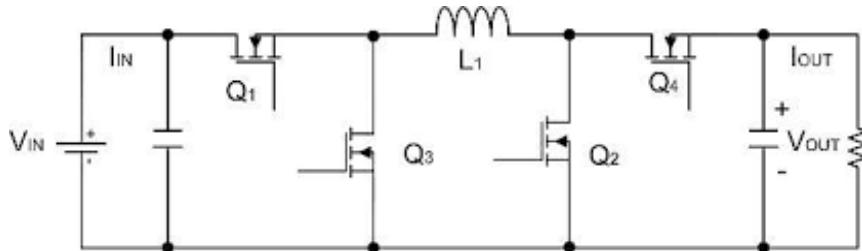
## Key Design Parameters

Parameter	Typical Value / Note
Input Voltage	3V to 30V
Output Voltage	Negative: -1.2V, -5V, -12V, etc.
Inductor Selection	Based on peak current and ripple
Capacitor Selection	Based on ripple and load demand
Diode	Fast-recovery Schottky recommended

# BUCK-BOOST CONVERTERS

## Non-inverting Buck-Boost

The Non-Inverting Buck-Boost Converter is a versatile DC-DC converter that can step up or step down the input voltage while maintaining the same output polarity as the input. This is particularly useful in battery-powered systems where the input voltage may vary above or below the desired output voltage.



### Basic Operation

The converter operates in two phases:

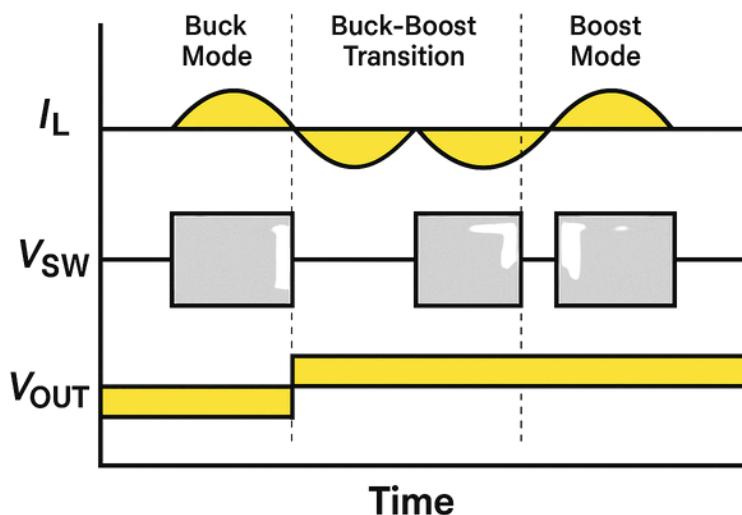
- **Buck Mode ( $V_{in} > V_{out}$ )**: Operates like a buck converter
- **Boost Mode ( $V_{in} < V_{out}$ )**: Operates like a boost converter
- **Buck-Boost Transition**: Seamlessly transitions between buck and boost

### Waveforms:

Waveforms are similar to those in buck and boost converters, but are dynamically adjusted based on input/output conditions. Key waveforms:

- **Inductor current ( $I_L$ )**: Biphasic rising and falling depending on control mode
- **Switch node ( $V_{SW}$ )**: Pulsed waveform with frequency and duty cycle adjusted dynamically
- **Output voltage ( $V_{out}$ )**: Regulated and smoother than  $V_{in}$

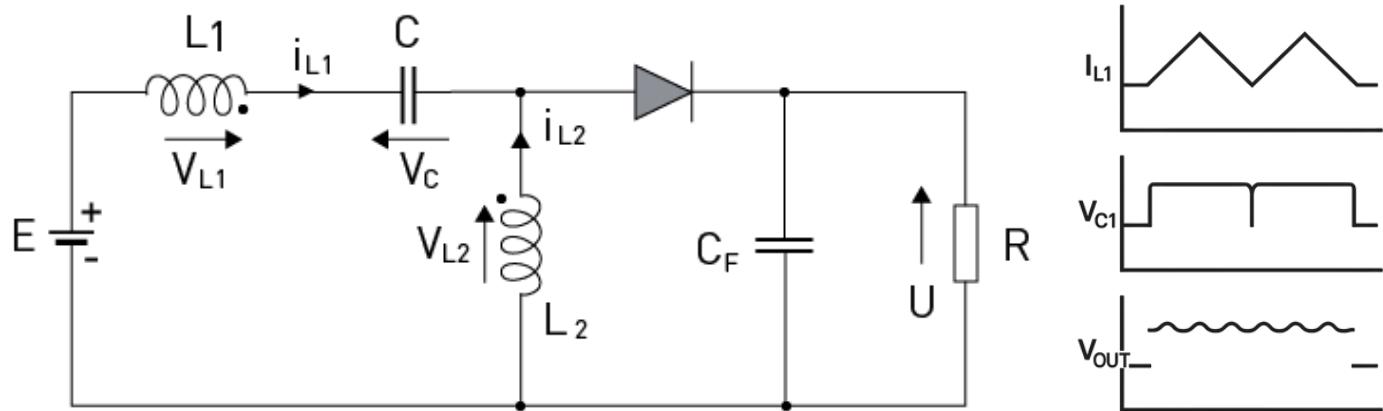
Non-Inverting Buck-Boost Converter



# BUCK-BOOST CONVERTERS

## SEPIC (Single-Ended Primary Inductance Converter)

SEPIC provides a non-inverting output that can be greater or less than the input voltage, which is ideal for systems where input voltage varies (e.g., battery)



### Basic Operation

A SEPIC converter allows the output voltage to be greater than, less than, or equal to the input voltage. It combines features of both buck and boost converters.

- It uses two inductors (or one coupled inductor), a series capacitor, and a diode.
- Power transfer occurs through the series capacitor ( $C_1$ ), which acts as a coupling element and energy storage medium.

#### • Switch ON:

- Inductors  $L1$  and  $L2$  store energy while  $C1$  charges.

#### • Switch OFF:

- Energy from both inductors and capacitor is transferred to the load via the diode.

### Advantages:

- Output voltage can be higher or lower than the input.
- Continuous input current (important for reducing EMI).
- Good isolation between input and output (via coupling capacitor).

### Disadvantages:

- Slightly more complex than buck/boost circuits.
- Higher component count (2 inductors + coupling capacitor).
- Voltage spikes due to parasitic elements.

# BUCK-BOOST CONVERTERS

## Applications:

- Battery-powered systems where the input may be above or below the regulated output (e.g., 3.7V Li-Ion to 5V output).
- Portable electronics.
- Automotive and industrial systems requiring flexible power conversion.

## Key Design Parameters:

Parameter	Consideration
Output Voltage ( $V_{OUT}$ )	Controlled via duty cycle (like buck-boost)
Coupling Capacitor (C1)	Must handle RMS current and voltage ripple
Inductors (L1, L2)	Chosen to avoid saturation and minimize ripple
Switching Frequency	Typically 100 kHz – 1 MHz

## Important Equation:

The steady-state output voltage relationship:

$$V_{OUT} = \frac{D}{1 - D} \times V_{IN}$$

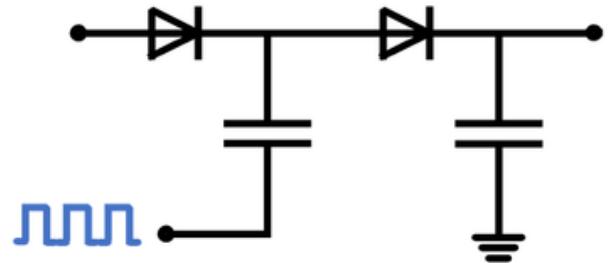
Where D is the duty cycle (ideal, neglecting losses).

Feature	SEPIC	Non-Inv Buck-Boost	Inv Buck-Boost
Output Polarity	Non-Inverting	Non-Inverting	Inverting
Inductors	2 (or coupled)	1 or 2	1
Ground Reference	Same	Same	Different
Switch Count	1	4	1
Control Complexity	Moderate	High	Low
Input Current	Continuous	Continuous	Discontinuous

# CHARGE PUMPS

Charge pumps are a type of DC-DC converter that use capacitors as energy storage elements instead of inductors. They are ideal for applications requiring low power, compact size, and simple design.

- Charge pumps work by switching capacitors between different configurations to step-up, step-down, or invert the input voltage.
- No inductors are used; switching is handled by transistors/MOSFETs and control logic.



## Topologies:

- **Voltage Doubler:** Output  $\approx 2 \times$  Input
- **Voltage Inverter:** Output  $\approx -\text{Input}$
- **Fractional or Tripler Multipliers:** Output  $\approx 1.5\times, 3\times, \text{ etc.}$ , depending on configuration
- Multi-stage designs

## Advantages:

- Simple and compact – no bulky inductors
- Low cost for low-current applications
- Efficient for moderate voltage conversion ratios
- Low EMI (no inductor radiation)

## Disadvantages:

- Limited current capability (typically  $< 100 \text{ mA}$ )
- Efficiency drops significantly at higher loads
- Ripple voltage can be high without sufficient output capacitance
- Output impedance increases with load

## Applications:

- EEPROM and Flash memory biasing
- Mobile phones and portable electronics
- LCD bias supplies
- White LED drivers
- Battery-powered systems with tight space constraints

## Example ICs:

- LM2660 – Inverting/voltage doubler
- TC7660 – Low-power voltage inverter
- MAX232 – Integrated charge pump for RS232 level shifting

# POWER IN PCB DESIGN

## Design Rules (Power Rule-of-Thumb)

- **Plane thickness calculations:**  $I = \rho \times T \times W \times \Delta T$ 
  - I: Current capacity (A)
  - $\rho$ : Resistivity coefficient
  - T: Copper thickness (oz)
  - W: Trace width (mils)
  - $\Delta T$ : Allowed temperature rise ( $^{\circ}$ C)
- **Current density limits:**
  - 1oz copper: 35A/mm<sup>2</sup> maximum
  - 2oz copper: 70A/mm<sup>2</sup> maximum
- **Common plane configurations:**
  - Power-Ground sandwich: Low inductance, good bypassing
  - Split planes: Separate regions for different voltages
  - Stitched islands: Connected power regions with bridges
- **Via considerations:**
  - Thermal relief connections reduce heat sinking during soldering
  - Direct connections provide lower impedance for high-current paths
  - Via size vs. current: 8mil diameter via handles ~0.5A at 10 $^{\circ}$ C rise
- **Separate Sensitive rails**
  - Digital ICs may need stable rails
  - Isolate the power rails (Analog / Digital)
  - Make separate grounds if necessary
- **High-current path optimization:**
  - Minimize loop area
  - Direct, wide traces
  - Multiple parallel vias for layer transitions
  - Keep paths as short as possible
- **High-current path optimization:**
  - Minimize loop area
  - Direct, wide traces
  - Multiple parallel vias for layer transitions
  - Keep paths as short as possible

# GROUNDING TECHNIQUES



## Grounding Strategies:

- **Single-point Ground:** Best for low-frequency analog systems. Reduces ground loops by tying all grounds to a single node.
- **Multi-point Ground:** Used in high-frequency systems to reduce impedance by having multiple paths.
- **Hybrid Grounding:** Combines both for mixed-signal designs (e.g., analog/digital).
- **Goal:** Minimize noise and avoid ground loops that can lead to interference or signal degradation.

## Ground Plane Impedance vs. Frequency:

- At low frequencies, the ground plane behaves mostly resistively.
- At high frequencies, inductive and capacitive effects dominate, increasing impedance.
- A solid ground plane with low inductance paths is crucial for high-speed or RF circuits.
- Use stitching vias to reduce inductive loops between layers.

## Special Considerations:

- Keep analog and digital grounds separate initially and connect at a single point (star ground).
- Never route high-speed digital traces over a split plane (causes return current discontinuity and EMI).
- For power electronics, minimize switching ground noise coupling to signal ground.

## Return Current Path Rules:

- Return currents follow the path of least impedance, not just resistance.
- At high frequencies, they flow directly under the signal trace to minimize loop area.
- Disruption of return paths (e.g., via plane splits) increases EMI and can cause functional failures.
- Always provide a continuous reference plane under high-speed or sensitive signals.

## Faraday Cage:

- Encloses the circuit in a conductive enclosure to block external electric fields and EMI.
- Common in sensitive analog front-ends, RF circuits, or EMI test setups.
- Best results when fully enclosed and grounded properly.

# POWER INTEGRITY GUIDELINES

- Importance of Low Impedance Power Rails
- Decoupling Capacitor Network Design
- Power Distribution Network (PDN) Analysis
- Avoiding Power Bounce and Ground Bounce

## Importance of Low Impedance Power Rails

- Low impedance ensures a stable voltage supply across varying load conditions.
- Helps prevent voltage drops, noise coupling, and signal integrity issues.
- Achieved through:
  - Wide copper planes
  - Proper via stitching
  - Distributed capacitance close to loads
- Target impedance ( $Z_{target}$ ) is often calculated as:

$$Z_{target} = \frac{V_{tol}}{I_{step}}$$

- $V_{tol}$  = maximum allowable voltage ripple (e.g., 50 mV)
- $I_{step}$  = maximum load current step (e.g., 2 A)
- Example: If 50 mV ripple is allowed at 2 A load change, then:

$$Z_{target} = \frac{0.05}{2} = 25 \text{ m}\Omega$$

### Achieved by:

- Wide power and ground planes (minimizes resistance and inductance)
- Dense via stitching (reduces loop area)
- Proper decoupling capacitor placement (closes high-frequency current loops)

### Design Goal:

- Maintain impedance below  $Z_{target}$  across a wide frequency range (from kHz to hundreds of MHz) for robust power integrity.

# POWER INTEGRITY GUIDELINES

## Decoupling Capacitors

### Purposes:

- Supply instantaneous current demands
- Filter power supply noise
- Reduce power/ground plane impedance
- Minimize voltage transients

### Placement guidelines:

- Low-value caps (0.01-0.1 $\mu$ F): Directly at IC power pins
- Mid-value caps (1-10 $\mu$ F): Within 1cm of high-current ICs
- Bulk caps (>47 $\mu$ F): Near power entry or regulators

### Capacitor values by frequency range:

- 100MHz+: 10-100pF
- 10-100MHz: 0.001-0.1 $\mu$ F
- 1-10MHz: 0.1-1 $\mu$ F
- 100kHz-1MHz: 1-10 $\mu$ F
- <100kHz: 10-100 $\mu$ F+

### Distributed decoupling:

- Multiple smaller capacitors in parallel outperform single large cap
- Example: 3×10 $\mu$ F better than 1×33 $\mu$ F at high frequency

### Guidelines:

Capacitor Type	Capacitance	Frequency	Use Case
Tantalum /Electrolytic	10 $\mu$ F – 470 $\mu$ F	LOW	Stabilize slow load transients
Ceramic MLCC	10nF – 10 $\mu$ F	MID-HIGH	Local bypass close to IC
Ceramic NPO/COG	10nF – 100nF	HIGH	RF bypass, clock lines

# POWER INTEGRITY GUIDELINES

## Power Distribution Network (PDN) Analysis

PDN analysis ensures that power is delivered cleanly and reliably from the voltage source (e.g., VRM or LDO) to every active component, across all frequencies and load conditions, with minimal noise, voltage drop, and impedance.

### Why PDN Analysis Matters:

#### 1. Avoids Voltage Droop

- High  $di/dt$  from digital ICs can cause power rails to dip.
- PDN analysis ensures capacitors and planes are adequate to handle transients.

#### 2. Ensures Stable Operation

- Prevents power rail ringing or oscillations due to poor impedance control.
- Maintains voltage levels within spec for sensitive analog and high-speed digital parts.

#### 3. Reduces EMI

- Helps in identifying and suppressing resonant peaks that can radiate noise.

### Key PDN Parameter: Impedance vs. Frequency:

- The target is to keep PDN below the specified impedance threshold across a wide frequency range.
- *Formula for PDN target impedance:*  $Z_{\text{target}} = \frac{V_{\text{allowed ripple}}}{I_{\max}}$

Example:

For a 1V rail with 50 mV ripple and 5 A load:  $Z_{\text{target}} = \frac{0.05}{5} = 0.01 \Omega$

### What PDN Analysis Includes:

Element	Description
VRM Output	Supplies regulated power; must match load
Planes & Traces	Introduce impedance and delay
Decoupling Caps	Mitigate transients and suppress resonance
IC Power Pins	Load that demands sharp transient current
Via Pathways	Inductive effects impact response time

# POWER INTEGRITY GUIDELINES

## Avoiding Power Bounce and Ground Bounce

**Power Bounce:** A transient fluctuation in the power rail voltage due to sudden switching current, especially in high-speed digital circuits.

**Ground Bounce:** A voltage shift in the ground reference level caused by simultaneous switching outputs (SSOs). It occurs because inductance in the return path causes a momentary voltage difference between ground points.

### Why It's a Problem:

- **Signal Integrity:** Bounce creates unpredictable reference levels, causing logic threshold errors.
- **EMI/EMC:** Bounce increases high-frequency noise and radiated emissions.
- **Reliability:** Excessive bounce can lead to false triggering, data corruption, or even IC damage over time.

### Real-World Effects:

- A high-output buffer driving capacitive loads can cause 1–2 V of bounce in fast transitions.
- Multiple outputs switching simultaneously (like in DDR memory) exacerbate the issue.

### Techniques to Minimize Bounce:

Technique	Description
Solid Ground Planes	Ensure low-impedance return paths
Short Return Paths	Minimize loop area for switching current
Decoupling Capacitors	Place close to power pins to absorb fast transients
Staggered Switching	Avoid SSOs by staggering edge transitions
Controlled Rise/Fall Times	Slows current slew rate to reduce bounce
Power/Ground via pairing	Maintain consistent reference during transitions

### Best Practices:

- Keep return current paths short and continuous.
- Use multiple ground vias near ICs and connectors.
- Distribute decoupling capacitors strategically by frequency.

# DIGITAL POWER MANAGEMENT

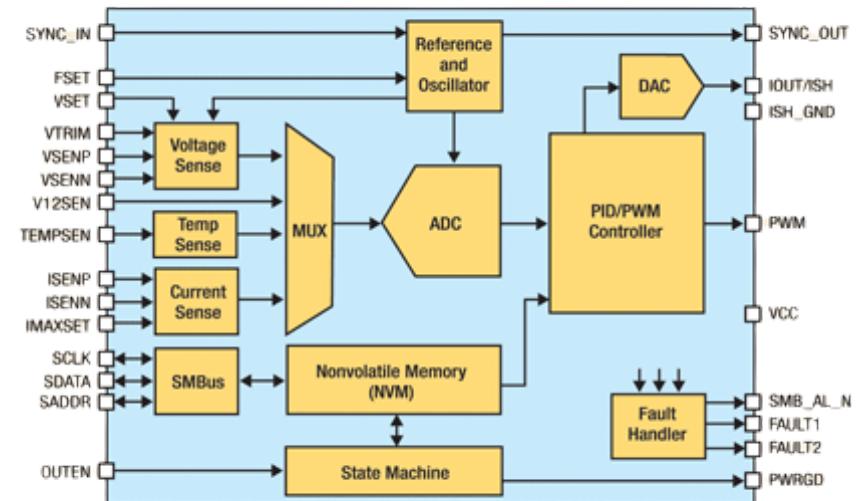
Digital Power Management refers to the integration of digital control and monitoring functions into power systems. It enhances flexibility, control, and diagnostics of power conversion systems using embedded controllers and communication protocols.

## Communication interfaces:

- PMBus/SMBus: Industry standard for power
- I<sup>2</sup>C: Simple two-wire interface
- SPI: Higher speed, more pins
- UART: Simple, asynchronous

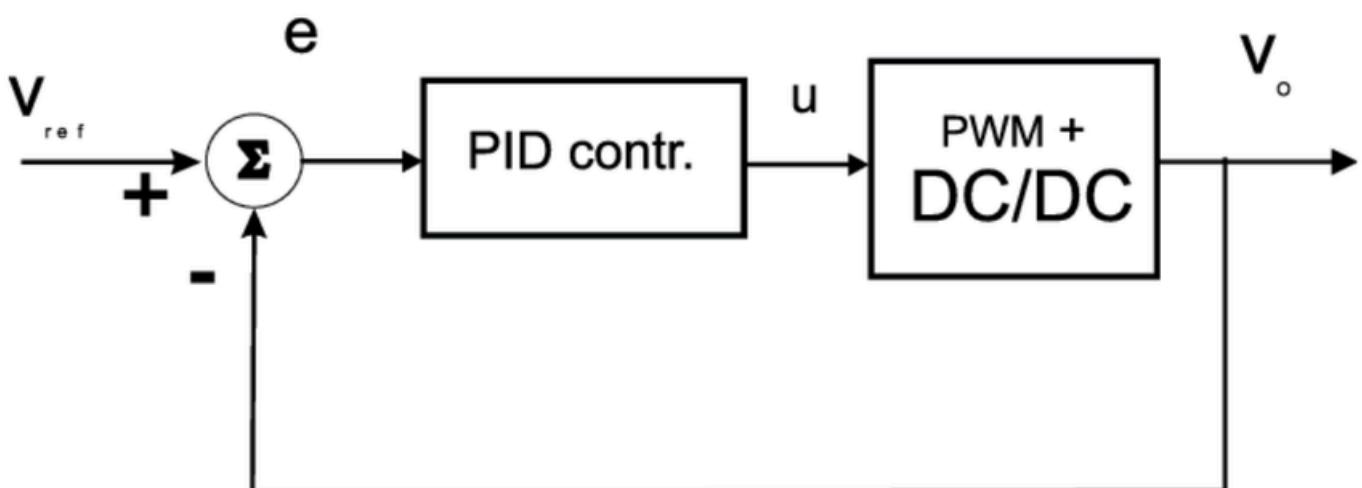
## Advanced features:

- Auto-tuning of compensation
- Fault logging
- Efficiency optimization algorithms
- Output voltage margining



## Controlled Buck converter:

- Design Controlled output for ripple sensitive loads
- Pick programmable converter and monitor the output
- Current sensing is critical



# HIGH-FREQUENCY DESIGN

## High-frequency power Mitigation

High-frequency power design typically involves switching converters operating at hundreds of kHz to several MHz, used to reduce component size, improve transient response, and increase efficiency in compact electronic systems.

### Why High Frequency?

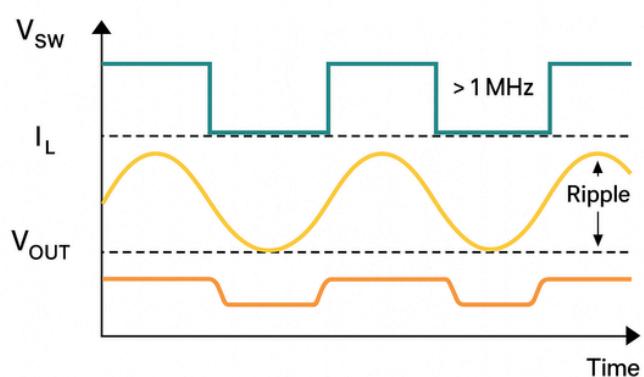
- Smaller magnetics: Higher switching frequency reduces the required size of inductors and transformers.
- Faster response: Quick reaction to load transients and input variations.
- Better filtering: Smaller capacitors can be used due to higher ripple frequency.
- Compact designs: Crucial for mobile, embedded, and automotive systems.

### Challenges:

Challenge	Explanation
Increased EMI	Faster edges and higher $dV/dt$ and $di/dt$ increase noise radiation.
Switching Losses	MOSFET gate charge and overlap losses increase with frequency.
Layout Sensitivity	Parasitics in layout (stray inductance and capacitance) affect performance.
Component Stress	Capacitors, inductors, and diodes experience higher ripple currents and temperatures.

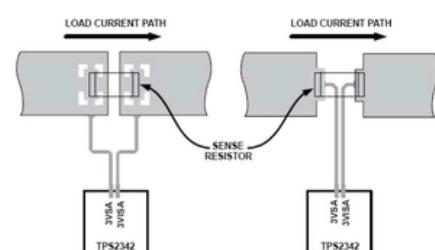
### Applications

- Fast chargers (USB-PD, GaN)
- Portable electronics
- Drones and robotics
- Industrial and automotive controllers
- High-density DC-DC modules



### Simulation and Validation

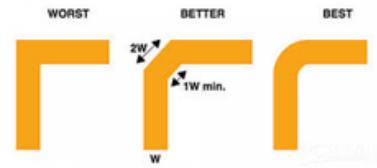
- Use SPICE, LTspice, or PI simulation tools to validate:
  - Switching waveforms
  - Stability (Bode plot)
  - Thermal profile
  - Efficiency vs. load curves



# HIGH-FREQUENCY DESIGN

## Design Considerations

### 1. PCB Layout



- Minimize loop areas in switching paths.
- Use tight component placement between MOSFETs, inductors, and output capacitors.
- Use wide traces and copper pours for power paths.
- Separate analog and switching grounds; rejoin at a single point (star grounding).

### 2. Switch Selection

- Choose MOSFETs with low  $Q_g$  (gate charge) and low  $R_{DS(on)}$ .
- Consider GaN FETs for >1 MHz designs due to faster switching and lower losses.

### 3. Gate Drive Strength

- Gate drivers must provide enough current for fast switching while avoiding ringing.
- Slower edges reduce EMI but increase switching losses—balance is key.

### 4. Inductor Selection

- Use shielded inductors with low core loss at high frequency.
- Select based on ripple current and frequency—verify saturation current rating.

### 5. Capacitor Choice

- Use ceramic capacitors (X7R/C0G) with low ESL and ESR.
- Place multiple values in parallel to flatten impedance curve (e.g.,  $0.1\ \mu F + 10\ \mu F$ ).

### 6. Snubber Circuits

- Used to damp switching node overshoot and ringing.
- Typically placed across MOSFETs or diodes.

### 7. Thermal Management

- High switching frequency = higher losses → more heat.
- Use thermal vias, copper planes, and heatsinks as needed.

### 8. EMI Filtering

- Use input/output LC filters, ferrite beads, and shielded layout techniques.
- Ensure compliance with CISPR and FCC EMI standards.

# MASTERING POWER TREE

## Power Tree

A Power Tree is a structured visual representation of how power is distributed from a single or multiple input sources to various system loads. It helps ensure each component receives correct voltage and current, and that the design is power-efficient and reliable.

### Key Elements of a Power Tree

- **Input Power Source** (Wall adapter, battery, solar panel, etc.)
- **Power Supply Blocks** (Buck, Boost, LDO, etc.)
- **Load Blocks** (MCUs, Displays, Sensors, etc.)
- **Rails** (Voltage levels like 12V, 5V, 3.3V, etc.)

### Methodology

- Each Power Supply (P.S) block must define:
  - Input Voltage Range
  - Output Voltage
  - Max Output Current
  - Efficiency
- Load Blocks should mention:
  - Operating Voltage
  - Typical and Max Current Consumption
- All components should be interconnected clearly via power rails.
- Perform efficiency analysis to evaluate overall power consumption and loss.

P.S Part Number		
Vin	Input Range Max Current Efficiency	Vout

### Implementation Guidelines

- Use graphical tools like Visio, Canva, or draw.io to visualize the tree.
- Represent each block with parameter boxes.
- **Include:**
  - Connection direction (input → output)
  - Voltage level labels
  - Load consumption per block
- **Calculate:**
  - Power consumed at each block
  - Total power required
  - Total power drawn
  - Overall system efficiency

Load Description

Typical Consumption

# MASTERING POWER TREE

## Example Use-Case

Input: 12V Wall Mount Adapter

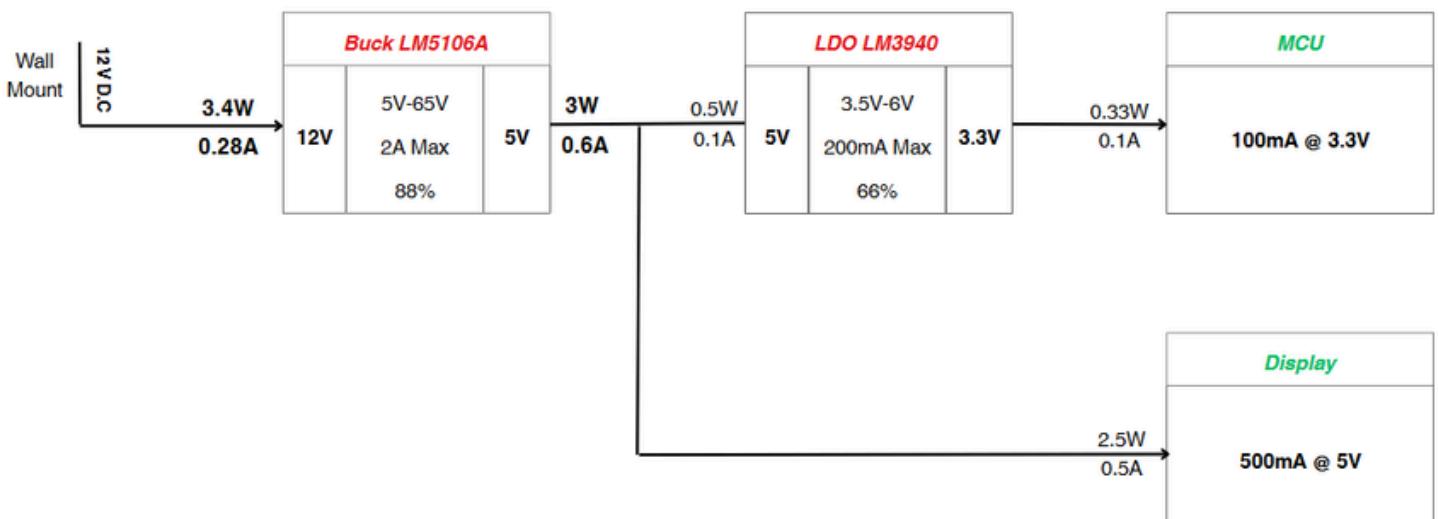
### Loads:

- MCU (100mA @ 3.3V)
- Display (0.5A @ 5V)

## Breakdown

Block	Input	Output	Power	Current	Efficiency
Wall Mount	230V AC	12V DC	-	0.28A	-
Buck LM5106A	12V	5V	3W	0.6A	88%
LDO LM3940	5V	3.3V	0.5W	0.1A	66%
MCU	3.3V	-	0.33W	0.1A	-
Display	5V	-	2.5W	0.5A	-

## Efficiency Calculation



$$MCU\ Power: P = VI \Rightarrow 3.3V \times 0.1A = 0.33W$$

$$Display\ Power: P = 5V \times 0.5A = 2.5W$$

$$Total\ Required\ Power: P_{out} = 0.33W + 2.5W = 2.83W$$

$$Input\ Power(From\ 12V\ Adaptor): P_{in} = 12V \times 0.28A = 3.36W$$

$$System\ Efficiency: \eta = \frac{P_{out}}{P_{in}} \Rightarrow \frac{2.83W}{3.36W} = 84\%$$

# POWER SIMULATION

## LTSpice

### How to Start?

- Very Easy, to simulate a power supply:
- Go Linear website and choose the one for you
- In LTS Find the component in the library (e.g. LTC1174)
- Choose Open Example Circuit
- And run the simulation
- The graphs allow you to probe every point
- You can check currents and voltage and many more things

### Unsupported Power Supply

Suppose you chose MAX639, but it's not supported in LTSpice. Not a problem

**Step 1:** compare the following parameters between the desired and supported P.S's.

Parameter	Min	Typ	Max	Units
Input Voltage	2.7	5.0	36	V
Output Voltage	0.8	-	VIN	V
Switch Current	-	-	3.5	A
Switching Frequency	0.2	1.0	2.2	MHz
Feedback Voltage	0.792	0.8	0.808	V
Quiescent Current	-	0.9	1.2	mA
Shutdown Current	-	0.1	1	µA
Switch On Resistance	-	0.11	0.18	Ω
Soft-Start Time	0.5	1.2	2.0	ms

**Step 2:** Find an alternative to the MAX639 from Linear Devices(supported by LTSpice). Create a comparison table with [7 relevant parameters], ensuring the alternative matches within  $\pm 20\%$  of each parameter. Include a column for difference calculations and ensure the comparison is clear and professional.

**Step 3:** Find the Linear match (LTC1174) in the library and run the Example Circuit

# POWER SIMULATION

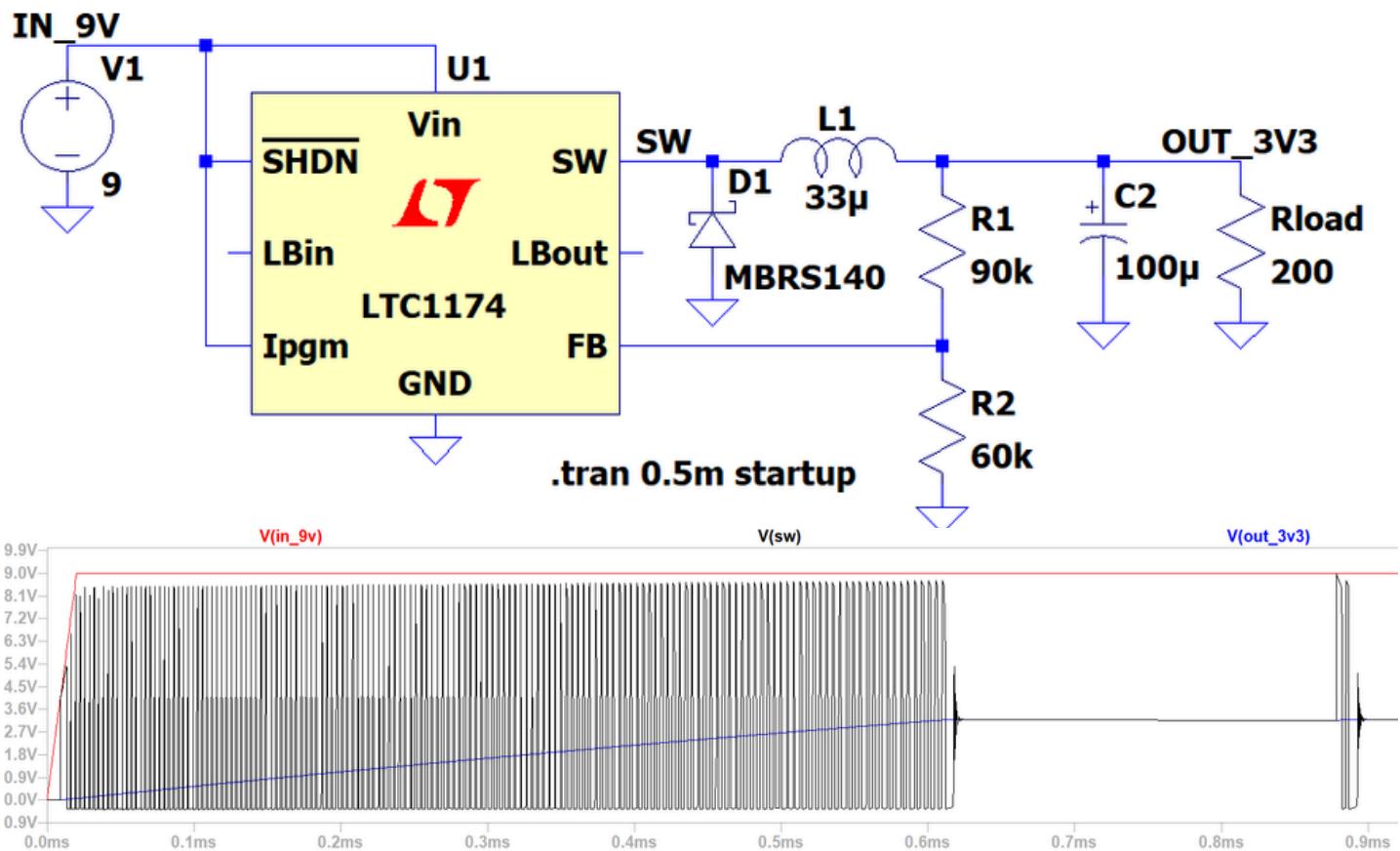
## Design Example:

We found a match for MAX639 And now it's time to simulate

*See Example for a Match:*

Parameter	LTC1174	MAX639	Difference (%)
Input Voltage Range	4V – 18.5V	4.5V – 18V	+2.7% (min) ✓
Output Voltage Range	3.3V or 5V	3.3V or 5V	0% ✓
Maximum Output Current	600mA	500mA	-16.7% ✓
Efficiency	Up to 94%	Up to 92%	-2.1% ✓
Quiescent Current	130µA	110µA	-15.4% ✓
Switching Frequency	Up to 200kHz	Up to 200kHz	0% ✓
Package Type	SOIC-8	SOIC-8	0% ✓

Schematics (LTS Example from library):



$$Vin = 9[V] \mid Vout = 3.3[V] \mid Time\ to\ stabilize = 630[\mu Sec] \mid Ripple = 60[mV]$$