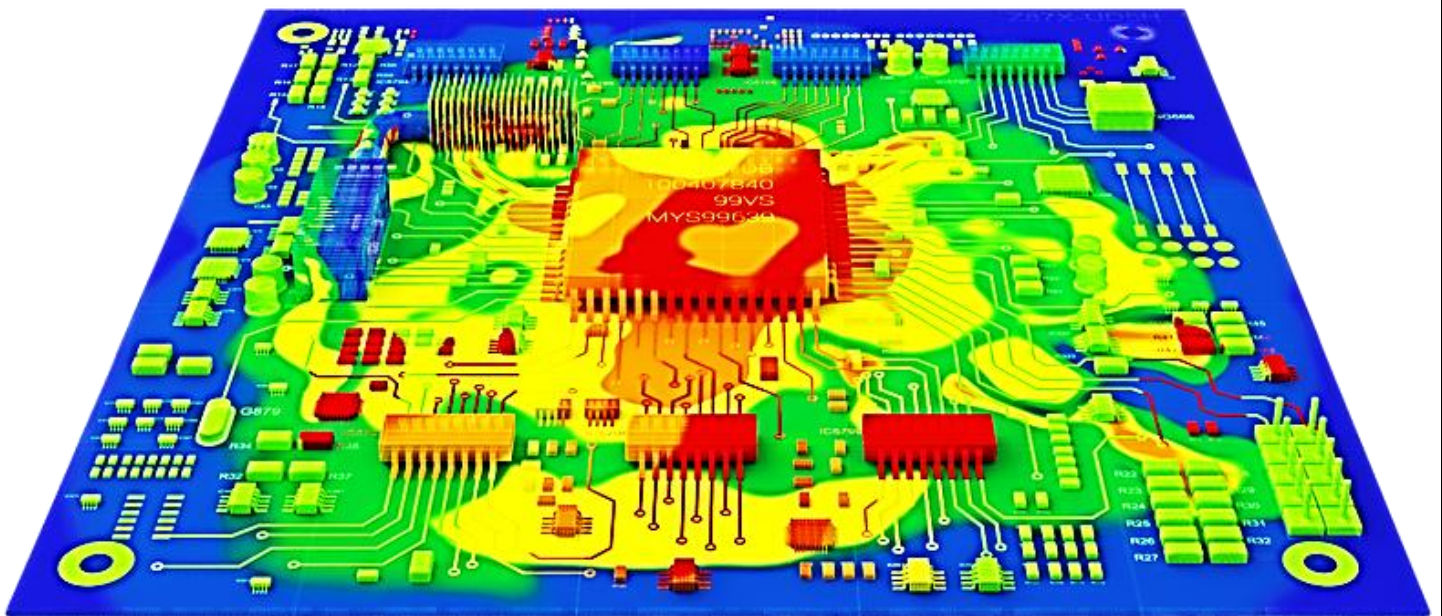


Hardware Engineer's Guide

# THERMAL MANAGEMENT



*By Shimi Cohen*

# HEAT EFFECT

## 1.1 Why Thermal Management Matters

### RELIABILITY IMPACT

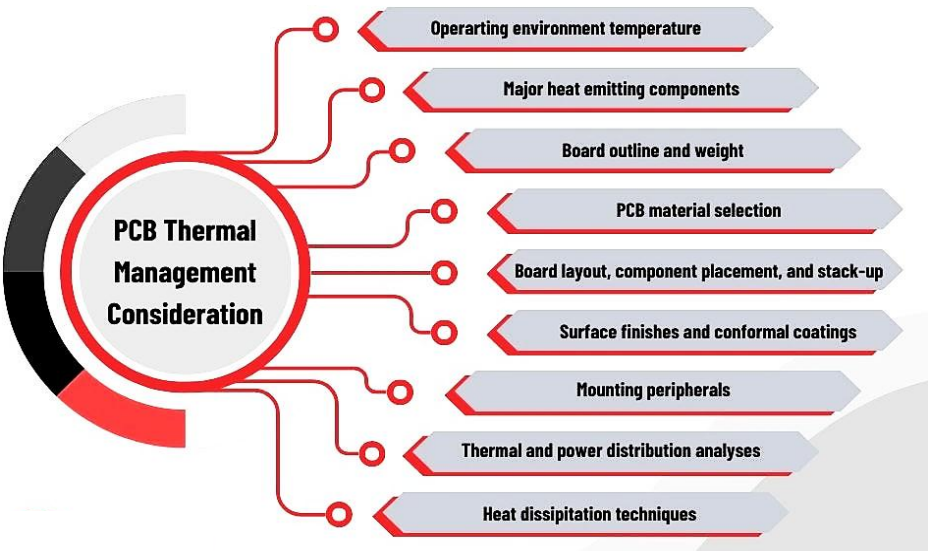
Every 10°C temperature increase reduces component life by 50%. This fundamental relationship drives all thermal design decisions.

### PERFORMANCE DEGRADATION

- Semiconductors: Leakage current doubles every 8-10°C
- Resistors: Drift increases with temperature coefficient
- Capacitors: ESR increases, capacity decreases
- Crystals: Frequency drift affects timing accuracy

### DESIGN TEMPERATURE TARGETS

COMPONENT TYPE	TARGET JUNCTION TEMP	AMBIENT +
MCU	≤ 85°C	25°C + 60°C
MOSFETS	≤ 125°C	25°C + 100°C
LDO	≤ 100°C	25°C + 75°C
ELEC CAPS	≤ 85°C	25°C + 60°C



## 1.2 Effects of Heat on Reliability

### ARRHENIUS RELATIONSHIP

Component failure rate increases exponentially with temperature. Arrhenius equation:

*Failure Rate* =  $A \times e^{(-Ea/kT)}$

Where:

- A = Pre-exponential factor
- Ea = Activation energy
- K = Boltzmann constant
- T = Absolute temperature

### PRACTICAL APPLICATION

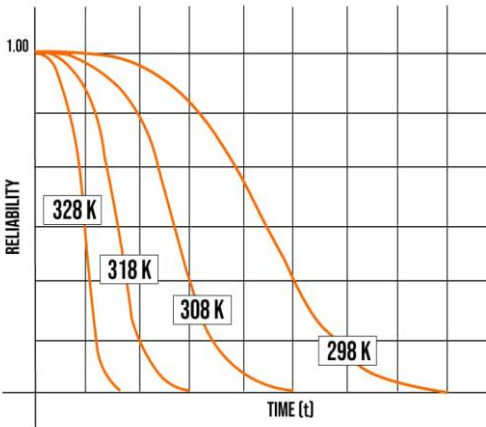
For every 10°C reduction in operating temperature, component life approximately doubles.

Repeated Thermal Cycling Outcome:

- Solder joint fatigue
- Wire bond failures
- Package cracking
- Delamination

### CRITICAL TEMPERATURE THRESHOLDS:

MATERIAL	THRESHOLD	FAILURE MODE
SOLDER (SAC305)	217°C	MELTING
FR-4 SUBSTRATE	130°C	GLASS TRANSITION
BOND WIRE	175°C	INTERMETALLIC GROWTH
DIE ATTACH	150°C	DELAMINATION



### 1.3 Common Heat Sources in PCBs

#### PRIMARY HEAT GENERATORS

**POWER MANAGEMENT:**

- Switching regulators: 5-15% power loss
- Linear regulators: (VIN-VOUT)/VIN loss percentage
- Battery chargers: 10-20% loss typical

**PROCESSING COMPONENTS:**

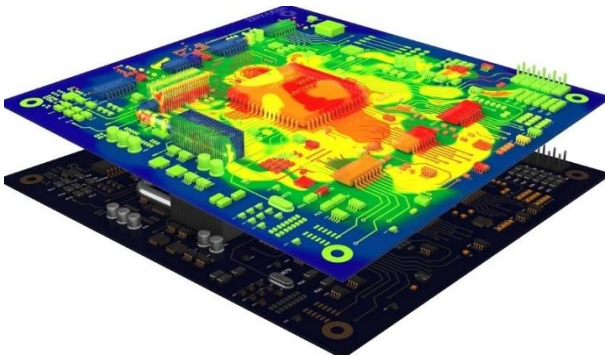
- Microprocessors: 0.5-50W depending on performance
- FPGAs: 1-100W based on utilization
- DSPs: 0.1-10W typical range

**POWER DEVICES:**

- MOSFETs:  $I^2R$  losses + switching losses
- Diodes:  $V_F \times I_F$  continuous
- LEDs: 60-80% electrical power as heat

**PASSIVE COMPONENTS:**

- Resistors:  $I^2R$  heating, especially current sensing
- Inductors: Core and copper losses
- Transformers: Primary and secondary losses



**HEAT DENSITY DISTRIBUTION:**

COMPONENT TYPE	TYPICAL W/CM <sup>2</sup>	COOLING CHALLENGE
CPU/GPU	50-200	VERY HIGH
POWER MOSFET	10-50	HIGH
LINEAR REGULATOR	5-25	MEDIUM
LED ARRAY	1-10	MEDIUM
RESISTORS	0.5-5	LOW

# HEAT TRANSFER FUNDAMENTALS

## 2.1 Conduction Principles

### FOURIER'S LAW & RESISTANCE MODEL

$$Q = -k \times A \times (dT/dx)$$

$$R_t = L / (k \times A)$$

Where:

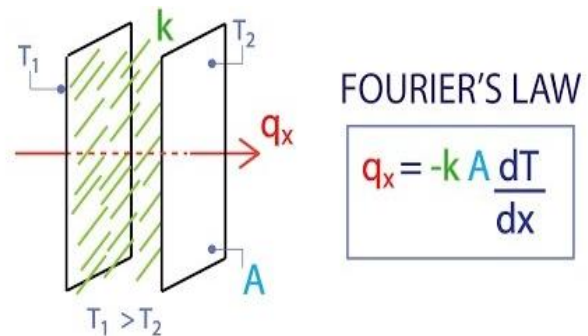
$Q$  = Heat flow rate (watts)

$R_t$  = Resistance Model

$k$  = Thermal conductivity (W/m·K)

$A$  = Cross-sectional area (m<sup>2</sup>)

$dT/dx$  = Temperature gradient (K/m)

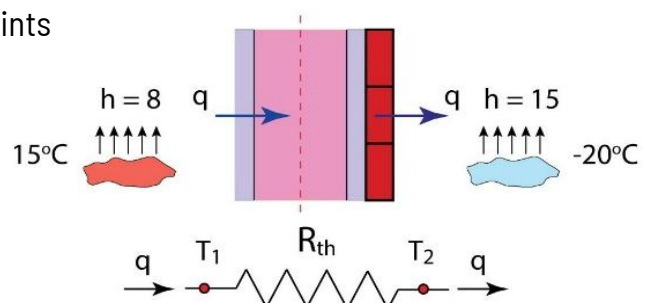


### MATERIAL THERMAL CONDUCTIVITIES:

MATERIAL	THERMAL CONDUCTIVITY	PCB APPLICATION
COPPER	400	TRACES, PLANES, VIAS
ALUMINUM	237	HEAT SINKS, SUBSTRATES
FR-4	0.3	STANDARD SUBSTRATE
POLYIMIDE	0.2	FLEXIBLE CIRCUITS
THERMAL EPOXY	1-3	DIE ATTACH, TIM

### PCB CONDUCTION PATHS

- Copper traces: Primary horizontal heat flow
- Copper planes: Large area heat spreading
- Thermal vias: Vertical heat transfer
- Component leads: Heat input/output points



## 2.2 Convection Mechanisms

### NEWTON'S LAW OF COOLING

$$Q = h \times A \times (T_{\text{surface}} - T_{\text{ambient}})$$

Where:

$h$  = Convection coefficient ( $\text{W}/\text{m}^2\cdot\text{K}$ )

$A$  = Surface area ( $\text{m}^2$ )

$T$  = Temperature ( $\text{K}$ )

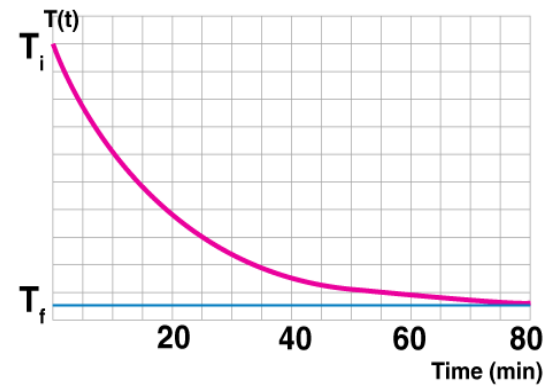
### CONVECTION TYPES

**NATURAL CONVECTION:**

- Buoyancy-driven air movement
- Typical  $h = 5\text{-}25 \text{ W}/\text{m}^2\cdot\text{K}$
- Orientation dependent
- Limited cooling capacity

**FORCED CONVECTION:**

- Fan or blower driven
- Typical  $h = 25\text{-}250 \text{ W}/\text{m}^2\cdot\text{K}$
- Velocity dependent
- Higher cooling capacity



Newton's Law of Cooling – Temperature vs Time

**CONVECTION COEFFICIENTS:**

CONDITION	H (W/M <sup>2</sup> ·K)	APPLICATION
NATURAL AIR, VERTICAL	5-25	PASSIVE COOLING
NATURAL AIR, HORIZONTAL	2-10	POOR ORIENTATION
FORCED AIR, 2 M/S	50-100	FAN COOLING
FORCED AIR, 10 M/S	100-300	HIGH-SPEED FANS

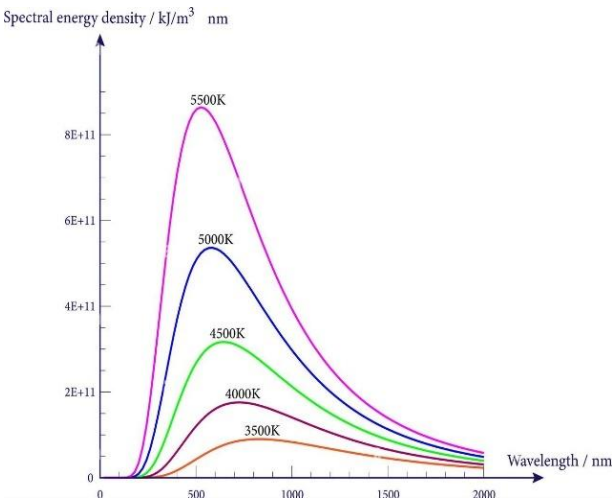
## 2.3 Radiation Effects

### STEFAN-BOLTZMANN LAW

$$Q = \epsilon \times \sigma \times A \times (T_1^4 - T_2^4)$$

Where:

- ε = Emissivity (0-1)
- σ = SB constant (5.67×10<sup>-8</sup> W/m<sup>2</sup>·K<sup>4</sup>)
- A = Surface area (m<sup>2</sup>)
- T = Absolute temperature (K)



### SURFACE EMISSIVITY VALUES:

SURFACE	EMISSIVITY	RADIATION EFFECTIVENESS
BLACK ANODIZED ALUMINUM	0.9	EXCELLENT
GREEN SOLDER MASK	0.8	GOOD
BARE COPPER	0.1	POOR
POLISHED METAL	0.05	VERY POOR

### RADIATION CONTRIBUTION

At typical PCB temperatures (60-80°C), radiation accounts for 20-40% of total heat transfer in natural convection environments.

### DESIGN IMPLICATIONS:

- Increase surface area for radiation
- Use high-emissivity finishes
- Avoid shiny metal surfaces
- Consider radiation in thermal budget



# THERMAL PROPERTIES

## 3.1 Standard FR-4 Performance

**FR-4 THERMAL PROPERTIES:**

PROPERTY	VALUE	UNIT	IMPACT
THERMAL CONDUCTIVITY	0.3	W/M·K	HEAT SPREADING
GLASS TRANSITION (TG)	130-180	°C	MAX OPERATING TEMP
DECOMPOSITION (TD)	300+	°C	ABSOLUTE LIMIT
CTE Z-AXIS	50-70	PPM/°C	VIA RELIABILITY

### FR-4 LIMITATIONS

- Low thermal conductivity limits heat spreading
- CTE mismatch causes via stress
- Tg limits high-temperature operation
- Moisture absorption affects properties

### ENHANCED FR-4 OPTIONS

**HIGH TG FR-4:**

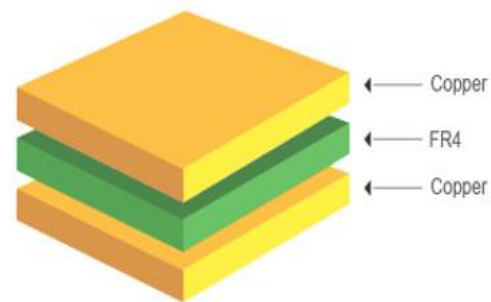
- Tg: 170-180°C vs 130°C standard
- Better high-temperature stability
- 15-20% cost premium
- Same processing requirements

**LOW CTE FR-4:**

- Reduced Z-axis expansion
- Better via reliability
- Improved thermal cycling performance
- 25-30% cost increase

**THERMAL DESIGN WITH FR-4:**

- Rely on copper for heat conduction
- Minimize through-substrate heat paths
- Use thermal vias extensively
- Consider heat spreading planes





## 3.2 Metal-Core PCB Applications

### METAL-CORE PCB (MCPCB)

- Metal base (aluminum/copper)
- Dielectric layer (thermally conductive)
- Copper circuit layer
- Solder mask and silkscreen

**THERMAL PERFORMANCE:**

MCPCB TYPE	THERMAL [W/M-K]	APPLICATION
STANDARD ALUMINUM	1.5-3.0	LED LIGHTING
HIGH PERFORMANCE	5.0-8.0	POWER ELECTRONICS
COPPER CORE	15-25	RF POWER AMPS
CERAMIC FILLED	3.0-12	HYBRID SOLUTIONS

### DESIGN CONSIDERATIONS

**ADVANTAGES:**

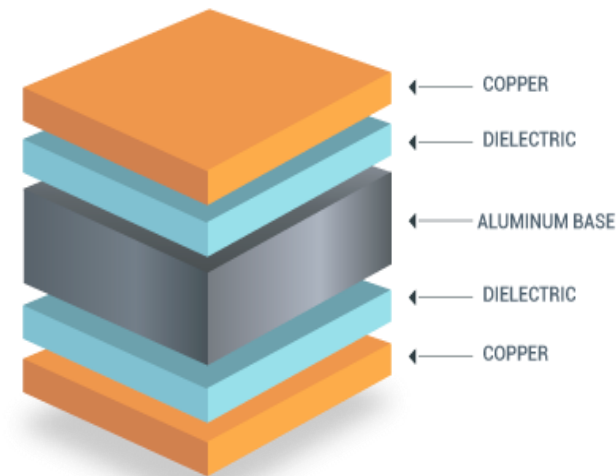
- Excellent heat dissipation
- Reduced thermal interface layers
- Direct mounting to heat sink
- Lower overall thermal resistance

**LIMITATIONS:**

- Single-sided circuits only
- Higher cost than FR-4
- Limited via options
- Special manufacturing process

**POWER ELECTRONICS:**

- Linear regulators > 5W
- Switching regulators > 20W
- Motor controllers
- Power amplifiers



### 3.3 Advanced Substrate Options

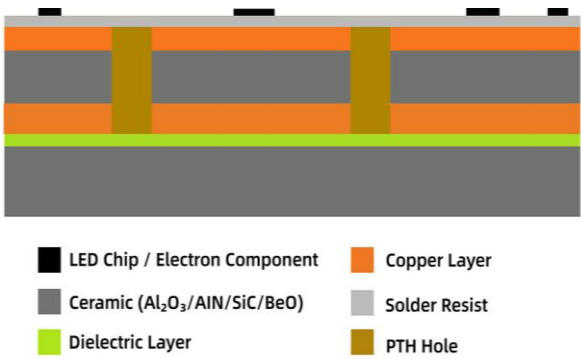
#### CERAMIC SUBSTRATES

**ALUMINUM NITRIDE (ALN):**

- Thermal conductivity: 170-200 W/m·K
- Electrical isolation
- Low CTE match to silicon

**BERYLLIUM OXIDE (BEO):**

- Thermal conductivity: 250-300 W/m·K
- Excellent electrical properties
- Toxic material, handling issues
- Specialized applications only



#### FLEXIBLE SUBSTRATES

**POLYIMIDE WITH THERMAL FILLERS:**

- Enhanced thermal conductivity: 1-3 W/m·K
- Maintains flexibility
- Higher cost than standard
- Specialized applications

**LIQUID CRYSTAL POLYMER (LCP):**

- Low loss at high frequencies
- Good thermal stability
- Moderate thermal conductivity
- RF/microwave applications



APPLICATION	PRIMARY NEED	RECOMMENDED SUBSTRATE
HIGH-POWER LED	HEAT DISSIPATION	ALUMINUM MCPCB
RF POWER AMP	HEAT + RF PERFORMANCE	COPPER MCPCB
PRECISION ANALOG	THERMAL STABILITY	HIGH TG FR-4
POWER MODULE	MAXIMUM HEAT REMOVAL	ALN CERAMIC

# COMPONENT HANDLING

## 4.1 Heat-Generating Components

### POWER DISSIPATION CALCULATION

#### LINEAR REGULATORS:

$$PD = (VIN - VOUT) \times IOUT + (VIN \times IQ)$$

Example LM1117-3.3:

- Input: 5V, Output: 3.3V, Current: 1A
- $PD = (5V - 3.3V) \times 1A + (5V \times 5mA) = 1.725W$

#### SWITCHING REGULATORS:

$$PD = POUT \times (1 - \eta) / \eta + PSWITCHING$$

MOSFETs:

- Conduction loss:  $I^2_{RMS} \times RDS(on)$
- Switching loss:  $\frac{1}{2} \times VDS \times IDS \times (tr + tf) \times f_{sw}$

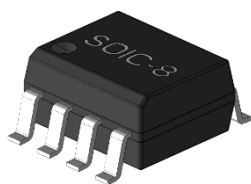
#### MICRO-CONTROLLER:

$$PD = VCC \times ICC + \text{Dynamic power}$$

#### COMPONENT POWER RATINGS:

##### PACKAGE TYPE    TYPICAL POWER    THERMAL RESISTANCE

SOT-23	0.2W	250°C/W
SOIC-8	0.5W	150°C/W
QFN-16	1.0W	50°C/W
T0-220	15W	60°C/W
D2PAK	25W	3°C/W



## 4.2 Optimal Placement Strategies

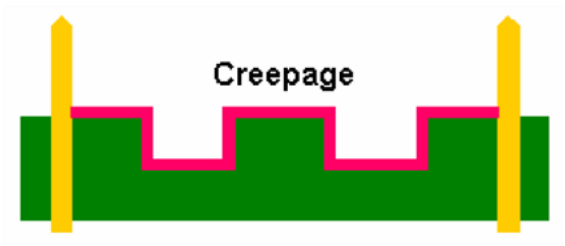
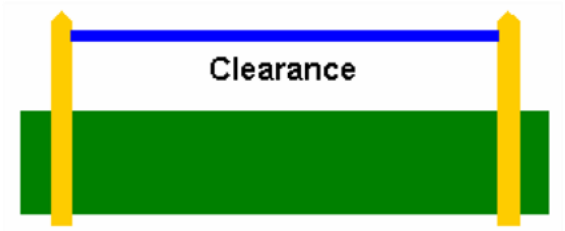
### HEAT SOURCE DISTRIBUTION

**SPACING REQUIREMENTS:**

- Minimum 5mm between HP components
- Consider airflow patterns

**PLACEMENT PRIORITY:**

1. **Highest Power Components:**
  - Center of board for heat spreading
  - Access to maximum copper area
  - Direct thermal path to heat sink
2. **Medium Power Components:**
  - Distribute around high-power devices
  - Consider cooling airflow
3. **Low Power Components:**
  - Fill remaining areas
  - Normal placement rules apply



**BOARD ZONES**

ZONE TYPE	TEMPERATURE	SUITABLE COMPONENTS
HOT ZONE	>70°C	POWER DEVICES ONLY
WARM ZONE	40-70°C	DIGITAL LOGIC, DRIVERS
COOL ZONE	<40°C	PRECISION ANALOG, REFERENCES

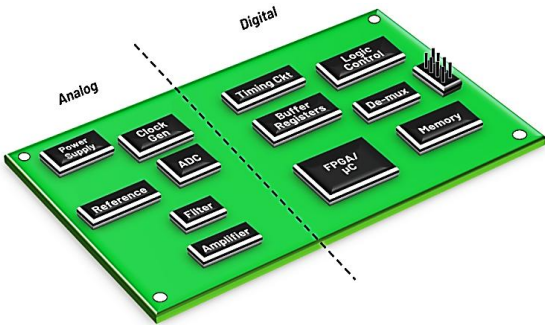
### PLACEMENT RULES

**POWER MANAGEMENT:**

- Place switching regulators away from sensitive analog
- Linear regulators need heat sinking above 1W
- Keep feedback components cool
- Minimize input/output ripple coupling

**PROCESSING UNITS:**

- Center placement for heat spreading
- Direct thermal path to system cooling
- Consider package orientation for airflow
- Separate power and I/O connections

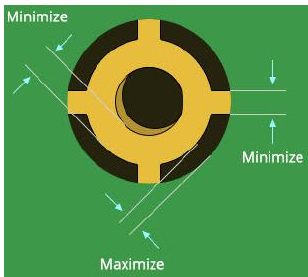


## 4.3 Layout for Heat Dispersion

### COPPER POUR STRATEGY

**GROUND PLANE UTILIZATION:**

- Connect hot components directly to ground plane
- Maximize copper area under components
- Use plane cutouts only when necessary



### THERMAL RELIEF CONSIDERATIONS

Standard thermal reliefs reduce heat conduction by 80-90%. Use direct connections for thermal management.

**TRACE WIDTH FOR THERMAL CONDUCTION:**

CURRENT	STD WIDTH	THR WIDTH	IMPROVEMENT
1A	0.5MM	2.0MM	4X HEAT CONDUCTION
3A	1.5MM	4.0MM	2.7X HEAT CONDUCTION
5A	2.5MM	6.0MM	2.4X HEAT CONDUCTION

### HEAT SPREADING TECHNIQUES

**COPPER FLOODING:**

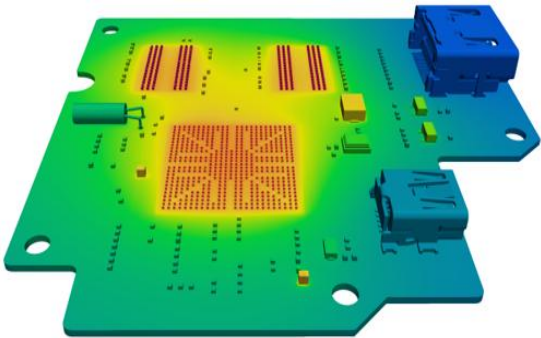
- Fill unused areas with copper
- Maintain electrical isolation where required
- Provide stitching vias between layers

**THERMAL PADS:**

- Large copper areas under components
- Multiple via connections to planes
- Solder mask opening for heat sink contact

**LAYER ASSIGNMENT:**

- Dedicate inner layers to heat spreading
- Use thick copper (2oz/70µm minimum)
- Provide cross-layer thermal connections



# LAYER STACK-UP

## 5.1 Layer Count Impact

### THERMAL PERFORMANCE VS LAYER COUNT

LAYER COUNT	THERMAL IMPROVEMENT	COST IMPACT	APPLICATION
2-LAYER	BASELINE	1X	SIMPLE, LOW POWER
4-LAYER	2-3X	1.5X	MODERATE COMPLEXITY
6-LAYER	3-4X	2X	HIGH PERFORMANCE
8+ LAYER	4-5X	3X+	COMPLEX SYSTEMS

### HEAT CONDUCTION PATHS

#### 2-LAYER BOARDS:

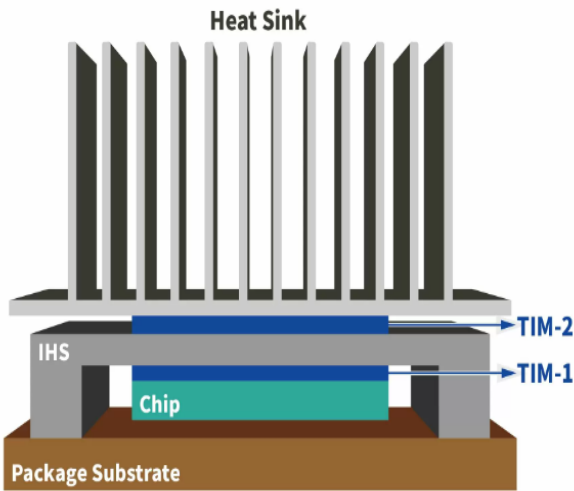
- Limited to top and bottom copper
- Thermal vias essential
- Component placement critical
- External heat sinking often required

#### 4-LAYER BOARDS:

- Internal power/ground planes
- Better heat spreading
- Reduced thermal resistance
- Standard for moderate power

#### 6+ LAYER BOARDS:

- Dedicated thermal planes possible
- Multiple heat spreading paths
- Lower overall thermal resistance
- Required for high-power density



## 5.2 Copper Thickness Optimization

### STANDARD COPPER WEIGHTS

COPPER WEIGHT	THICKNESS	RESISTANCE	THERMAL BENEFIT
0.5OZ	17µM	HIGH	LIMITED
1OZ	35µM	STANDARD	GOOD
2OZ	70µM	LOW	VERY GOOD
3OZ	105µM	VERY LOW	EXCELLENT

### THERMAL CONDUCTANCE SCALING

Thermal conductance increases linearly with copper thickness. 2oz copper provides 2x thermal performance vs 1oz.

### PERFORMANCE

**1OZ COPPER (STANDARD):**

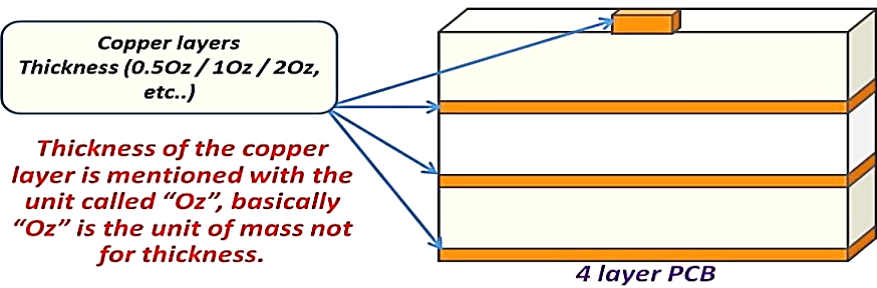
- Adequate for  $<2\text{W}/\text{cm}^2$
- Most common choice

**2OZ COPPER:**

- 2x thermal performance
- Good for  $2\text{--}5\text{W}/\text{cm}^2$

**3OZ COPPER:**

- 3x thermal performance
- Required for  $>5\text{W}/\text{cm}^2$





## 5.3 Power/Ground Plane Design

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### THERMAL STRATEGY

**DEDICATED THERMAL PLANES:**

- Separate layer for heat spreading
- Not used for electrical connections
- Maximum copper retention
- Connected via thermal vias

**POWER PLANE UTILIZATION:**

- VCC planes conduct heat
- Multiple power domains create thermal barriers
- Ground planes typically best thermal conductors
- Consider plane assignment for thermal management

### PLANE CONNECTION METHODS

CONNECTION TYPE	THERMAL RESISTANCE	ELECTRICAL FUNCTION
DIRECT CONNECT	LOWEST	POWER/GROUND
THERMAL VIA	LOW	ISOLATION
THERMAL RELIEF	HIGH	STANDARD ELECTRICAL
NO CONNECTION	INFINITE	ISOLATION

### PLANE SPLITS

**THERMAL IMPACT OF SPLITS:**

- Plane splits block heat flow
- Create thermal barriers
- Force heat through limited paths
- Should be minimized in hot areas

**DESIGN RULES:**

- Avoid splits under hot components
- Provide thermal bridges across splits
- Use multiple narrow splits vs single wide
- Consider thermal via arrays at splits

# THERMAL VIAS

## 6.1 Thermal Via Design

### VIA THERMAL RESISTANCE

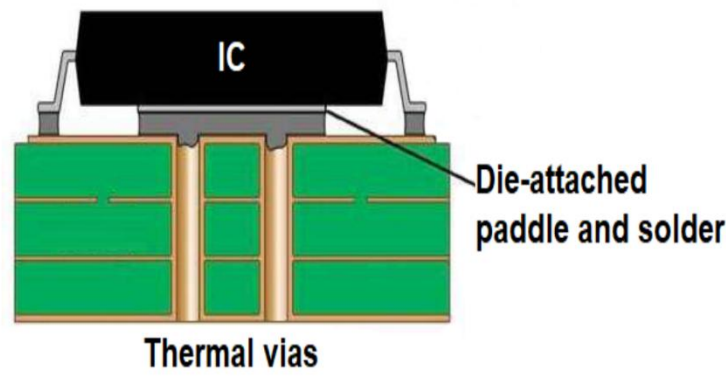
$R_{th\_Via} = L / (k \times A) + \text{Contact resistances}$

Where:

L = Via length (board thickness)

k = Copper thermal conductivity

A = Via barrel area



STANDARD VIA THERMAL PERFORMANCE:

VIA SIZE	DRILL/PAD	THERMAL RESISTANCE	CURRENT CAPACITY
0.2MM	0.2/0.4MM	100°C/W	1A
0.3MM	0.3/0.5MM	70°C/W	2A
0.5MM	0.5/0.8MM	40°C/W	4A
0.8MM	0.8/1.2MM	25°C/W	8A

### VIA ARRAY DESIGN

$N = R_{total} / R_{via}$

EXAMPLE:

- Required thermal resistance: 5°C/W
- Single via resistance: 50°C/W
- Required vias: 50/5 = 10 vias minimum

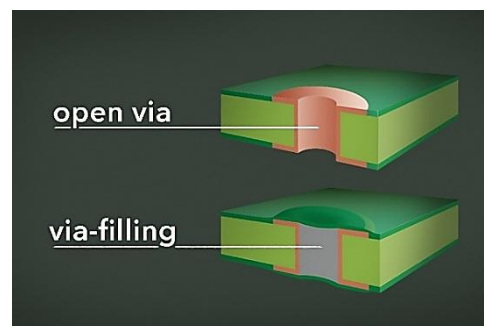
VIA SPACING:

- Minimum: 3x drill diameter
- Optimal: 5x drill diameter for manufacturing
- Maximum: Constrained by component size
- Pattern: Regular grid preferred

## VIA FILL OPTIONS

### UNFILLED VIAS:

- Lowest cost
- Good thermal performance
- Potential solder wicking
- Standard manufacturing

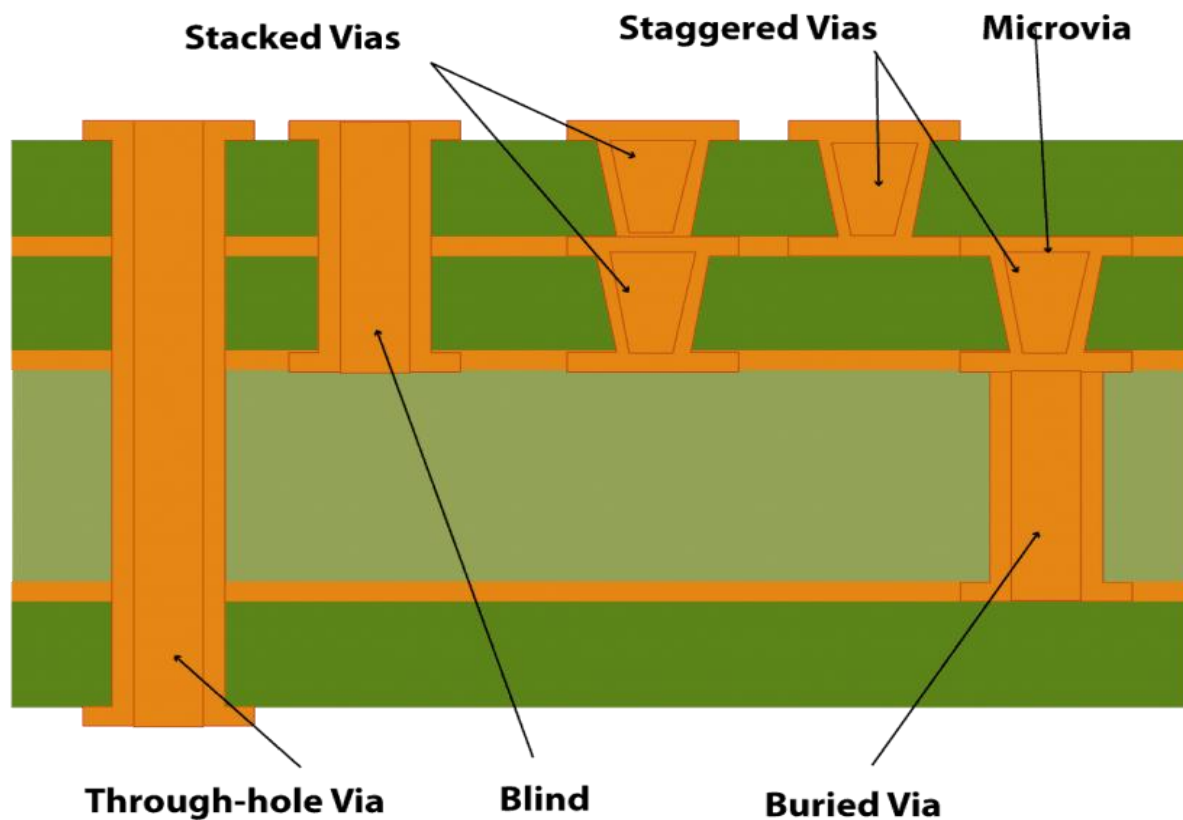


### FILLED VIAS:

- Prevent solder wicking
- Slightly better thermal performance
- Higher manufacturing cost
- Required for via-in-pad

### CAPPED VIAS:

- Plugged with soldermask
- Lowest cost fill option
- Good for most applications
- Standard capability



## 6.2 Via-in-Pad Implementation

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### VIA-IN-PAD BENEFITS

- Maximum thermal efficiency
- Shortest thermal path
- Reduced PCB area
- Better electrical performance

### MANUFACTURING REQUIREMENTS

- Via filling mandatory
- Planarization required
- Higher cost process
- Extended lead times

### DESIGN GUIDELINES

**VIA SIZE SELECTION:**

- Smaller vias preferred for filling
- 0.1-0.2mm typical for via-in-pad
- Aspect ratio <8:1 recommended
- Consider manufacturing capabilities

**PAD DESIGN:**

- Pad size accommodates via and tolerances
- Via centered in pad
- Multiple vias per pad if size allows
- Maintain solder joint integrity

**PROCESS COMPATIBILITY:**

FILL METHOD	COST	THERMAL PERFORMANCE	RELIABILITY
CONDUCTIVE EPOXY	MEDIUM	GOOD	GOOD
ELECTROPLATED COPPER	HIGH	EXCELLENT	EXCELLENT
SOLDERMASK PLUG	LOW	FAIR	FAIR

## 6.3 Advanced Via Techniques

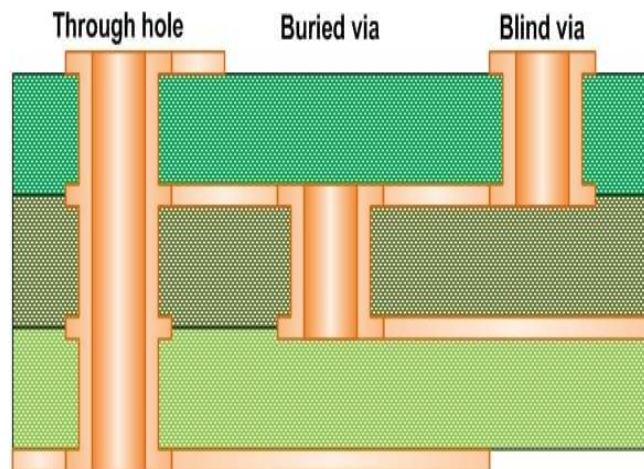
### MICRO-VIAS

#### BURIED THERMAL VIAS:

- Connect internal layers only
- Lower thermal resistance
- Higher manufacturing complexity

#### STACKED MICRO-VIAS:

- Sequential build-up
- Very low thermal resistance
- Advanced HDI capability required



### VIA PATTERNING STRATEGIES

#### THERMAL VIA ARRAYS:

- Regular grid pattern
- Uniform heat distribution
- Predictable thermal performance

#### VIA WALLS:

- Linear via arrangements
- Thermal barriers or channels
- Direct heat flow control

#### HYBRID VIA STRATEGIES:

- Combine different via types
- Optimize cost vs performance
- Match thermal requirements

### THERMAL VIA PLACEMENT

#### COMPONENT-CENTRIC:

- Radial pattern from heat source
- Shortest thermal path
- Maximum effectiveness

#### SYSTEM-LEVEL:

- Board-wide thermal network
- Heat spreading and collection
- Multiple heat sources

# HEATSINK MATERIALS

## 7.1 Heat Sink Selection

### HEAT SINK THERMAL RESISTANCE

$$R_{th} = (T_j - T_a) / P - R_{th\_jc} - R_{th\_interface}$$

### HEAT SINK TYPES

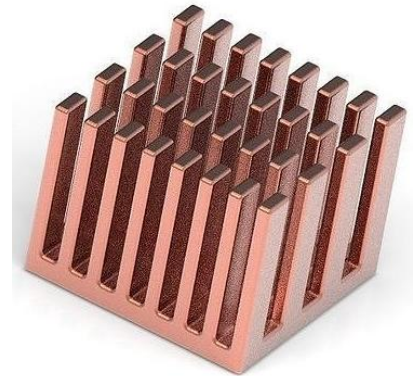
TYPE	THERMAL RESISTANCE	COST	APPLICATION
STAMPED ALUMINUM	15-50°C/W	LOW	<5W COMPONENTS
EXTRUDED ALUMINUM	5-20°C/W	MEDIUM	5-25W COMPONENTS
BONDED FIN	2-10°C/W	HIGH	25-100W COMPONENTS
VAPOR CHAMBER	0.5-3°C/W	VERY HIGH	>100W COMPONENTS

### HEAT SINK SIZING

$$Required\ area \approx Power / (h \times \Delta T)$$

#### EXAMPLE:

- Power dissipation: 10W
- Temperature rise limit: 40°C
- Natural convection  $h = 10\text{ W/m}^2\cdot\text{K}$
- Required area:  $10\text{W} / (10 \times 40) = 0.025\text{m}^2 = 250\text{cm}^2$



### FIN EFFICIENCY:

Longer, thinner fins have reduced efficiency due to thermal resistance along the fin length.

#### OPTIMAL FIN SPACING:

CONVECTION TYPE	FIN SPACING	OPTIMIZATION
NATURAL	8-12MM	MINIMIZE INTERFERENCE
LOW SPEED FORCED	4-8MM	BALANCE AREA/FLOW
HIGH SPEED FORCED	2-4MM	MAXIMUM AREA

## 7.2 Integration Methods

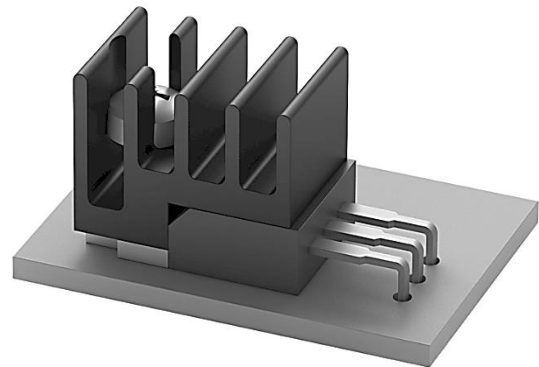
### COMPONENT-LEVEL INTEGRATION:

#### TO-220 PACKAGES:

- Thermal interface required
- Electrical isolation considerations
- Multiple mounting options

#### SURFACE MOUNT PACKAGES:

- Heat sink attachment to PCB
- Thermal pad connections
- Assembly complexity



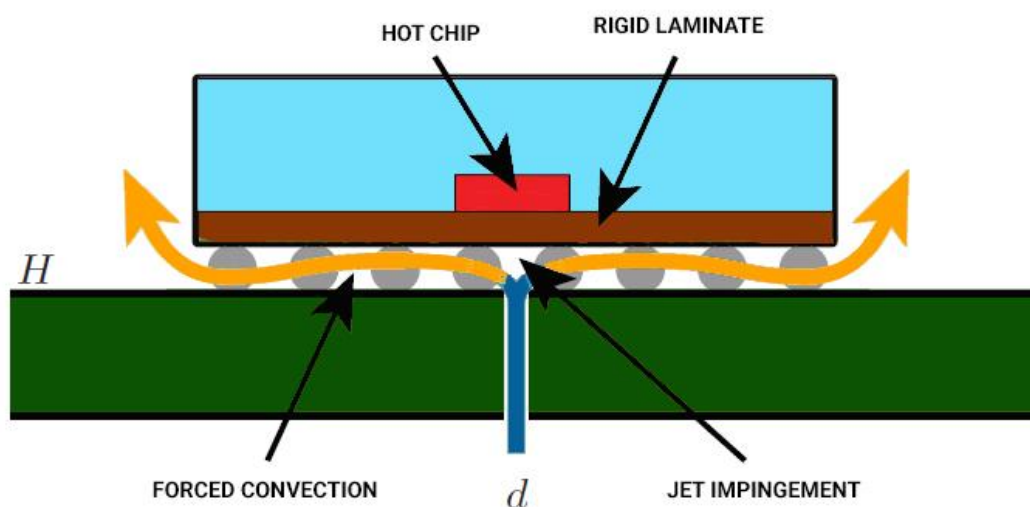
### SYSTEM-LEVEL INTEGRATION:

#### CHASSIS INTEGRATION:

- PCB mounted to chassis
- Component thermal pads contact chassis
- Maximum heat dissipation

#### DEDICATED COOLING SYSTEMS:

- Separate heat sink assemblies
- Heat pipes for heat transport
- Liquid cooling for extreme cases





# ACTIVE & PASSIVE COOLING

## 8.1 Natural Convection Design

### BUOYANCY-DRIVEN FLOW

Natural convection relies on density differences in heated air to create airflow.

### HEAT TRANSFER COEFFICIENT

$$h = C \times (\Delta T / L)^n$$

Where:

C = Constant based on geometry

$\Delta T$  = Temperature difference

L = Characteristic length

n = Exponent (typically 0.25)

### BOARD ORIENTATION EFFECTS:

#### VERTICAL ORIENTATION:

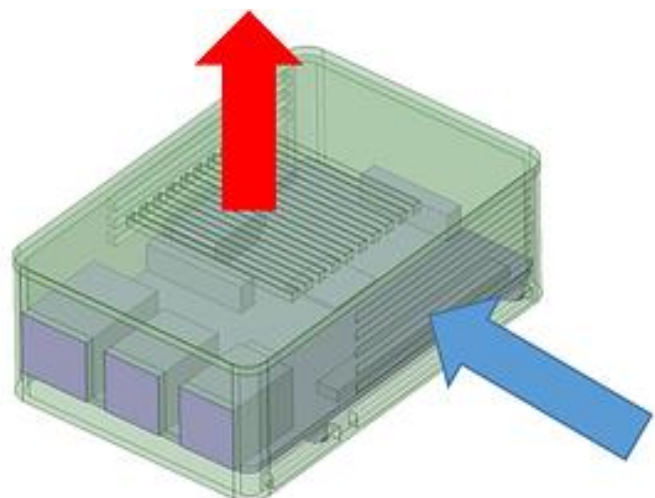
- Best natural convection
- Unobstructed airflow
- 25-30% better than horizontal
- Recommended when possible

#### HORIZONTAL (COMPONENTS UP):

- Moderate convection
- Component interference
- Hot air pooling
- Standard orientation

#### HORIZONTAL (COMPONENTS DOWN):

- Poor convection
- Heat trapped
- Worst case scenario
- Avoid if possible



## 8.2 Forced Air Systems

### FAN SELECTION CRITERIA:

**AIRFLOW VS STATIC PRESSURE:**

- High airflow: Open systems, low restriction
- High static pressure: Restricted systems, heat sinks

### FAN CURVES

Every fan has a characteristic curve relating airflow to static pressure.

**TYPICAL FAN PERFORMANCE:**

FAN SIZE	FREE AIR FLOW	MAX STATIC PRESSURE	NOISE LEVEL
40MM	10-20 CFM	5-15 MMH2O	25-40 DBA
60MM	25-50 CFM	8-20 MMH2O	20-35 DBA
80MM	40-80 CFM	10-25 MMH2O	18-30 DBA
120MM	80-150 CFM	12-30 MMH2O	15-25 DBA

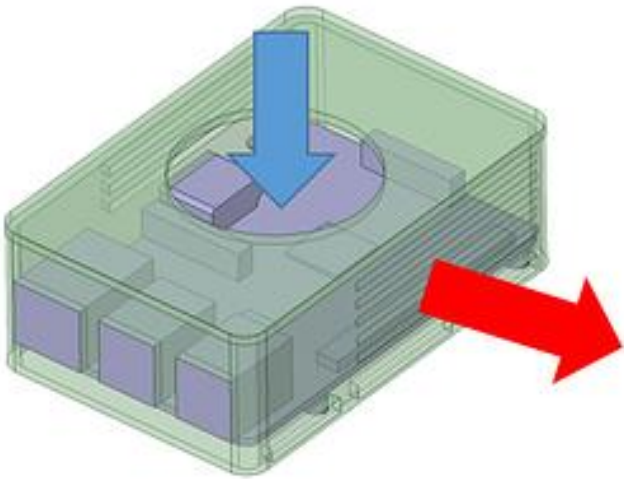
### FAN PLACEMENT STRATEGIES

**EXHAUST CONFIGURATION:**

- Fan pulls air through system
- Negative pressure inside enclosure
- Slightly better cooling efficiency

**INLET CONFIGURATION:**

- Fan pushes air through system
- Positive pressure inside enclosure
- Direct component cooling

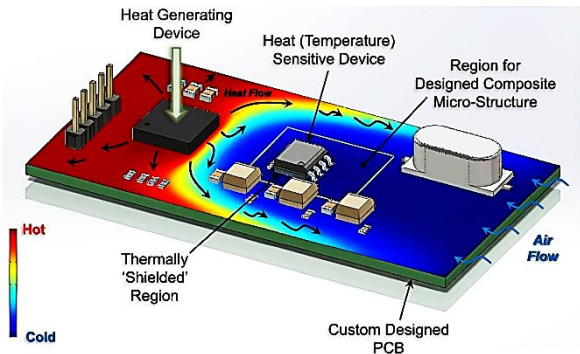


### 8.3 System-Level Integration

#### THERMAL ARCHITECTURE PLANNING

**HEAT SOURCE MAPPING:**

- Identify all significant heat sources
- Calculate individual power dissipation
- Map thermal interaction zones
- Plan heat removal paths



**SYSTEM THERMAL BUDGET:**

COMPONENT	POWER (W)	LOCAL TEMP RISE (°C)	COOLING METHOD
CPU	25	45	HEAT SINK + FAN
POWER SUPPLY	15	35	NATURAL CONVECTION
LED ARRAY	8	30	MCPCB + HEAT SINK
LINEAR REGULATOR	3	25	COPPER PLANE
TOTAL	51	-	SYSTEM FAN

#### LIQUID COOLING INTEGRATION

**WHEN TO CONSIDER LIQUID COOLING:**

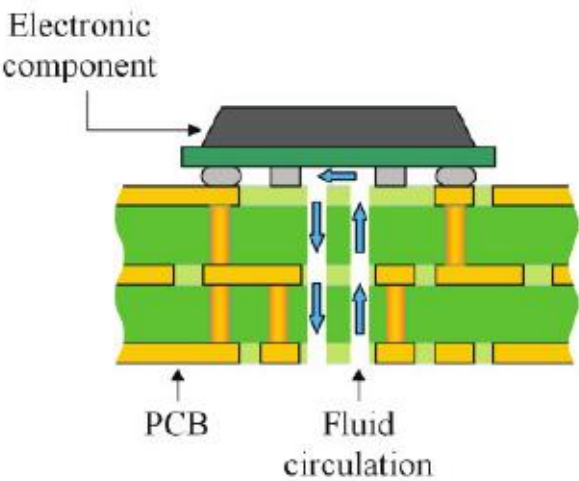
- Power density >200W/L
- Quiet operation required
- Remote heat rejection needed

**LIQUID COOLING TYPES:**

- Closed loop systems
- Custom loops
- Phase change cooling

**IMPLEMENTATION CHALLENGES:**

- Leak prevention critical
- Pump reliability
- Maintenance requirements



## 8.4 Simulation Tools and Methods

### THERMAL SIMULATION CATEGORIES

**COMPONENT-LEVEL:**

- Package thermal models
- Junction-to-case resistance
- Thermal test chip data
- JEDEC standard models

**BOARD-LEVEL:**

- PCB layer stack-up modeling
- Component placement optimization
- Via thermal network analysis
- Airflow interaction

**SYSTEM-LEVEL:**

- Enclosure thermal modeling
- Fan curve integration
- Multi-board interactions
- Environmental conditions



**POPULAR SIMULATION TOOLS:**

TOOL	CAPABILITY	COST	APPLICATION
ANSYS ICEPAK	FULL 3D CFD	HIGH	PROFESSIONAL
MENTOR FLOTHERM	ELEC FOCUSED	HIGH	PROFESSIONAL
SIWAVE	SI/PI/THERMAL	MEDIUM	BOARD LEVEL
OPENFOAM	OPEN SOURCE CFD	FREE	ACADEMIC



## 8.5 Measurement and Validation

### TEMPERATURE MEASUREMENT METHODS

**THERMOCOUPLES:**

- Wide temperature range
- Good accuracy ( $\pm 1-2^{\circ}\text{C}$ )
- Multiple point monitoring

**INFRARED CAMERAS:**

- Full surface temperature map
- Real-time monitoring
- Emissivity compensation required

**THERMAL TEST POINTS:**

- PCB-mounted temperature sensors
- Specific location monitoring
- Continuous operation data



**MEASUREMENT ACCURACY FACTORS:**

FACTOR	IMPACT	MITIGATION
THERMAL MASS	MEASUREMENT DELAY	SMALL SENSORS
CONTACT RESISTANCE	LOWER READINGS	THERMAL INTERFACE
AIR CURRENTS	FLUCTUATING READINGS	SHIELD SENSORS
EMISSIVITY VARIATION	IR CAMERA ERRORS	CALIBRATION

### VALIDATION PROCESS

**THERMAL TEST PROTOCOL:**

- Power-up sequence documentation
- Steady-state temperature recording
- Transient response measurement

**CORRELATION WITH SIMULATION:**

- Compare measured vs predicted
- Update simulation models
- Refine design parameters

# ADVANCED TOPICS

## 9.1 Thermal Reliability Engineering

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### ACCELERATED TESTING

#### TEMP CYCLING:

- -40°C to +125°C typical
- 1000+ cycles standard
- Solder joint reliability
- Package stress analysis

#### POWER CYCLING:

- On/off thermal stress
- Bond wire fatigue
- Die attach reliability
- Real-world simulation

### LIFE PREDICTION MODELS

#### ARRHENIUS MODEL:

$$h = C \times (\Delta T/L)^n$$

#### COFFIN-MANSON MODEL:

$$Nf = A \times (\Delta T)^{-n}$$

Where:

Nf = Cycles to failure

$\Delta T$  = Temperature swing

n = Material constant

A = Material constant

### DESIGN FOR RELIABILITY

- 20°C margin from limits
- Conservative design approach
- Extended operational life
- Reduced warranty costs

## 9.2 Future Trends and Technologies

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### ADVANCED PCB TECHNOLOGIES

#### EMBEDDED COMPONENTS:

- Components inside PCB
- Improved thermal paths
- Reduced assembly height
- Manufacturing complexity

#### 3D PRINTED HEAT EXCHANGERS:

- Complex geometries
- Optimized heat transfer
- Custom solutions
- Rapid prototyping

### SMART THERMAL MANAGEMENT

#### ADAPTIVE COOLING:

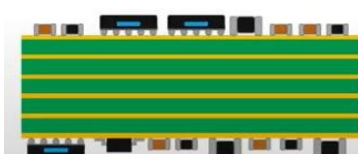
- Temperature-based fan control
- Dynamic power management
- Predictive thermal control
- System optimization

#### THERMAL MONITORING NETWORKS:

- Distributed sensors
- Real-time monitoring
- Predictive maintenance
- System health assessment

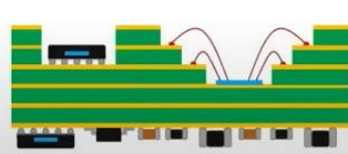
Normal Multilayer-PCB

Components on Top and Bottom



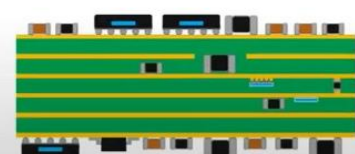
PCB with Cavities

Components in the defined cavities on defined layers and assembly from "outside".



PCB with Embedded Components

Components on the defined inner layers with layer connection and orientation (up/down)





# DESIGN GUIDELINES SUMMARY

## Material Selection Guide

DENSITY	PCB MATERIAL	COPPER	COOLING METHOD
<1W/CM <sup>2</sup>	STANDARD FR-4	10Z	NATURAL CONVECTION
1-5W/CM <sup>2</sup>	HIGH TG FR-4	20Z	HEAT SINK + NATURAL
5-15W/CM <sup>2</sup>	MCPCB	30Z	FORCED AIR
>15W/CM <sup>2</sup>	CERAMIC	HEAVY	LIQUID COOLING

## Thermal Via Guidelines

POWER	VIA COUNT	VIA SIZE	SPACING
<1W	4	0.2MM	1.5MM
1-5W	9	0.3MM	2.0MM
5-15W	16	0.5MM	2.5MM
>15W	25+	0.8MM	3.0MM

## Heat Sink Selection

POWER	HEAT SINK TYPE	TH RESISTANCE	TYPICAL COST
1-5W	STAMPED ALUMINUM	20-50°C/W	\$0.50-2.00
5-25W	EXTRUDED ALUMINUM	5-20°C/W	\$2.00-10.00
25-100W	BONDED FIN	2-10°C/W	\$10.00-50.00
>100W	VAPOR CHAMBER	0.5-3°C/W	\$50.00-200.00

## Design Checklist

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### **THERMAL ANALYSIS:**

- ☐ Power dissipation calculated for all components
- ☐ Junction temperatures verified within limits
- ☐ Thermal resistance paths analyzed
- ☐ Worst-case scenarios considered

### **PCB DESIGN:**

- ☐ Appropriate PCB material selected
- ☐ Copper weight optimized for thermal performance
- ☐ Thermal vias properly designed and placed
- ☐ Component placement optimized for heat flow

### **COOLING SYSTEM:**

- ☐ Heat sinks properly sized and selected
- ☐ Thermal interface materials specified
- ☐ Airflow requirements calculated
- ☐ Fan selection and placement optimized

### **VALIDATION:**

- ☐ Thermal simulation completed
- ☐ Temperature measurements planned
- ☐ Reliability analysis performed
- ☐ Design margins verified