Hardware Engineer's Guide

BRING-UP PLAN

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- Component Placement Verification
- Solder Joint Quality Assessment
- PCB Physical Damage Check

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- Critical Net Continuity Verification
- Power Domains solation Testing

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ANALOG & DESCRETE
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- Relays and Drivers

By Shimi Cohen

(INTRO) WHAT'S THE BOOK ABOUT?

In the journey from schematic to reality, receiving your first assembled PCB prototype is an exciting milestone. But what comes next? This book is a practical guide to taking those prototypes—the heart of your innovation—from delivery to reliable, fully-tested systems.

THE BOOK'S MAIN GOALS

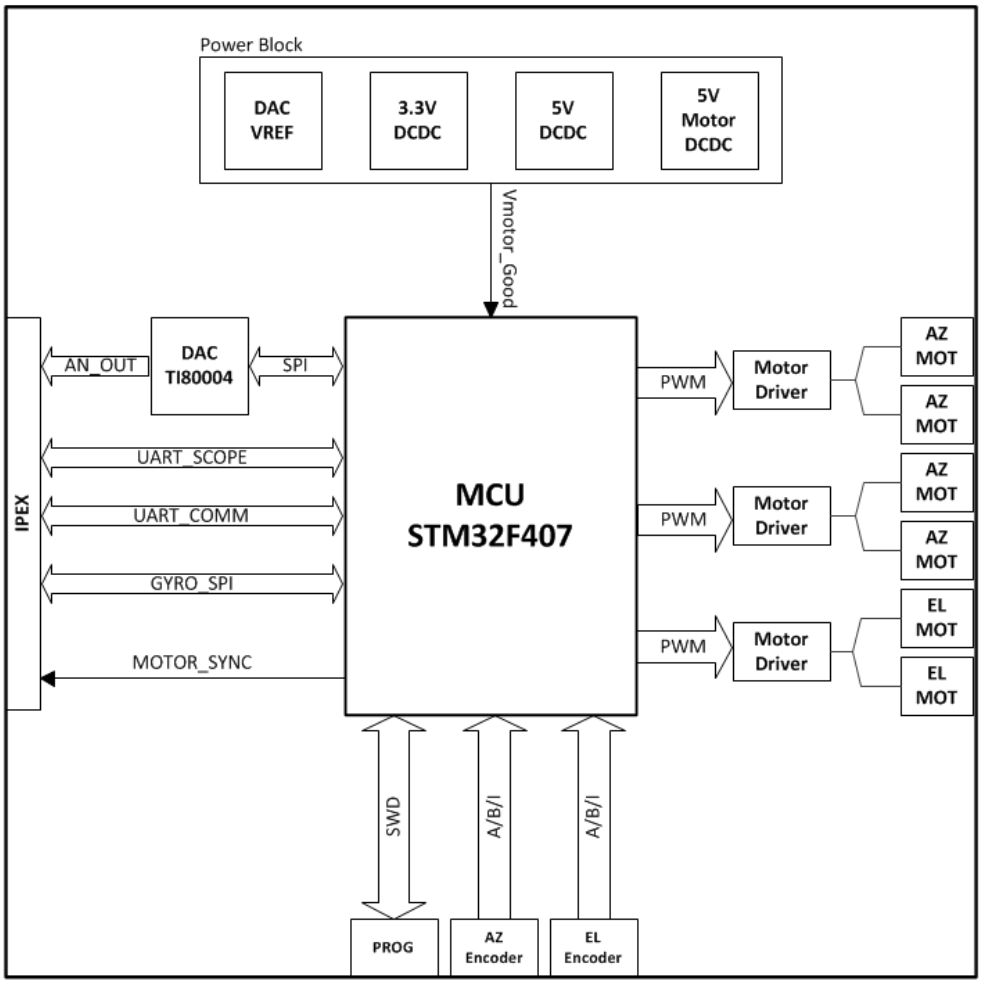
- What to Test
- Testing Order
- Documentation
- Troubleshooting Issues

BOOK SCOPE

This guide focuses on the practical aspects of prototypes that incorporate:

- MCUs as the core processing element.
- PC interfaces for monitoring or data transfer.
- Serial Communications (such as UART, SPI, I2C).
- Analog Circuits

REFRENCE BLOCK DIAGRAM



(1)VISUAL & ASSEMBLY INSPECTION

Initial visual inspection forms the foundation of successful board bring-up.

This phase identifies assembly errors before power application.

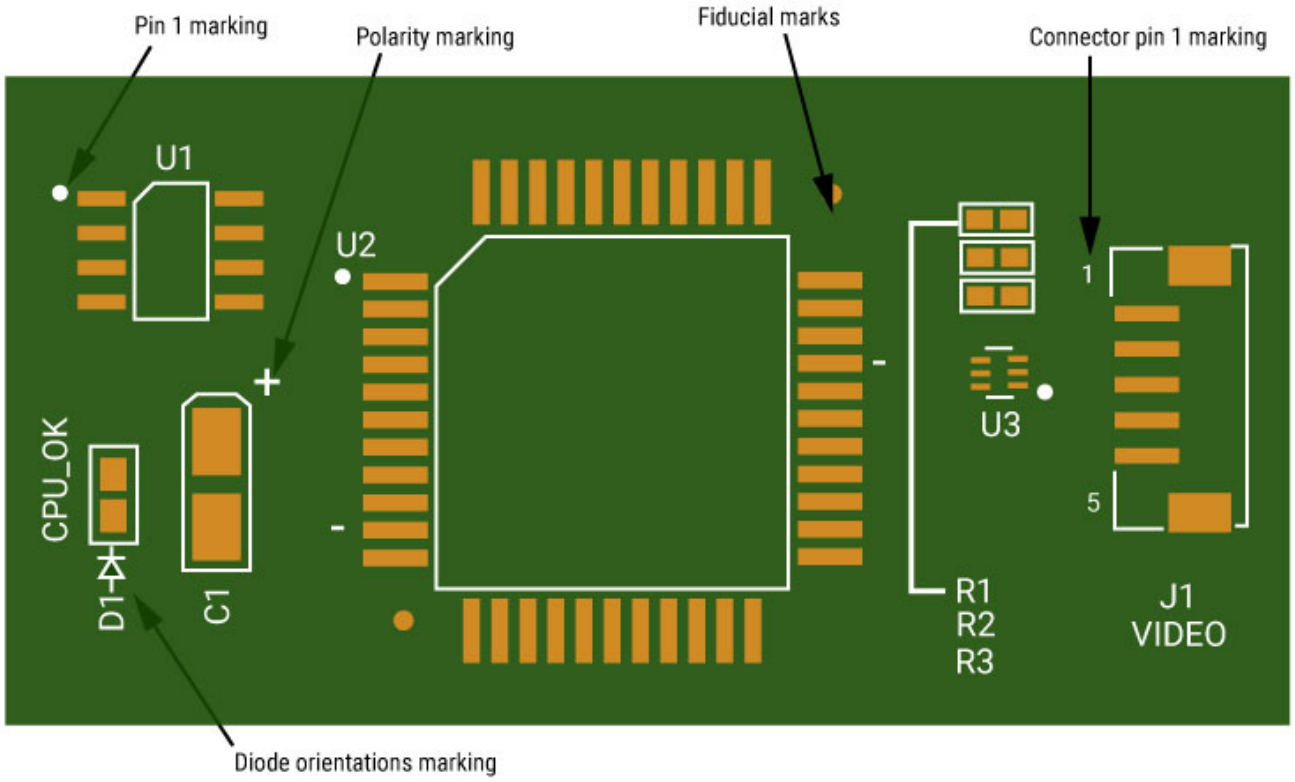
1.1 COMPONENT PLACEMENT VERIFICATION

Visual inspection must cover all populated components systematically.

Critical Components to Verify:

- Polarized components (electrolytic capacitors, diodes, LEDs)
- IC orientation markers (pin 1 indicators, notches)
- Connector pin assignments
- Crystal oscillator placement
- Power management components

Component Type	Verification Method	Common Issues
ICs	Pin 1 alignment with PCB silkscreen	180° rotation
Electrolytic Caps	Polarity marking alignment	Reverse polarity
Diodes	Cathode band orientation	Wrong direction
Connectors	Pin 1 position match	Offset placement



1.2 SOLDER JOINT QUALITY ASSESSMENT

Solder joint integrity directly impacts board functionality and reliability.

Joint Quality Indicators:

- Shiny, smooth surface finish
- Proper fillet formation
- No bridging between adjacent pins
- Complete pad wetting
- Appropriate solder volume

Common Solder Defects:

- Cold joints (dull, grainy appearance)
- Insufficient solder (poor mechanical connection)
- Excess solder (bridging risk)
- Tombstoning on passive components

1.3 PCB PHYSICAL DAMAGE CHECK

Physical damage assessment prevents intermittent failures during testing.

- Via integrity examination
- Trace continuity visual check
- Laminate delamination signs
- Edge connector damage
- Mounting hole integrity

(2)CONTINUITY TESTING

Testing without power prevents damage from assembly errors or short circuits.

2.1 POWER RAIL CONTINUITY TESTING

Power rail verification ensures proper distribution before energizing the board.

Test Sequence:

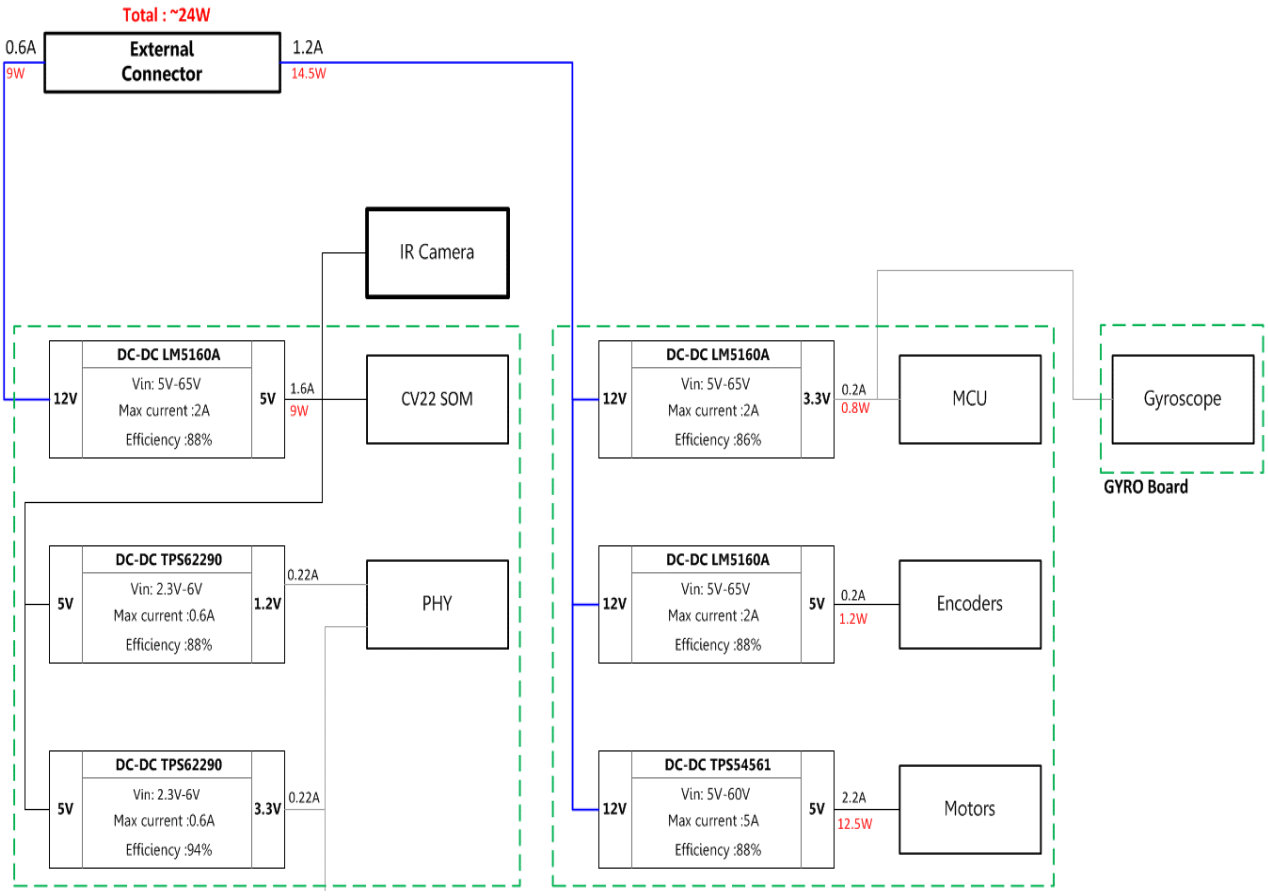
1. Locate main power input connector
2. Identify all voltage domains from schematic
3. Measure resistance from power pins to ground
4. Verify expected resistance ranges

Voltage Rail	Expected Resistance	Acceptable Range
Digital VCC	10Ω - 1kΩ	Load dependent
Analog AVCC	100Ω - 10kΩ	Higher due to filtering
I/O Rails	50Ω - 500Ω	Pin count dependent

2.2 POWER TREE

Follow the power tree when verifying power domains.

Power Tree block diagram Example:



2.2 CRITICAL NET CONTINUITY VERIFICATION

Essential signal paths require verification before power application.

Priority Nets for Testing:

- Crystal oscillator connections
- Reset circuit paths
- Boot configuration pins
- Programming interface signals
- Power enable/control signals

Testing Method:

- Use multimeter continuity function
- Verify end-to-end connectivity
- Check for unintended connections to adjacent nets
- Confirm pull-up/pull-down resistor values

2.3 ISOLATION TESTING BETWEEN POWER DOMAINS

Multi-rail designs require isolation verification to prevent cross-domain issues.

- Measure resistance between different voltage domains
- Verify isolation exceeds 1MΩ minimum
- Check analog/digital ground separation (if implemented)
- Confirm power domain switching circuits

(3)POWER BRING-UP

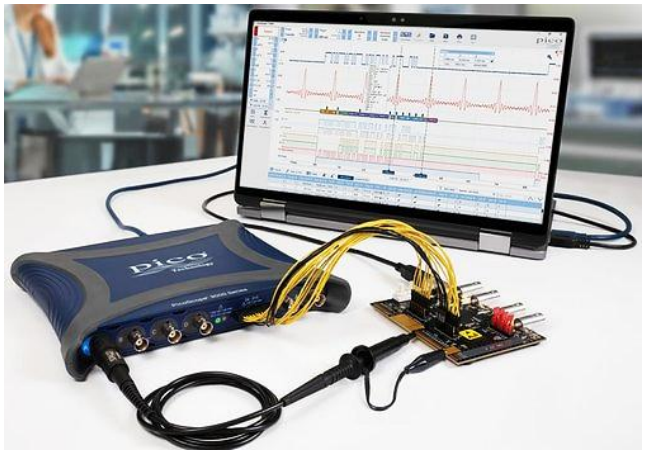
Power system verification follows a systematic approach from input to load regulation.

3.1 INPUT POWER VERIFICATION

Input power validation ensures safe operation before connecting sensitive loads.

Input Voltage Verification:

- Measure input voltage at the connector using scope
- Verify polarity correctness
- Check voltage stability under no-load
- Confirm current limiting if present



Protection Circuit Testing:

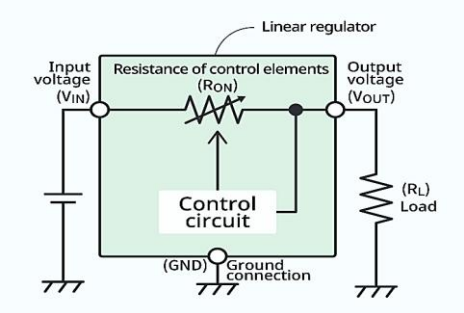
- Reverse polarity protection operation
- Overvoltage protection thresholds
- Overcurrent protection functionality
- ESD protection integrity

3.2 LINEAR REGULATOR BRING-UP

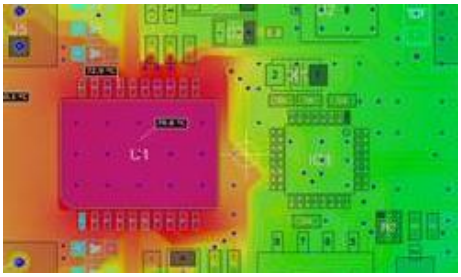
Linear regulators provide stable voltage references and low-noise supplies.

LDO Verification Sequence:

1. Input voltage application
2. Enable signal assertion (if applicable)
3. Output voltage measurement
4. Load regulation testing
5. Thermal monitoring



Parameter	Test Method	Acceptance Criteria
Output Voltage	DMM measurement	±2% of nominal
Load Regulation	Variable load application	<50mV change
Thermal Performance	Thermal imaging	<85°C junction



3.3 SWITCHING REGULATOR VERIFICATION

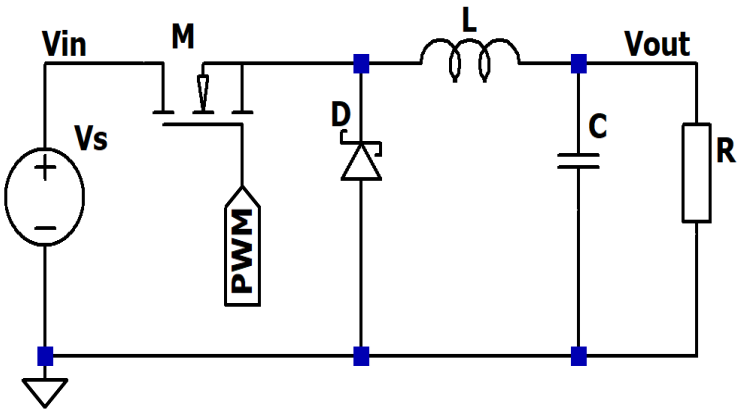
Switch-mode P.S requires additional verification steps due to its complexity.

Buck Converter Testing:

- Input voltage ramp-up monitoring
- Switching frequency measurement
- Output ripple characterization
- Efficiency verification at rated load

Critical Measurements:

- Switching node voltage
- Inductor current waveform
- Output capacitor ESR effects
- Control loop stability indicators

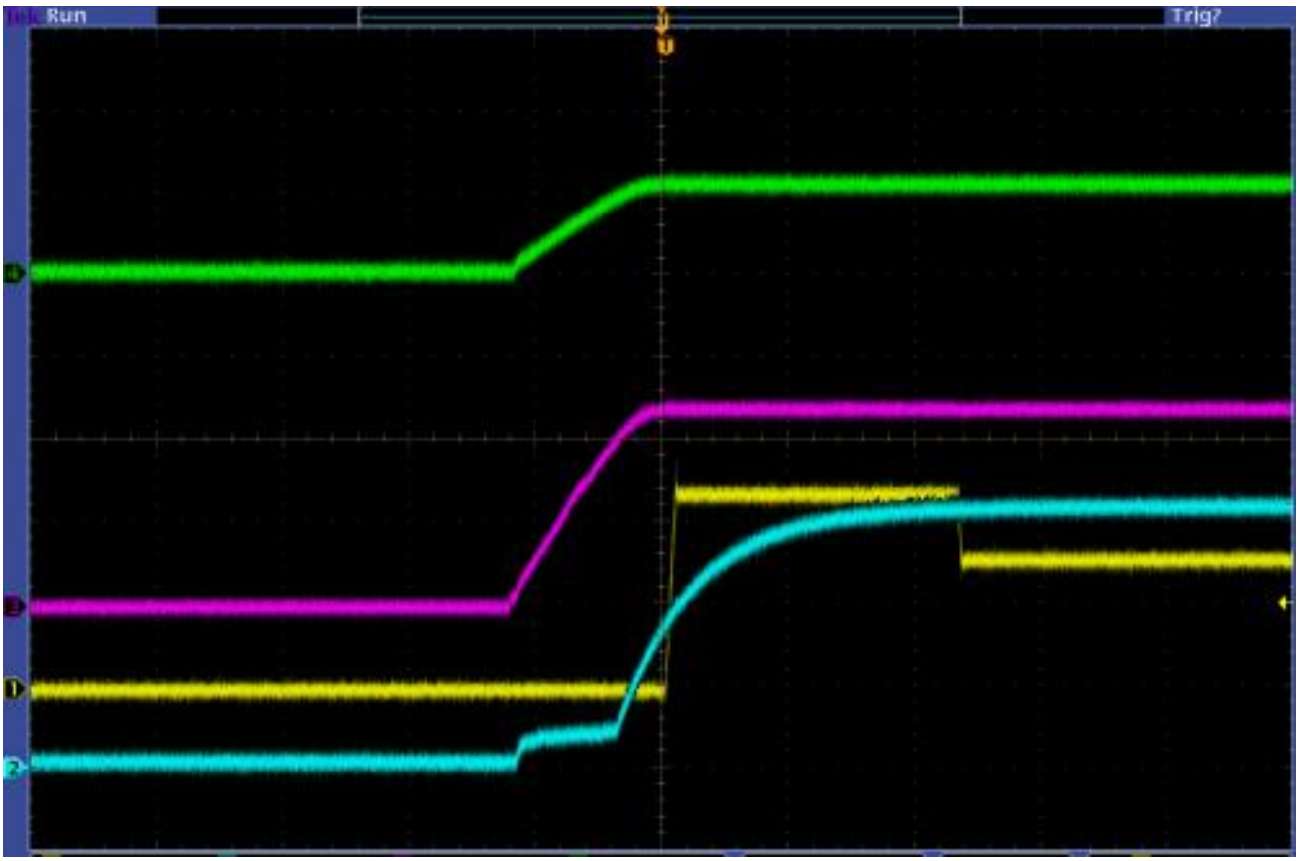


3.4 POWER SEQUENCING VERIFICATION

Multi-rail systems often require specific power-up sequences for proper operation.

Sequencing Validation:

- Record power-up timing with oscilloscope
- Verify rise time specifications
- Check inter-rail timing relationships
- Monitor for voltage overshoot during startup



(4)CLOCK & TIMING

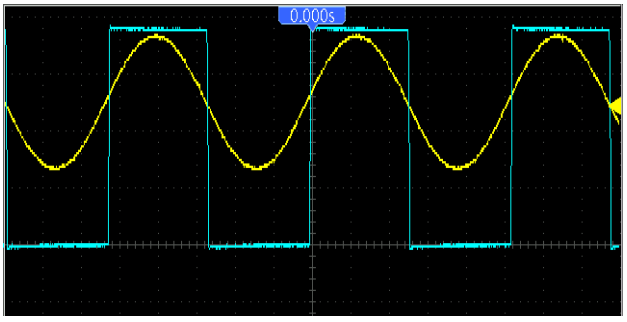
Clock system integrity determines overall system timing accuracy and stability.

4.1 CRYSTAL OSCILLATOR TESTING

Crystal oscillators provide the fundamental timing reference for MCU operation.

Primary Crystal Verification:

- Oscillation frequency measurement
- Amplitude level checking
- Startup time characterization
- Load capacitance verification



Measurement Technique:

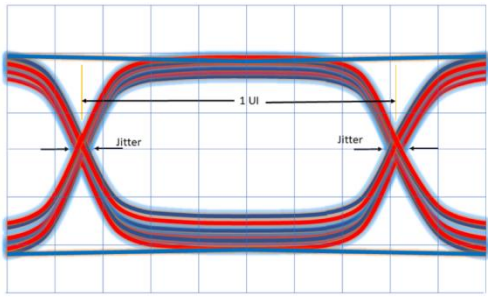
- Use high-impedance oscilloscope probe
- Minimize probe loading effects
- Measure at MCU crystal input pin
- Document frequency accuracy

4.2 CLOCK DISTRIBUTION VERIFICATION

Clock signals must maintain integrity throughout the distribution network.

Distribution Testing:

- Signal integrity at each clock destination
- Rise/fall time measurements
- Duty cycle verification
- Jitter characterization (if critical)

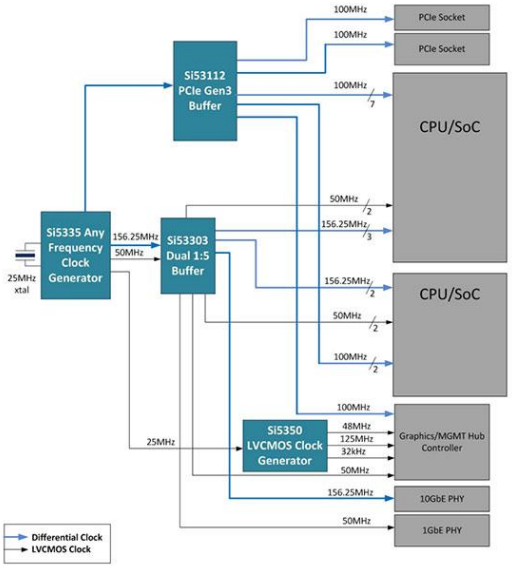


4.3 PLL AND CLOCK MULTIPLICATION

Phase-locked loops multiply reference frequencies for higher-speed operation.

PLL Verification Process:

- Reference clock stability confirmation
- PLL lock indication monitoring
- Output frequency accuracy
- Lock time measurement



(5)MCU VERIFICATION

MCU functionality verification establishes the foundation for all subsequent testing.

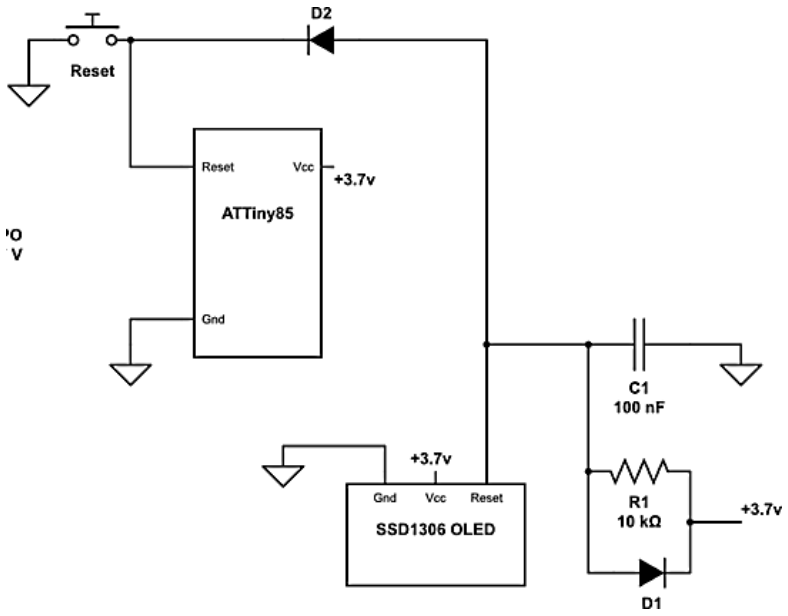
5.1 RESET CIRCUIT TESTING

Reset circuit proper operation ensures reliable startup and recovery capability.

Reset Signal Verification:

- Power-on reset timing
- External reset button functionality
- Reset signal voltage levels
- Reset duration measurement

Reset Type	Test Method	Expected Result
Power-On Reset	Power cycle monitoring	Clean reset assertion
External Reset	Button press test	Immediate reset response
Watchdog Reset	Software timeout	Automatic recovery

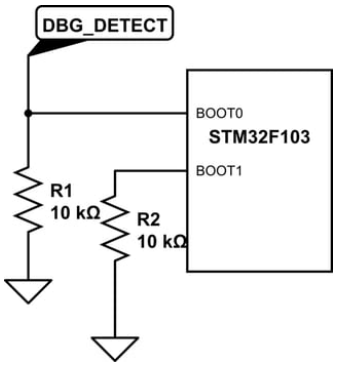


5.2 BOOT CONFIGURATION VERIFICATION

Boot mode selection determines MCU startup behavior and programming accessibility.

Boot Pin States:

- Boot mode pin voltage levels
- Pull-up/pull-down resistor values
- Mode selection switching (if implemented)
- Programming mode accessibility



5.3 PROGRAMMING INTERFACE TESTING

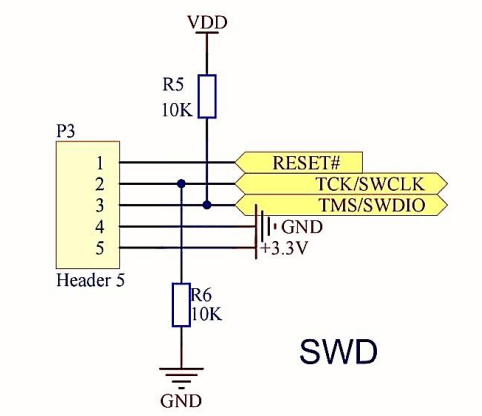
Programming interface verification enables FW loading and debugging capabilities.

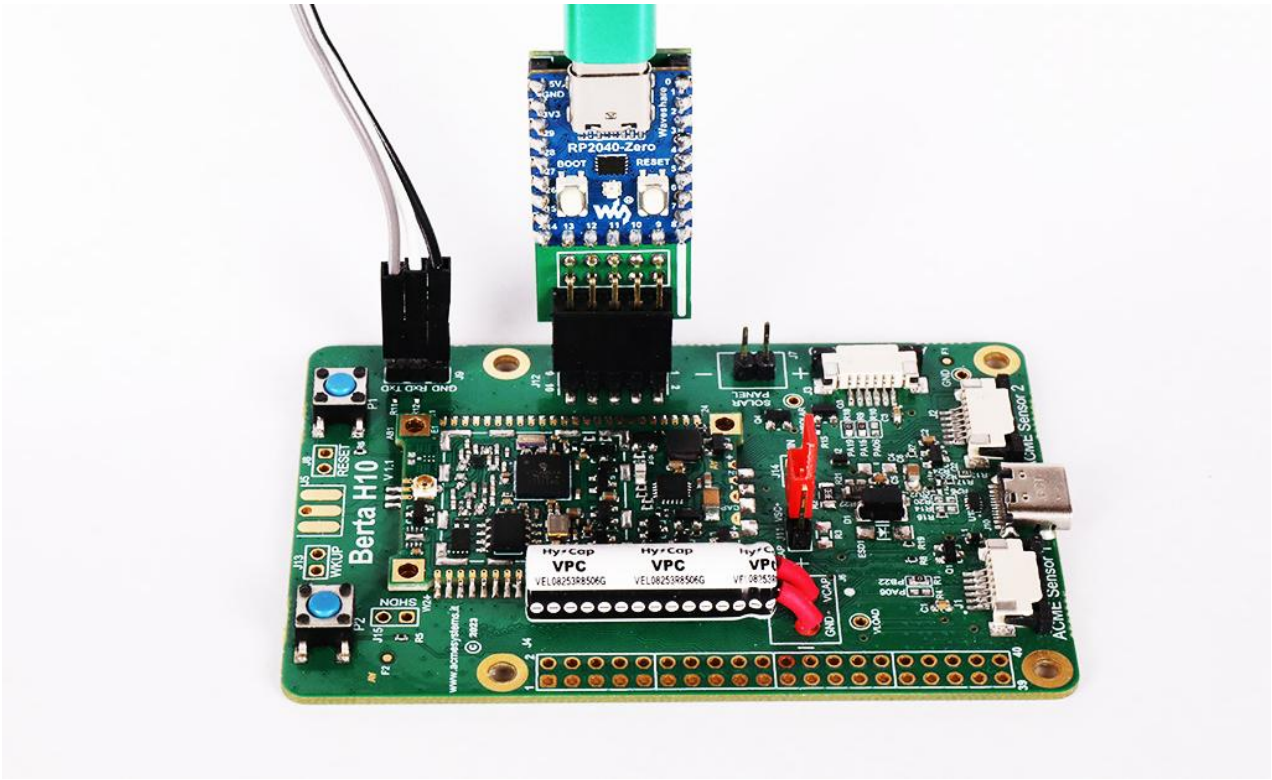
SWD/JTAG Interface Testing:

- Signal level verification (3.3V or 1.8V)
- Connection integrity to programming connector
- Debugger recognition test
- Basic communication establishment

Programming Connector Verification:

- Pin assignment correctness
- Mechanical connection reliability
- Signal integrity through connector
- Power delivery capability (if applicable)





(6)COMM INTERFACE

Comm. interfaces enable data exchange with external systems and peripherals.

6.1 UART INTERFACE TESTING

UART interfaces provide simple serial communication for debugging and data transfer.

UART Verification Process:

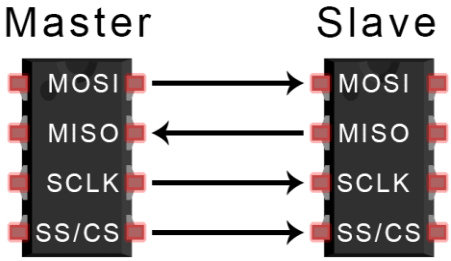
- Baud rate generator accuracy
- Signal level verification (RS-232, TTL, or LVTTL)
- Loopback testing capability
- Flow control signal operation (if implemented)

6.2 SPI INTERFACE VERIFICATION

SPI interfaces enable high-speed communication with sensors and peripheral devices.

SPI Signal Verification:

- Clock signal integrity (SCLK)
- Data line functionality (MOSI, MISO)
- Chip select operation (CS/SS)
- Signal timing relationships



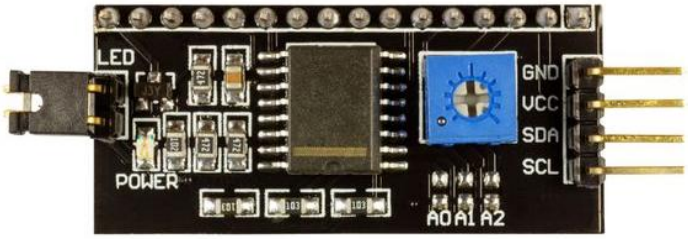
SPI Signal	Test Method	Verification Point
SCLK	Oscilloscope measurement	Frequency and duty cycle
MOSI	Logic analyzer capture	Data transmission accuracy
MISO	Loopback or device response	Data reception capability
CS	Timing analysis	Setup and hold times

6.3 I2C INTERFACE TESTING

I2C interfaces provide multi-device communication capability with address-based selection.

I2C Bus Verification:

- Pull-up resistor values (typically 4.7kΩ for 3.3V)
- Signal voltage levels (VIH, VIL compliance)
- Bus capacitance effects
- Address collision avoidance



(7)ANALOG CIRCUITS

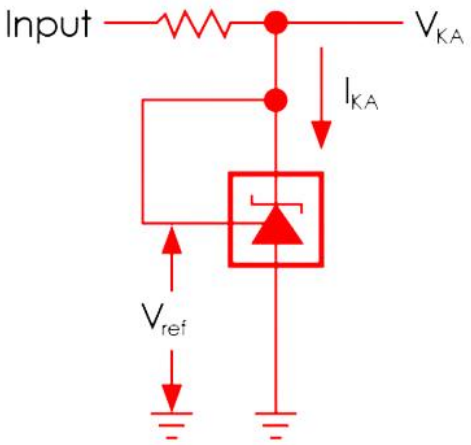
Analog circuits require specialized testing due to their continuous signal nature.

7.1 REFERENCE VOLTAGE TESTING

Reference voltages provide stable voltage standards for ADC and DAC operations.

Reference Verification:

- Output voltage accuracy measurement
- Temperature stability assessment
- Load regulation characterization
- Noise measurement (if critical)



Voltage Reference Testing:

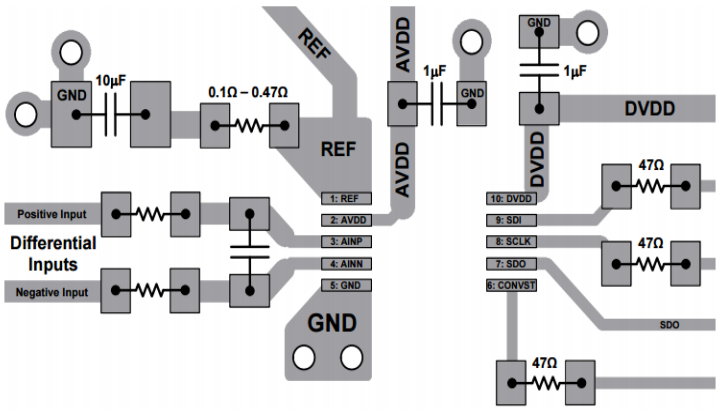
- Use precision DVM for accuracy measurement
- Apply varying loads to test regulation
- Monitor temperature coefficient effects
- Verify initial accuracy specifications

7.2 ADC INPUT CIRCUIT VERIFICATION

ADC input circuits condition analog signals for accurate digital conversion.

Input Circuit Testing:

- Input impedance measurement
- Gain accuracy verification
- Offset voltage measurement
- Input protection functionality



ADC Verification Process:

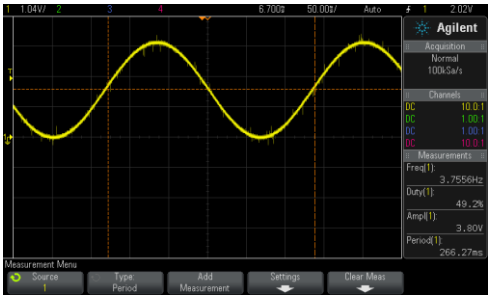
1. Apply known input voltage
2. Read ADC conversion result
3. Calculate conversion accuracy
4. Verify full-scale range operation

7.3 DAC OUTPUT CIRCUIT TESTING

DAC output circuits convert digital values to analog voltages or currents.

DAC Testing Methodology:

- Linearity measurement across full range
- Output impedance characterization
- Settling time measurement
- Glitch impulse evaluation



(8)SENSOR INTERFACE

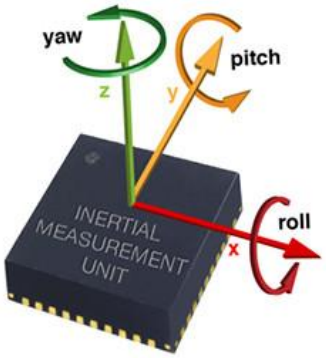
Sensor interfaces enable measurement and monitoring of physical parameters.

8.1 IMU SENSOR TESTING

Inertial measurement units provide acceleration and angular velocity information.

IMU Verification Steps:

- Power supply voltage verification
- I2C/SPI communication establishment
- Device ID register readback
- Basic sensor response testing

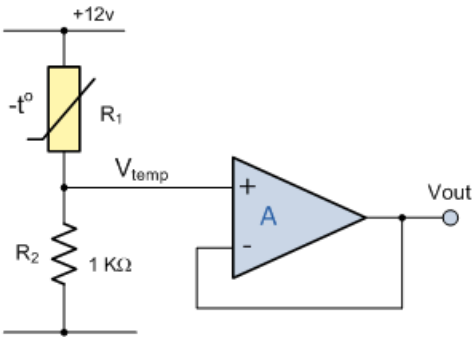


8.2 TEMPERATURE SENSOR VERIFICATION

Temperature sensors provide thermal monitoring and compensation capabilities.

Temperature Sensor Testing:

- Sensor communication protocol verification
- Ambient temperature reading accuracy
- Resolution and precision assessment
- Response time characterization

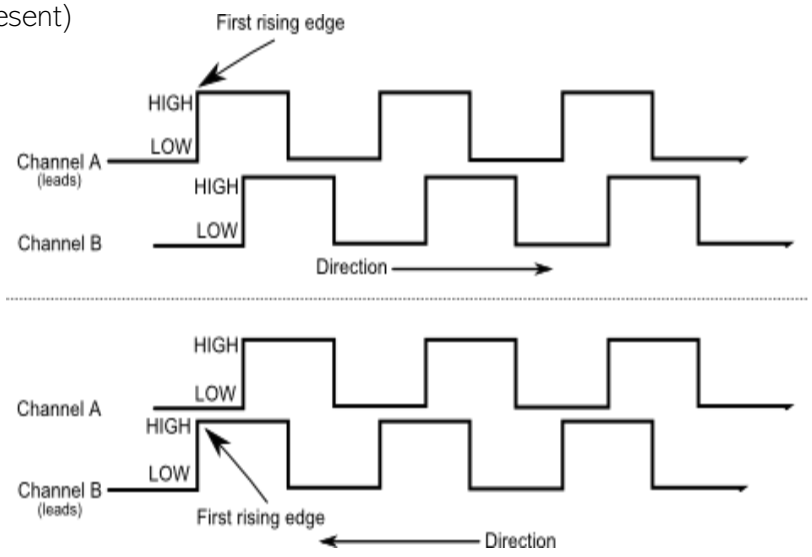


8.3 POSITION ENCODER INTERFACE

Position encoders provide feedback for motion control applications.

Encoder Interface Testing:

- Signal level verification (differential or single-ended)
- Count accuracy during manual rotation
- Direction sensing capability
- Index pulse functionality (if present)

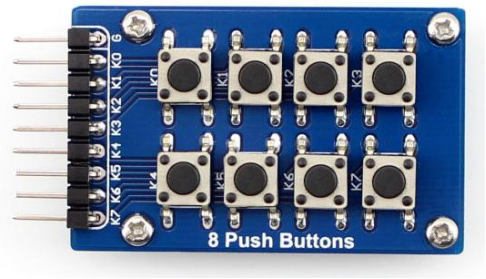


(9)DISCRETE HARDWARE

Discrete HW components provide switching, indication, and user interface functions.

9.1 SWITCH AND BUTTON TESTING

Switches and buttons provide user input and control capabilities.



Switch Verification:

- Contact resistance measurement
- Bounce characteristics assessment
- Pull-up/pull-down resistor verification
- Debouncing circuit functionality

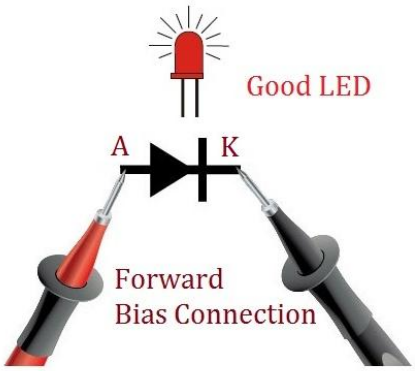
Switch Type	Test Method	Expected Result
Mechanical Button	Resistance measurement	<1Ω closed, >1MΩ open
DIP Switch	State verification	Clean logic levels
Rotary Switch	Position testing	Correct encoding

9.2 LED INDICATOR TESTING

LED indicators provide visual feedback for system status and operation.

LED Verification Process:

- Forward voltage measurement
- Current limiting resistor calculation
- Brightness level assessment
- Color accuracy verification



LED Test Calculation:

$LED\ Current\ =\ (VCC\ -\ Vf)\ /\ R\_series$

$For\ 3.3V\ supply, 2.1V\ red\ LED, 330\Omega\ resistor$:

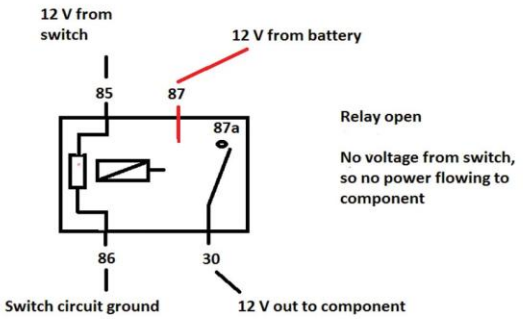
$I\_LED\ =\ (3.3V\ -\ 2.1V)\ /\ 330\Omega\ =\ 3.6mA$

9.3 RELAY AND DRIVER TESTING

Relays provide electrical isolation and high-current switching capabilities.

Relay Circuit Verification:

- Coil resistance measurement
- Driver circuit functionality
- Contact resistance verification
- Flyback diode operation



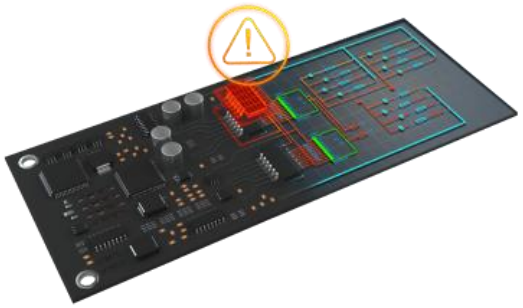
(10)FINAL VERIFICATION

System integration testing verifies coordinated operation of all subsystems.

10.1 POWER CONSUMPTION ANALYSIS

Power consumption verification ensures design meets specification requirements.

Power Measurement Methodology:



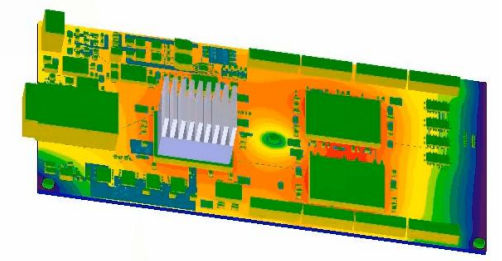
- Measure current in each power domain
- Calculate total system power consumption
- Verify sleep mode current levels
- Assess battery life implications (if applicable)

Operating Mode	Typical Current	Measurement Method
Active Mode	50-200mA	In-line current measurement
Sleep Mode	10-100μA	Precision current monitor
Deep Sleep	1-10μA	Specialized low-current meter

10.2 THERMAL PERFORMANCE VERIFICATION

Thermal performance ensures reliable operation across temperature ranges.

Thermal Testing Approach:



- Identify heat-generating components
- Measure component case temperatures
- Verify thermal design margin
- Assess cooling requirements

10.3 FUNCTIONAL INTEGRATION TESTING

Integration testing verifies coordinated subsystem operation.

System-Level Test Sequence:

1. Power-up sequence verification
2. Boot process completion
3. Communication interface initialization
4. Sensor data acquisition
5. Output device control
6. Error handling verification

(11)DOCUMENTATION & REPORT

Proper documentation ensures reproducibility and supports production transition.

11.1 TEST RESULTS DOCUMENTATION

Test result documentation provides traceability and verification records.

Documentation Requirements:

- Measured values with tolerances
- Test equipment calibration status
- Environmental conditions
- Pass/fail criteria assessment
- Anomaly identification and resolution

11.2 ISSUE TRACKING AND RESOLUTION

Issue tracking ensures systematic problem resolution and design improvement.

Issue Management Process:

- Problem identification and categorization
- Root cause analysis methodology
- Corrective action implementation
- Verification of fix effectiveness
- Documentation update requirements

11.3 PRODUCTION READINESS ASSESSMENT

Production readiness evaluation determines manufacturing suitability.

Readiness Criteria:

- All functional tests passed
- Design margins verified
- Manufacturing tolerances confirmed
- Quality control procedures established
- Documentation completeness verified

(12)TROUBLESHOOTING GUIDE

Common issues and troubleshooting approaches for efficient problem resolution.

12.1 POWER SYSTEM ISSUES

Power system problems affect all downstream circuits.

No Output Voltage:

- Verify input voltage presence and polarity
- Check enable signals (if applicable)
- Measure feedback network integrity
- Verify regulator IC functionality

Unstable Output Voltage:

- Examine output capacitor ESR and value
- Check compensation network components
- Verify load current within specifications
- Assess thermal shutdown conditions

12.2 COMMUNICATION INTERFACE PROBLEMS

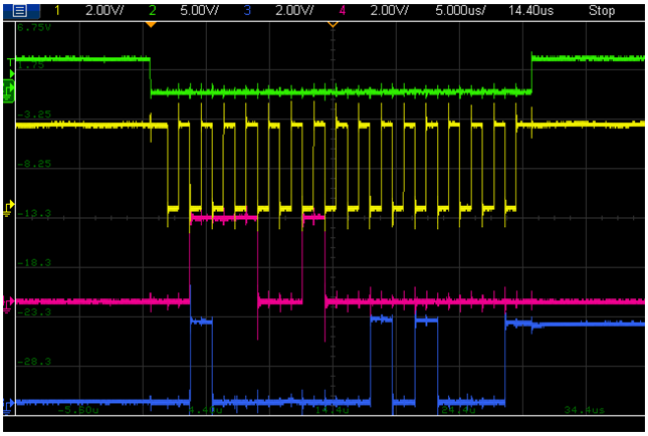
Communication failures prevent proper system operation and debugging capability.

SPI Communication Failure:

- Verify clock signal generation and routing
- Check MOSI/MISO signal integrity
- Confirm chip select timing and polarity
- Validate pull-up/pull-down requirements

I2C Bus Issues:

- Measure pull-up resistor values and bus voltage
- Verify address conflicts between devices
- Check for stuck bus conditions
- Confirm timing parameter compliance



12.3 CLOCK SYSTEM MALFUNCTIONS

Clock system failures prevent MCU operation and require immediate resolution.

Crystal Not Oscillating:

- Verify load capacitor values and placement
- Check crystal series resistance specification
- Measure drive level and amplitude
- Confirm PCB layout parasitics

Frequency Inaccuracy:

- Validate load capacitance calculation
- Assess temperature coefficient effects
- Verify crystal specification compliance
- Check for interference sources