

CAPACITOR



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CAPACITOR



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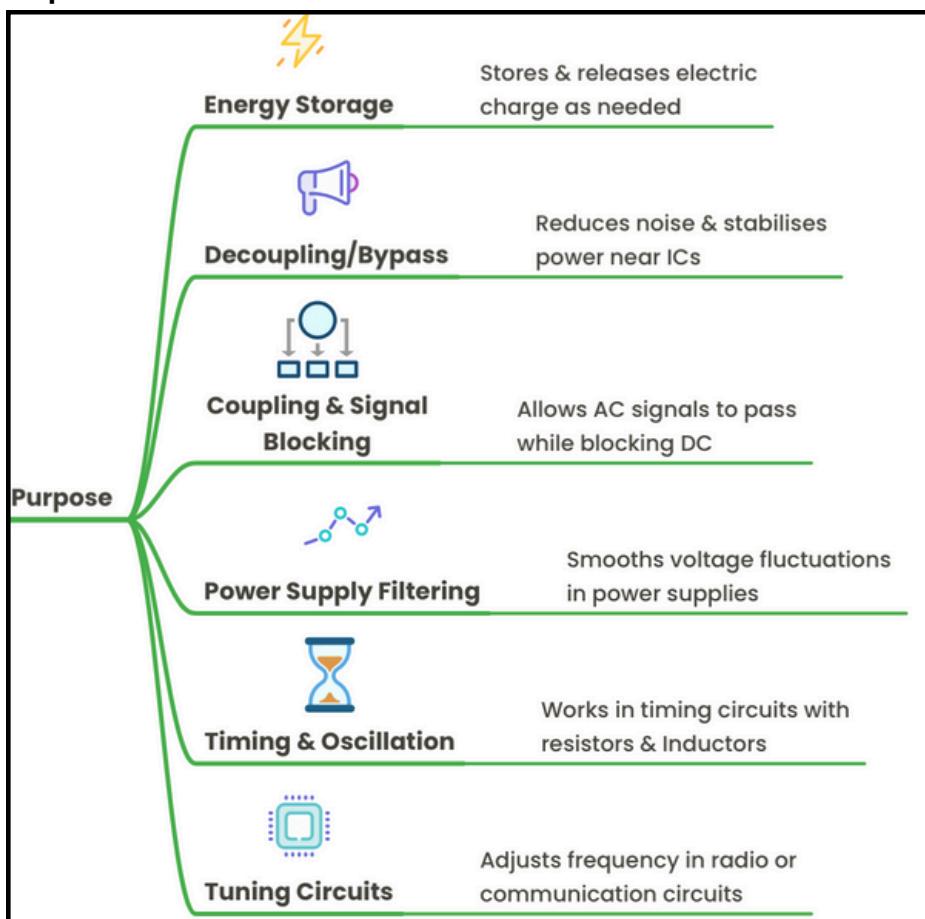
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CAPACITOR

A capacitor is a passive electronic component that stores and releases electrical energy in the form of an electric field. It plays a crucial role in managing voltage, smoothing signals, filtering noise, and stabilizing power in circuits.

Purpose of Capacitor

Capacitors are versatile and are used for various functions, such as:



How it works?

A capacitor stores energy between two conductive plates separated by an insulating material called the dielectric. When a voltage is applied across the plates, an electric field builds up and charge accumulates.

The key relationship is: $Q=C\times V$

Capacitors oppose changes in voltage—a property that makes them ideal for filtering and stabilization.

TYPES OF CAPACITORS / TECHNOLOGIES

Type	Characteristics	Use Case
Ceramic Capacitor	Small, cheap, low ESR	Decoupling, general use
Electrolytic Capacitor	High capacitance, polarized	Power filtering
Tantalum Capacitor	Stable, compact, polarized	Space-constrained, low-ESR needs
Film Capacitor	High precision, reliable	Audio, high-frequency
Supercapacitor	Very high capacitance	Backup power, energy storage

Key Specifications

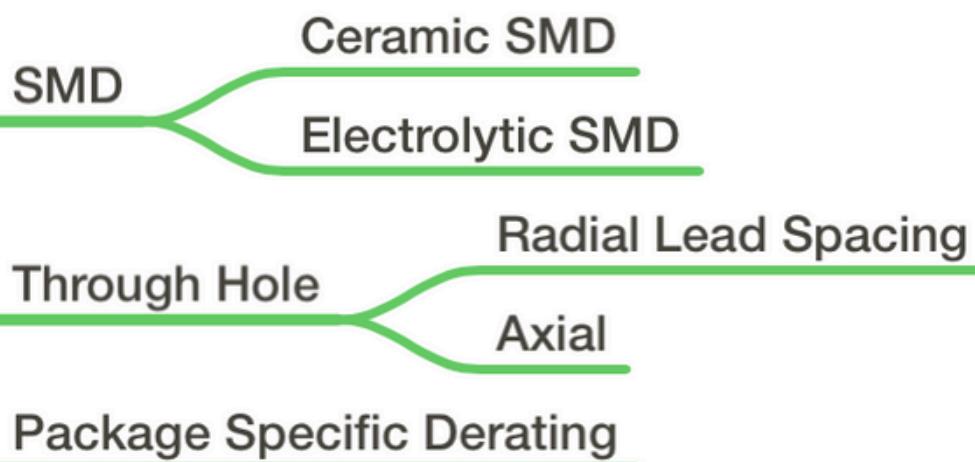
- 1. Capacitance (in Farads):** Indicates how much charge it can store. Common values: pF, nF, μ F
- 2. Voltage Rating (V):** Maximum voltage it can handle. Always choose at least $1.5 \times$ the operating voltage.
- 3. Type & Dielectric:** Choose based on frequency response, stability, and tolerance needs.
- 4. Tolerance:** Indicates variation from the nominal value (e.g., $\pm 10\%$, $\pm 20\%$).
- 5. ESR (Equivalent Series Resistance):** Important in power applications and high-speed switching circuits.

HOW TO CHOOSE A CAPACITOR?

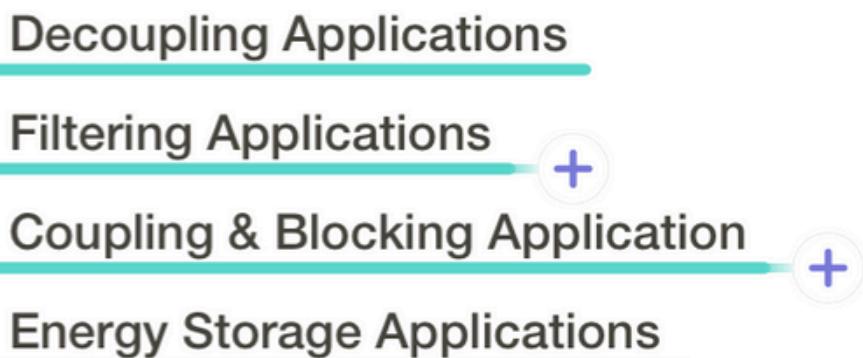
- How to Choose

1. Define the Application Purpose:
2. Determine Capacitance Value
3. Select Voltage Rating
4. Choose Dielectric Type
5. Check ESR and Ripple Current
6. Consider Physical Size and Mounting
7. Consider Temperature and Aging
8. Check Frequency Behavior

Packages



- Applications



HOW TO CHOOSE A CAPACITOR?

1. Define the Application Purpose:

Is the capacitor used for decoupling, filtering, energy storage, timing, coupling, or noise suppression?

2. Determine Capacitance Value

Common Calculations:

- **For Decoupling:** Use standard $0.01\mu F$ to $0.1\mu F$ near IC power pins.
- **For Power Filtering:** $C = \frac{I}{8 \times f \times V_{ripple}}$
- **For Timing (RC Circuits):** $t = R \times C \Rightarrow C = \frac{t}{R}$
- **For AC Coupling:** $C = \frac{1}{2\pi f_c R_{load}}$
- **Pro Tip:** Always select higher capacitance than minimum to allow for tolerances and derating.

3. Select Voltage Rating

- Choose a voltage rating at least $2\times$ your operating voltage for safety margin.
- For ceramic capacitors, account for DC bias derating (effective capacitance drops at higher applied voltages).

4. Choose Dielectric Type

- Choose a voltage rating at least $2\times$ your operating voltage for safety margin.
- For ceramic capacitors, account for DC bias derating (effective capacitance drops at higher applied voltages).
- NP0 (C0G) | X7R | Y5V/Z5U | Electrolytic | Tantalum | Film

HOW TO CHOOSE A CAPACITOR?

5. Check ESR and Ripple Current

- Low ESR is essential for switching regulators.
- Check manufacturer's ripple current rating to avoid overheating.
- **For Power Circuits:** Use ceramic or low-ESR electrolytic capacitors to minimize ripple voltage.

6. Consider Physical Size and Mounting

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Package Type	Use Case
SMD (MLCC)	Compact, automated assembly
Through-Hole	High current, mechanical stability
Supercapacitor	Large energy storage, low-voltage

7. Consider Temperature and Aging

- Check the temperature rating (usually -40°C to +125°C).
- Class II/III ceramics (X7R, Y5V) age over time (~1% per decade).
- Use NP0/ C0G for stability-critical circuits.

8. Check Frequency Behavior

- Self-Resonant Frequency (SRF): Above SRF, capacitor behaves inductively.
- For high-speed circuits (MHz+), use multiple parallel capacitors (0.1µF, 1µF, 10µF) to cover wide frequency ranges.

CERAMIC CAPACITORS

CLASS-I CERAMICS:

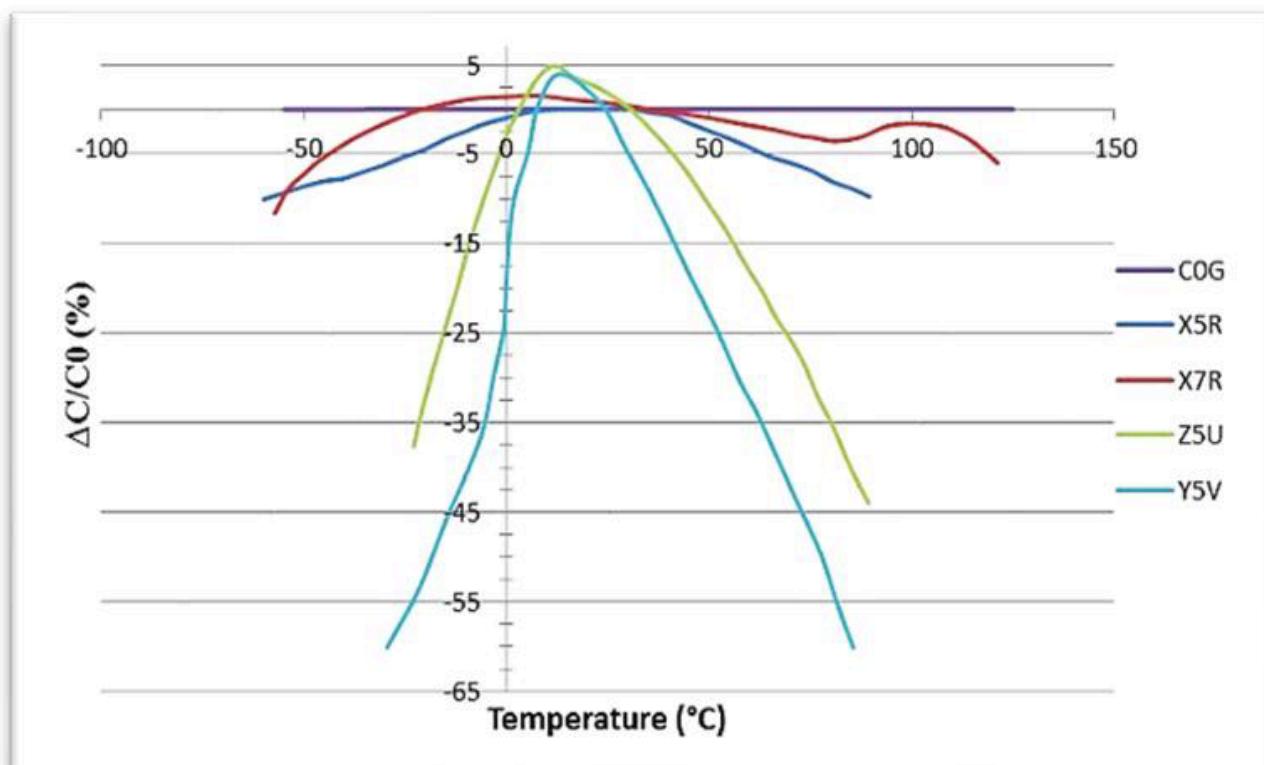
Type	Material	Voltage Range	Capacitance Range	Temperature Coefficient	Tolerance
C0G/NP0	Titanium Dioxide	16V – 3kV	1pF – 47nF	$\pm 30 \text{ ppm}/^\circ\text{C}$	$\pm 1\%$ to $\pm 5\%$
U2J	Neodymium Titanate	16V – 500V	1.5pF – 1nF	$\pm 120 \text{ ppm}/^\circ\text{C}$	$\pm 5\%$
P3K	Mixed Titanates	25V – 500V	2.2pF – 560pF	$\pm 250 \text{ ppm}/^\circ\text{C}$	$\pm 10\%$

C0G/NP0 Characteristics:

- Linear capacitance vs voltage
- Stable across temperature
- Excellent for timing circuits
- High Q factor (>1000)

Applications:

- Oscillator circuits
- Filter networks
- Sample and hold circuits
- RF coupling/bypass



CERAMIC CAPACITORS

CLASS-II CERAMICS:

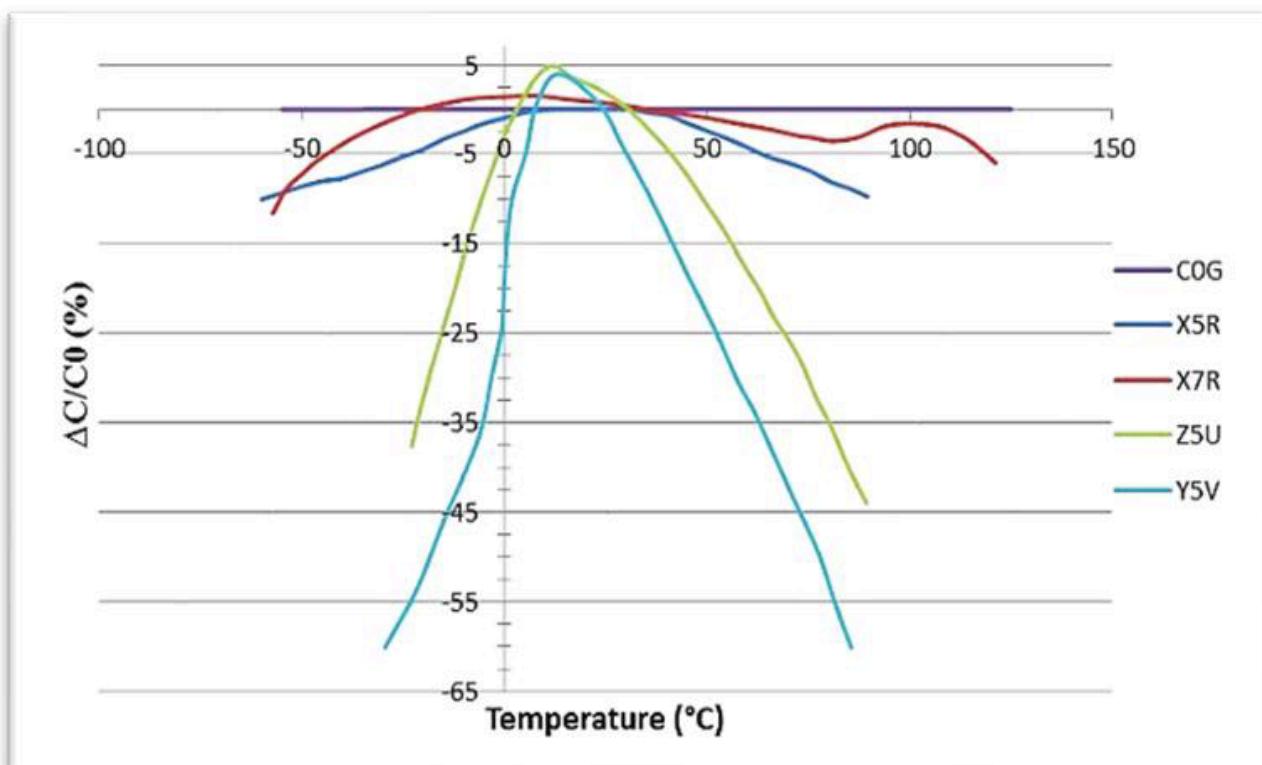
Type	Material	Voltage	Capacitance	Temperature	DC Bias Effect
X7R	Barium	6.3V – 2kV	100pF – 100μF	±15% (-55°C to +125°C)	-15% to -56%
X5R	BaTiO ₃	4V – 50V	100pF – 47μF	±15% (-55°C to +85°C)	-10% to -40%
Y5V	High-K Material	6.3V – 50V	1nF – 10μF	+22/-82% (-30°C to +85°C)	-20% to -80%

X7R Performance:

- Capacitance loss at rated voltage: 15–35%
- Aging rate: 2.5%/time decade
- Dissipation factor: 2.5% max
- Insulation resistance: >10GΩ or 100GΩ-μF

Voltage Coefficient:

- 0805 10μF 6.3V: -56% at rated voltage
- 0603 1μF 16V: -35% at rated voltage
- 1206 22μF 6.3V: -65% at rated voltage



ELECTROLYTIC CAPACITORS

Aluminum Electrolytic

Series	Electrolyte	Voltage	Capacitance	ESR @ 100kHz	Ripple Current
Standard	Liquid	6.3V – 450V	1µF – 47mF	0.01 – 10Ω	0.1 – 5A
Low ESR	Liquid	6.3V – 100V	10µF – 10mF	0.003 – 0.5Ω	1 – 10A
Polymer	Solid	2.5V – 35V	2.2µF – 1.5mF	0.003 – 0.1Ω	2 – 15A

Aluminum Construction:

- Anode:** Etched aluminum foil
- Dielectric:** Aluminum oxide (Al_2O_3)
- Cathode:** Electrolyte + aluminum foil
- Separator:** Paper spacer



Performance Characteristics:

- Capacitance tolerance:** $\pm 20\%$ standard
- Leakage current:** 0.01CV or $3\mu\text{A}$ (whichever greater)
- Operating temperature:** -40°C to $+105^\circ\text{C}$
- Life expectancy:** 2000–10000 hours @ 85°C

Failure Mechanisms:

- Electrolyte evaporation (main failure mode)
- Seal degradation
- Corrosion of terminals
- Oxide layer breakdown



ELECTROLYTIC CAPACITORS

Tantalum Electrolytic

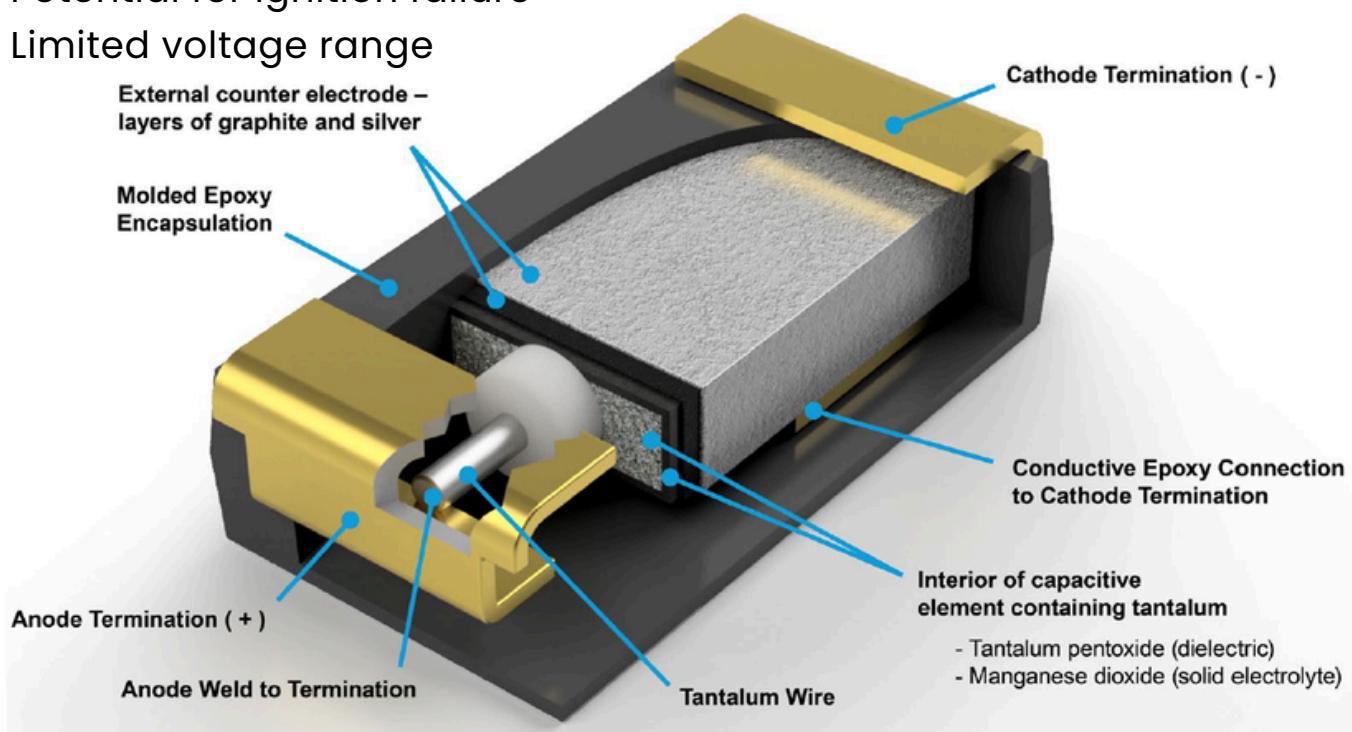
Type	Construction	Voltage	Capacitance	ESR @ 100kHz	Failure Rate
Solid MnO₂	Sintered	2.5V – 50V	0.1µF – 1mF	0.01 – 1Ω	0.1 – 1% per 1000 hours
Polymer	Sintered	2.5V – 35V	1µF – 1.5mF	0.005 – 0.5Ω	0.01 – 0.1% per 1000 hours
Wet Slug	Foil	6V – 125V	1µF – 22mF	0.1 – 50Ω	0.001% per 1000 hours

Tantalum Advantages:

- Stable capacitance vs temperature
- Low leakage current
- High capacitance density
- No electrolyte evaporation (solid)

Tantalum Disadvantages:

- Sensitivity to voltage transients
- Higher cost than aluminum
- Potential for ignition failure
- Limited voltage range



FILM CAPACITORS

PolyPropylene (PP)

Parameter	Value	Units	Notes
Dielectric Constant	22	-	Measured at 1kHz, 20°C
Loss Factor	2	-	Measured at 1kHz, 20°C
Breakdown Voltage	650	V/ μ m	DC
Temperature Coefficient	-200	ppm/°C	Negative coefficient
Moisture Absorption	<0.02	%	ASTM D570 Standard

PP Applications:

- Snubber circuits
- High-frequency switching
- Audio crossovers



Polyester (PET)

Parameter	Value	Units	Notes
Dielectric Constant	33	-	Measured at 1kHz, 20°C
Loss Factor	5	-	Measured at 1kHz, 20°C
Breakdown Voltage	580	V/ μ m	DC
Temperature Coefficient	400	ppm/°C	Positive coefficient
Moisture Absorption	4	%	ASTM D570 Standard

PET Characteristics:

- Higher dielectric constant than PP
- Better temperature stability than ceramic Class II
- Good mechanical properties
- Cost effective for general purpose



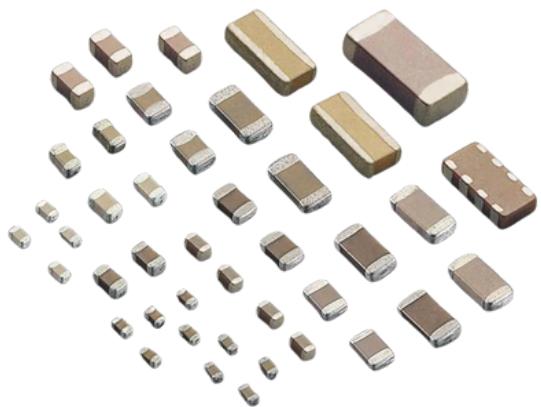
SMD PACKAGES

CERAMIC SMD PACKAGES

Package	Dimensions (L×W×H)	Voltage	Capacitance	Power Rating
1005	0.4 × 0.2 × 0.2 mm	4V	100nF	1/32W
201	0.6 × 0.3 × 0.3 mm	25V	220nF	1/20W
402	1.0 × 0.5 × 0.5 mm	50V	1µF	1/16W
603	1.6 × 0.8 × 0.8 mm	100V	10µF	1/10W
805	2.0 × 1.25 × 1.25 mm	200V	47µF	1/8W
1206	3.2 × 1.6 × 1.6 mm	500V	100µF	1/4W
1210	3.2 × 2.5 × 2.5 mm	500V	220µF	1/2W

Package Selection Criteria:

- Voltage rating vs dielectric thickness
- Capacitance achievable vs volume
- ESL vs package size (smaller = lower ESL)
- Mechanical stress vs size
- Cost vs performance requirements



ELECTROLYTIC SMD

Package	(D × H) [mm]	Voltage	Capacitance	ESR (Min)
Size A	3.2 × 1.6	50V	10µF	4Ω
Size B	3.2 × 2.8	50V	22µF	2Ω
Size C	6.3 × 5.8	50V	470µF	0.3Ω
Size D	7.7 × 4.3	35V	1000µF	0.15Ω



THROUGH-HOLE PACKAGES

RADIAL LEAD SPACING

Lead Spacing	Capacitance	Voltage	Applications
2.5mm	1pF – 100nF	50V – 1kV	Signal Coupling
5.0mm	100nF – 10µF	16V – 450V	Power Filtering
7.5mm	1µF – 100µF	16V – 400V	Bulk Storage
10.0mm	10µF – 47mF	16V – 450V	Power Supplies



Axial Vs. Radial Packages

Axial Advantages:

- Lower inductance
- Better for high frequency
- Easier automated insertion
- Better heat dissipation

Radial Advantages:

- Higher capacitance density
- Lower board area
- Standard footprints
- Cost effective



PACKAGE-SPECIFIC DERATING

Temperature Derating by Package

Package Size	Thermal Resistance	Power Rating	Power Derating Factor
402	300°C/W	0.063W	1.6 mW/°C
603	200°C/W	0.1W	2.0 mW/°C
805	160°C/W	0.125W	2.5 mW/°C
1206	120°C/W	0.25W	4.2 mW/°C

Voltage Derating Guidelines

Ceramic Capacitors:

- Class I (C0G): No derating required
- Class II (X7R): 50% derating recommended
- Class II (Y5V): 75% derating recommended

Electrolytic Capacitors:

- Aluminum: 80% voltage derating
- Tantalum: 50% voltage derating
- Polymer: 90% voltage derating

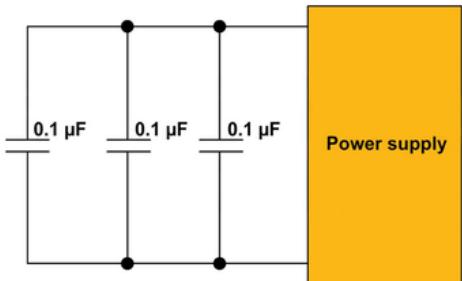
DECOUPLING APPLICATIONS

Power Supply Decoupling Strategy

Function	Capacitor	Range	Placement	ESR
Bulk	Aluminum Electrolytic	100 – 1000 μ F	PSU Output	< 0.1 Ω
Intermediate	Ceramic X7R	1 – 47 μ F	Per IC Group	<0.01 Ω
Local	Ceramic COG/X7R	10 – 100nF	Per Pin	<0.001 Ω

Ceramic Capacitors:

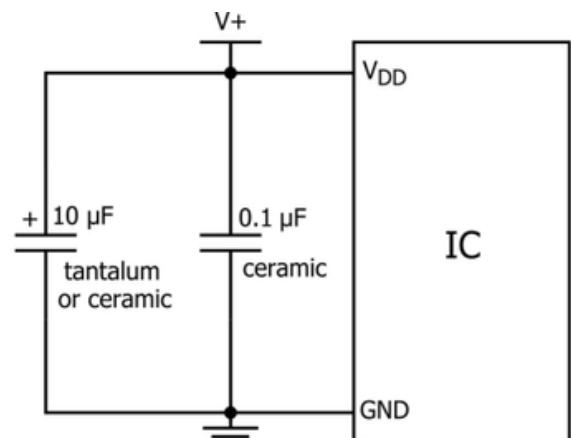
- Multiple capacitor values for frequency coverage
- 10:1 to 100:1 ratio between adjacent values
- Minimum three capacitor network recommended
- Consider impedance vs frequency response



Digital IC Decoupling

Microprocessor Decoupling:

- Core supply: 10 μ F + 100nF per supply pin
- I/O supply: 1 μ F + 10nF per supply pin
- PLL supply: 1 μ F + 100nF + 10nF
- Analog supply: 10 μ F + 1 μ F + 100nF + 10nF



FPGA Decoupling Network:

- VCC: 470 μ F bulk + 10 μ F per bank + 100nF per pin
- VCCINT: 220 μ F bulk + 47 μ F intermediate + 100nF local
- VCCIO: 100 μ F bulk + 10 μ F per bank + 100nF per pin
- VCCAUX: 47 μ F bulk + 1 μ F + 100nF + 10nF

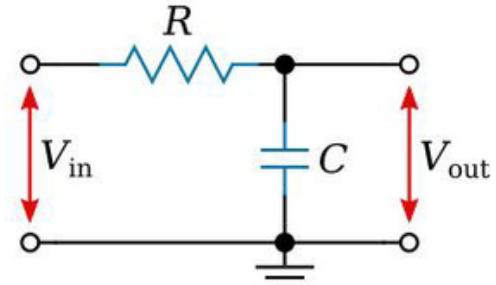
FILTERING APPLICATIONS

RC Low-Pass Filters

Cutoff Frequency	R Value	C Value	Application
1 Hz	1.6 MΩ	100 nF	DC Measurement
10 Hz	160 kΩ	100 nF	Sensor Filtering
100 Hz	16 kΩ	100 nF	Audio Filtering
1 kHz	1.6 kΩ	100 nF	Anti-Aliasing
10 kHz	160 Ω	100 nF	Switching Noise

Filter Design Considerations:

- Source impedance affects frequency response
- Capacitor tolerance impacts cutoff accuracy
- Temperature coefficient affects stability
- Leakage current creates DC offset



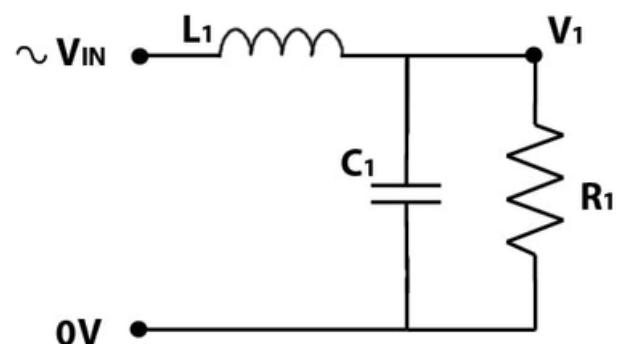
LC Filters

Pi-Filter Configuration:

- Input capacitor: 10–100µF electrolytic
- Inductor: 10–100µH ferrite core
- Output capacitor: 10–100µF electrolytic
- Ripple attenuation: 40–60dB

T-Filter Configuration:

- Series inductors: $L_1 = L_2 = L/2$
- Shunt capacitor: C
- Better common-mode rejection
- Higher component count



COUPLING & BLOCKING APPLICATIONS

AC Coupling

Audio Coupling:

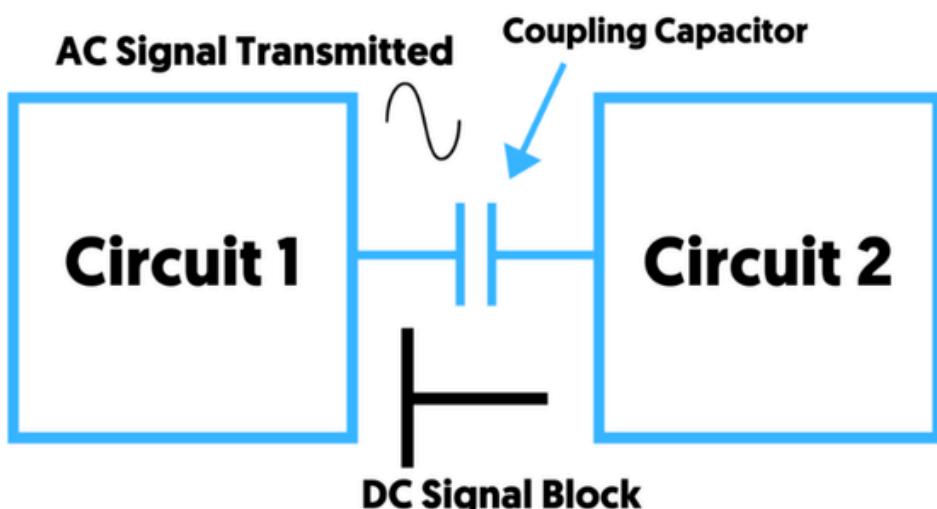
- Frequency response: 20Hz-20kHz
- Coupling capacitor: 1-10 μ F film
- Input impedance consideration
- DC blocking requirement

RF Coupling:

- Frequency range: 1MHz-6GHz
- Coupling capacitor: 1-100nF ceramic
- Low ESL requirement
- Temperature stability

DC Blocking

Application	Frequency	Capacitor Type	Capacitance
Audio Amplifier	20 Hz – 20 kHz	Film / Electrolytic	1 – 47 μ F
RF Amplifier	1 MHz – 1 GHz	Ceramic COG	1 – 100 nF
Video Amplifier	DC – 10 MHz	Ceramic X7R	100 nF – 1 μ F
Digital Logic	1 kHz – 100 MHz	Ceramic X7R	10 – 100 nF



ENERGY STORAGE APPLICATIONS

Flash Photography

Requirements:

- Energy: 1-10 Joules
- Voltage: 300-400V
- Discharge time: 1-10ms
- Capacitor type: Film or electrolytic

Calculation Example:

- Energy = $\frac{1}{2}CV^2$
- For 5J at 350V: $C = 2E/(V^2) = 81\mu F$
- Film capacitor preferred for low ESR

Backup Power

Requirements:

- Hold-up time: 10ms-10s
- Voltage droop: <10%
- Capacitor type: Supercapacitor or electrolytic

Design Considerations:

- ESR limits discharge current
- Leakage current affects hold-up time
- Temperature affects capacitance
- Voltage rating must exceed peak voltage



CERAMIC CAPACITOR FAILURE

MECHANICAL STRESS FAILURES

Flex Cracking:

- Cause: PCB flexing during handling/operation
- Failure mode: Hairline cracks in ceramic
- Prevention: Proper PCB design, keep-out zones
- Detection: Insulation resistance measurement

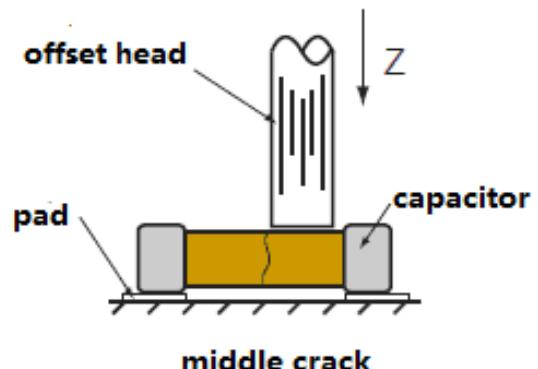
Thermal Shock Failures:

- Temperature cycling: -55°C to $+125^{\circ}\text{C}$
- Coefficient of expansion mismatch
- Solder joint stress
- Package size dependency

Prevention Methods:

- Flexible terminations
- Smaller package size
- Proper PCB thickness
- Controlled heating profiles

Pick-and-place head offset causes breakage



ELECTRICAL OVERSTRESS

Voltage Breakdown:

- Mechanism: Dielectric breakdown
- Typical voltage: 2-3× rated voltage
- Failure mode: Short circuit
- Recovery: Usually not recoverable

Surge Current Damage:

- Mechanism: I^2R heating of terminations
- Critical current: >1A for 0603 package
- Failure mode: Open circuit
- Prevention: Current limiting

FILM CAPACITOR FAILURE

METALLIZATION MIGRATION

Self-Healing Mechanism:

- Localized breakdown creates arc
- Metal evaporates around fault
- Capacitance loss: <1% per event
- Cumulative effect over time

Degradation Factors:

- Applied voltage stress
- Temperature elevation
- Humidity exposure
- AC voltage frequency

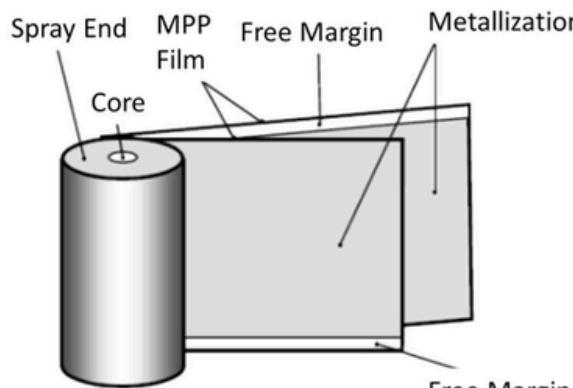
DIELECTRIC ABSORPTION

Mechanism:

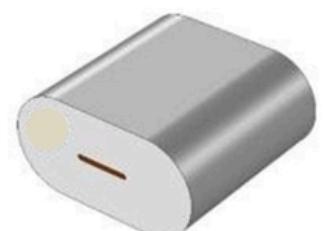
- Dielectric polarization effects
- Time-dependent recovery
- Affects precision applications
- Material dependent property

Typical Values:

- Polypropylene: 0.02%
- Polyester: 0.2%
- Polycarbonate: 0.1%
- Polystyrene: 0.01%



Cylindrical Winding



Flattened winding

EQUIVALENT SERIES RESISTANCE (ESR)

ESR SOURCES AND MECHANISMS

Dielectric Losses:

- Dielectric loss factor ($\tan \delta$)
- Frequency dependent
- Temperature dependent
- Material specific property

Conductor Losses:

- Electrode resistance
- Termination resistance
- Lead resistance
- Skin effect at high frequency

ESR Frequency Dependence:

- Low frequency: Dominated by dielectric losses
- High frequency: Dominated by conductor losses
- Transition frequency: Material and construction dependent

ESR BY CAPACITOR TYPE

Capacitor Type	Capacitance	ESR @ 100kHz	ESR @ 1MHz	ESR @ 10MHz
Ceramic COG	1 nF	0.1 Ω	0.05 Ω	0.02 Ω
Ceramic X7R	1 μF	0.01 Ω	0.005 Ω	0.002 Ω
Aluminum	100 μF	0.1 Ω	0.2 Ω	0.5 Ω
Tantalum	10 μF	0.05 Ω	0.08 Ω	0.15 Ω
Film PP	1 μF	0.002 Ω	0.001 Ω	0.0005 Ω

ESR Impact on Applications:

- Power loss: $P = I^2 ESR$
- Voltage ripple: $V_r = I_r \times ESR$
- Self-heating: $\Delta T = P \times R_{th}$
- Efficiency reduction in switching circuits

EQUIVALENT SERIES RESISTANCE (ESR)

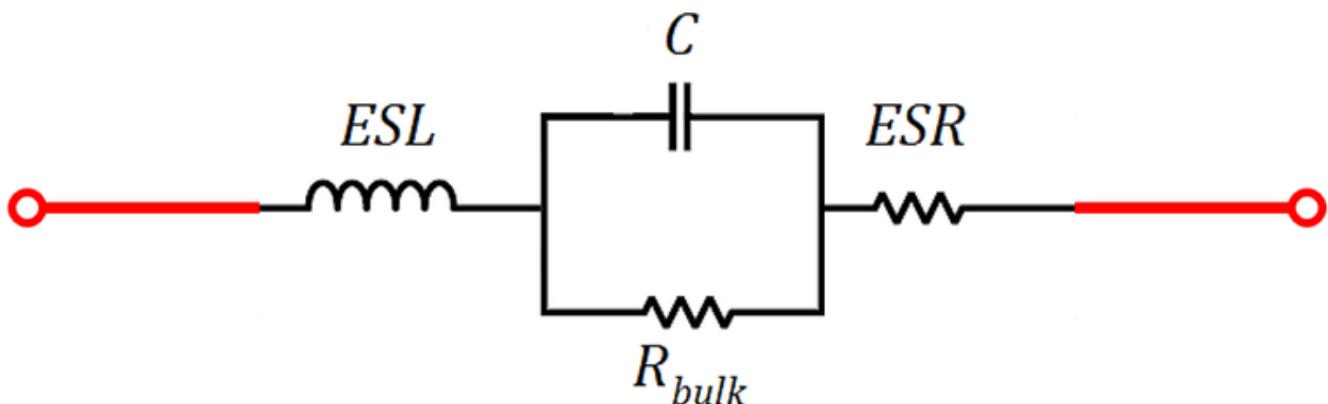
ESR MEASUREMENT TECHNIQUES

LCR Meter Method:

- Test signal: 1V RMS maximum
- Accuracy: $\pm 2\%$ typical
- Temperature: 25°C standard

Impedance Analyzer Method:

- Frequency range: 40Hz to 110MHz
- Dynamic range: 100dB
- Accuracy: $\pm 1\%$ impedance, $\pm 3^\circ$ phase
- Automated test capability



EQUIVALENT SERIES INDUCTANCE (ESL)

ESL SOURCES

Package Inductance:

- Lead length and geometry
- Package construction
- Termination design
- Via inductance in PCB



Typical ESL Values:

- 0402 ceramic: 0.5nH
- 0603 ceramic: 1.0nH
- 0805 ceramic: 1.5nH
- 1206 ceramic: 2.0nH
- Radial electrolytic: 5–15nH
- Axial electrolytic: 10–30nH

SELF-RESONANT FREQUENCY

Resonance Equation:

- $f_r = 1/(2\pi\sqrt{LC})$
- Below f_r : Capacitive behavior
- Above f_r : Inductive behavior
- Impedance minimum at f_r

Typical Self-Resonant Frequencies:

Capacitor Type	Capacitor Value	Package	Self-Resonant Frequency (SRF)
Ceramic	100 pF	603	500 MHz
Ceramic	1 nF	603	160 MHz
Ceramic	10 nF	603	50 MHz
Ceramic	100 nF	603	16 MHz
Ceramic	1 μ F	603	5 MHz

EQUIVALENT SERIES INDUCTANCE (ESL)

MULTIPLE RESONANCE EFFECTS

Anti-Resonance Phenomenon:

- Series combination of different value capacitors
- Impedance peak between individual SRFs
- Degrades decoupling effectiveness
- Mitigation: Proper value selection

Parallel Resonance:

- Multiple capacitors of similar value
- Resonance frequency splitting
- Better decoupling performance

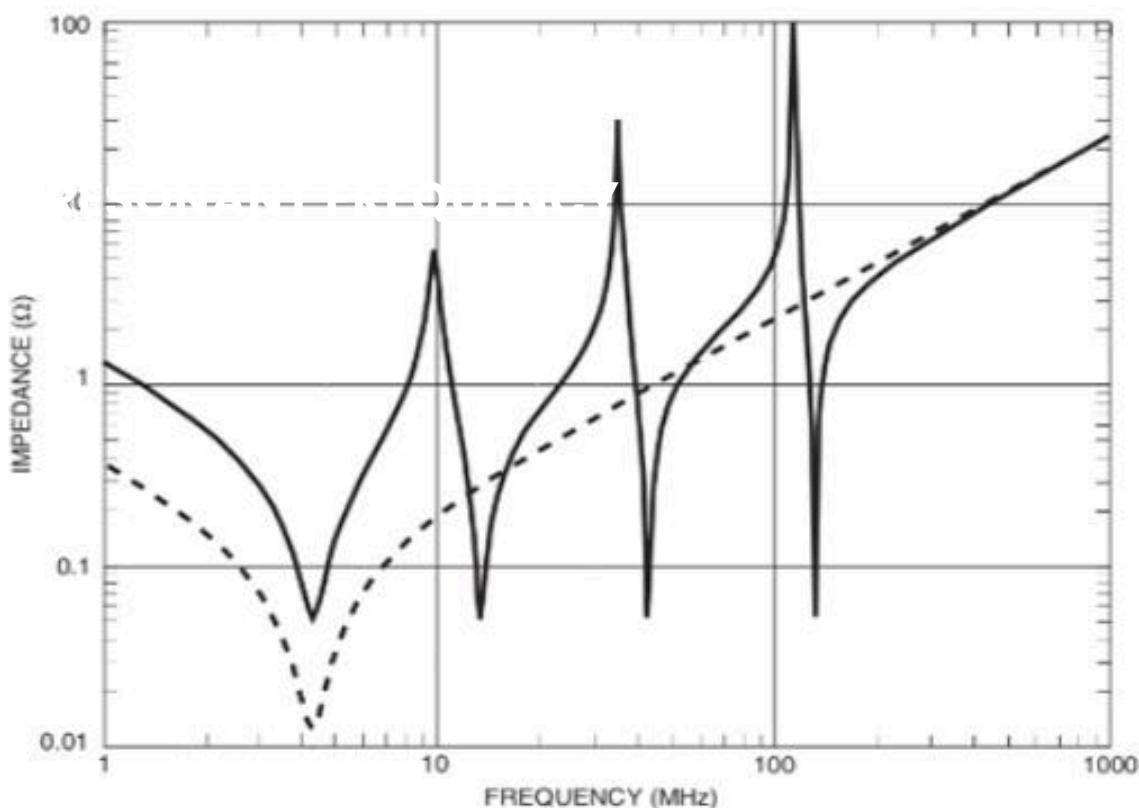


FIGURE 11-16. Impedance versus frequency for a decoupling network consisting of a 0.1, a 0.01, and a 0.001 μ F plus a 100-pF capacitor (solid line), and a network that consists of four 0.1- μ F capacitors (dashed line). For both networks, the capacitors are in series with 15 nH of inductance.

IMPEDANCE VS FREQUENCY BEHAVIOR

IMPEDANCE REGIONS

Capacitive Region ($f < f_r$):

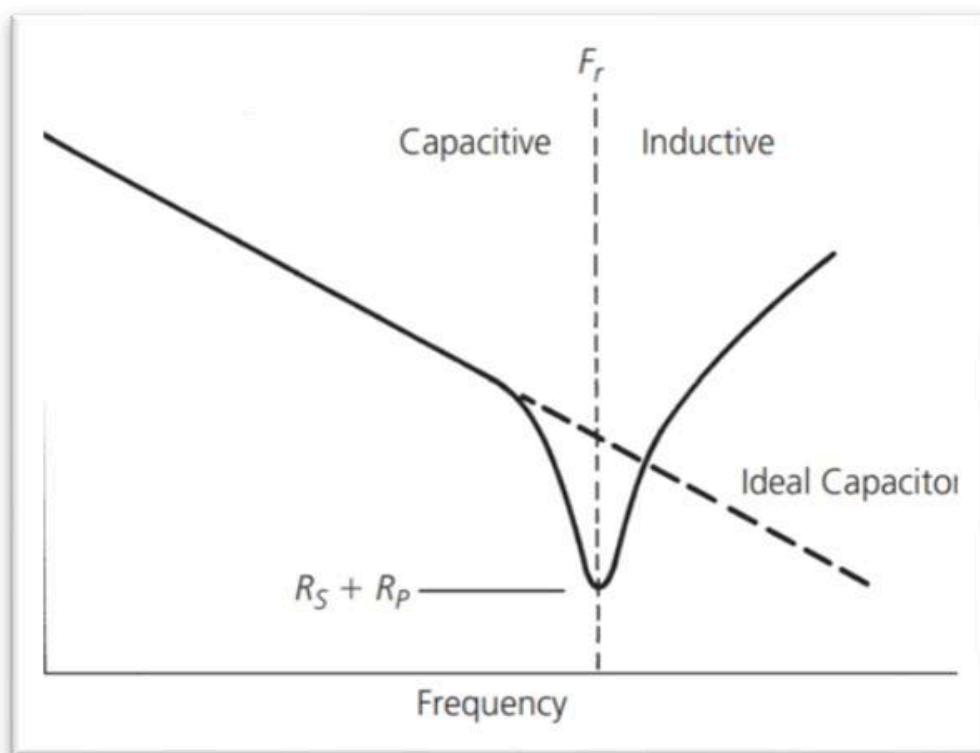
- $Z = \sqrt{(R^2 + (1/2\pi f C)^2)}$
- Dominated by capacitive reactance
- Impedance decreases with frequency
- Phase approaches -90°

Resistive Region ($f \approx f_r$):

- $Z \approx \text{ESR}$
- Minimum impedance point
- Phase approaches 0°
- Optimal decoupling frequency

Inductive Region ($f > f_r$):

- $Z = \sqrt{(R^2 + (2\pi f L)^2)}$
- Dominated by inductive reactance
- Impedance increases with frequency
- Phase approaches $+90^\circ$



IMPEDANCE VS FREQUENCY BEHAVIOR

TEMPERATURE EFFECTS ON IMPEDANCE

Ceramic Capacitors:

- C0G: Minimal temperature coefficient
- X7R: -15% to +15% over temperature
- Y5V: +22% to -82% over temperature

Electrolytic Capacitors:

- Capacitance: Decreases at low temperature
- ESR: Increases significantly at low temperature
- Useful life: Halves every 10°C increase

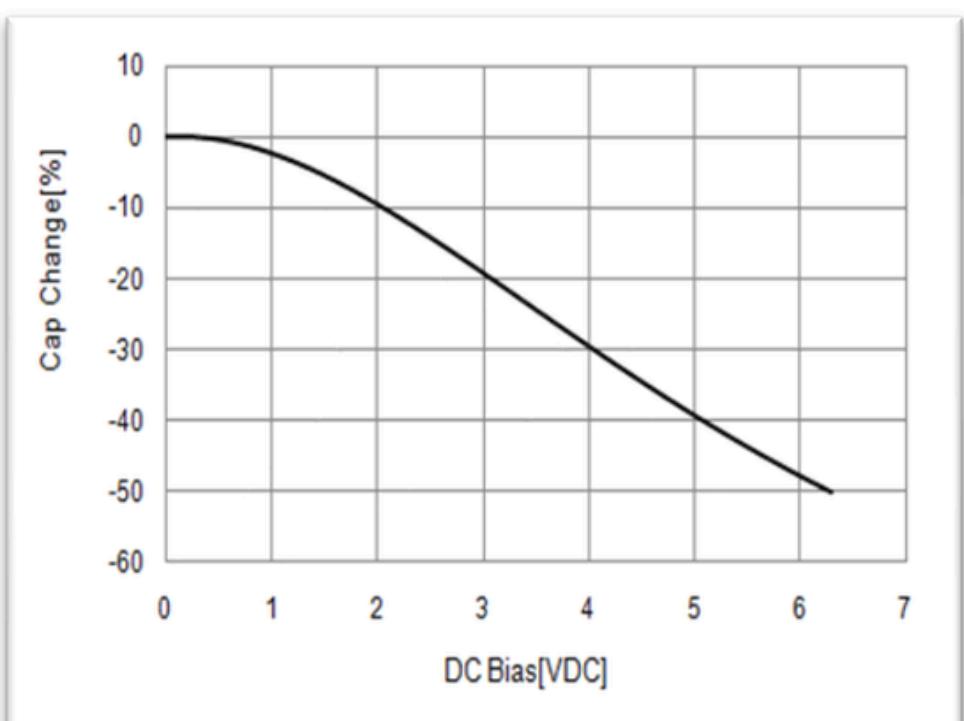
DC BIAS EFFECTS

Ceramic Class II Behavior:

- Capacitance loss with applied DC voltage
- Non-linear relationship
- Worse at higher dielectric constants

DC Bias Test Data (X7R 1µF 25V):

Applied Voltage	CAP (%)
0V	100%
5V	85%
10V	65%
15V	45%
20V	35%
25V	25%



PARASITIC EFFECTS IN CIRCUITS

PCB PARASITICS ON IMPEDANCE

Via Inductance:

- Typical value: 1-2nH per via
- Length dependent
- Diameter dependent
- Multiple vias reduce inductance

Trace Inductance:

- Microstrip: ~1nH/mm
- Stripline: ~0.8nH/mm
- Ground plane spacing dependent
- Width dependent

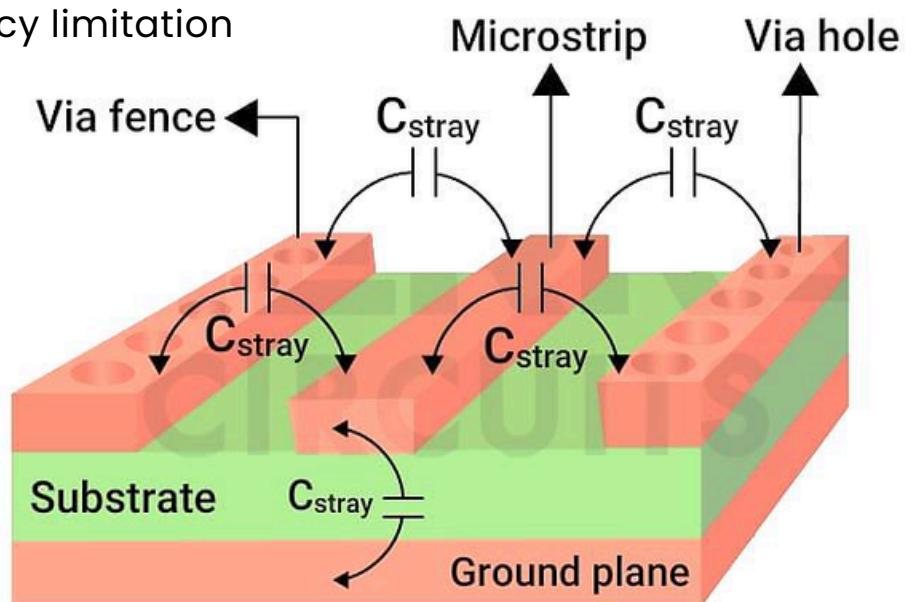
COMPONENT PARASITICS

Resistor Parasitic Capacitance:

- Chip resistors: 0.05-0.5pF
- Creates low-pass filter with capacitor
- Affects high-frequency response
- Layout dependent

DC Bias Test Data (X7R 1 μ F 25V):

- Winding capacitance: 1-50pF
- Self-resonant frequency limitation
- Q factor degradation
- Shielding effects

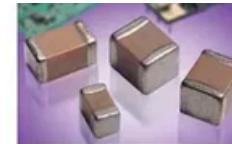


CAPACITOR SELECTION – DATASHEET INTERPRETATION

KEY SPECIFICATIONS

Electrical Parameters:

- Nominal capacitance and tolerance
- Rated voltage (DC and AC)
- Temperature coefficient/stability
- Dissipation factor/ESR
- Insulation resistance
- Self-resonant frequency



X7R fall into EIA Class II materials. X7R is the most popular of these intermediate dielectric constant materials. Its temperature variation of capacitance is within ±15% from -55°C to +125°C. This class covers the widest range of applications.

Capacitance for X7R varies under the influence of electrical operating conditions such as voltage and frequency.

X7R dielectric chip usage covers the broad spectrum of industrial applications where known changes in capacitance due to applied voltages are acceptable.

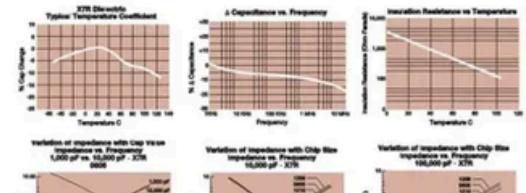


PART NUMBER (see page 2 for complete part number explanation)

0805	5	C	103	M	A	T	2	A
Size (L" x W")	Voltage	Dielectric	Capacitance	Capacitance	Failure	Termination	Packaging	Special
	4V = 4	X7R = C	Code (in pF):	Tolerance:	Rate:	2 x 1" Plated Ni and Sn	4.0 mm	Code A, M, Product
	10V = 2		103 = 100 pF	K = ±15%	Δ = 0.1%	ZIF FLEXITERMINI™		Content
	120V = Y		103 = 100 pF	M = ±20%				Factory For
	20V = 3							Multiples
	50V = 5							
	100V = 1							
	200V = 2							
	500V = 7							

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

Contact factory for non-specified capacitance values.



Environmental Ratings:

- Operating temperature range
- Humidity resistance
- Vibration/shock resistance
- Flammability rating

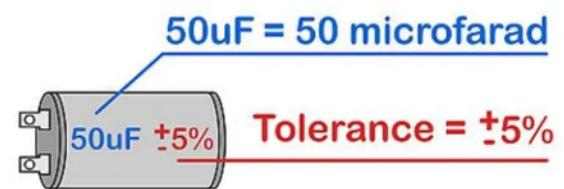
Physical Specifications:

- Package dimensions and tolerances
- Termination finish and solderability
- Marking and orientation
- Tape and reel specifications

UNDERSTANDING TOLERANCE SPECIFICATIONS

Capacitance Tolerance Codes:

- B: ±0.1pF ($C < 10\text{pF}$)
- C: ±0.25pF ($C < 10\text{pF}$)
- D: ±0.5pF ($C < 10\text{pF}$)
- F: ±1%
- G: ±2%
- H: ±3%
- J: ±5%
- K: ±10%
- M: ±20%
- Z: +80/-20% (Y5V)



$$+5\% \uparrow 50\mu\text{F} + (50\mu\text{F} \times 0.05) = 5.25 \mu\text{F}$$
$$-5\% \downarrow 50\mu\text{F} - (50\mu\text{F} \times 0.05) = 4.75 \mu\text{F}$$

Temperature Coefficient Codes:

- NP0/C0G: ±30ppm/°C
- X7R: ±15% (-55°C to +125°C)
- X5R: ±15% (-55°C to +85°C)
- Y5V: +22/-82% (-30°C to +85°C)

CAPACITOR SELECTION – DATASHEET INTERPRETATION

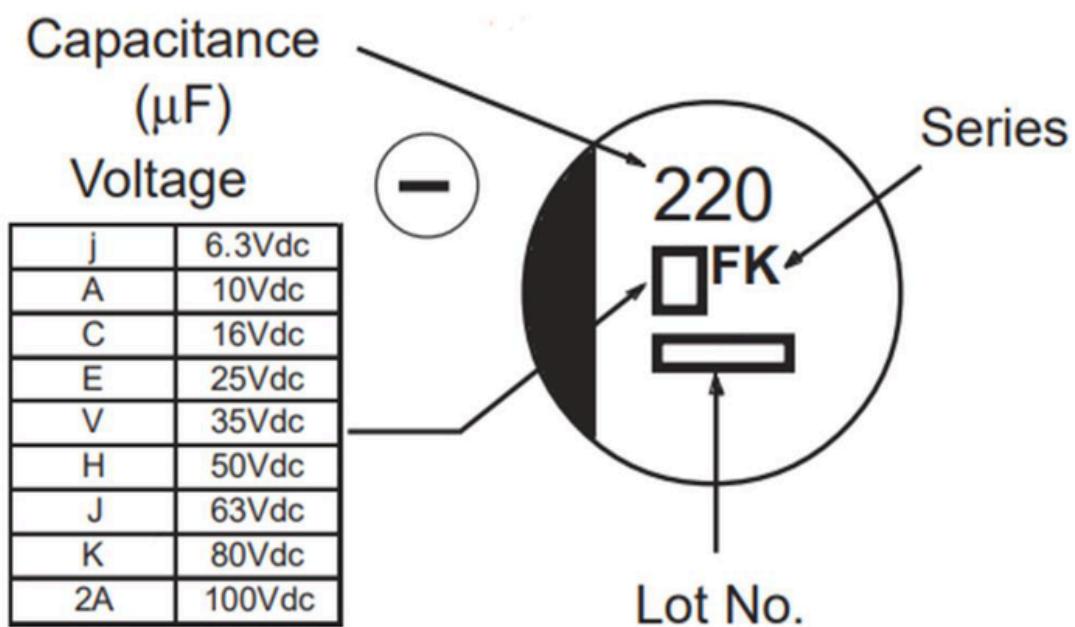
VOLTAGE RATING INTERPRETATION

DC Voltage Rating

- Maximum continuous DC voltage
- At maximum rated temperature
- Includes safety margin
- No derating for most ceramics

AC Voltage Rating:

- RMS voltage for AC applications
- Frequency dependent
- Self-heating limitations
- Power dissipation limits
- Short duration overvoltage capability
- Normally 1.5–2× DC rating
- Duration: microseconds to milliseconds
- Energy limited applications



CAPACITOR SELECTION – APPLICATION-SPECIFIC SELECTION CRITERIA

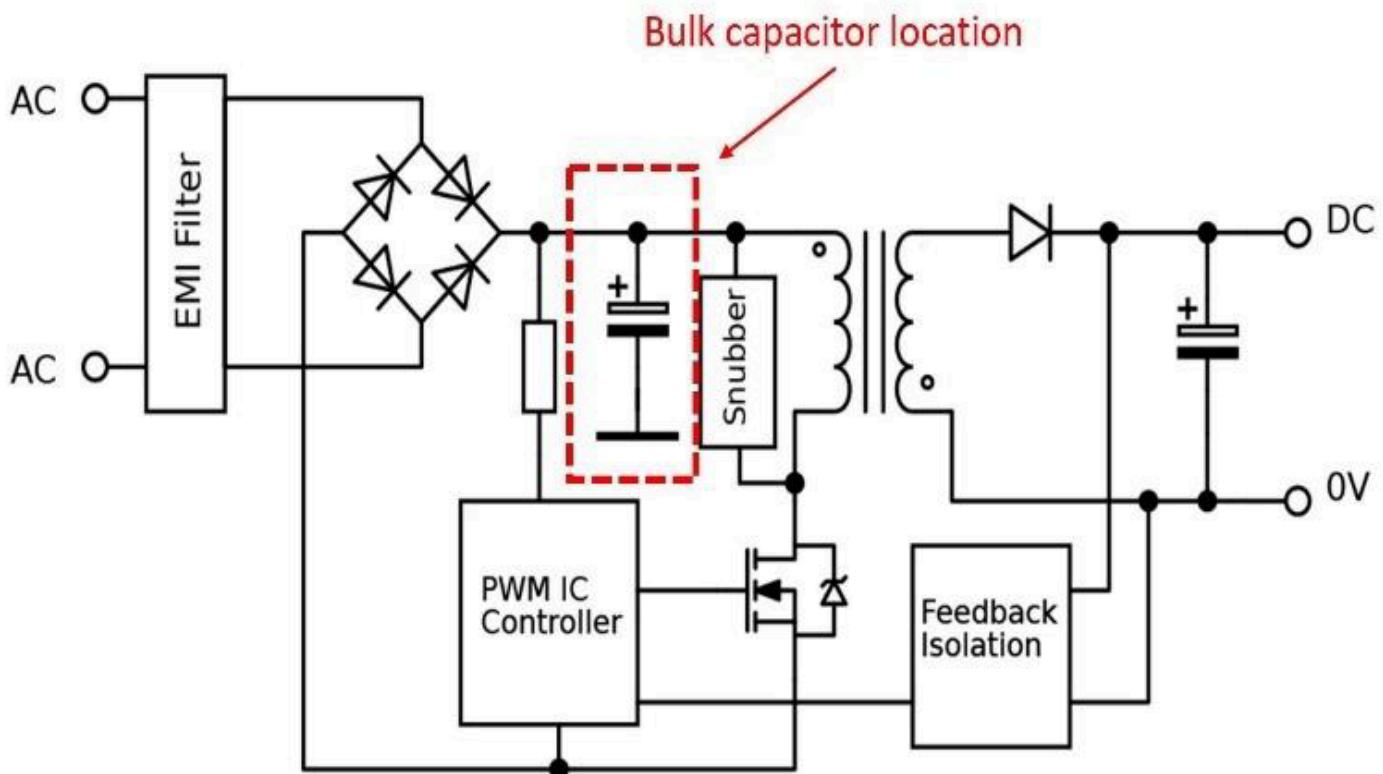
POWER SUPPLY APPLICATIONS

Bulk Capacitors:

- Primary requirement: High capacitance
- Secondary: Low ESR for ripple current
- Aluminum electrolytic preferred
- Ripple current rating critical

Selection Checklist:

- Capacitance: 2–5× calculated minimum
- Voltage rating: 25% derating minimum
- ESR: <50mΩ for switching supplies
- Ripple current: 2× calculated RMS
- Operating temperature: -40°C to +105°C



CAPACITOR SELECTION – APPLICATION-SPECIFIC SELECTION CRITERIA

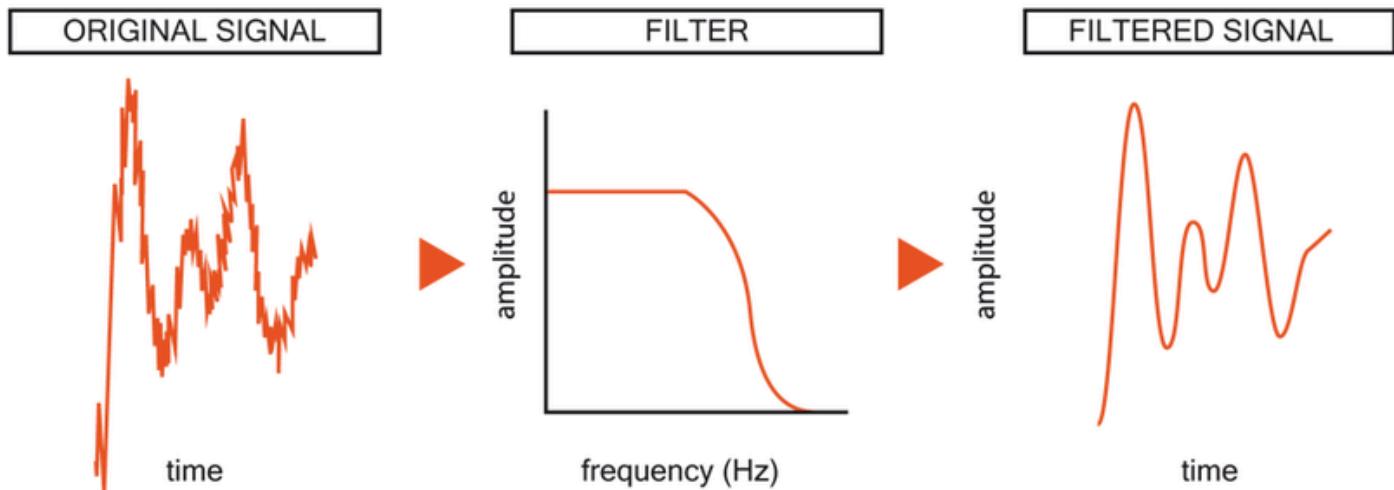
SIGNAL PROCESSING APPLICATIONS

Coupling Capacitors:

- Low distortion requirement
- Stable over temperature
- Low dielectric absorption
- Film capacitors preferred

Critical Parameters:

- Capacitance stability: $\pm 5\%$ max
- Temperature coefficient: $< 200 \text{ ppm}/^\circ \text{C}$
- Dielectric absorption: $< 0.1\%$
- Voltage coefficient: $< 100 \text{ ppm/V}$
- Frequency response: Flat to $100 \times$ signal frequency



CAPACITOR SELECTION – APPLICATION-SPECIFIC SELECTION CRITERIA

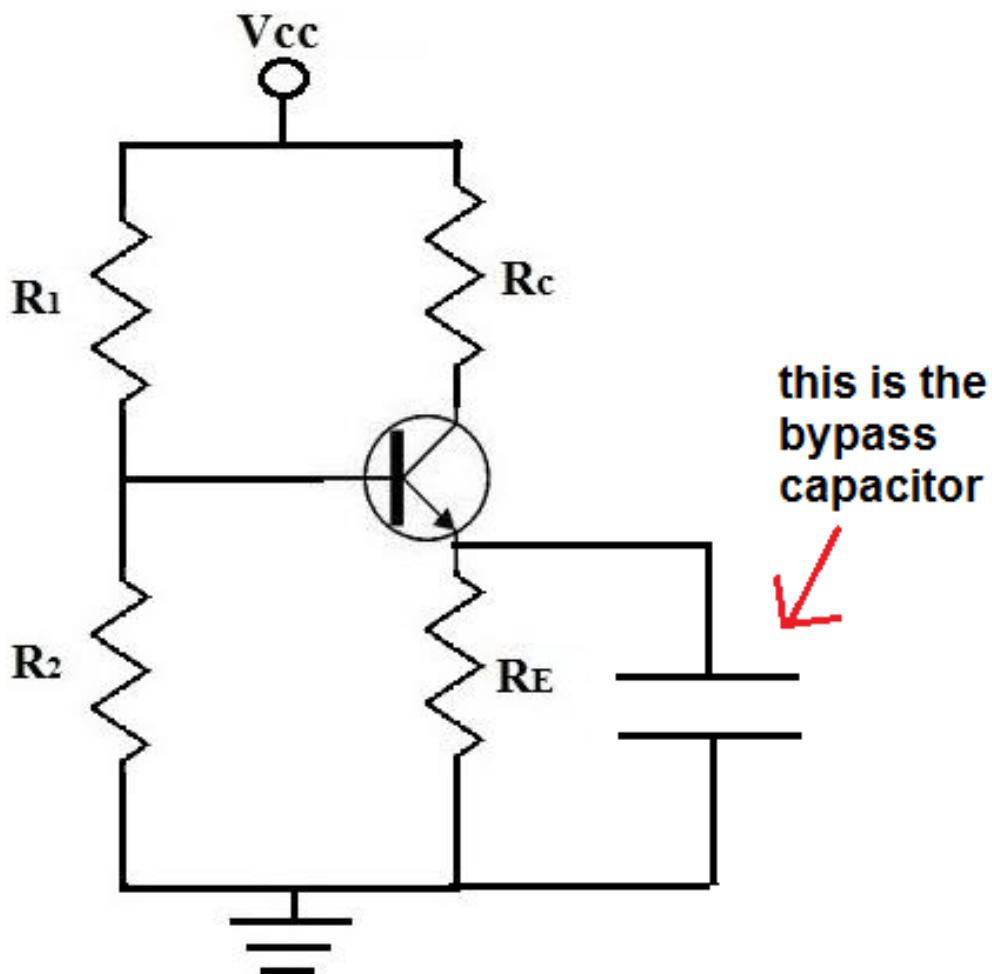
RF/MICROWAVE APPLICATIONS

Bypass Capacitors:

- Low ESL requirement
- Broadband impedance control
- Multiple values in parallel
- Ceramic C0G preferred

Design Requirements:

- ESL: <1nH for >100MHz applications
- Q factor: >200 @ 1MHz
- Temperature stability: $\pm 30\text{ppm}/^\circ\text{C}$
- Package size: Minimize for lower ESL



CAPACITOR IN POWER : POWER DISTRIBUTION NETWORK (PDN) DESIGN

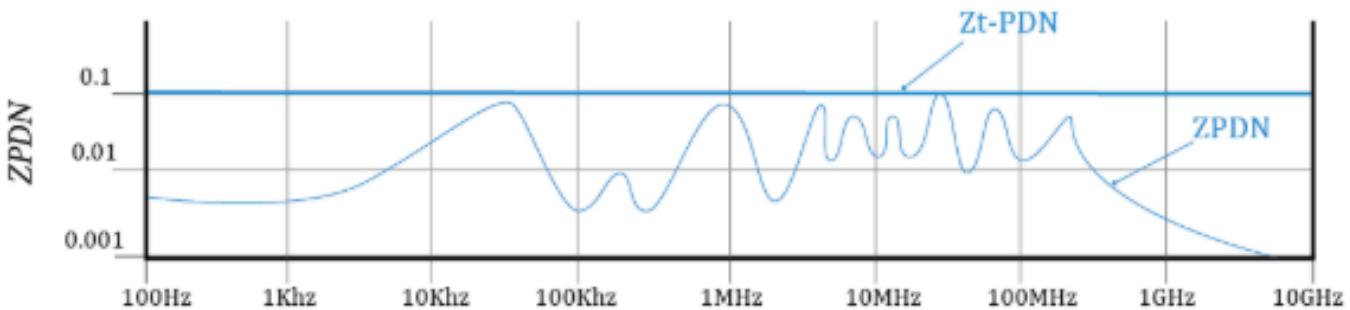
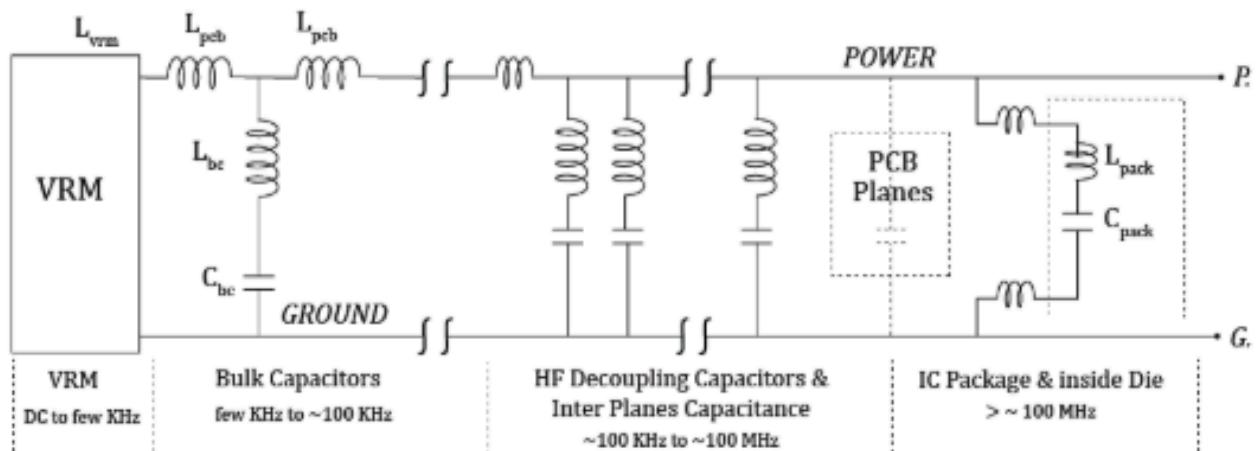
PDN IMPEDANCE REQUIREMENTS

Target Impedance Calculation:

- $Z_{target} = V_{ripple} / I_{transient}$
- Example: 5% ripple on 3.3V, 1A transient
- $Z_{target} = (0.05 \times 3.3V) / 1A = 165m\Omega$

Frequency-Dependent Requirements:

- DC to 1kHz: Bulk capacitors (electrolytic)
- 1kHz to 100kHz: Intermediate capacitors (ceramic)
- 100kHz to 10MHz: Local bypass capacitors
- 10MHz: PCB capacitance and design



CAPACITOR IN POWER : POWER DISTRIBUTION NETWORK (PDN) DESIGN

MULTI-STAGE FILTERING STRATEGY

Stage 1 – Bulk Filtering:

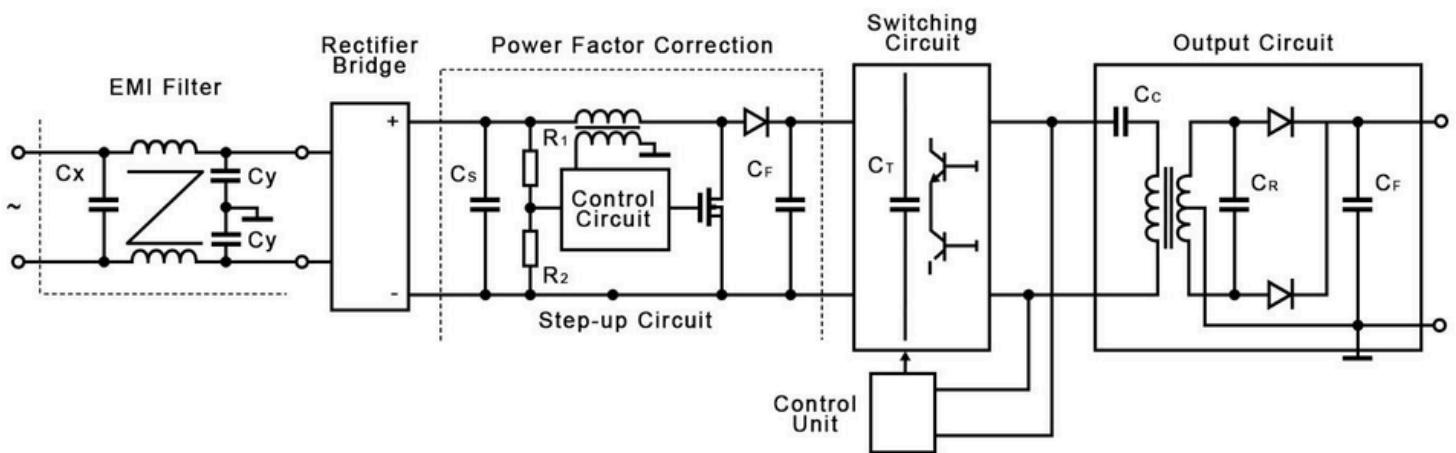
- Aluminum electrolytic: 100–1000 μ F
- Location: Power supply output
- Function: Energy storage, low-frequency filtering
- ESR target: <100m Ω

Stage 2 – Intermediate Filtering:

- Ceramic X7R: 1–47 μ F
- Location: Power distribution points
- Function: Medium frequency decoupling
- ESR target: <10m Ω

Stage 3 – Local Bypass:

- Ceramic C0G/X7R: 10–100nF
- Location: IC power pins
- Function: High-frequency bypass
- ESR target: <1m Ω



CAPACITOR IN POWER: SWITCHING POWER SUPPLY CAPACITOR DESIGN

INPUT FILTER DESIGN

Requirements:

- Input ripple current handling
- EMI filtering
- Holdup time during dropout
- Inrush current limiting

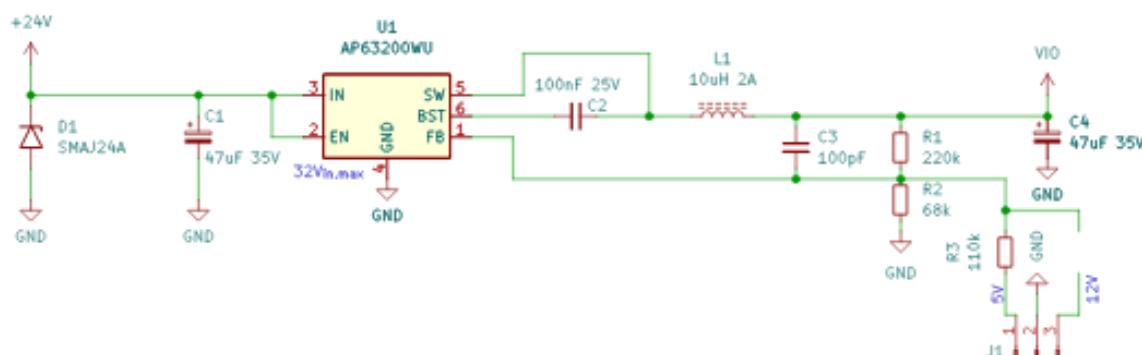
Capacitor Selection:

- Primary: Low ESR electrolytic
- Secondary: High-frequency ceramic
- Ripple current: $\sqrt{2} \times I_{out} \times D$
- Where D = duty cycle

Design Example – 12V to 3.3V, 5A Converter:

- Switching frequency: 500kHz
- Duty cycle: $3.3V/12V = 27.5\%$
- Input ripple current: $\sqrt{2} \times 5A \times 0.275 = 1.94A$ RMS
- Required capacitance: $220\mu F$ minimum
- ESR requirement: $< 25m\Omega$ for $< 100mV$ ripple

Selectable 12V / 5V / 3.3V supply



Jumper selectability:
No jumper: 3.3V
Jumper [1] & [2] = 5V
Jumper [2] & [3] = 12V

No possibility of bad jumpering

CAPACITOR IN POWER: SWITCHING POWER SUPPLY CAPACITOR DESIGN

OUTPUT FILTER DESIGN

Critical Parameters:

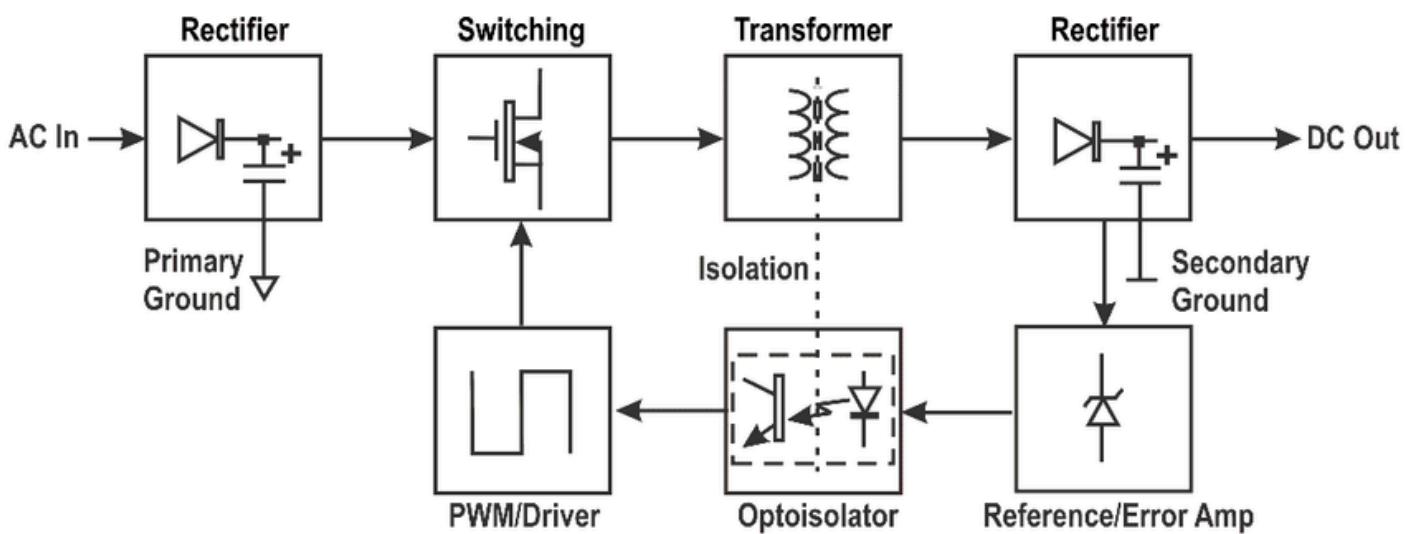
- Output voltage ripple
- Load transient response
- ESR contribution to ripple
- Capacitance contribution to ripple

Ripple Components:

- ESR ripple: $V_{r_esr} = I_r \times ESR$
- Capacitive ripple: $V_{r_cap} = I_r / (8 \times f \times C)$
- Total ripple: $\sqrt{(V_{r_esr}^2 + V_{r_cap}^2)}$

Optimization Strategy:

- Balance ESR and capacitance contributions
- Multiple parallel capacitors
- Different technologies for frequency coverage
- Minimize loop inductance



CAPACITOR IN POWER: LINEAR REGULATOR APPLICATIONS

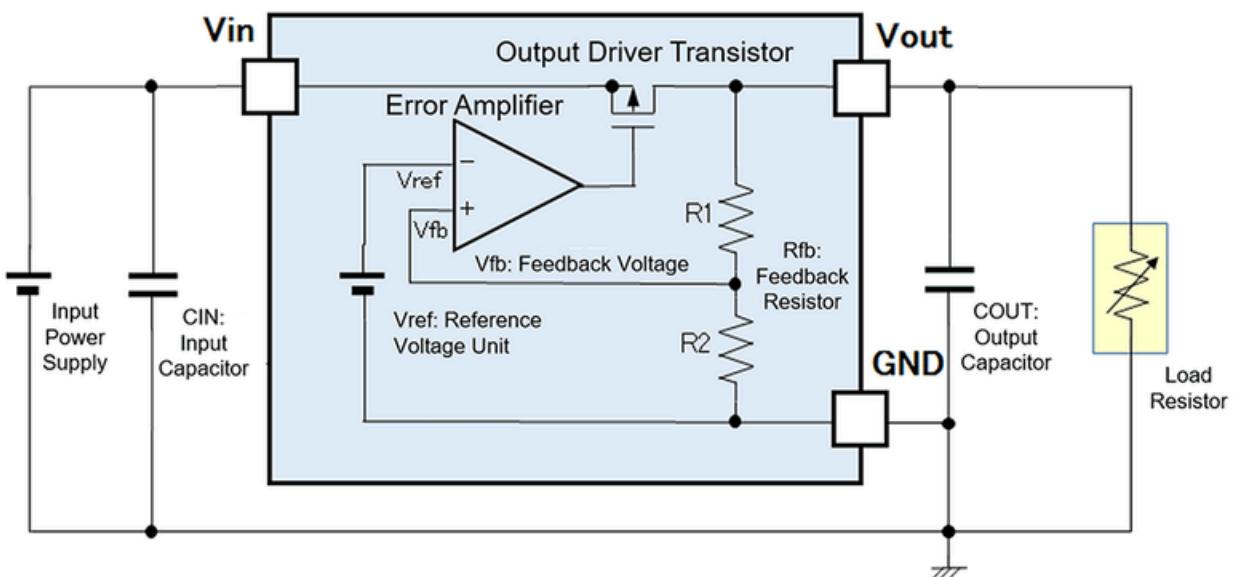
INPUT CAPACITORS

Function:

- Provide instantaneous current during load transients
- Reduce input impedance
- Improve PSRR at higher frequencies
- Prevent oscillation

Typical Requirements:

- LDO input: 1-10 μ F ceramic + 10-100 μ F electrolytic
- Switching pre-regulator: 100-1000 μ F electrolytic
- ESR: <100m Ω for stability
- Placement: <10mm from regulator input



CAPACITOR IN POWER: LINEAR REGULATOR APPLICATIONS

OUTPUT CAPACITORS

Stability Requirements:

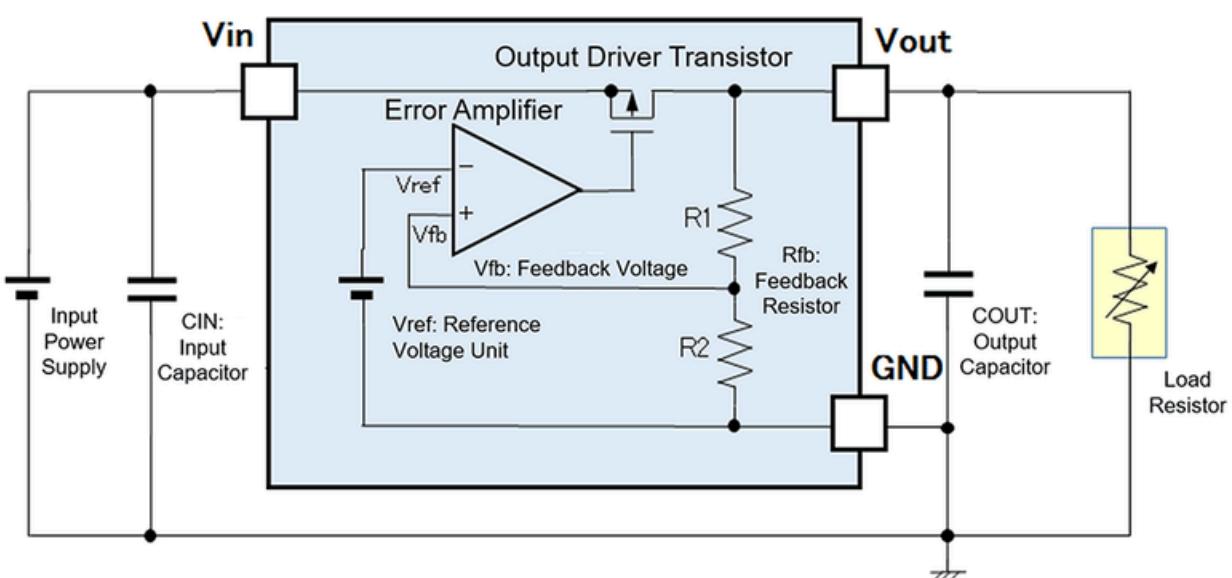
- Compensation for regulator loop
- ESR zero for phase margin
- Load transient response
- Output noise filtering

ESR Requirements for Stability:

- Most LDOs require minimum ESR
- Typical range: $10\text{m}\Omega$ to 1Ω
- Too low ESR can cause oscillation
- Series resistance may be added

Transient Response:

- $\Delta V_{\text{out}} = (\text{ESR} \times \Delta I_{\text{load}}) + (\Delta I_{\text{load}} \times \Delta t/C)$
- First term: Immediate response
- Second term: Capacitive charging
- Minimize both for best performance



CAPACITOR IN POWER : DIGITAL IC POWER DISTRIBUTION

MICROPROCESSOR POWER DESIGN

Multiple Supply Requirements:

- Core voltage: 0.8V-1.2V, high current
- I/O voltage: 1.8V-3.3V, moderate current
- PLL voltage: Clean, low noise
- Analog voltage: Ultra-low noise

Decoupling Strategy per Supply:

- Core: $470\mu F + 47\mu F + 10 \times 100nF + 10 \times 10nF$
- I/O: $100\mu F + 10\mu F + 4 \times 100nF + 4 \times 10nF$
- PLL: $47\mu F + 4.7\mu F + 470nF + 47nF + 4.7nF$
- Analog: $22\mu F + 2.2\mu F + 220nF + 22nF + 2.2nF$

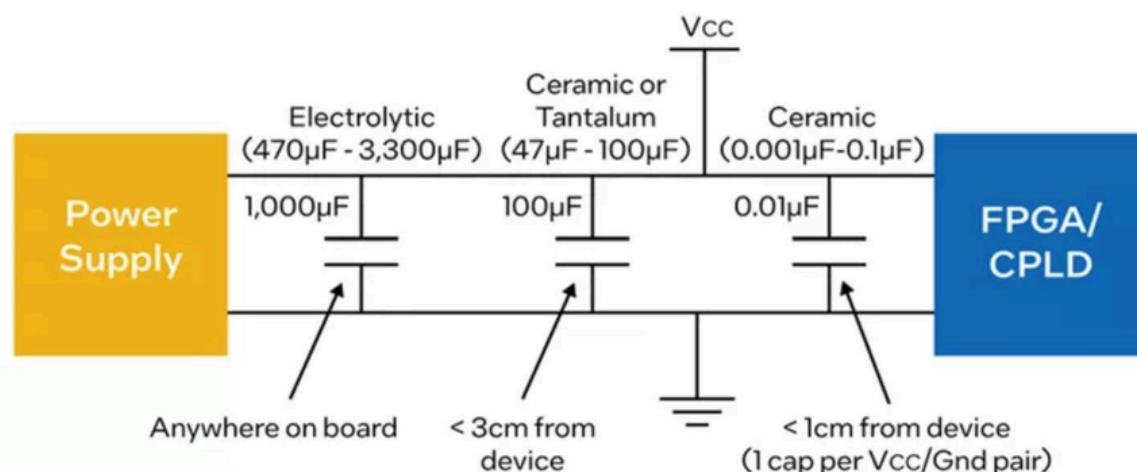
FPGA POWER DISTRIBUTION

Power Rail Classification:

- VCCINT: Core logic supply
- VCCIO: I/O bank supplies
- VCCAUX: Auxiliary circuits
- VCCO: Output driver supplies

Bank-Based Decoupling:

- Each I/O bank: $10\mu F + 1\mu F + 100nF$
- Core supply: $22\mu F$ per 100 logic elements
- PLL supplies: Separate LC filter + decoupling
- Configuration supply: $47\mu F + 4.7\mu F + 470nF$



CAPACITOR LAYOUT – PCB FUNDAMENTALS

PLACEMENT PRIORITY RULES

Priority 1 – Critical Bypass:

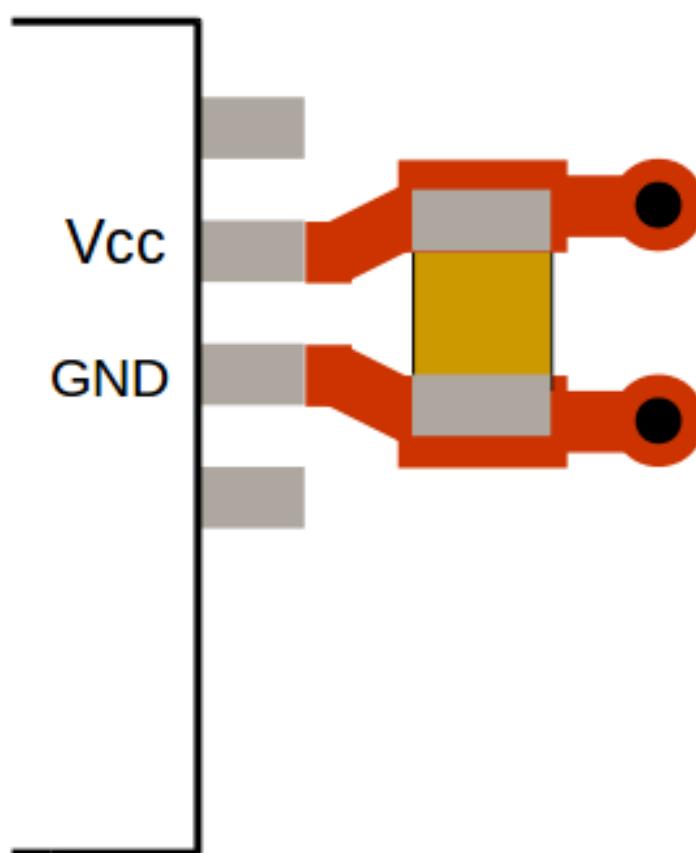
- CPU/FPGA power pins: <5mm trace length
- High-speed digital: <3mm trace length
- RF circuits: <1mm trace length
- Analog precision: Direct connection preferred

Priority 2 – Power Distribution:

- Switching regulator output: <10mm
- Linear regulator output: <15mm
- Power connector filtering: <20mm
- Bulk storage: <50mm acceptable

Priority 3 – Signal Conditioning:

- Coupling capacitors: Near signal source
- Filter capacitors: At circuit input
- Timing capacitors: Near oscillator
- Snubber capacitors: Across switching element



LOOP MINIMIZATION TECHNIQUES

Current Loop Analysis:

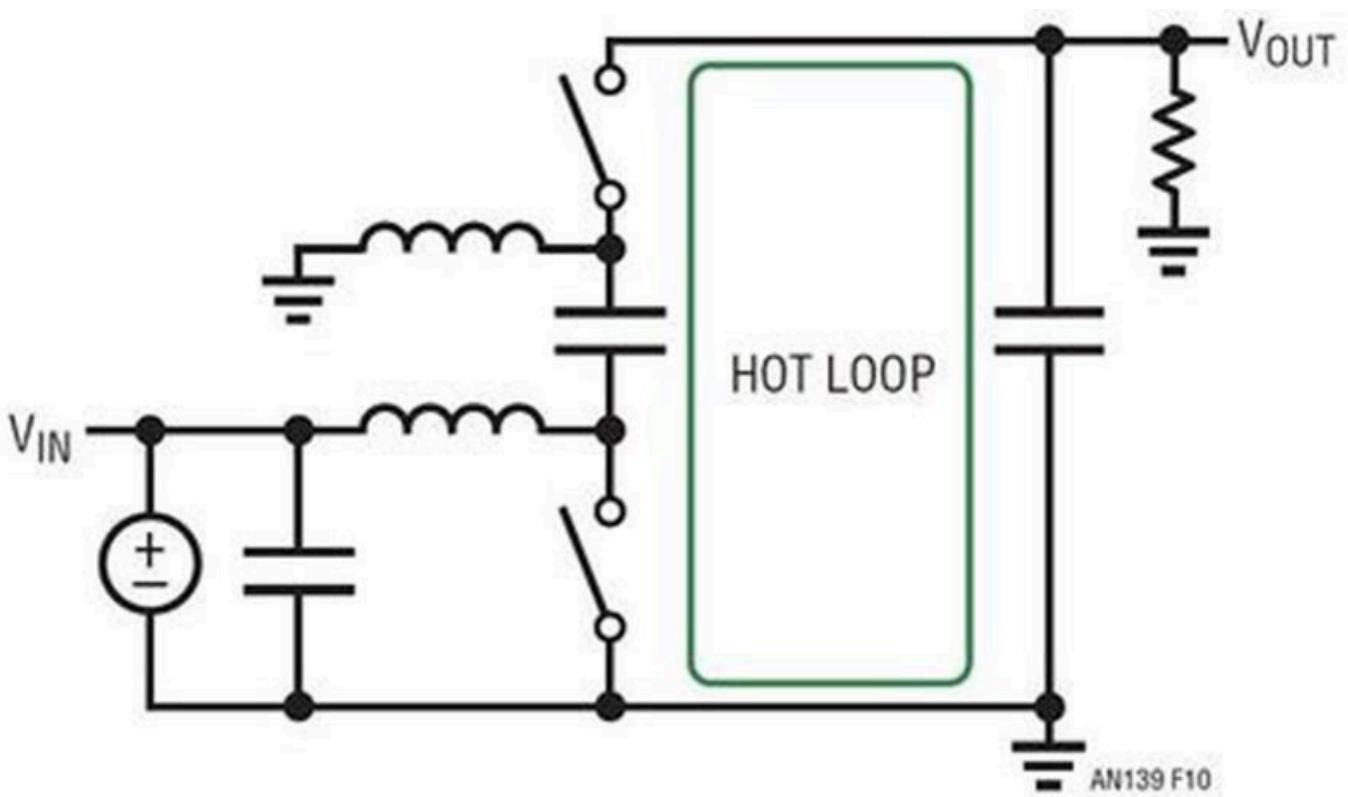
- High-frequency current path identification
- Minimize loop area = minimize inductance
- Power and ground connection optimization
- Via placement strategy

Via Inductance Reduction:

- Multiple parallel vias: $L_{\text{total}} = L_{\text{single}}/N$
- Via diameter: Larger reduces inductance
- Via length: Shorter reduces inductance
- Typical values: 0.5-2nH per via

Trace Inductance:

- Microstrip inductance $\approx 1\text{nH/mm}$
- Stripline inductance $\approx 0.8\text{nH/mm}$
- Wide traces reduce inductance
- Ground proximity reduces inductance



CAP- HIGH-SPEED DIGITAL LAYOUT

POWER DELIVERY NETWORK LAYOUT

Plane-Based Design:

- Dedicated power and ground planes
- Multiple power planes for different voltages
- Solid reference planes for signals
- Controlled impedance for power distribution

Decoupling Capacitor Placement:

- Symmetric placement around IC
- Shortest possible connections
- Multiple capacitor values
- Avoid placement under IC package

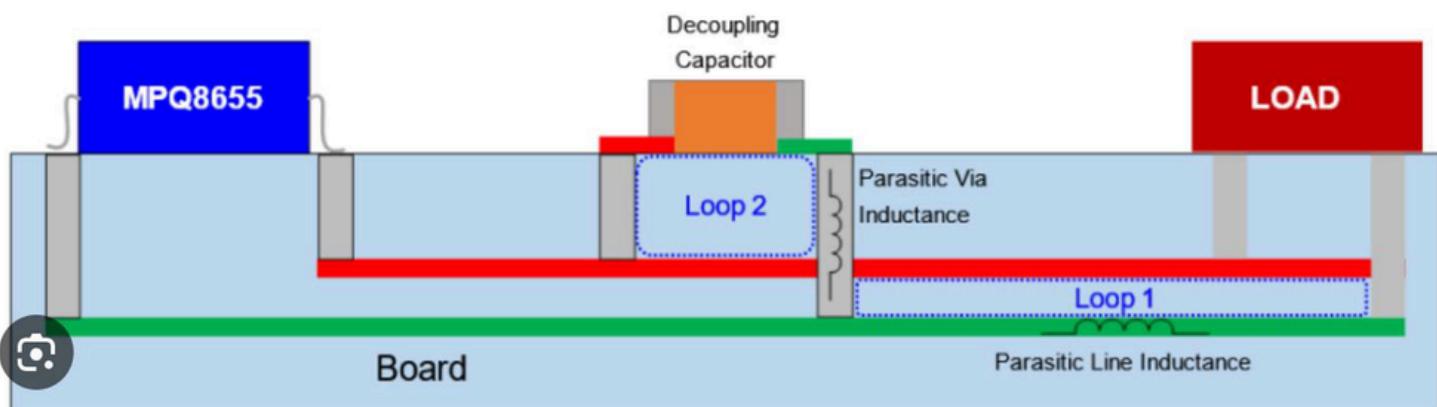
CLOCK CIRCUIT CONSIDERATIONS

Crystal Oscillator Layout:

- Load capacitors: <5mm from crystal
- Ground guard rings around crystal
- Separate analog ground region
- Shield from digital switching

PLL Power Supply:

- Dedicated LDO regulator
- LC input filter: $10\mu\text{H} + 47\mu\text{F}$
- Multiple bypass capacitors: $10\mu\text{F} + 1\mu\text{F} + 100\text{nF} + 10\text{nF}$
- Separate ground region



CAP IN ANALOG- ACTIVE FILTER DESIGN

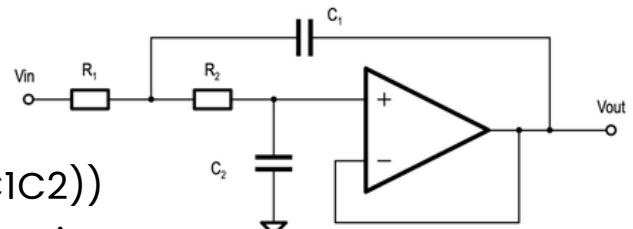
SALLEN-KEY TOPOLOGY

Component Matching:

- Capacitor ratio accuracy: $\pm 1\%$
- Temperature tracking: $< 10 \text{ ppm}/^\circ\text{C}$ difference
- Frequency response: Flat within passband
- Q factor stability: $\pm 5\%$ maximum

Low-Pass Filter Design:

- Corner frequency: $f_c = 1/(2\pi\sqrt{(R_1 R_2 C_1 C_2)})$
- Q factor: Dependent on component ratios
- Gain: Set by feedback resistor ratio
- Phase response: -180° at high frequency



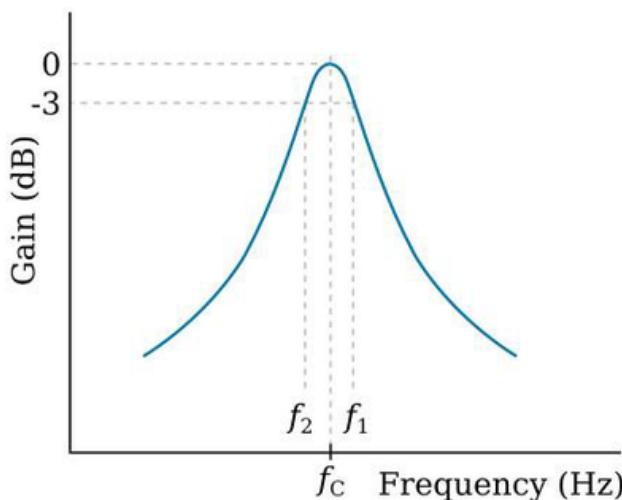
MULTIPLE FEEDBACK TOPOLOGY

Bandwidth Considerations:

- Op-amp GBW: $> 100 \times$ filter frequency
- Capacitor selection affects stability
- Temperature coefficient matching
- Aging characteristics

High-Q Filter Challenges:

- Component tolerance sensitivity
- Temperature drift effects
- Op-amp offset voltage impact
- Parasitic effects at high frequency



CAP IN ANALOG- OSCILLATOR CIRCUITS

CRYSTAL OSCILLATOR DESIGN

Load Capacitance:

- Crystal specification: $CL = 12\text{pF}$ typical
- PCB parasitic capacitance: 2–5pF
- Required external capacitance: $CL - C_{\text{parasitic}}$
- Capacitor matching: $\pm 5\%$ for frequency accuracy

Frequency Pulling:

- Load capacitance variation: $\pm 1\text{pF}$
- Frequency change: $\pm 50\text{ppm}$ typical
- Temperature coefficient: Crystal + capacitor
- Aging rate: $< \pm 5\text{ppm/year}$

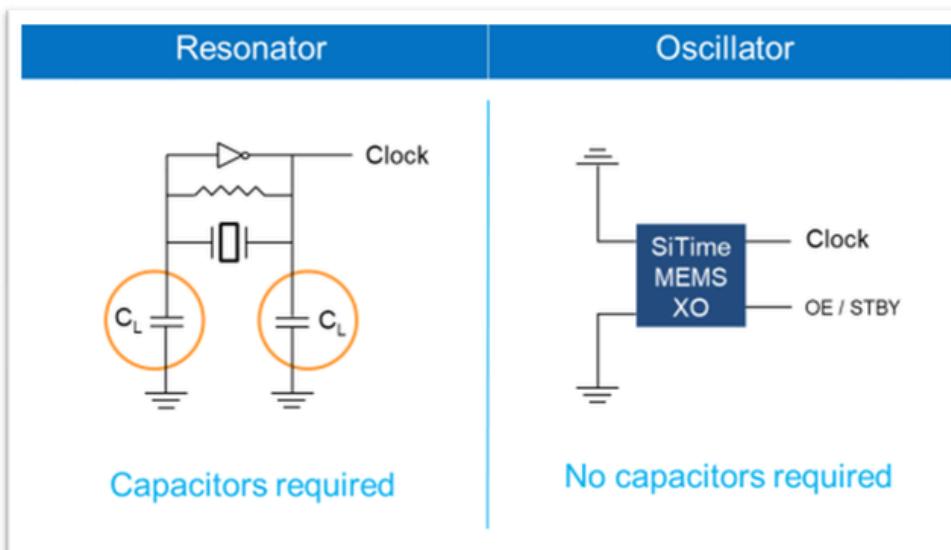
VOLTAGE-CONTROLLED OSCILLATORS

Varactor Tuning:

- Tuning voltage range: 0–5V typical
- Capacitance variation: 10:1 ratio
- Tuning sensitivity: MHz/V
- Linearity: Deviation from ideal

Coupling Networks:

- AC coupling: High-pass characteristic
- Buffer amplifier isolation
- Load impedance effects
- Phase noise considerations



POWER SUPPLY DESIGN CASE STUDIES

BUCK CONVERTER DESIGN

Specifications:

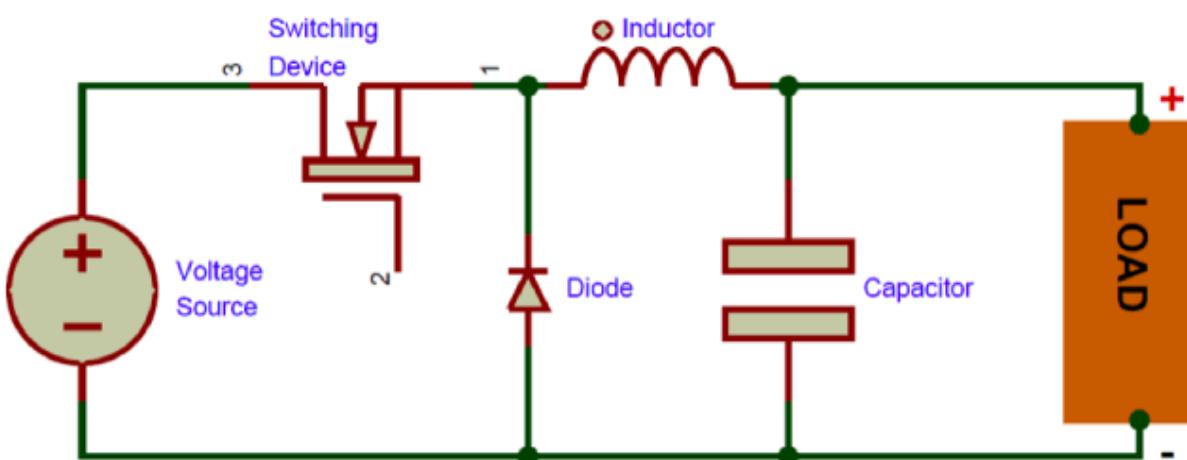
- Output voltage: $3.3V \pm 3\%$
- Output current: 0-10A
- Switching frequency: 500kHz
- Efficiency target: >90%

Input Capacitor Selection:

- RMS ripple current: $\sqrt{I_{out}^2 \times D \times (1-D)}$
- Where $D = V_{out}/V_{in} = 3.3/12 = 0.275$
- $I_{rms} = \sqrt{(10^2 \times 0.275 \times 0.725)} = 4.46A$
- Selected: 220 μ F low-ESR electrolytic, $I_{rms} = 5A$

Output Capacitor Design:

- Ripple current: $\Delta I_L/2 = (V_{out} \times (1-D)) / (2 \times L \times f_{sw})$
- For $L = 2.2\mu H$: $\Delta I_L = 2.75A$
- Ripple current in capacitor: $2.75A/2 = 1.38A$
- ESR requirement: $< 10m\Omega$ for $< 50mV$ ripple
- Selected: 470 μ F + 47 μ F ceramic parallel



POWER SUPPLY DESIGN CASE STUDIES

FLYBACK CONVERTER DESIGN

Specifications:

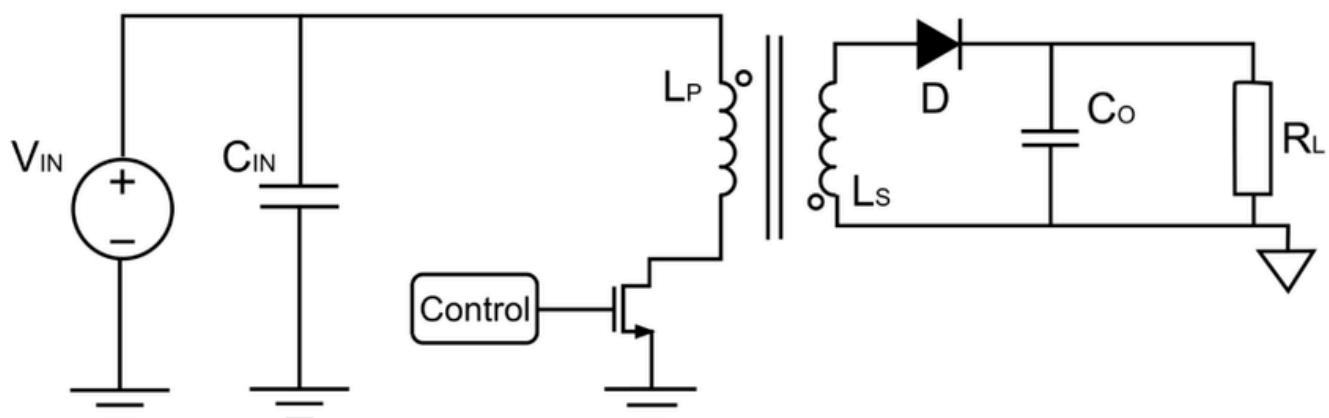
- Input voltage: 85-265VAC
- Output voltage: 12V, 2A
- Isolation: 3kVAC
- Regulation: $\pm 5\%$

Primary Side Capacitor:

- Bulk capacitance: $C = 2 \times P_{out} / (\eta \times V_{min}^2 \times 2 \times f_{line})$
- $C = (2 \times 24W) / (0.8 \times 108^2 \times 2 \times 60Hz) = 43\mu F$
- Selected: $47\mu F$, 400V electrolytic

Secondary Side Filter:

- Output ripple at $2 \times f_{line} = 120Hz$
- Required capacitance: $C = I_{out} / (2 \times f_{ripple} \times V_{ripple})$
- For 1% ripple: $C = 2A / (2 \times 120Hz \times 0.12V) = 69\mu F$
- Selected: $220\mu F$, 25V low-ESR electrolytic



EX: SWITCH-MODE PWR SUPPLY DECOUPLING

SYSTEM REQUIREMENTS

Switching Frequency: 500kHz Output Current: 5A Voltage Ripple: <50mV Input Voltage: 12V Output Voltage: 3.3V

CAPACITOR SELECTION PROCESS

Bulk Capacitance Calculation:

- $\Delta I = 5\text{A}$ (worst case)
- $\Delta t = 1/(2 \times 500\text{kHz}) = 1\mu\text{s}$
- $C = \Delta I \times \Delta t / \Delta V = 5 \times 1\mu\text{s} / 50\text{mV} = 100\mu\text{F}$

ESR Requirement:

- Ripple current: 2.5A RMS
- Voltage ripple from ESR: <25mV
- Maximum ESR: $25\text{mV} / 2.5\text{A} = 10\text{m}\Omega$

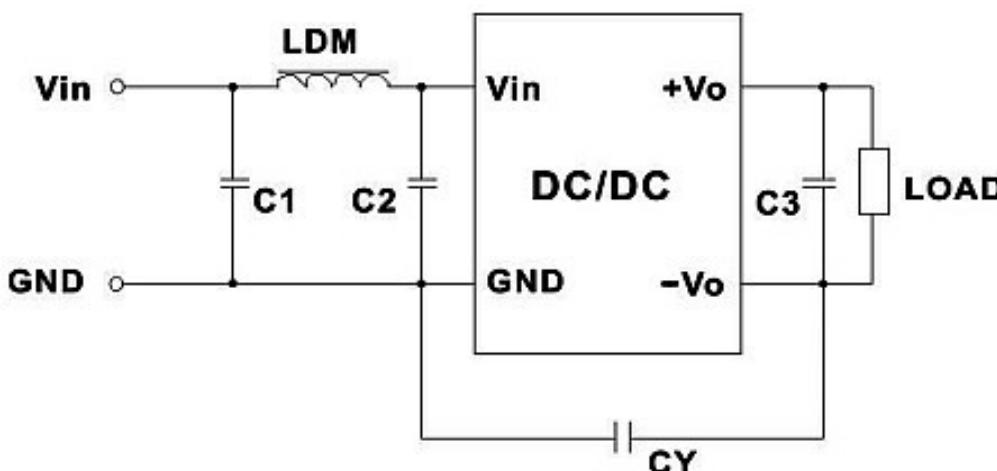
Selected Components:

- Bulk: 220 μF aluminum electrolytic, ESR = 8 $\text{m}\Omega$
- High-frequency: 47 μF ceramic X7R, ESR = 2 $\text{m}\Omega$
- Local: 1 μF ceramic X7R, ESR = 5 $\text{m}\Omega$

PERFORMANCE VERIFICATION

Measured Results:

- Output ripple: 35mV (meets requirement)
- Transient response: 100mV overshoot
- Efficiency: 92% (ESR losses = 0.5%)
- Temperature rise: 15°C above ambient



SIGNAL PROCESSING IMPLEMENTATIONS

AUDIO AMPLIFIER DESIGN

Preamplifier Stage:

- Input coupling: $1\mu\text{F}$ film cap
- Feedback network: 100pF C0G
- P.S bypass: $47\mu\text{F} + 1\mu\text{F} + 100\text{nF}$
- Output coupling: $10\mu\text{F}$ film cap

Critical Requirements:

- THD+N: $<0.01\% @ 1\text{kHz}$
- Frequency: $20\text{Hz}-20\text{kHz} \pm 0.1\text{dB}$
- Input impedance: $>10\text{k}\Omega$
- Output impedance: $<100\Omega$

Component Selection Rationale:

- Film capacitors: Low distortion, stable
- C0G ceramic: Precise frequency response
- Electrolytic: Cost-effective bulk storage
- Layout: Star grounding, short signal paths

