

Design *for* Testability

voltage
output interface
programmable adc
adc design
raw BULK injection
MODE sensing header
EXTERNAL supply pins
level RESISTOR comm
ground ADVANTAGES use

DFT
digital probe score
OVERVOLTAGE/UNDERVOLTAGE one flag
one flag pa7 THERMAL protocol
pa5 3.2V tp2
2.1V-20V can circuit reference
RAIL RAIL strategy
measurements boot 0Ω PA4
red criteria GND data case
PA3 PA1
PA2 R R
will smart PA2
specification
REVISION
active LED 2.54mm
signals STANDARD

COMMUNICATION CURRENT points
testability indication components calibration requirements internal
control diagnostics tpt CLK Blue trace plane
NOMS 12Ω NORMAL PA1
dwt POINT 12V green
LEDS CONNECTION 1x4
POINT 1x4
conditioning
power SWD miso
monitoring 2ma visual
jumper capability 5V arm
reduction temperature
shutdown VCC detection
GUIDE
debug LED 2.54mm
signals STANDARD

By Shimi Cohen

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1. INTRODUCTION TO DFT PHILOSOPHY

1.1 CORE PRINCIPLES

DFT is not an afterthought. It's fundamental design methodology.

PRIMARY GOALS:

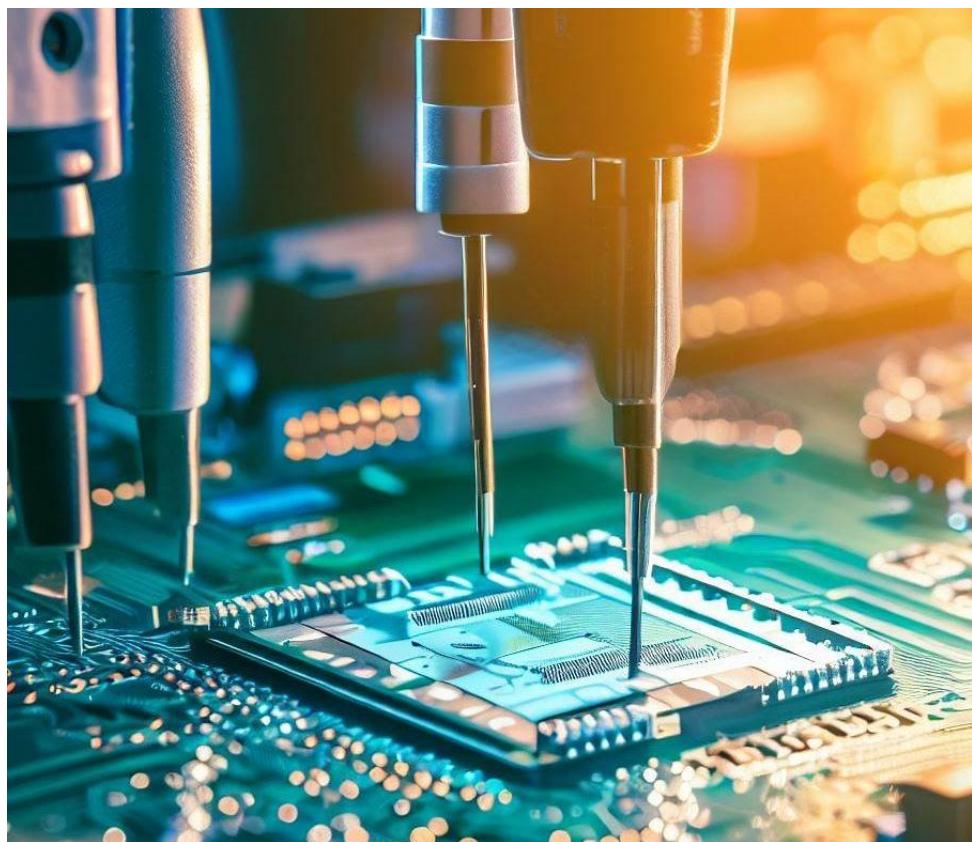
- Reduce debug time by 80%
- Enable production test automation
- Facilitate field service diagnostics
- Minimize expensive test equipment requirements

1.2 DFT HIERARCHY

Level 1: Basic accessibility (test points, headers)

Level 2: Intelligent monitoring (current sensing, voltage dividers)

Level 3: Advanced injection/isolation (switches, jumpers)



2. TEST POINTS STRATEGY

2.1 CRITICAL NODE IDENTIFICATION

Always Include Test Points For:

Signal Type	Rationale	Placement Priority
Power rails	<i>Voltage verification</i>	<i>High</i>
Clock signals	<i>Timing validation</i>	<i>High</i>
Reset lines	<i>System state control</i>	<i>High</i>
Communication buses	<i>Protocol debugging</i>	<i>Medium</i>
Analog references	<i>Calibration points</i>	<i>Medium</i>
PWM outputs	<i>Waveform verification</i>	<i>Low</i>

2.2 TEST POINT TYPES

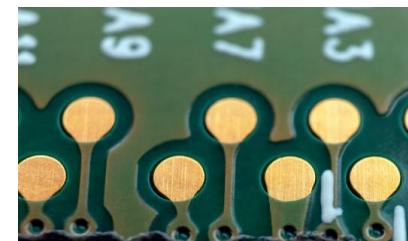
2.2.1 STANDARD THROUGH-HOLE (1MM)

- Use:** General purpose probing
- Density:** 2.54mm pitch minimum



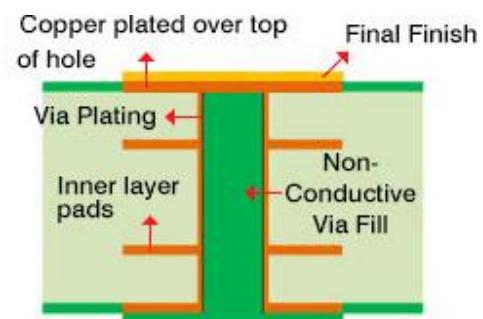
2.2.2 SMD PADS (0.5MM)

- Use:** High-density designs
- Access:** Requires fine-pitch probes
- Advantage:** Minimal board space



2.2.3 VIA-IN-PAD

- Use:** Ultra-compact designs
- Access:** Standard probe tips
- Limitation:** Single-use per manufacturing



2.3 TEST POINT PLACEMENT RULES

Power Rails:

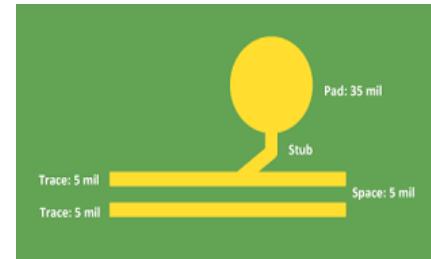
- Place immediately after regulation circuitry
- Include both input and output of regulators

Digital Signals:

- Position close to driving IC
- Avoid signal integrity impact
- Group by functional blocks

Analog Signals:

- Minimize parasitic capacitance
- Use guard traces where necessary
- Include reference voltages



2.4 REAL-WORLD EXAMPLE

MOTOR CONTROLLER BOARD

Critical Test Points Required:

- TP1: DCBUS (24V input)
- TP2: 12V_REG (intermediate rail)
- TP3: 3.3V MCU (MCU supply)
- TP4: 1.65V_REF (ADC reference)
- TP5: PWM_U, PWM_V, PWM_W (motor drive signals)
- TP6: CURRENT_U, CURRENT_V, CURRENT_W (feedback signals)
- TP7: CAN_H, CAN_L (communication)
- TP8: SPI_CLK, SPI_MOSI, SPI_MISO (encoder interface)



3. DEBUG INFRASTRUCTURE

3.1 DEBUG HEADER STRATEGY

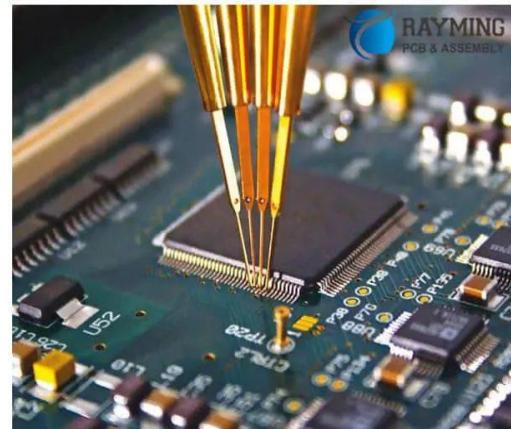
3.1.1 STANDARD DEBUG INTERFACES

<i>Interface</i>	<i>Connector</i>	<i>Signals</i>	<i>Use Case</i>
SWD	2x5 pin 1.27mm	SWDIO, SWCLK, nRST, GND, VCC	MCU Prog/debug
UART	1x4 pin 2.54mm	TX, RX, GND, VCC	Console/logging
SPI	1x6 pin 2.54mm	CLK, MOSI, MISO, CS, GND, VCC	Sensor debugging
I2C	1x4 pin 2.54mm	SDA, SCL, GND, VCC	Multi-device bus

3.1.2 CUSTOM DEBUG HEADERS

Power Monitoring Header:

- Pin 1: DCBUS
- Pin 2: 12V_REG
- Pin 3: 5V_REG
- Pin 4: 3.3V_REG
- Pin 5: 1.8V_REG
- Pin 6: GND_REF



3.2 PROBE-FRIENDLY DESIGN

3.2.1 COMPONENT SPACING

- Minimum 1.27mm between probe points
- Avoid components under 2mm height near TP
- Orient test points for probe access angles

3.2.2 GROUND REFERENCE STRATEGY

- Place ground TP 10mm of signal test points
- Use dedicated ground plane for test points
- Avoid ground loops in test connections

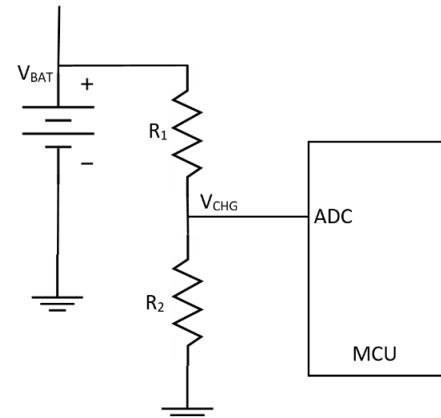
4. DC-DC AND POWER SUPPLY

4.1 POWER RAIL MONITORING

4.1.1 VOLTAGE DIVIDER NETWORKS

Standard 3.3V ADC Monitoring:

Voltage	R1 (kΩ)	R2 (kΩ)	ADC	Resolution
5V	10	20	1.67V	1.2mV/bit
12V	22	10	1.03V	2.9mV/bit
24V	47	10	1.42V	5.9mV/bit
48V	100	10	1.45V	11.7mV/bit



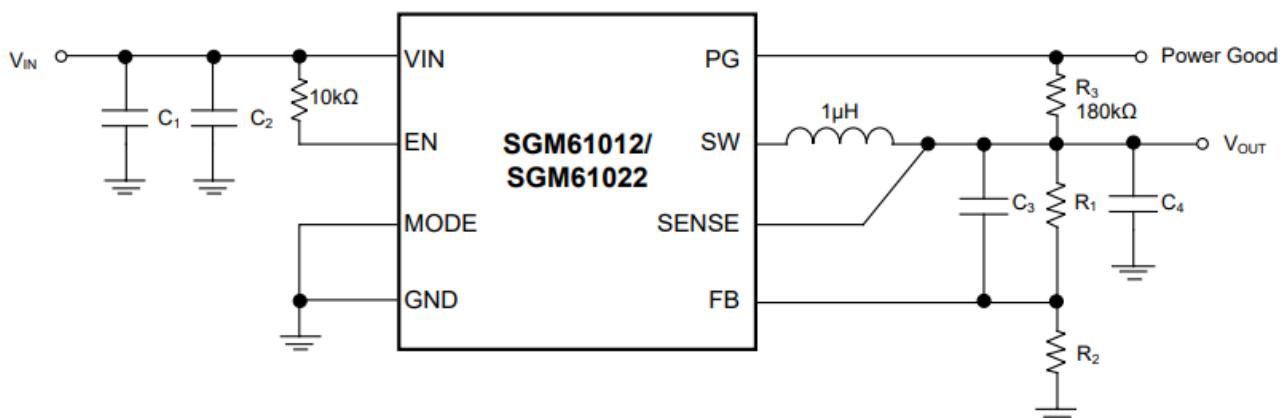
4.1.2 POWER GOOD INDICATORS

Voltage Supervisor:

- Connect Power Good to MCU GPIO
- It will be used as interrupt for fault ('0' = No Power)
- Pull-up resistor: 10kΩ (keeps the line active during boot)

Benefits:

- Immediate power rail status
- MCU interrupt capability
- Visual confirmation without instruments



4.2 LED STATUS INDICATORS

4.2.1 POWER RAIL LEDs

Standard Implementation:

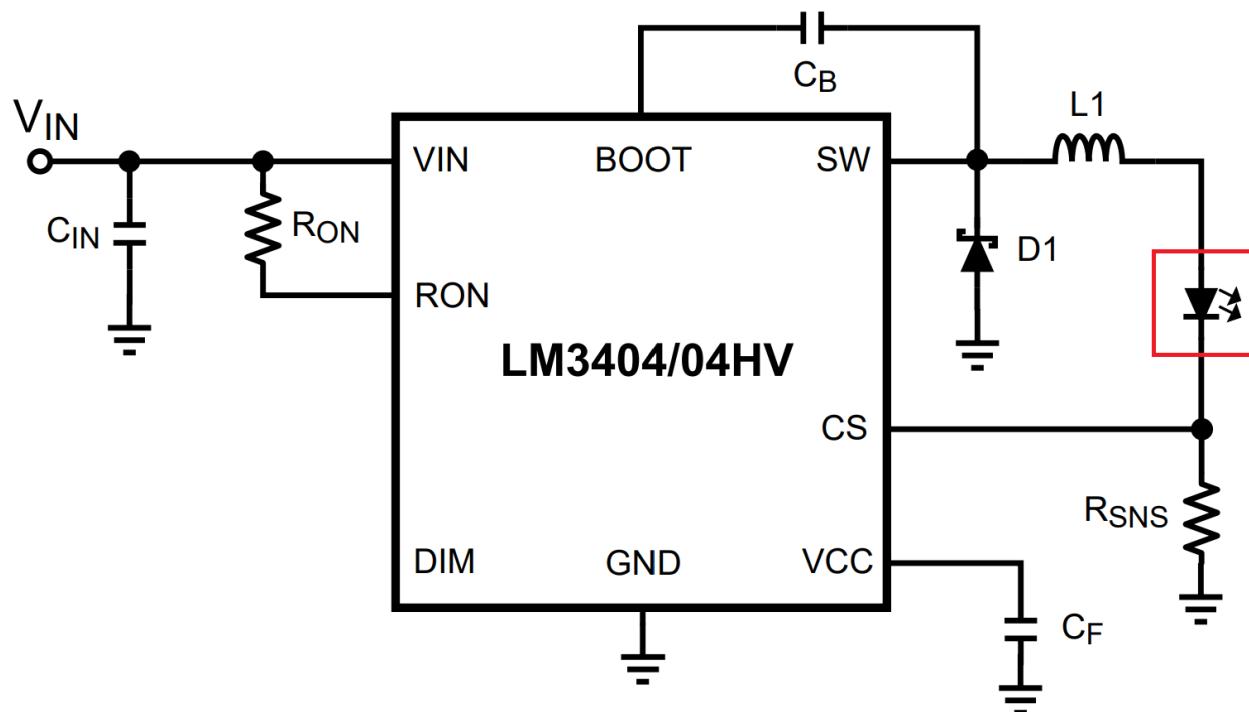
Per power rail:

- Series resistor: Calculate for 2mA current
- **Red**: Primary power (DCBUS)
- **Green**: Regulated supplies (3.3V, 5V)
- **Blue**: Reference voltages (1.65V, 2.5V)
- **Yellow**: Communication power (CAN, RS485)

4.2.2 SMART LED CIRCUITS

Voltage Window Comparator:

- Green LED: Voltage within $\pm 5\%$ specification
- Red LED: Voltage outside specification
- No LED: No power present



4.3 REAL-WORLD EXAMPLE:

SWITCH-MODE POWER SUPPLY

Design Requirements:

- Input: 18-36V DC
- Outputs: 12V/3A, 5V/2A, 3.3V/1A

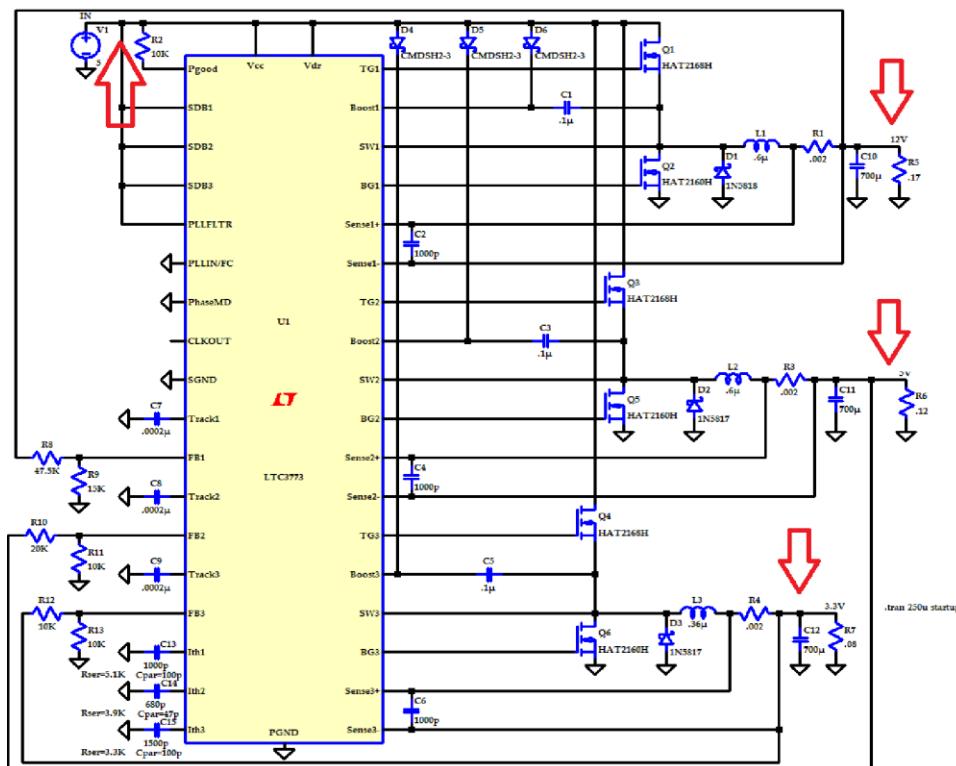
DFT Implementation:

Test Points:

- TP1: VIN
- TP2: 12V_OUT
- TP3: 5V_OUT
- TP4: 3.3V_OUT

Current Monitoring:

- R_SHUNT_IN: 0.01Ω input current
- R_SHUNT_12V: 0.05Ω 12V rail current
- R_SHUNT_5V: 0.1Ω 5V rail current



5. POWER AND GROUND

5.1 GROUND PLANE STRATEGY

5.1.1 DEDICATED TEST GROUND

- Separate test ground plane from circuit ground
- Connect via single point (star ground)
- Prevents test equipment from affecting circuit operation

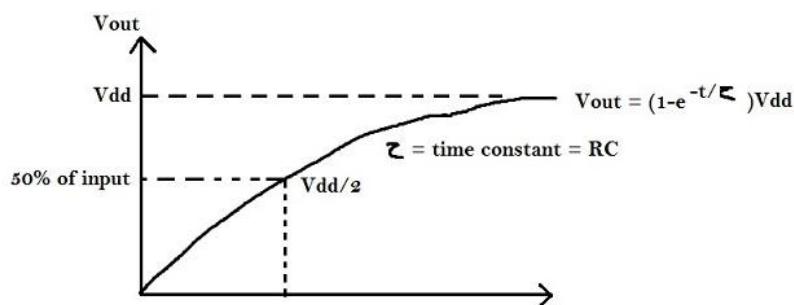
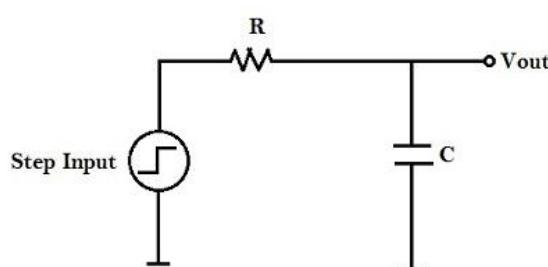
5.1.2 GROUND TEST POINTS

- One ground test point per functional block
- Remote ground reference for differential measurements
- Kelvin connections for precision measurements

5.2 POWER DISTRIBUTION TESTABILITY

5.2.1 POWER TESTABILITY TECHNIQUES

- RC Network on rail for Power Up Testability
- 0Ω resistor footprints in power paths
- Replace with current sense resistors during debug
- Remove for production (populate with 0Ω)



5.3 ISOLATION AND SEGMENTATION

5.3.1 POWER RAIL ISOLATION SWITCHES

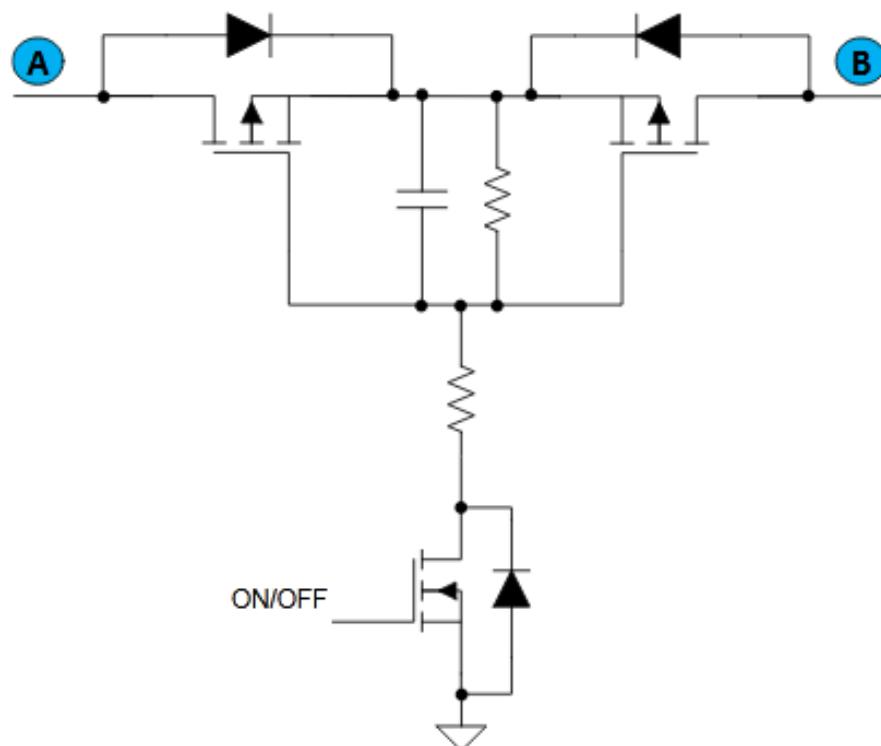
MOSFET Load Switches:

- P-channel MOSFET for high-side switching
- Enable/disable individual circuit blocks
- Current limiting capability
- Fault detection integration

5.3.2 GROUND LIFT CAPABILITY

Technique: Jumper-Selectable Ground Connections

- Normal operation: Jumper installed (solid ground)
- Debug mode: Jumper removed, insert current meter
- Enables per-block current measurement



6. MCU TESTABILITY

6.1 DEBUG INTERFACE ACCESSIBILITY

6.1.1 STANDARD DEBUG CONNECTORS

SWD Interface (ARM Cortex):

Standard 5-pin connector (2x5, 1.27mm pitch):

Pin 1: Supply (MCU voltage)

Pin 2: SWDIO (data)

Pin 3: RESET (reset)

Pin 4: SWCLK (clock)

Pin 5: GND



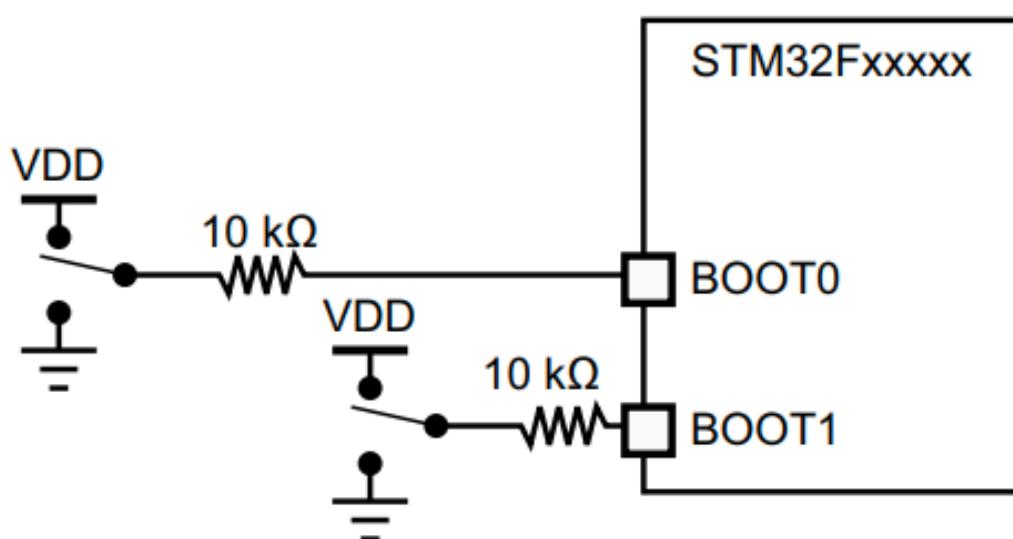
6.1.2 BOOT MODE SELECTION

Hardware Boot Selection:

- Boot mode pins accessible via jumpers
- Test points on boot configuration pins
- Visual indicators for current boot mode

Boot Mode Options:

- Normal flash execution
- System bootloader (UART/USB programming)
- Debug mode (JTAG/SWD priority)



6.2 GPIO TESTABILITY

6.2.1 GPIO TEST HEADERS

Port-Based Grouping:

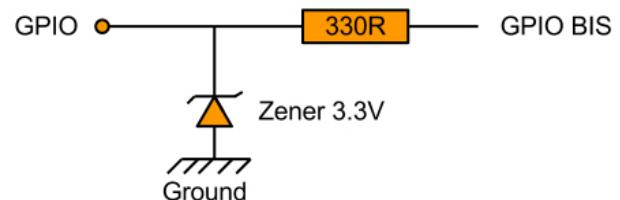
PORTA Header (8-pin):

PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7

PORTB Header (8-pin):

PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7

6.2.2 GPIO ISOLATION TECHNIQUES

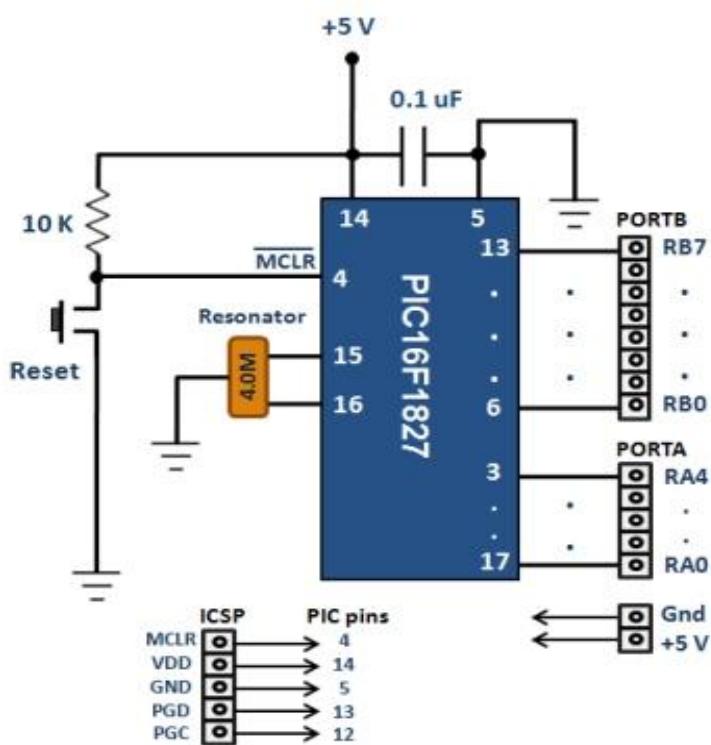


Series Resistor Method:

- 330Ω series resistors on all GPIO
- Where sensitive: Use Zener 3.3V
- Protects MCU from drive conflicts/overvoltage

Jumper Isolation:

- 0Ω resistor footprints in GPIO paths
- Remove jumper to isolate MCU from external circuit
- Insert test signals via isolated test points



6.3 ADC TESTABILITY

6.3.1 REFERENCE VOLTAGE ACCESS

Internal Reference Externalization:

- Internal VREF to test point
- Allows calibration verification
- Reference loading analysis

6.3.2 ADC INPUT CONDITIONING

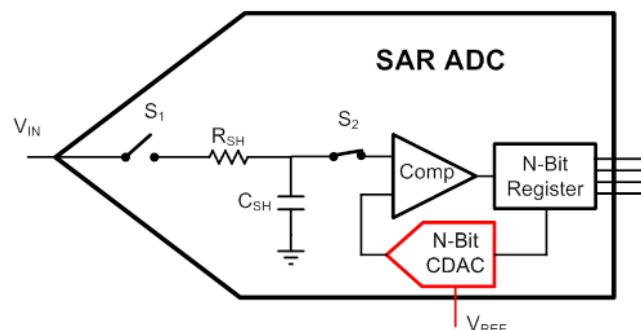
Signal Injection Points:

Before input conditioning:

- Raw sensor input
- Allows sensor simulation

After input conditioning:

- Conditioned signal to ADC
- Verifies signal conditioning accuracy

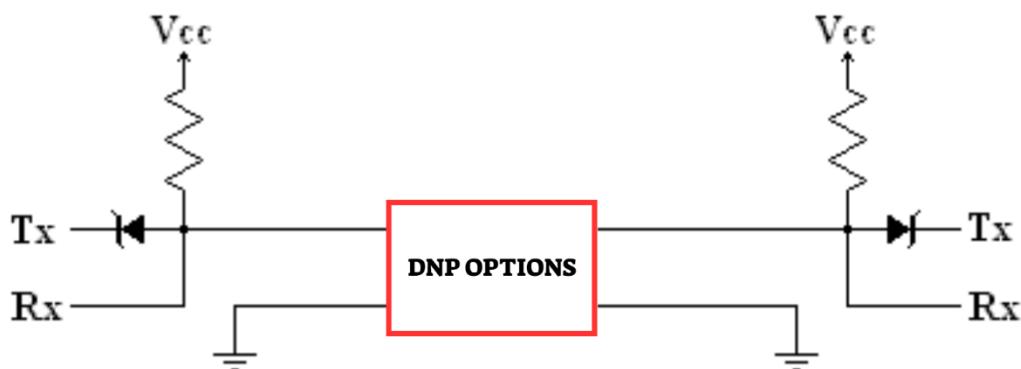


6.4 COMMUNICATION INTERFACE TESTING

6.4.1 UART TEST INFRASTRUCTURE

Use DNP resistors for crossed option ($\text{TX} \leftrightarrow \text{RX}$)

- Allows crossed path option
- Avoids Re-Spin if path is crossed
- Allows probing the data
- Allows direct injection



6.5 SIGNAL INJECTION ARCHITECTURE

6.5.1 MCU DISCONNECT CAPABILITY

Jumper-Based Disconnection:

MCU PIN —[0Ω Jumper]— EXTERNAL CIRCUIT



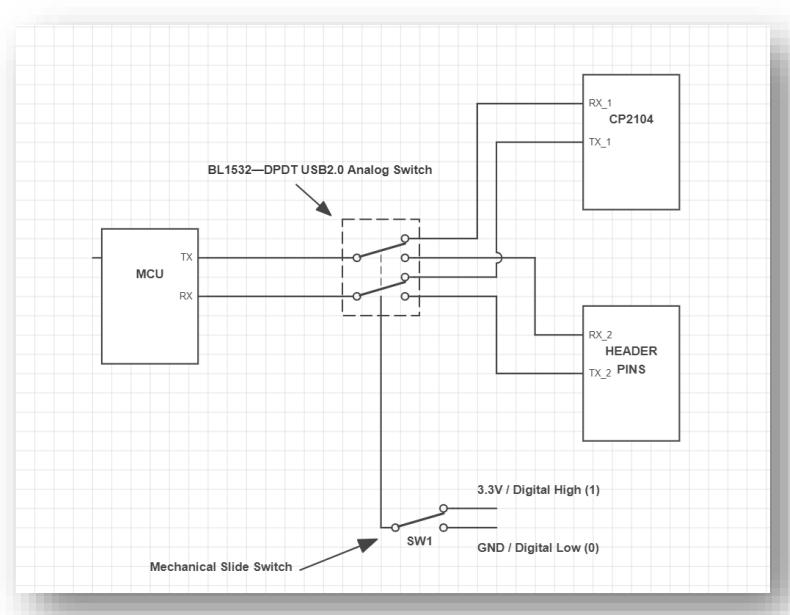
Debug mode:

1. Remove 0Ω jumper
 2. MCU pin isolated from external circuit
 3. Inject test signals via TP_INJECT
 4. Monitor circuit response

6.5.2 PROTOCOL GENERATOR CONNECTION

External Protocol Injection:

- Test connectors for each communication interface
 - Switchable connection between MCU and external
 - Protocol analyzer/generator connection capability



7. VISUAL INDICATION SYSTEMS

7.1 POWER RAIL INDICATION

7.1.1 LED Selection Criteria

<i>LED Type</i>	<i>Forward Voltage</i>	<i>Current</i>	<i>Visibility</i>
Red	1.8V	2mA	Excellent
Green	2.1V	2mA	Good
Blue	3.2V	2mA	Fair
White	3.2V	2mA	Excellent

7.1.2 CURRENT LIMITING RESISTOR CALCULATION

Formula:

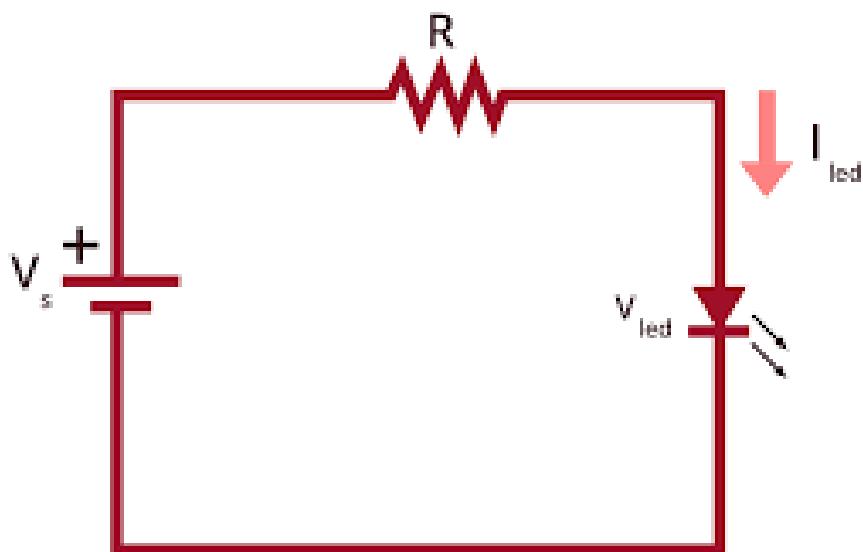
$$R = (V_{supply} - V_{led}) / I_{led}$$

Common Values:

$$3.3V \text{ supply, Red LED (1.8V, 2mA): } R = (3.3 - 1.8) / 0.002 = 750\Omega$$

$$5V \text{ supply, Green LED (2.1V, 2mA): } R = (5 - 2.1) / 0.002 = 1450\Omega$$

$$12V \text{ supply, Blue LED (3.2V, 2mA): } R = (12 - 3.2) / 0.002 = 4400\Omega$$

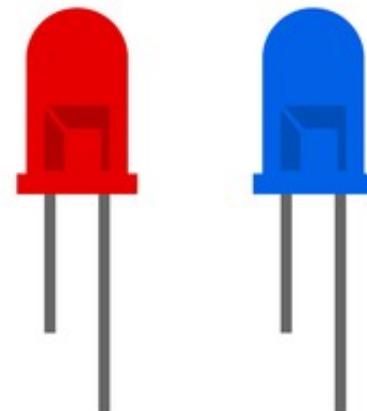


7.2 STATUS INDICATION HIERARCHY

7.2.1 PRIORITY-BASED LED ASSIGNMENT

Level 1 - Critical (Red LEDs):

- Overcurrent protection triggered
- Overvoltage/undervoltage fault
- Thermal shutdown active
- Communication timeout
- System fault condition



Level 2 - Warning (Yellow LEDs):

- Approaching thermal limit
- Voltage rail marginal
- Communication errors detected
- Calibration required

Level 3 - Normal (Green LEDs):

- Power rails within specification
- Communication active
- All systems normal

Level 4 - Information (Blue LEDs):

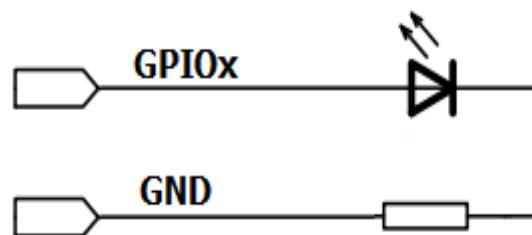
- Boot/initialization sequence
- Data transfer activity
- Test mode active

7.3 MCU-CONTROLLED INDICATION

7.3.1 STATUS LED PATTERNS

Single LED Multiple States:

- **Solid ON:** Normal operation
- **Slow blink (1Hz):** Warning condition
- **Fast blink (5Hz):** Error condition
- **Double blink:** Specific fault code



8. CURRENT SENSING FOR DEBUG

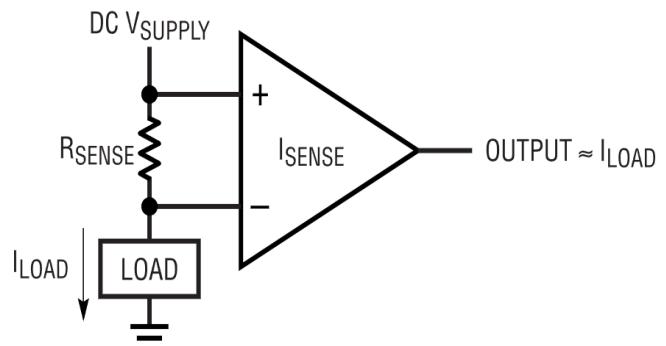
8.1 CURRENT SENSING FUNDAMENTALS

8.1.1 SENSING TOPOLOGY SELECTION

High-Side Current Sensing:

Advantages:

- Load protection from ground faults
- Detects load-to-ground shorts
- Preserves system ground integrity



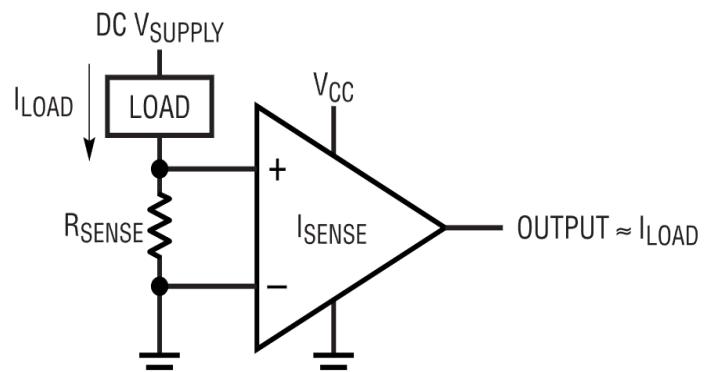
Disadvantages:

- Complex common-mode voltage handling
- Higher cost amplifier requirements
- Power supply rejection challenges

Low-Side Current Sensing:

Advantages:

- Simple signal conditioning (ground-referenced)
- Lower cost implementation
- Wide amplifier selection



Differential Current Sensing:

Advantages:

- Bidirectional current measurement
- High common-mode rejection
- Precise measurement capability

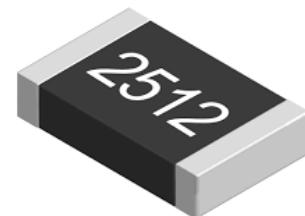
Disadvantages:

- Higher complexity
- Requires precision matched components
- Additional calibration requirements

8.2 SHUNT RESISTOR DESIGN STRATEGY

8.2.1 SHUNT RESISTOR VALUE SELECTION

<i>Current</i>	<i>Shunt</i>	<i>Power</i>	<i>Voltage @ Max</i>	<i>Resolution @ 12b</i>
0-100mA	10Ω	0.25W	1V	0.024mA
0-1A	0.1Ω	0.25W	0.1V	0.024mA
0-10A	0.01Ω	1W	0.1V	0.24mA
0-50A	0.002Ω	5W	0.1V	1.2mA



8.3 CURRENT SENSE AMPLIFIER SELECTION

8.3.1 AMPLIFIER COMPARISON MATRIX

<i>PN</i>	<i>Supply</i>	<i>Comm Mode</i>	<i>Gain Options</i>	<i>BW</i>	<i>Accuracy</i>	<i>Package</i>
INA180A1	2.7V-20V	-0.2V to 20V	20V/V	350kHz	±0.1%	SOT-23-5
INA190A2	2.7V-20V	-0.2V to 40V	50V/V	120kHz	±0.05%	SOT-23-5
INA219	3V-5.5V	0V to 26V	Programmable	N/A	±0.5%	SOT-23-8
INA226	2.7V-5.5V	0V to 36V	Programmable	N/A	±0.1%	VSSOP-10
AD8418	4.5V-80V	4V to 80V	20V/V	1MHz	±0.02%	SOIC-8

8.3.2 DIGITAL VS ANALOG OUTPUT SELECTION

Analog Output (INA180 family):

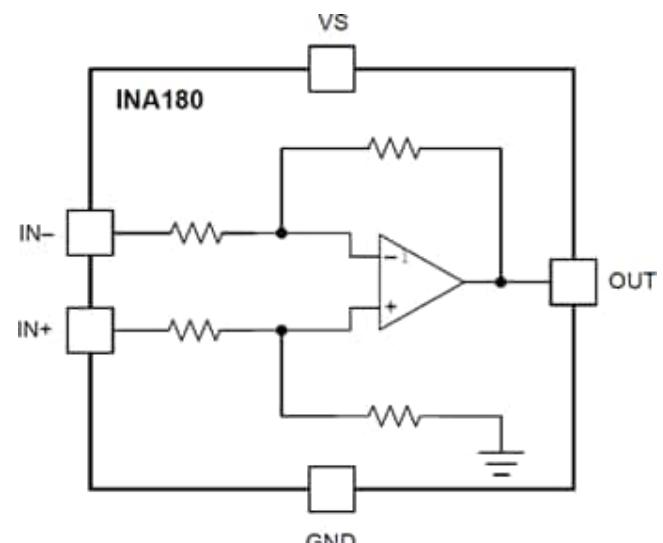
Advantages:

- Direct ADC interface
- Real-time monitoring capability
- Oscilloscope connectivity
- Simple implementation

Digital Output (INA219/INA226):

Advantages:

- Integrated ADC and calculation
- I2C interface simplicity
- Built-in calibration registers
- Multi-channel capability

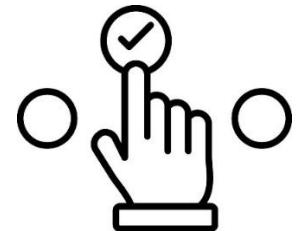


9. COMPONENT SELECTION

9.1 IC SELECTION PHILOSOPHY

9.1.1 TESTABILITY-FIRST SELECTION CRITERIA

<i>Priority</i>	<i>Criteria</i>	<i>Weight</i>	<i>Impact on Time</i>
1	<i>Built-in diagnostic features</i>	40%	<i>60-80% reduction</i>
2	<i>Pin accessibility</i>	25%	<i>40-60% reduction</i>
3	<i>Status indication capability</i>	20%	<i>30-50% reduction</i>
4	<i>Communication interfaces</i>	15%	<i>20-40% reduction</i>



Secondary Factors:

- Register visibility and control
- Internal monitoring capabilities
- Fault flag generation
- Reset and initialization control
- Clock output availability

9.1.2 "SMART" VS "DUMB" COMPONENT STRATEGY

"Smart" Components (Preferred):

- Integrated diagnostics
- Status registers
- Fault detection
- Communication interfaces
- Internal monitoring



"Dumb" Components (Avoid when possible):

- No status feedback
- Limited observability
- No diagnostic capability
- Requires external monitoring



9.2 POWER MANAGEMENT IC SELECTION

9.2.1 DC-DC CONVERTER COMPARISON

Feature	Basic LM2596	Smart TPS54331	Advanced LTC3891
Efficiency Monitor	No	Pin Output	I2C Register
Fault Flags	Thermal only	4 fault pins	16 fault registers
Enable Control	Simple EN	EN + UVLO	I2C + Pin control
Frequency Control	Fixed	Resistor select	I2C programmable
Current Monitoring	External only	Internal sense	Telemetry output
Thermal Monitoring	Shutdown only	Warning flag	Temperature readback
Testability Rating	Low (2/10)	Medium (6/10)	High (9/10)

9.2.2 ADVANCED POWER MANAGEMENT FEATURES

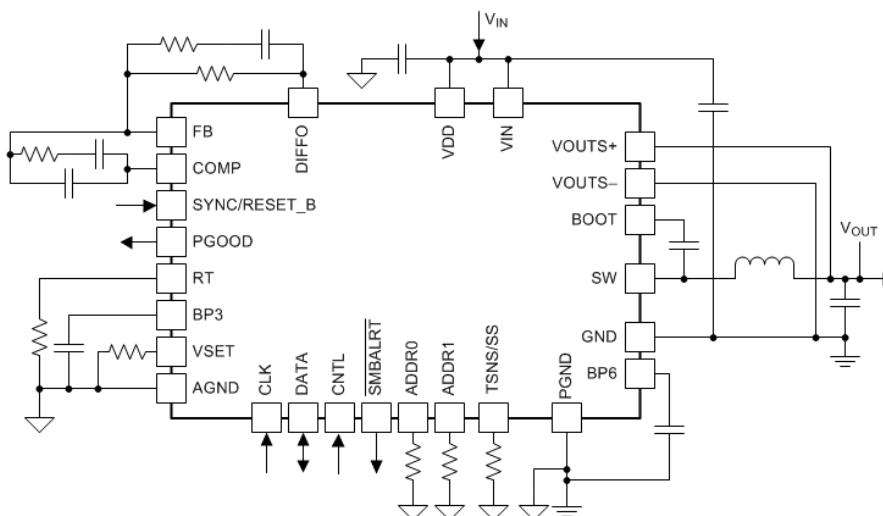
Texas Instruments TPS544C25 (Digital Power):

Diagnostic Capabilities:

- Input/output voltage/current monitoring
- Temperature monitoring
- Efficiency calculation
- Fault logging with timestamps
- Black box data recording

Accessible Parameters:

- Switching frequency adjustment
- Sequence timing control



9.3 MCU SELECTION FOR MAXIMUM OBSERVABILITY

9.3.1 DEBUG INTERFACE COMPARISON

<i>MCU Family</i>	<i>Debug</i>	<i>Trace</i>	<i>Built-in Monitors</i>	<i>Testability Score</i>
AVR ATmega	<i>debugWIRE</i>	No	<i>WDT only</i>	4/10
ARM Cortex-M0+	<i>SWD</i>	No	<i>SysTick</i>	6/10
ARM Cortex-M4	<i>SWD + ETM</i>	Yes	<i>DWT, ITM</i>	8/10
ARM Cortex-M7	<i>SWD + ETM</i>	Yes	<i>DWT, ITM, PMU</i>	9/10

9.3.2 MCU INTERNAL MONITORING FEATURES

STM32F405 Advanced Features:

Built-in Diagnostics:

- Internal temperature sensor
- Internal voltage reference monitoring
- Supply voltage monitoring (VDD/VDDA)
- Backup domain voltage monitoring
- PLL lock detection
- HSE/LSE oscillator failure detection

Debug Capabilities:

- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Wire Viewer (SWV) output
- Real-time variable monitoring
- Performance monitoring unit (PMU)

