

File.exe /file.hex

Types of Errors { Syntax - Runtime - Logical - Semantic }

Optimizer { Functionality - Size - Execution }

Padding Problem → `#Pragma pack(1)`

Enum → Enumeration to not use magic numbers to describe Variable structure → User-Defined Data-type that holds different Data-types.

"type def. → Renaming Primitive Data type (Defined /User-Defined)

define ptr int*
int* x,y;
Pointer ← ↗ integer

(1)

type def ptr int*

int* x,y;

Both are Pointers.

(2)

Bit-Math

>>	Shift Right
<<	Shift Left
~	Not
&	AND
	OR
^	XOR

Mask → to get specific Value of Register

SET-BIT (Reg,bit) → Reg l = (1 << bit)

CLEAR-BIT (Reg,bit) → Reg b = (1 << bit)

TGL-BIT (Reg,bit) → Reg n = (1 << bit)

GET-BIT (Reg,bit) → ((Reg >> bit) & 1)

GET-Low-NIPPLE (Reg) → Reg & 0b00001111

GET-HIGH-NIPPLE (Reg) → (Reg >> 4) & 0b00001111

GET-Port (Reg) → Reg & 0X FF

@ TGL-PORT (Reg) → Reg ^= 0xFF

- Const** → Variable that can't be changed in any place in code
Volatile → Garbage Collector Avoidance (according to optimizer)
Static → extend lifetime of variable to end of program
extern → use variable value in another file.

#structure: User defined data type that can holds different datatypes

#Enum: To not use magic numbers to describe variable state or name.

#Type of Enum:

- Describe state
- Describe name
- Describe Mode

- Use `typedef` before enum to make user-defined datatype
- enum took only 1 byte or 2 bytes according to compiler

#Dynamic Memory Allocation....

(`malloc`, `calloc`, `realloc`)

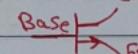
- ↳ Are not allowed to use in Embedded Automotive, as it uses only static memory (.stack)

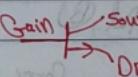
Computer Arch.

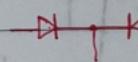
Automotive → static memory
IoT → dynamic memory

~~Diodes~~ → 

~~Transistors~~

• BJT →  collector
Base
Emitter

• MOSFET →  Gate
Source
Drain

• PNP → 

• NPN → 

~~Logical Gates~~

• AND → 

• OR → 

• XOR → 

• NOT → 

Diodes

Transistors

logical Gates

Latches

Flip FLOP

Register

Logic → Actual

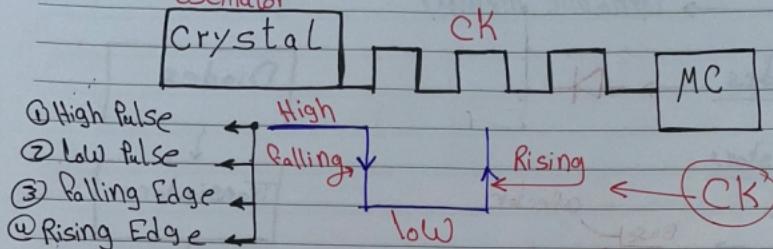
Zero (0) → 0 Volt

One (1) → 5 Volt

Flip_Flop → When to Keep charge...

• It Uses clock...

• Each instruction will be executed While high pulse oscillator

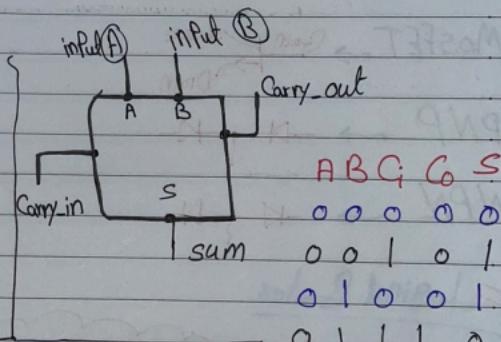


Full_Adder

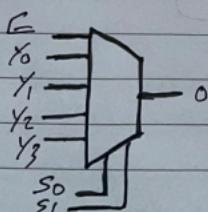
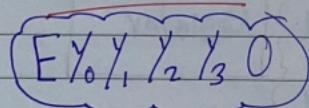
Carry_out ← ①

$$\begin{array}{r} 0101 \\ + 1011 \\ \hline 1110 \end{array}$$

"Adding Two Binary Numbers"



Multiplexer



E	S ₀	S ₁	O
Y ₀	0	0	Y ₀
Y ₁	0	1	Y ₁
Y ₂	1	0	Y ₂
Y ₃	1	1	Y ₃
X	X	X	None

Binary Decoder (2 inputs - 4 outputs)

if ("enable" \rightarrow E) is low (0)

so, the result is W_0

zero, when input W_1

is, result will be

always low ...

E



$E \ W_0 \ W_1 \ Y_0 \ Y_1 \ Y_2 \ Y_3$

1 0 0 1 0 0 0

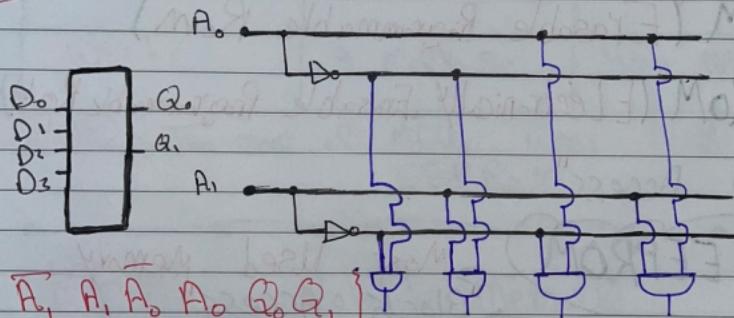
1 0 1 0 1 0 0

1 1 0 0 0 1 0

1 1 1 0 0 0 1

0 X X 0 0 0 0

Binary Encoder



$A_1 \ A_0 \bar{A}_1 \bar{A}_0 \ A_0 \bar{Q}_0 \bar{Q}_1$

0 0 0 1 0 0

0 0 1 0 0 1

0 1 0 0 1 0

1 0 0 0 1 1

0 0 0 0 XX

summary

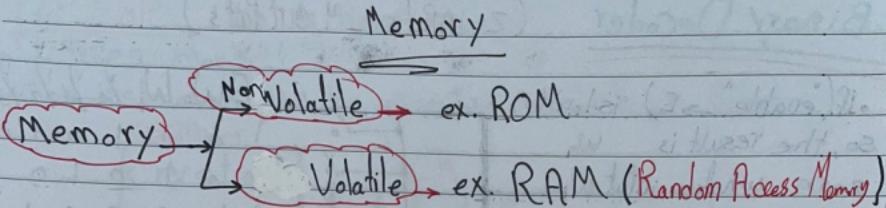
- Logical gates (AND, OR, XOR...)

latches

flip flop

$\} \rightarrow$ sequential logic component

Combinational logic Component ..
(Multiplexer, Full Adder, Decoder, Encoder)



ROM (Read ONLY Memory)

OTP ROM (One Time Programmable ROM)

EPRoM (Erasable Programmable Rom)

EEPRoM (Electronically Erasable Programmable RoM)

"Byte Access"

Flash EEPROM → "Most Used Memory" → "Block Access"

TYPES of Flash EEPROM :

- ① NoR Memory
- ② NAND Memory

Hint

RoM uses floating gate transistor, which is
give (supply) Memory With excess Voltage higher than
needed to be sure it keeps 5V charge inside

class	Flash EEPROM	NoR Flash EEPROM	NoNAND Flash EEPROM
SIZE	$\leq 512\text{ MB}$	From 1-8 GB	
BLOCK	1 MB	1 MB	
Speed _{Read}	< 80 Nanos	20 millis	
Erase	1s / Block	1s / Sector	
Write	9 micros.	400 micros	

(Note) → The most of MCUs uses NoR Flash - EEPROM

RAM

Volatile Memory

class	RAM	Static RAM	Dynamic RAM
		Made of Transistors	Made of Capacitors
Power Behavior		need Continuous Power Source	High Power Consumption

Registers

- User-Accessible Register → Register Can be read/Write by machine instruction → Accumulator

Address register

general purpose register

special purpose register

[status, Program Counter, stack pointer]

- Internal Register → Register used internally for processor operation and not accessible by instruction

Instruction Register

Memory Buffer Register

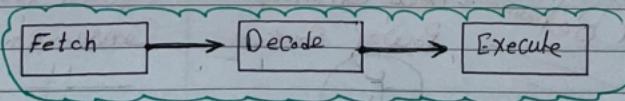
Memory Data Register

Memory Address Register

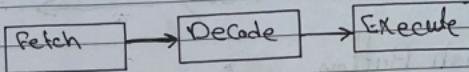
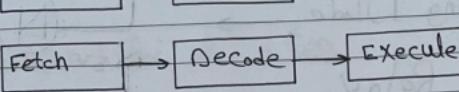
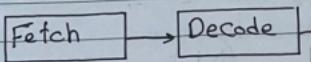
Example

Instruction Cycle

- Fetch → Get instruction from **RAM** and send it to **ALU**
- Decode → specify type def operation to **ALU**
- Execute → Execute Atomic instruction

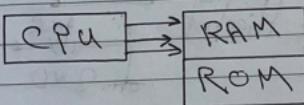


Pipeline

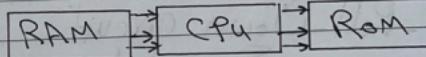


Computer Architecture

Von-Neumann

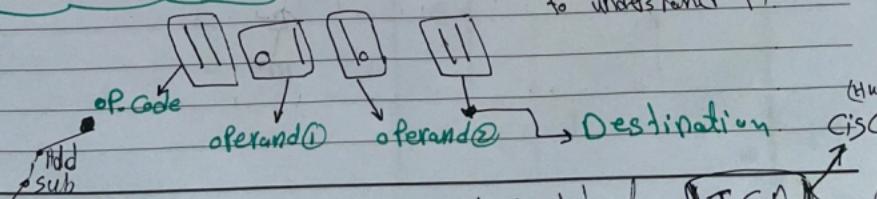


Harvard



instruction Decade

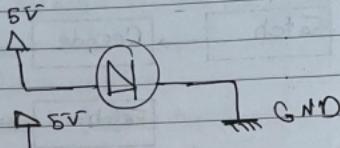
Divide instruction to several bits
to understand it



get IF from instruction set Architecture ISA RIS

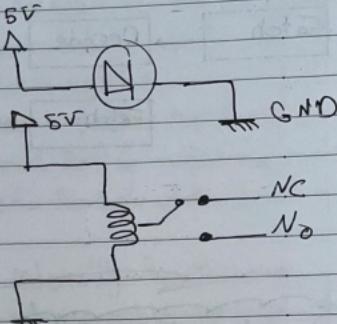
Input and Output Modules

Light Emitting Diode →



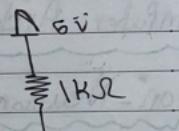
Mechanical Relay →

Push Button →



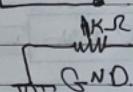
Pull-up Circuit [Active Low]

≡ Wait logic Zero"

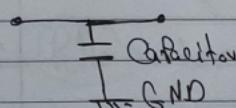


Pull-Down Circuit [Active High]

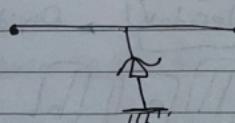
≡ Wait logic one"



LOW-Pass Filter

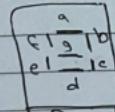


Safety Circuit



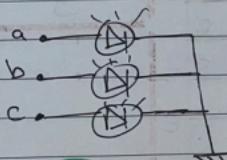
٩ / ٣ / ٢٣ التاريخ

7-Segment

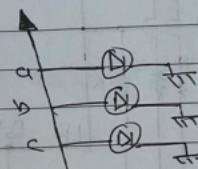


It Contains several LEDs (Light Emitting Diode)

There are two types of 7 Seg:

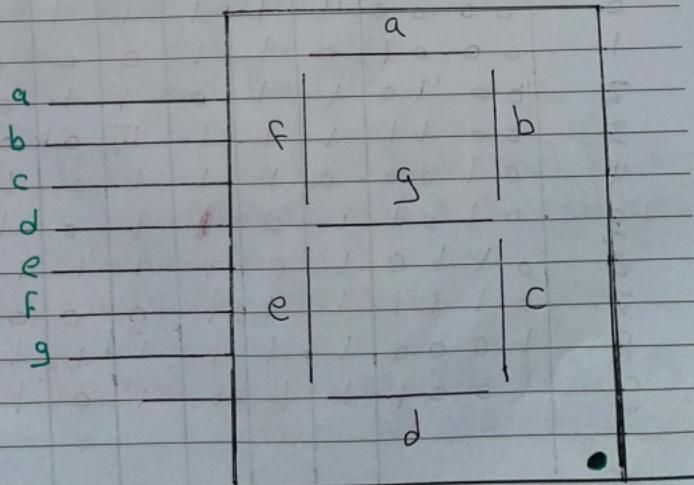


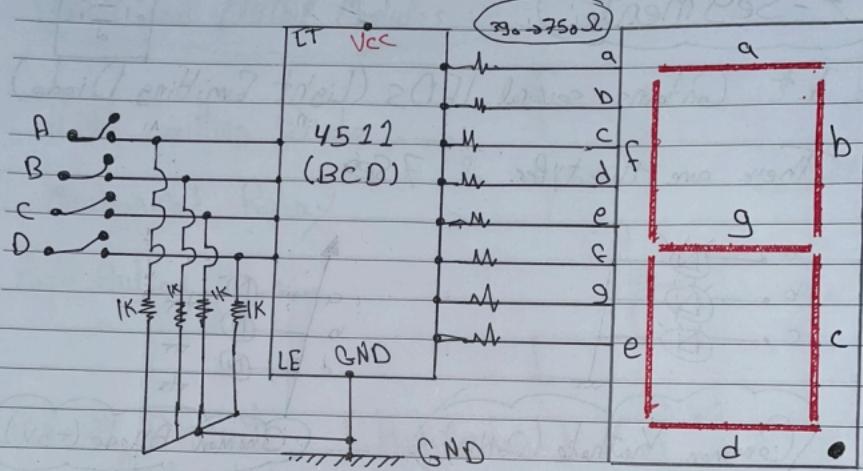
Common Cathode (GND)



Common Anode (+5V)

- It depends on decode (Binary Decoder), 4 inputs (4 Pins)
with 8 outputs (8 LEDs)



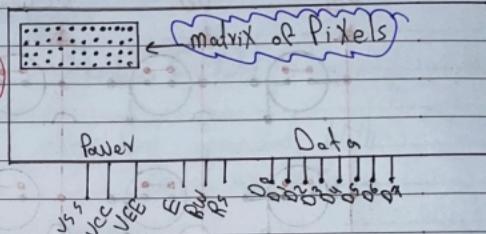


Decimal	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	1	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Liquid Crystal Display (LCD)

- LCD has two memories

\nwarrow CG-RAM \searrow DD-RAM



- CG → character Generator

- DD → Data Display

• LCD saves internally 256 Ascii characters inside DDRAM

- RS → Register Select to switch betw Registers
 - ↳ Logic (0) Write inside Command Control Register
 - ↳ Logic (1) Write inside Command Data Register

- R/W → Read & Write from LCD

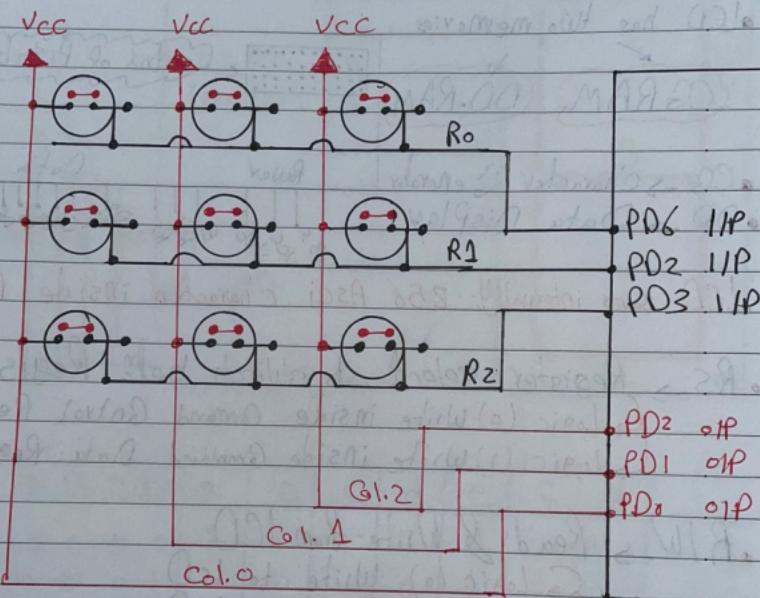
- ↳ Logic (0) Write to LCD
- ↳ Logic (1) Read from LCD

- E → Enable LCD - "Latch Logic High until finish Writing", "Wait till get high pulse"

- ↳ Logic (0) Disable LCD
- ↳ Logic (1) Enable LCD

- LCD has two modes →
 - ① 8-Bit Mode (0x38)
 - ② 4-Bit Mode (0x28)

Key Pad Considered as matrix of Buttons



- Each Pin Connected internally by Pull-up Resistor
Why?
- Activate internal pull-up Resistor AVR

- Define DDRX direction as input
- Define PORTX , Pin needed by set logic(1)
- $DDRA = 0x00 = 0000\ 0000$
- $PORTA = 0x01 = 0000\ 0001$