

The Real **Transformer Book**

By Shimi Cohen



TABLE OF CONTENT

PRELUDER A: TRANSFORMER SELECTION.....	3
PRELUDER B: MULTI-WINDING.....	4
CHAPTER 1: FUNDAMENTAL ELECTROMAGNETIC PRINCIPLES	5
CHAPTER 2: NON-IDEAL TRANSFORMER MODEL.....	6
CHAPTER 3: DOT CONVENTION AND PHASE RELATIONSHIPS	8
CHAPTER 4: IMPEDANCE TRANSFORMATION.....	9
CHAPTER 5: CORE MATERIAL SELECTION	11
CHAPTER 6: CORE SATURATION AND FLUX MANAGEMENT.....	12
CHAPTER 7: EFFICIENCY AND LOSS CALCULATION	13
CHAPTER 8: FREQUENCY DOMAIN BEHAVIOR	14
CHAPTER 9: SMPS ISOLATED TOPOLOGIES.....	15
CHAPTER 10: SIGNAL AND RF APPLICATIONS	17
CHAPTER 11: ISOLATION AND SENSING	18
CHAPTER 12: TRANSFORMER DESIGN - PART 1.....	19
CHAPTER 13: TRANSFORMER DESIGN - PART 2.....	22
CHAPTER 14: LTSPICE SIMULATION	24
CHAPTER 15: DESIGN NOTES.....	26
CHAPTER 16: SMART DESIGN TOOLS.....	27

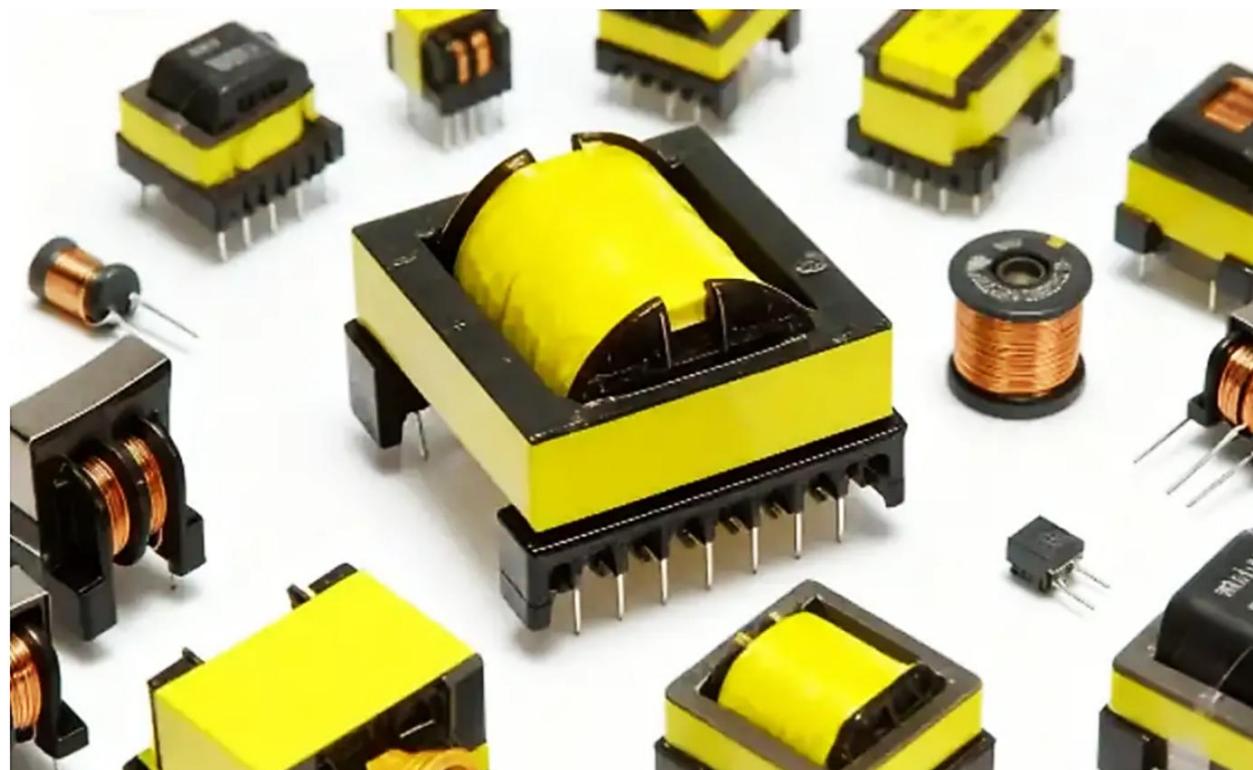
Prelude A: Transformer Selection

THESE ARE THE MOST COMMON TRANSFORMER TYPES:

	Trans Type	Primary Function	Core Material	Frequency	Key Design
POWER	Line/Mains	Voltage Conversion	Silicon Steel	50/60Hz	Efficiency
	Flyback	Isolated DC-DC	Ferrite	50kHz–300kHz	Energy Storage
	Forward	Isolated DC-DC	Ferrite	50 kHz–500kHz	Efficiency
	Bridge (LLC)	High-Power SMPS	Ferrite	100kHz–500kHz	High Power Density
	Autotransformer	Voltage Adjustment	Silicon Steel	50/60Hz	Minimal Size/Cost
SIGNAL	AUDIO	Isolation/Matching	Steel/Ferrite	20Hz–20kHz	Signal Flatness/THD
	RF (Radio)	Impedance Matching	Ferrite Toroid	1MHz–100MHz	Q-Factor / VSWR
	Balun	Balanced/Unbalanced	Ferrite Toroid	MHz to GHz	CMRR
	Pulse/Gate Drive	Switching Isolation	Ferrite	50kHz–1MHz	Rise Time
	Ethernet	Isolation/Filtering	Ferrite	10MHz–125MHz	Insertion/Return Loss
SENSING	Current Trans (CT)	Current Scaling	Ferrite/Steel	50 Hz–1MHz	Accuracy (Ratio Error)
	Potential Trans (PT)	Voltage Scaling	Silicon Steel	50/60Hz	Accuracy (Phase Error)
	Rogowski Coil	Current Change	Air	DC–1MHz	Linearity/Bandwidth

THE MOST COMMON MATERIALS:

Material	Core State	Freq.	Resistivity (Ω)	Key Application
Silicon Steel	Laminated	Low	Medium	Handles High (Max AC Power)
Ferrite	Ceramic	High	Very High	Low Eddy Currents (High Efficiency at High Freq.)
Powdered Alloy	Compressed	Wide	Medium-Low	Resists DC Bias (Energy Storage/Filtering)
Air Core	Non-Magnetic	High	Neglectable	Zero Core Loss (Max Bandwidth)



Prelude B: Multi-Winding

1. SINGLE PRIMARY CONFIGURATIONS

1-in 1-out (Standard Two-Winding)

Type	Application	Example
Line transformer	Wall adapter	230V → 12V
Flyback	DC-DC converter	48V → 5V isolated
Audio	Signal coupling	600Ω → 600Ω
CT	Current sensing	100A → 5A

Popularity: ★ ★ ★ ★ ★



1-in 2-out (Dual Secondary)

Configuration	Application	Example
Two isolated outputs	Multi-voltage supply	230V → 12V + 5V
Center-tapped	Dual-rail supply	230V → +12V, 0V, -12V
Split winding	Push-pull rectifier	AC → ±15V

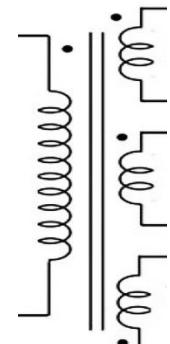
Popularity: ★ ★ ★ ★



1-in 3-out (Triple Secondary)

Application	Example
Multi-rail power	230V → 12V + 5V + 3.3V
Bias supplies	Main + gate drive + control
Triple isolated	Three independent channels

Popularity: ★ ★ ★



2. DUAL PRIMARY CONFIGURATIONS

2-in 1-out (Dual Primary)

Configuration	Application	Topology
Center-tapped primary	Push-pull converter	Each primary driven alternately
Parallel primaries	High current input	Current sharing
Series primaries	Voltage doubling	Input voltage selection

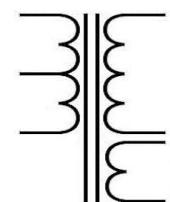
Popularity: ★ ★ ★ ★ (SMPS)



2-in 2-out (Dual Primary, Dual Secondary)

Application	Example
Push-pull with dual output	Symmetric supply with 2 primaries
Universal input multi-output	120/240V → 12V + 5V
Balanced power	Audio, balanced drive

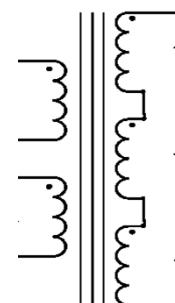
Popularity: ★ ★ ★



2-in 3-out (Dual Primary, Triple Secondary)

Application	Example
Push-pull triple output	Complex isolated supply
Flyback with reset + outputs	Primary + reset winding + 2 secondaries

Popularity: ★ ★



Chapter 1: Fundamental Electromagnetic Principles

1.1 MAGNETIC COUPLING FUNDAMENTALS

Magnetic coupling defines how a varying current in one coil produces a changing magnetic flux. The degree of this coupling, described by the coefficient k , determines how much of the magnetic flux generated by one coil links to the other. In practical windings, k is always less than unity due to inevitable leakage.

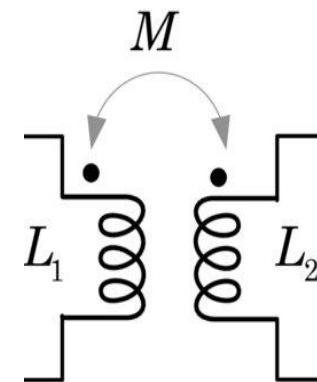
Key Relationship:

$$V_1 = -N_1 \frac{d\Phi}{dt}$$

$$V_2 = M \frac{di_1}{dt}$$

$$k = \frac{M}{\sqrt{L_1 L_2}}$$

$$M = k \sqrt{L_1 L_2}$$



1.2 IDEAL TRANSFORMER MODEL

An ideal transformer assumes perfect coupling ($k = 1$), zero winding resistance, infinite core permeability, no frequency limits, and no losses. These core equations provide the foundation for all transformer circuit calculations, with corrections applied for non-idealities as necessary.

Key Relationship:

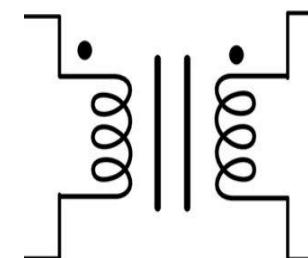
$$N = \frac{N_2}{N_1}$$

$$\frac{V_2}{V_1} = N$$

$$\frac{I_2}{I_1} = \frac{1}{N}$$

$$Z_2 = N^2 Z_1$$

$$N_1 : N_2$$



1.2 TWO-INDUCTOR → TRANSFORMER

Two magnetically coupled inductors can always be described by transformer equations. Each winding experiences voltage not only from its own self-inductance but also from the changing current in the other (mutual inductance). By arranging the coupled inductor equations, standard transformer relationships emerge. The turns ratio that matches primary and secondary inductance is the square root of their ratio, a key parameter in all transformer calculations.

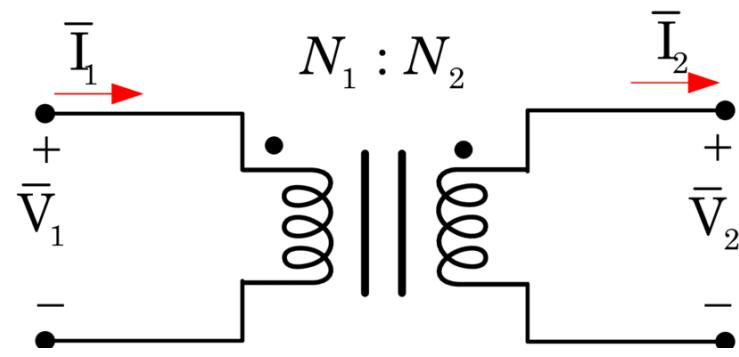
Key Relationship:

$$V_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$

$$V_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}$$

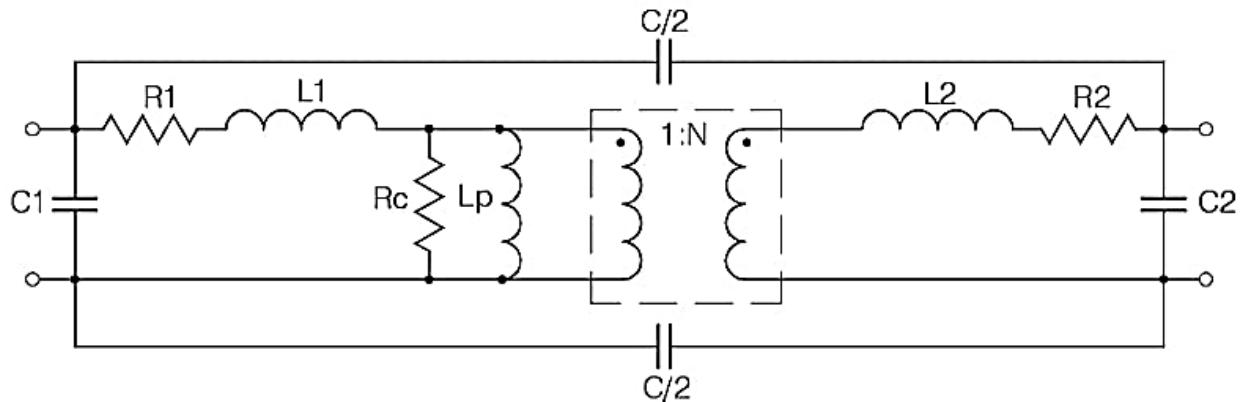
$$M = k \sqrt{L_1 L_2}$$

$$N = \sqrt{\frac{L_2}{L_1}}$$



Chapter 2: Non-Ideal Transformer Model

2.1 EQUIVALENT CIRCUIT



Primary Side:

- $C_1 \rightarrow$ Coupling or termination capacitor (used for AC coupling).
- $R_1 \rightarrow$ Winding resistance of the primary (copper loss).
- $L_1 \rightarrow$ Leakage inductance of the primary (flux that doesn't couple to secondary).
- $R_c \rightarrow$ Core loss resistance – represents eddy current + hysteresis losses in the magnetic core.
- $L_p \rightarrow$ Magnetizing inductance – models the main mutual flux path linking both windings.

Transformer Core:

- $1:N \rightarrow$ Ideal transformer with turns ratio $N = \frac{N_s}{N_p}$.
- Transfers voltage/current between primary and secondary ideally (no loss).

Secondary Side

- $L_2 \rightarrow$ Leakage inductance of the secondary winding.
- $R_2 \rightarrow$ Secondary winding resistance (copper loss).
- $C_2 \rightarrow$ Load coupling or termination capacitor.

$C/2$ (Middle Path)

- Two $C/2$ capacitors represent distributed interwinding capacitance or AC coupling paths.
- Sometimes they model midpoint DC blocking or symmetry in AC-coupled circuits
- The magnetizing branch (R_c and L_p) is where flux balance happens.
- Any DC offset or imbalance in applied voltage causes net volt-seconds across L_p (flux Drift \rightarrow Saturation)

Parameter	Symbol	Represents	Typical Value / Range
Primary resistance	R_1	Copper loss (primary winding)	$10 \text{ m}\Omega - 1 \Omega$
Primary leakage	L_1	Uncoupled primary flux	$100 \text{ nH} - 10 \mu\text{H}$
Core loss resistance	R_c	Core hysteresis + eddy losses	$10 \text{ k}\Omega - 1 \text{ M}\Omega$
Magnetizing inductance	L_p	Main mutual flux path	$0.1 \text{ mH} - 100 \text{ mH}$
Turns ratio	$1:N$	Voltage/current scaling	Application-specific (e.g., 1:1 – 1:10)
Secondary leakage	L_2	Uncoupled secondary flux	$100 \text{ nH} - 10 \mu\text{H}$
Secondary resistance	R_2	Copper loss (secondary winding)	$10 \text{ m}\Omega - 1 \Omega$
Coupling capacitors	$C/2$	AC-coupling / symmetry caps	$0.01 \mu\text{F} - 1 \mu\text{F}$
External coupling caps	C_1, C_2	Input/output coupling	$0.1 \mu\text{F} - 10 \mu\text{F}$

2.2 PARAMETER MEASUREMENT AND EXTRACTION

To accurately model a real transformer, the equivalent circuit parameters must be extracted from standardized tests:

Open-Circuit Test:

With the secondary winding open, apply rated voltage to the primary. This measures core loss resistance R_c and magnetizing inductance L_p , captured from input current and power under no-load conditions. It reflects iron losses and magnetizing current.

Short-Circuit Test:

With the secondary shorted, a reduced voltage is applied to the primary to circulate full-load current. This test gives the copper loss resistances R_1, R_2 and leakage inductances L_1, L_2 , evident by voltage drop and power dissipation under load.

Winding Resistance Measurement:

Direct measurement of primary and secondary DC resistances using a four-wire meter accurately quantifies copper loss components R_1, R_2 separately.

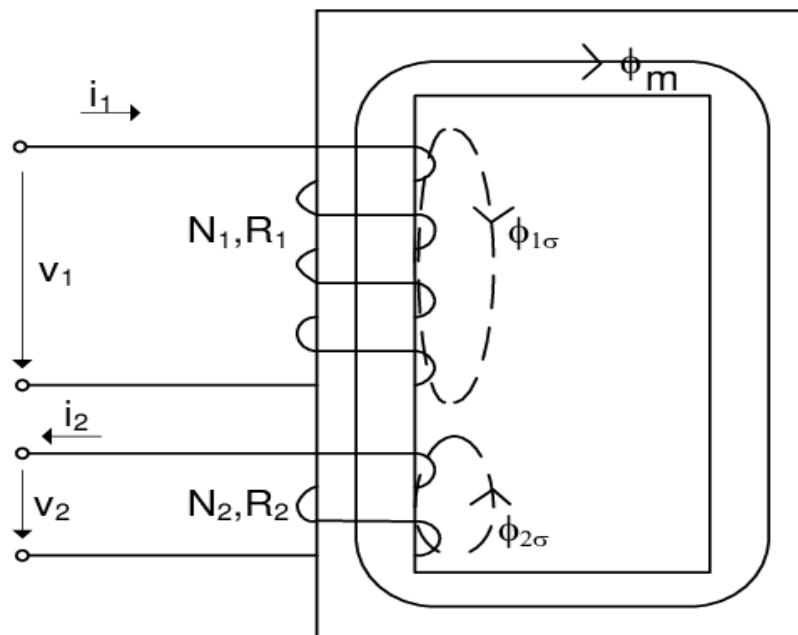
Frequency Dependence:

Note that L_p, L_1 , and L_2 have frequency dependence; skin and proximity effects increase equivalent resistance and inductive reactance, which can be accounted for in detailed designs.

2.3 EFFECTS OF NON-IDEALITIES ON TRANSFORMER PERFORMANCE

Understanding the practical impact of non-ideal elements aids design optimization:

- Copper Losses (R_1, R_2) reduce efficiency and cause temperature rise
- Leakage Inductances (L_1, L_2) reduce voltage regulation precision, introduce voltage spikes in switching (EMI).
- Core Loss Resistance (R_c) directly impacts no-load losses and heat generation.
- Magnetizing Inductance (L_p) represents the transformer's ability to sustain mutual flux
- Interwinding Capacitance ($C/2$) introduces high-frequency parasitic pathways, limiting transformer BW.
- AC Coupling Capacitors (C_1, C_2) serve functions such as DC blocking and noise filtering.
-

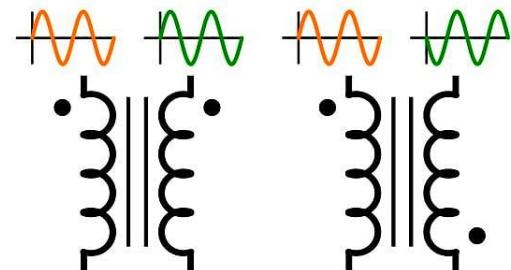


Chapter 3: Dot Convention and Phase Relationships

3.1 DOT NOTATION STANDARDS

Dot convention is the formal system for indicating the polarity of transformer windings, showing which terminals will exhibit the same instantaneous voltage polarity. This ensures proper phase alignment and prevents feedback errors. By convention, current entering the dotted end on the primary leaves the dotted end on the secondary.

- Dots at matching terminals indicate in-phase voltages.
- Reversing a dot produces a 180° phase shift.



3.2 PHASE RELATIONSHIPS

In-phase (0°) relationships result when both primary and secondary connect their dots to the same voltage potential; out-of-phase (180°) means the dot numbering is reversed. The correct configuration depends on circuit topology: most isolation transformers require in-phase coupling, while push-pull and flyback designs use out-of-phase.

Key Relationship:

$$V_2 = \pm NV_1$$

For time-varying voltage, phase shift between windings is generally negligible except at extremely high frequencies or with substantial core lag.

Time Dependency:

$$V_2(t) = NV_1(t - \Delta t)\varphi = 360^\circ f \Delta t$$

3.3 REVERSED DOT CONSEQUENCES

Improper dot orientation leads to phase errors, destabilizing feedback amplifiers and creating shoot-through in push-pull converters. In rectifier outputs, reversal can cause large voltage overshoot, reverse conduction of diodes, and destruction of output polarity.

3.4 ADDITIVE VS SUBTRACTIVE COUPLING

Series-aiding (additive) and series-opposing (subtractive) winding connections are used to manage voltage summation or difference, with the dot orientation dictating whether voltages add or subtract.

Add & Subtract:

$$V_{total, aiding} = V_1 + V_2, L_{total} = L_1 + L_2 + 2M$$

$$V_{total, opposing} = V_1 - V_2, L_{total} = L_1 + L_2 - 2M$$

Configuration	Voltage Sum	Inductance	Application
Aiding	V_1+V_2	L_1+L_2+2M	Autotransformer
Opposing	V_1-V_2	L_1+L_2-2M	Differential mode

Chapter 4: Impedance Transformation

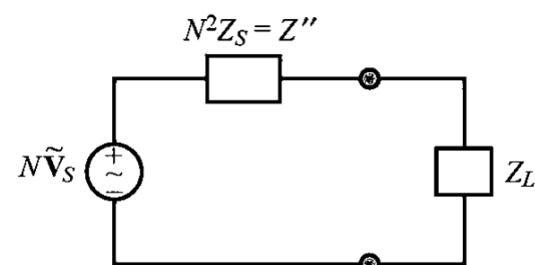
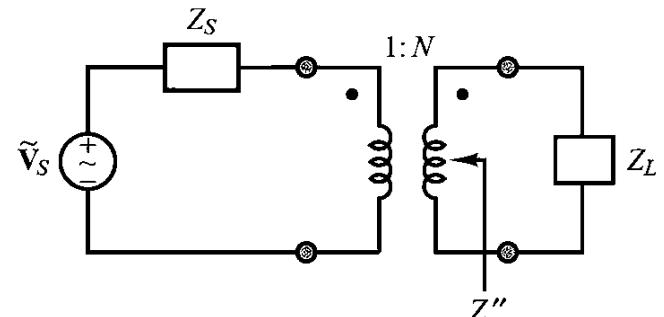
4.1 IMPEDANCE REFLECTION

A fundamental property of transformers is their ability to reflect an impedance from secondary to primary, scaled by the square of the turns ratio. This allows for matching load impedances to sources for optimal power transfer. The design target is often to select a turns ratio that matches the source and load for either maximum power or maximum efficiency, according to application priorities.

Reflection Parameter Calculation:

$$Z_{\text{reflected}} = N^2 Z_s, \quad N = \frac{N_2}{N_1}$$

$$N_{\text{opt}} = \sqrt{\frac{Z_{\text{source}}}{Z_{\text{load}}}}$$



4.2 MULTI-WINDING CONFIGURATIONS

Transformers with more than two windings (multi-secondary or multi-primary) are common in advanced designs. Voltage division among windings is determined by their respective turns ratios relative to the primary.

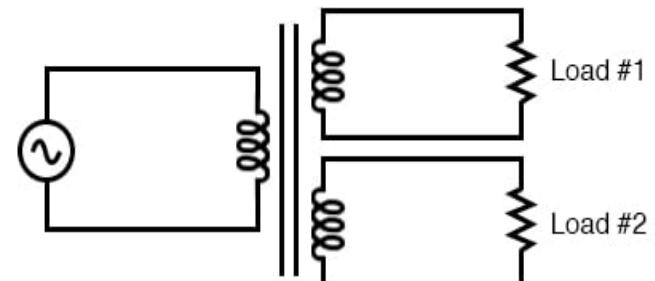
Key Relationship:

$$V_k = \frac{N_k}{N_1} V_1 N_1 I_1 = \sum_k N_k I_k$$

$$V_1 I_1 = \sum_k V_k I_k + P_{\text{loss}}$$

Matrix methods of multi-terminal transformers

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}$$



where the off-diagonal (mutual) elements are $Z_{ij} = j\omega M_{ij}$.

Parameter	Symbol	Range
Turns ratio	N_k/N_1	0.1-10
Multi-winding eff.	η	85-98%
Cross-regulation	$\Delta V\%$	2-10%
Power split acc.	(±%)	5-15%

4.3 POWER BALANCE EQUATIONS

For accurate analysis, input and output powers must be balanced, with explicit allocation to copper loss and core loss. Each winding's copper loss is a function of current squared times resistance, and core loss depends on flux density, frequency, and core material.

Power Equations:

$$P_{in} = V_1 I_1 \cos \varphi_1$$

$$P_{out} = \sum_{k=2}^n V_k I_k \cos \varphi_k$$

$$P_{loss} = \sum_k I_k^2 R_k + P_{core}$$

$$P_{core} = K_h f B_{max}^\alpha + K_e f^2 B_{max}^2$$

Transformer loss calculation formula

$$\text{Efficiency} = \frac{\text{Power Output}}{\text{Power Input}} = \frac{P_s}{P_p} \times 100$$

$$\text{Efficiency} = \frac{\text{Power Output}}{\text{Power Output} + \text{Copper Loss} + \text{Core Loss}} \times 100$$

$$\text{Efficiency} = \frac{V_s I_s \times \text{PF}}{(V_s I_s \times \text{PF}) + \text{Copper Loss} + \text{Core Loss}} \times 100$$

Chapter 5: Core Material Selection

5.1 MATERIAL PERMEABILITY COMPARISON

Core material choice targets maximum efficiency within designer constraints of frequency, cost, size, and flux.

- Ferrite: Preferred in high-frequency, low-core-loss applications
- Powder Iron: Good for DC-biased and wideband circuit
- Silicon Steel, Amorphous, Nanocrystalline: Best for low-frequency, high-flux needs

Material	μ_r	Freq Range	B _{sat} (T)	Relative Cost
MnZn Ferrite	1500–3000	10k–500kHz	0.35–0.50	Low
NiZn Ferrite	100–800	100k–100MHz	0.20–0.40	Low
Powder iron	10–100	DC–10MHz	0.80–1.20	Low
Silicon steel	1.5k–5k	50–1kHz	1.8–2.0	Medium
Nanocrystalline	50k–100k	10k–1MHz	1.2–1.3	Very high

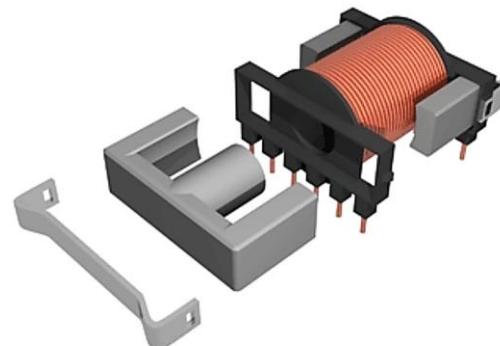
5.2 CORE LOSS COMPONENTS

Core losses result from two mechanisms: hysteresis (reversal of domains with each AC cycle) and eddy currents (induced currents opposing magnetization). The standard Steinmetz equation predicts total core loss as a function of frequency and flux density.

Core Loss:

$$P_{core} = K_h f^\alpha B_{max}^\beta \cdot Vol$$

- Where:
- K_h : material constant
- α : frequency exponent (1.0–2.0 typical)
- β : flux exponent (2.6–2.8 typical)



5.3 SELECTION CRITERIA TABLE

Material choice is dictated by required frequency, flux density, and acceptable loss. Manufacturing data can be used to interpolate core loss densities at the application's working point (typically given in mW/cm³ or W/kg).

Frequency	Material Choice	B _{sat}	μ_r	Core Loss @ 0.1T
50–60Hz	Silicon steel	1.8–2.0	3000	1–2 W/kg
1–10kHz	Amorphous	1.5–1.6	5000	0.5–1 W/kg
10–100kHz	MnZn ferrite	0.35–0.50	2000	50–150 mW/cm ³
100k–1MHz	NiZn ferrite	0.20–0.40	300	100–300 mW/cm ³
1–10MHz	NiZn/powder	0.3–0.8	50	200–500 mW/cm ³
>10MHz	Powder iron	0.8–1.2	20	300–800 mW/cm ³

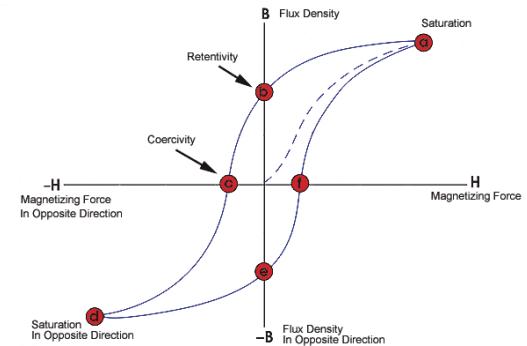


Chapter 6: Core Saturation and Flux Management

6.1 B-H CURVE CHARACTERISTICS

Transformer core behavior is fundamentally nonlinear, described by its B-H (magnetic flux density vs. magnetizing force) curve. Each material has a characteristic saturation flux density, beyond which permeability collapses and the transformer loses its inductive properties. Safe design limits the working flux (B_{op}) to 60-80% of B_{sat} , depending on core geometry, thermal conditions, and reliability requirements.

Core Material	B_{sat} (T)	Relative μ (μ_r)	Freq Range
Silicon steel	1.8-2.0	1500-5000	50-400 Hz
Ferrite (MnZn)	0.3-0.5	1500-3000	10 kHz-1 MHz
Ferrite (NiZn)	0.2-0.4	100-800	1-100 MHz
Amorphous	1.5-1.6	2000-10,000	50 Hz-10 kHz



6.2 SATURATION CONSEQUENCES

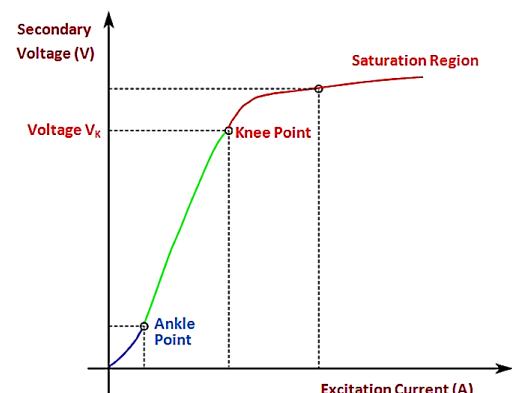
When the transformer core is driven into saturation, its inductance collapses, the magnetizing current rises sharply, and severe waveform distortion occurs. The immediate effects include loss of voltage transformation, generation of current spikes, and the onset of harmonics or system instability.

Saturation dramatically reduces transformer effectiveness and may cause catastrophic circuit failure.

Inductance at Saturation:

$$L_{sat} = L_{initial}/\mu_r$$

$$THD = \sqrt{\sum V_n^2}/V_1 \times 100\%$$



6.3 FLUX BALANCE REQUIREMENTS

For AC-coupled, switching, or pulse transformer circuits, the net volt-seconds balanced on each cycle is critical. Any offset (such as excessive DC or flux imbalance) causes unidirectional core excitation—eventually driving the core into saturation. Commonly, flux reset techniques such as dedicated reset windings, active clamp circuits, or resonant methods are employed to ensure reliable operation and maintain flux symmetry.

Volt-Second Balance:

$$\int_0^T V(t)dt = 0$$

Chapter 7: Efficiency and Loss Calculation

7.1 LOSS BREAKDOWN

Transformer losses consist primarily of copper losses (winding resistance) and core losses (magnetic hysteresis and eddy current losses). Copper loss includes both DC and AC resistance components, as AC losses increase due to skin and proximity effects. Copper loss is calculated using the RMS winding current and frequency-dependent resistance.

Power & Core Losses:

$$P_{cu,dc} = I_{rms}^2 R_{dc}$$

$$P_{cu,ac} = I_{rms}^2 R_{ac}(f)$$

$$P_{core} = K_f \cdot f^\alpha \cdot B_{pk}^\beta \cdot Vol$$

$$P_{loss} = P_{cu,pri} + P_{cu,sec} + P_{core}$$

7.2 EFFICIENCY CALCULATION

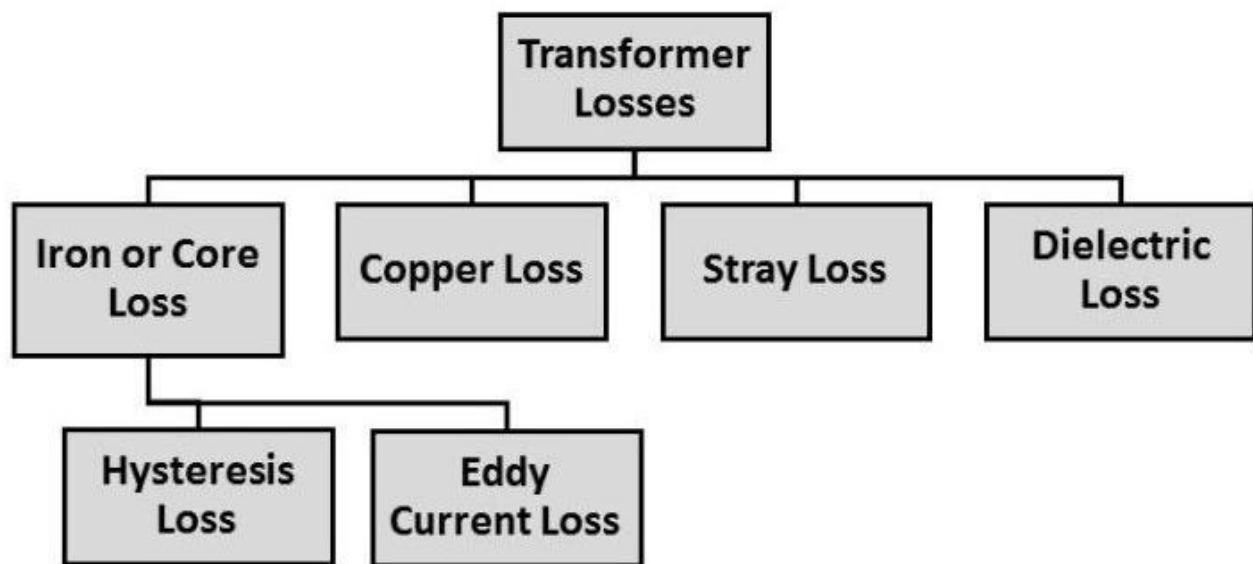
Efficiency (η) is the ratio of output power to total input power, accounting for losses. Individual efficiency components reveal the fraction lost in copper (η_{cu}) and core (η_{core}). Efficiency vs. load curves typically peak at 30–60% load, where copper and core losses balance.

Efficiency (core and Copper):

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \times 100\%$$

$$\eta_{cu} = 1 - \frac{P_{cu}}{P_{out} + P_{loss}}$$

$$\eta_{core} = 1 - \frac{P_{core}}{P_{out} + P_{loss}}$$



Chapter 8: Frequency Domain Behavior

8.1 TRANSFER FUNCTION DERIVATION

Transformer frequency response is governed by its inductive, capacitive, and resistive elements. At low frequencies, magnetizing inductance (L_m) dominates and acts as a high-pass filter with a roll-off set by the load resistance. At high frequencies, leakage inductance (L_l) and parasitic capacitance (C_w) set an upper roll-off, often producing filter or resonant behavior.

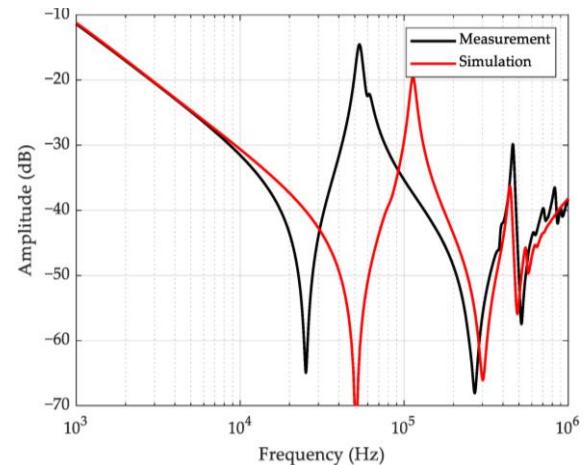
Transfer and Cutoff:

$$H(s) = N \frac{sL_m}{sL_m + R_{load}}$$

$$f_{low} = \frac{R_{load}}{2\pi L_m}$$

$$H(s) = \frac{N}{1 + s^2 L_l C_w + s R C_w}$$

$$f_{high} = \frac{1}{2\pi\sqrt{L_l C_w}}$$



8.2 BANDWIDTH DETERMINATION

The transformer's passband, determined by the lower (f_{low}) and upper (f_{high}) cutoff frequencies, marks the region with flat transmission and minimal attenuation. Below f_{low} , the output drops due to insufficient magnetizing current; above f_{high} , losses rise rapidly due to parasitics.

Bandwidth and Frequency Dependency:

$$BW = f_{high} - f_{low}$$

8.3 ATTENUATION CHARACTERISTICS

Frequency-dependent attenuation outside the flat-band region follows predictable slopes:

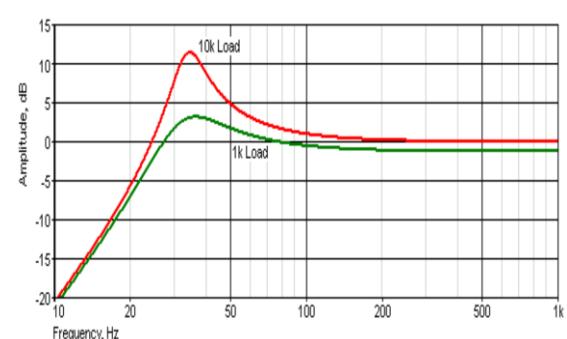
- Below the low-frequency cutoff, attenuation increases at +20dB/decade.
- Above the high-frequency cutoff, single-pole slopes are -20dB/decade; parasitic capacitance can steepen this to -40 dB/decade.

Attenuation vs Freq.

$$\text{Attenuation}_{f < f_{low}} = 20 \log_{10} \left(\frac{f}{f_{low}} \right) \text{ dB}$$

$$\text{Attenuation}_{f > f_{high}} = 20 \log_{10} \left(\frac{f_{high}}{f} \right) \text{ dB}$$

Freq Region	Element	Slope	Phase
$f \ll f_{low}$	L_m	+20dB/dec	+90°
$f_{low} < f < f_{high}$	Ideal/LI, R_w	0 dB	0°--10°
$f \gg f_{high}$	L_l, C_w	-40dB/dec	-180°
$f \sim f_{SRF}$	C_w, L_p	Resonant	0°



Chapter 9: SMPS Isolated Topologies

9.1 FLYBACK CONVERTER

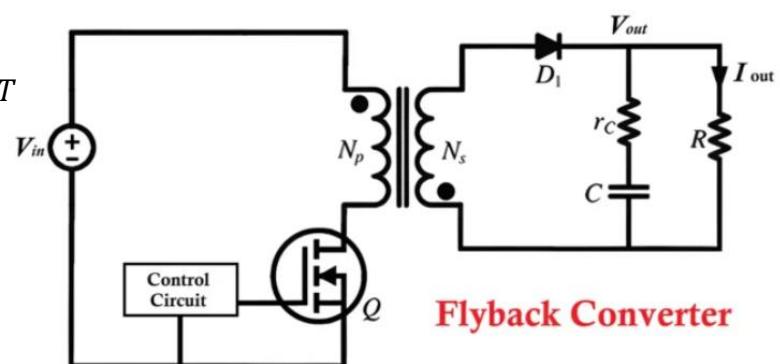
The key feature of a Flyback Converter transformer is that it operates as a coupled inductor that stores energy, which necessitates the opposite dot convention (180° out of phase) between the primary and secondary windings. During the "ON" cycle when the primary switch (like a MOSFET) is closed, voltage is applied to the primary winding, causing current to ramp up and energy to be stored in the core's air gap; the opposing dot on the secondary winding forces the induced voltage to be negative, which reverse-biases the output diode, preventing energy transfer to the load and ensuring energy storage. Conversely, during the "OFF" cycle when the primary switch opens, the magnetic field collapses, causing the voltage polarity across both windings to reverse (the "flyback" action), which now forward-biases the secondary diode, allowing the stored energy to be released and transferred to the output.

Volt-second balance:

$$V_{in} \cdot D \cdot T = (V_{out} \cdot N + V_f) \cdot (1 - D) \cdot T$$

Output voltage:

$$V_{out} = \frac{V_{in} \cdot D}{N \cdot (1 - D)} - V_f$$



9.2 FORWARD CONVERTER

The key feature of a Forward Converter transformer is that it acts as a traditional transformer, transferring energy from the primary to the secondary winding while the primary switch is ON. To facilitate this energy transfer, the primary (N_p) and secondary (N_s) windings must share the same dot convention.

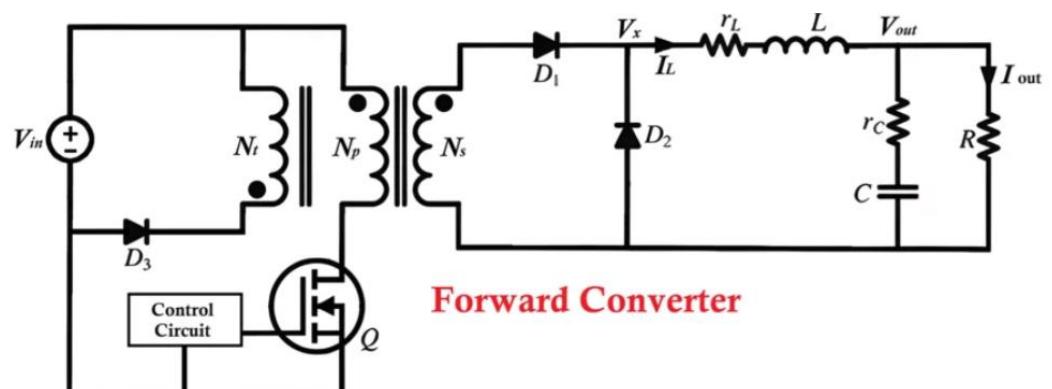
During the "ON" cycle, voltage is applied to N_p , and the resulting induced positive voltage on N_s forward-biases the main rectifier diode (D_1), sending energy to the output LC filter and load. Conversely, when the switch opens for the "OFF" cycle, the transformer must be reset; the voltage polarity reversal causes the dedicated reset winding (N_t), which has the opposite dot convention, to forward-bias its associated diode (D_3), safely returning the stored magnetizing energy to the input source and preventing core saturation.

Reset winding ratio:

$$\frac{N_s}{N_t} \geq \frac{D}{1 - D}$$

Reset voltage:

$$V_{reset} = V_{in} \cdot \frac{N_s}{N_t}$$

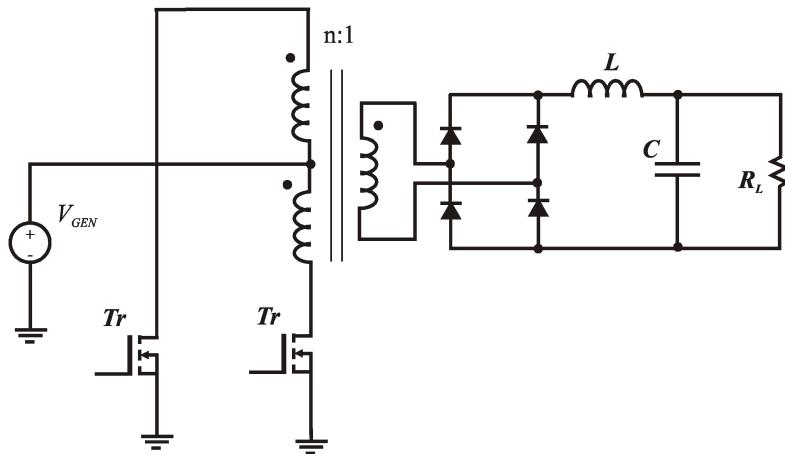


9.3 PUSH-PULL TOPOLOGY

The key feature of a Push-Pull Converter transformer is that it has a center-tapped primary winding and is driven symmetrically by two switches (Tr), which allows the transformer to operate as AC transformer with bi-directional core excitation. This design provides symmetrical volt-second balance over each cycle, inherently avoiding unidirectional flux accumulation and core saturation. During the "ON" cycles, the two switches are driven alternately; when one switch is closed, voltage is applied to one half of the primary, inducing a voltage in the secondary via a standard in-phase dot convention, which then rectifies the power to the output filter (L and C). Conversely, when the first switch opens, the second switch closes, applying the voltage in the opposite direction across the primary winding, which fully utilizes the core by driving the flux in the negative direction.

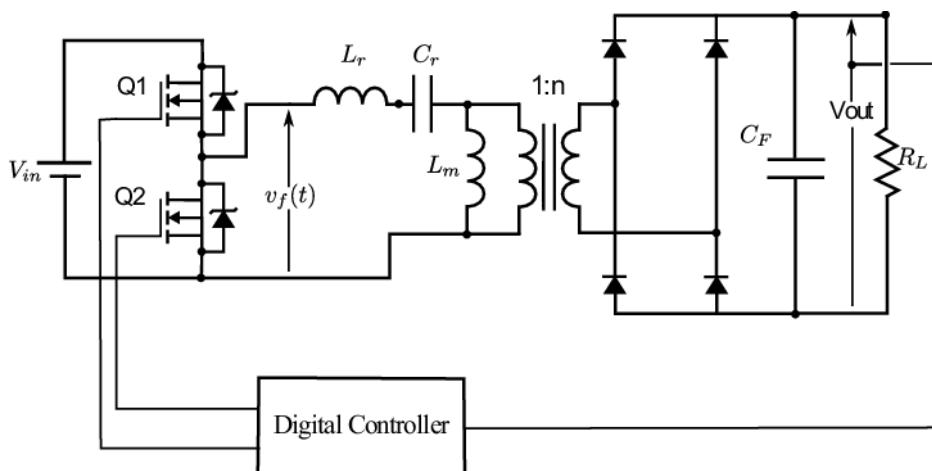
Flux accumulation:

$$\Delta B(n) = \Delta B(n - 1) + \frac{V_{GEN}(D_1 - D_2)T}{N \cdot A_e}$$



9.4 HALF-BRIDGE (LLC)

The key feature of the Resonant LLC Converter transformer is that it operates as part of a resonant tank (L_r , C_r , and the magnetizing inductance L_m) to achieve highly efficient soft-switching conditions. It uses a transformer core operating in the AC regime with a standard in-phase dot convention for efficient power transfer [Implied logic]. By switching at or near its resonant frequency, the circuit allows the primary switches ($Q1$ and $Q2$) to turn ON at Zero-Voltage Switching (ZVS), dramatically reducing switching losses and enabling high-frequency operation and high power density.



Chapter 10: Signal and RF Applications

10.1 IMPEDANCE MATCHING

Transformers provide impedance transformation according to turns ratio squared, facilitating conjugate impedance matching for maximum power transfer in RF and signal circuits.

Resonant frequency:

$$Z_{in} = N^2 Z_{out}$$

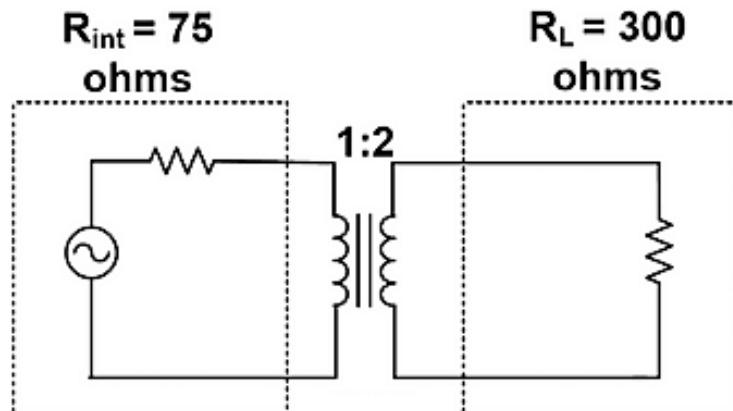
$$N = \sqrt{\frac{Z_{in}}{Z_{out}}}$$

Reflection coefficient:

$$\Gamma = \frac{Z_{load} - Z_{source}}{Z_{load} + Z_{source}}$$

Return loss (dB):

$$RL = -20 \log_{10} |\Gamma|$$



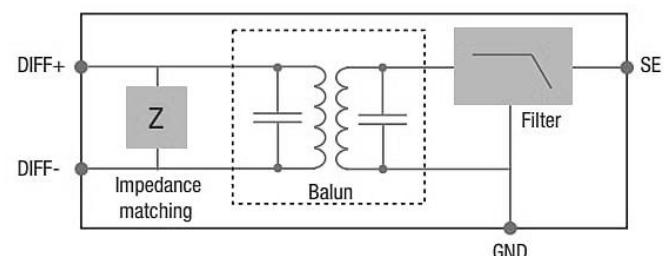
10.2 BALUN CONFIGURATIONS

Baluns convert unbalanced to balanced signals, common in RF front ends. Standard configurations include 1:1 and 4:1 impedance ratios achieved via turns ratios or transmission line transformers.

Common Mode Rejection Ratio:

$$CMRR = 20 \log_{10} \left(\frac{V_{diff}}{V_{common}} \right)$$

Typical CMRR values range from 30 to 60 dB.



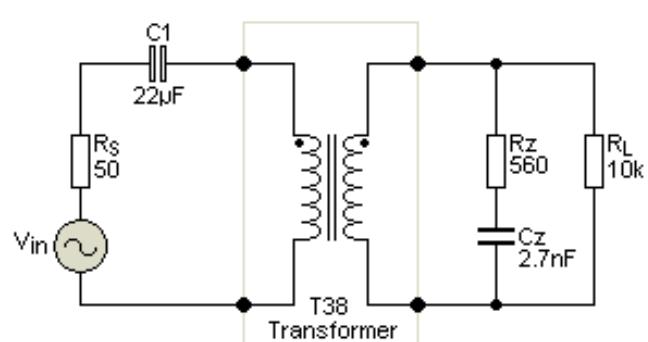
10.3 AUDIO TRANSFORMERS

Audio transformers cover the full audible band (20 Hz – 20 kHz) and require very low distortion. Total Harmonic Distortion & Noise: (THD+N) is specified for application classes. Bandwidth and frequency response flatness specifications ensure clarity and fidelity appropriate to microphone, line, or output stages.

Harmonic Distortion & Noise:

$$THD + N = \frac{\sqrt{\sum V_n^2 + V_{noise}^2}}{V_1} \times 100\%$$

Application	THD+N (%)	Bandwidth (Hz)
Microphone	<0.05	20-20k
Line Level	<0.1	20-50k
Output (SS)	<0.01	5-50k



Chapter 11: Isolation and Sensing

11.1 CURRENT TRANSFORMERS (CT)

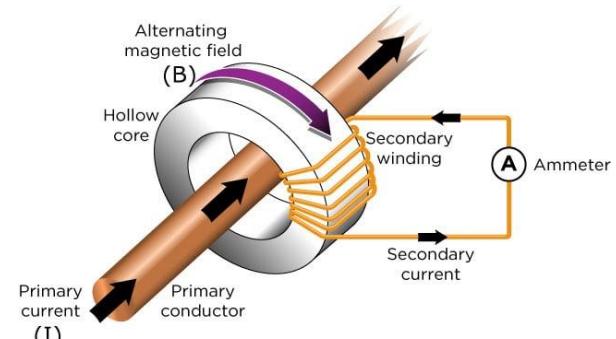
CTs provide isolated current measurement by inducing a proportional voltage across a burden resistor. Accuracy depends on phase shift, bandwidth, and saturation limits. The secondary must never be open-circuited to avoid dangerous voltages.

Voltage Output:

$$V_{out} = \frac{I_{primary}}{N} \cdot R_{burden}$$

Phase error:

$$\phi = \arctan\left(\frac{\omega L_m}{R_{burden}}\right)$$

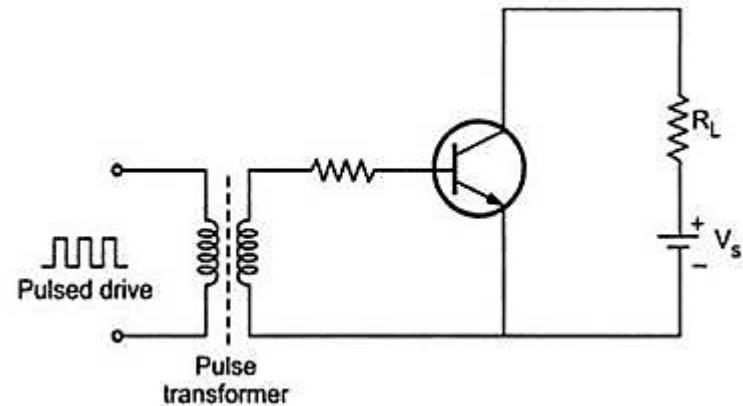


11.2 PULSE TRANSFORMERS

Require very fast rise times and minimal droop for clean pulse fidelity. Output rise time degradation relates to leakage inductance and load capacitance.

Rise Time Degradation:

$$t_{r,out} = \sqrt{t_{r,in}^2 + (2.2 \cdot L_l \cdot C_{load})^2}$$



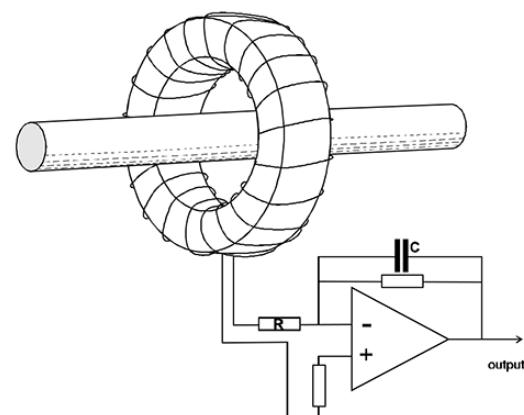
11.3 ROGOWSKI COIL

Air-core Rogowski coils provide derivative measurements of current with wide bandwidth and saturation immunity. The coil output voltage is proportional to the rate of change of current, requiring an integrator for actual current reconstruction.

Output Voltage and Current:

$$V_{out} = M \frac{di}{dt}$$

$$I(t) = \frac{1}{M} \int V_{out} dt$$



Chapter 12: Transformer Design - Part 1

12.1 DESIGN SPECIFICATION CAPTURE

Before selecting any components, establish complete electrical and mechanical requirements. Incomplete specifications lead to costly iterations and potential field failures.

Electrical Requirements:

- Input voltage range (min/nominal/max): e.g., 90-265 VAC or 48 VDC $\pm 10\%$
- Output voltage(s) and tolerance: e.g., 12V $\pm 5\%$, 5V $\pm 3\%$
- Output current per winding (continuous and peak)
- Operating frequency: 50/60 Hz, 20 kHz, 100 kHz, 1 MHz, etc.
- Duty cycle (for switching applications): typically 0.3-0.7 for flyback, <0.5 for forward
- Isolation voltage requirement: 1.5 kV, 3 kV, 4 kV per safety standards

Thermal and Environmental:

- Ambient temperature range: -40°C to +85°C typical
- Maximum allowable temperature rise: $\Delta T = 40^\circ\text{C}$ typical, 60°C max
- Cooling method: natural convection, forced air, liquid cooling
- Altitude and humidity conditions

Physical Constraints:

- Maximum height/width/depth (PCB clearance)
- Mounting orientation and method
- Weight limitations

Regulatory:

- Safety standards: UL, IEC, CSA requirements
- EMI compliance: EN 55011, FCC Part 15
- Agency approvals needed

Key Relationship - Power Throughput:

$$P_{out} = \sum_{k=2}^n V_k I_k$$

$$P_{in} = \frac{P_{out}}{\eta_{est}}$$

Where η_{est} is estimated efficiency (start with 0.85-0.92 for initial sizing).

12.2 CORE MATERIAL SELECTION

Core selection determines transformer size, losses, and cost. Wrong core choice leads to saturation/excessive loss.

Step 1: Determine Operating Frequency Range

Frequency Range	Preferred Core Material	Why
50-400 Hz	Silicon steel, Amorphous	High B_{sat} (1.5-2.0 T), low cost
1-20 kHz	Amorphous, MnZn ferrite	Balance of B_{sat} and core loss
20-200 kHz	MnZn ferrite (3C90, 3F3)	Low core loss, adequate B_{sat}
200 kHz-1 MHz	NiZn ferrite, MnZn ferrite	High frequency, moderate loss
>1 MHz	NiZn ferrite, powder iron	Very high frequency capability

Step 2: Calculate Required Core Size

Core Size Calculation:

$$A_p = A_w \cdot A_e$$

Where:

A_w = window area available for windings (cm^2)

A_e = effective core cross-sectional area (cm^2)

Area Product Calculation:

$$A_p = \frac{P_{out}}{K_u \cdot K_f \cdot f \cdot B_{max} \cdot J}$$

Where:

K_u = window utilization factor (0.3-0.5 typical, 0.4 good target)

K_f = waveform factor (4.0 for square wave, 4.44 for sine wave)

f = operating frequency (Hz)

B_{max} = maximum flux density (T), typically 0.25-0.35 T for ferrite

J = current density (A/mm^2), typically 3-5 A/mm^2 for natural cooling



Example:

Design a 50W flyback transformer at 100 kHz:

$$A_p = \frac{50}{0.4 \cdot 4.0 \cdot 100,000 \cdot 0.3 \cdot 4} = \frac{50}{192,000} = 0.26 \text{ cm}^4$$

Select core with $A_p \geq 0.26\text{cm}^4$.

Step 3: Core Geometry Selection

Common core shapes and their characteristics:

Core Type	Advantages	Disadvantages	Best For
E-E cores	Easy winding, bobbin available	Moderate coupling	General purpose, SMPS
E-I cores	Low cost, standard sizes	Air gap control difficult	Line frequency, audio
Toroid	Best coupling ($k>0.98$), self-shielding	Difficult to wind, no bobbin	High efficiency, RF
Pot core	Excellent shielding, good coupling	Higher cost, limited sizes	Low EMI requirements
Planar	Low profile, PCB mount	Complex manufacturing	High current, low voltage

12.3 AIR GAP SELECTION

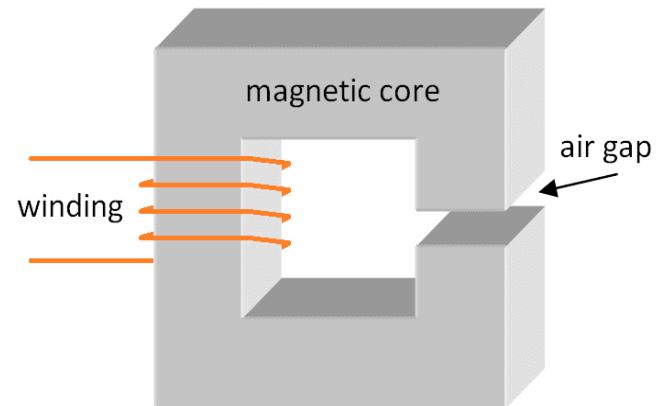
Air gaps are required in most power transformers to prevent saturation and store energy.

When Air Gap is Needed:

- DC current flows through winding (flyback, forward with DC bias)
- Energy storage is required (flyback, boost, buck-boost)
- Tight inductance tolerance needed ($\pm 5\%$ or better)

When Air Gap is NOT Needed:

- Pure AC coupling (audio, signal transformers)
- Full-bridge, half-bridge with symmetric drive
- Current transformers (CT)



Air Gap Length Calculation:

$$l_g = \frac{\mu_0 \cdot N^2 \cdot A_e}{L} - \frac{l_e}{\mu_r}$$

Where:

$$\mu_0 = 4\pi \times 10^{-7} \text{ H/m}$$

l_e = effective magnetic path length (from core datasheet)

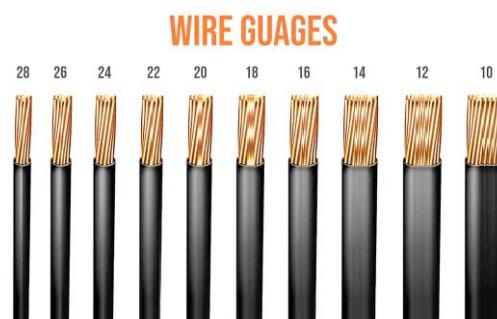
μ_r = relative permeability of core material

12.4 WIRE GAUGE AND CURRENT DENSITY SELECTION

Proper wire sizing balances copper loss, thermal rise, and winding fill factor.

Current Density Guidelines:

Cooling Method	Curr Density (A/mm ²)
Natural convection	2.5-4.0
Moderate airflow	4.0-6.0
Forced air cooling	6.0-10.0
Liquid cooling	10.0-20.0



Wire Area Calculation:

$$A_{wire} = \frac{I_{rms}}{J}$$

Common wire gauges for power transformers:

AWG	Diameter (mm)	Area (mm ²)	Max Current @ 4 A/mm ²
18	1.02	0.823	3.3 A
20	0.812	0.519	2.1 A
22	0.644	0.326	1.3 A
24	0.511	0.205	0.82 A
26	0.405	0.129	0.52 A
28	0.321	0.081	0.32 A

Chapter 13: Transformer Design - Part 2

13.1 PRIMARY TURNS CALCULATION

Primary turns determine operating flux density and must prevent core saturation.

Primary Turns Calculation:

$$N_1 = \frac{V_1}{4.44 \cdot f \cdot B_{max} \cdot A_e}$$

Where:

- V_1 = RMS primary voltage
- 4.44 = form factor for sine wave
- f = line frequency (50 or 60 Hz)
- B_{max} = peak flux density (0.8-1.5 T for silicon steel)
- A_e = effective core area (cm^2)

Example:

230 VAC, 50 Hz, E-I core with $A_e = 2.5 \text{ cm}^2$, $B_{max} = 1.3 \text{ T}$

Primary Turns Calculation:

$$N_1 = \frac{230}{4.44 \cdot 50 \cdot 1.3 \cdot 2.5} = \frac{230}{722.5} = 318 \text{ turns}$$

For Flyback Converter:

$$N_1 = \frac{V_{in,min} \cdot D_{max} \cdot 10^8}{2 \cdot f \cdot B_{max} \cdot A_e}$$

Where:

- D_{max} = maximum duty cycle (typically 0.4-0.5)
- B_{max} = 0.25-0.35 T for ferrite
- A_e in cm^2

Design Procedure:

1. Calculate minimum input voltage: $V_{in,min} = V_{nominal} \cdot 0.9$ (for 10% ripple)
2. Select $D_{max} = 0.45$ (safe starting point)
3. Choose $B_{max} = 0.3 \text{ T}$ (conservative for ferrite)
4. Calculate N_1
5. Verify saturation margin with peak current

For Forward Converter:

$$N_1 = \frac{V_{in,min} \cdot D_{max} \cdot 10^8}{f \cdot \Delta B \cdot A_e}$$

Where ΔB = flux swing (typically 0.2-0.3 T).

13.2 SECONDARY TURNS CALCULATION

Secondary turns are determined by voltage ratio and must account for losses.

Ideal Turns Ratio:

$$N_2 = N_1 \cdot \frac{V_{out} + V_{drops}}{V_{in}}$$

Where V_{drops} includes:

- Diode forward drop: 0.4-1.0 V (Schottky to standard)
- Winding resistance drop: $I_{out} \cdot R_{sec}$ (estimate 2-5% of V_{out})
- PCB trace resistance: typically 0.1-0.3 V

For Flyback Secondary:

$$N_2 = N_1 \cdot \frac{V_{out} + V_f}{V_{in,min} \cdot D_{max}} \cdot (1 - D_{max})$$

Multiple Secondary Outputs:

For each output:

$$N_k = N_1 \cdot \frac{V_{out,k} + V_{f,k}}{V_{in}}$$

13.3 INDUCTANCE CALCULATION AND VERIFICATION

Primary Inductance (Flyback):

$$L_m = \frac{V_{in,min}^2 \cdot D_{max}}{2 \cdot f \cdot P_{out}}$$

Example:

$V_{in,min} = 36$ V, $D_{max} = 0.45$, $f = 100$ kHz, $P_{out} = 30$ W

Inductance Calculation:

$$L_m = \frac{36^2 \cdot 0.45}{2 \cdot 100,000 \cdot 30} = \frac{583.2}{6,000,000} = 97\mu H$$

Verify with Turns and Gap:

$$L_m = \frac{\mu_0 \cdot N_1^2 \cdot A_e}{l_g}$$

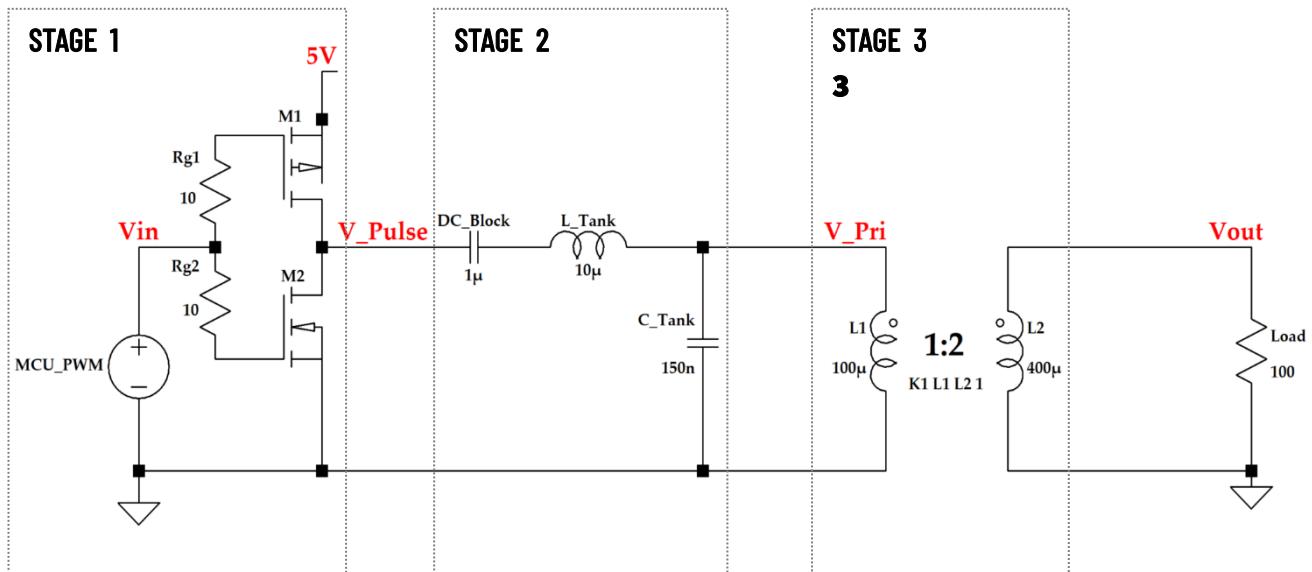
Rearrange to find required gap:

$$l_g = \frac{\mu_0 \cdot N_1^2 \cdot A_e}{L_m}$$

Chapter 14: LTSpice Simulation

14.1 DIRECT DIGITAL SYNTHESIS CIRCUIT

The following Circuit is a sine generator (DDS). Pulses are fed by MCU to dictate the frequency and the analog part Takes care of the Current and Voltage Amplification. The Transformer is placed to double the voltage and isolate the input from load (100Ω). In summary, DDS function : **Pulse In → Sine Out.**



14.2 CIRCUIT STAGES

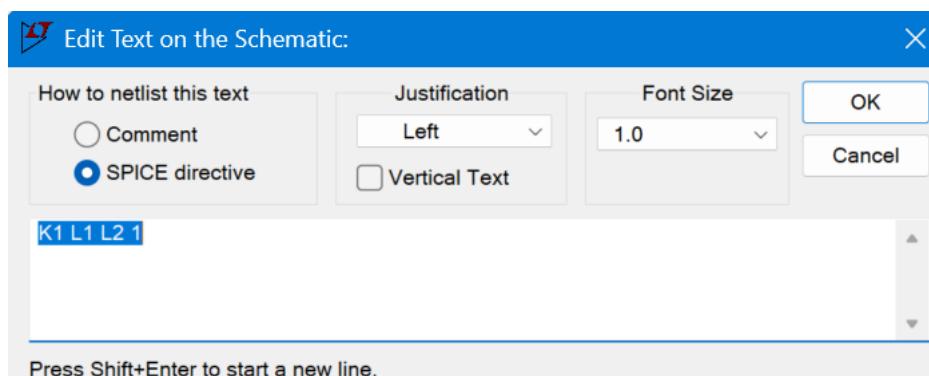
This circuit is divided to stages.

- Stage 1: Pulse Level Shifting $3.3V \rightarrow 5V$
- Stage 2: DC Blocking and LC Tank Resonant
- Stage 3: Transformation of 1:2

14.3 LTSPICE TRANSFORMER SETUP (QUICK STEPS)

1. Place two inductors → name them L1, L2.
2. Set inductances → e.g. L1=100uH, L2=400uH (for 1:2 Ratio).
3. "T" Open up the Spice Directive Box: Put this phrase: K1 L1 L2 1
4. Set Resistance and Capacitance of each inductor (Specification or datasheet)

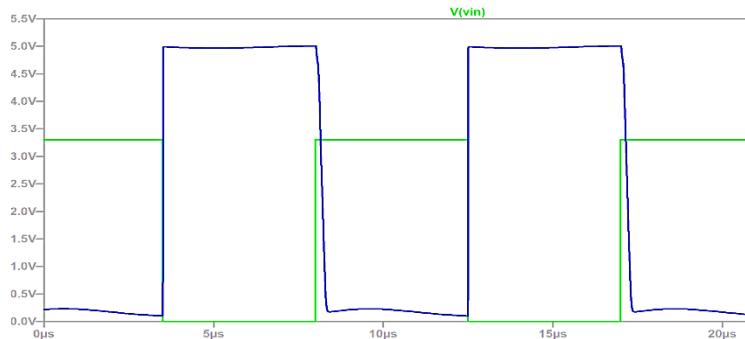
* Pay Attention to the Dot Alignment - They must be both Up or Both Down



14.4 SIMULATION RESULTS

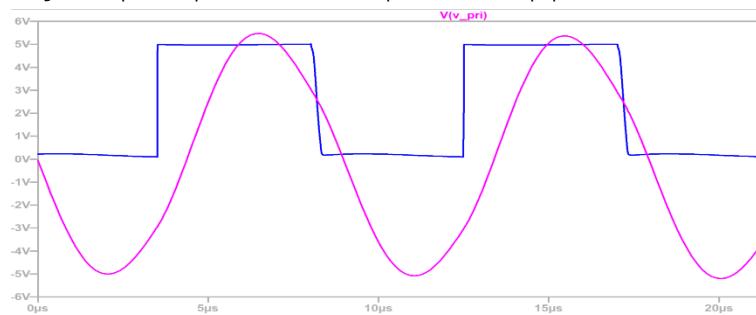
The signal starts as a pulse and ends as high voltage high current sinewave. Let's check each stage transition :

Stage 1: Input: V_{in} {0-3.3}V Output: V_{pulse} {0-5}V



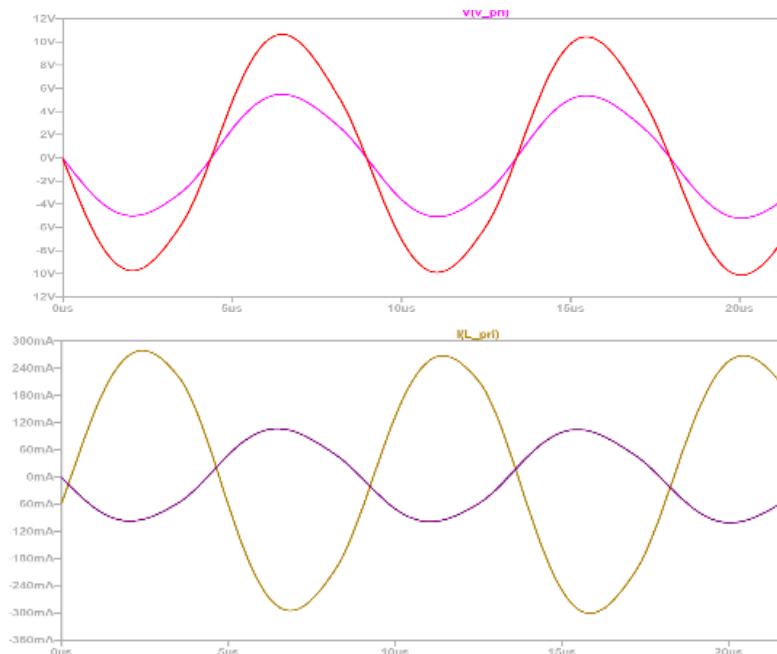
Level Shift
Pulse Voltage increases
 $3.3V \rightarrow 5V$
Current is amplified

Stage 2: Input: V_{pulse} {0-5}V Output: V_{Pri} {5Vptp}sine



DC Block Filter
LC Tank ("BPF" filter)
Pulse → Sine

Stage 3: Input: V_{Pri} {5Vptp}sine Output: V_{out} {10Vptp}sine



Voltage and current show opposite behavior between Pri & Sec :
 $V_{pri} < V_{sec}$
 $I_{pri} > I_{sec}$
The current should maintain the same ratio (2:1), but the Transformer is not Ideal in the simulation.

Chapter 15: Design Notes

15.1 CORE & MAGNETIC

- Choose a core grade with low $P_{core}(f, B)$ – power savings matter above 100 kHz.
- Always check the datasheet's recommended winding window occupancy.
- Test a ferrite magnet after winding: weak stick means possible cracks.
- When margining, verify temperature at installer's ambient, not lab.
- Add a round to your turns if insulation thickness is above 1 mm.
- For gapped cores, overgap by 10% then trim after bench test – real flux leaks.

15.2 ELECTRICAL

- Place safety margins in both voltage and isolation spec—UL creepage/clearance.
- For split primary designs, ensure secondary matches both centertaps.
- Star ground measurement during short-circuit testing to avoid ground loops.
- Use voltage probe with smallest tip. Big probe = dirty waveform.
- Always simulate winding inductance with $\pm 10\%$ real-world tolerance.

15.3 MECHANICAL

- Secure bobbin edges with additional hot-glue for vibration-prone systems.
- Validate terminal spacing vs. solder blob—avoid shorts by layout, not luck.
- Press down every winding with a plastic tool after layer complete—flat packs matter.
- Choose wire insulation by system max voltage $\times 3$ for safety.
- Use shrink tubes on exposed leads, even when inside enclosure.

15.4 DEBUG & VALIDATION

- Check for “singing” at high load—acoustic noise = poor attachment or resonance.
- Test with ESR meter after assembly to catch shorts.
- When output ripple jumps under load, inspect for winding shorts or insulation breach.
- Try thermal imaging after overnight load, not just 10 min—creep failures show later.
- Mark measured primary and secondary inductance values, not just simulated ones.

15.5 PRODUCTION & TESTING TIPS

- Run a pass/fail functional test for every batch—catch early build errors fast.
- Use quick insulation resistance testers; log values by batch lot for traceability.
- Add a sticker or stamp to each tested unit—visual trace for QA.
- Record first failure mode seen in production—helpful for process tuning.

Chapter 16: Smart Design Tools

16.1 ONLINE TOOLS (FREE)

Purpose	Tool / Method	Quick Use Tip
Core Selection	Ferroxcube Core Selector	Enter frequency above nominal: aging margin
Wire Gauge	Omnicalc, RapidTables	For >10 A, cross-check with IEC tables
Inductance Estimate	Coil32, EEWeb	Include wire length, not just turns
Winding Fill	Cu Fill Factor via Litz Opt	For >50%, use multifilar
Temp Rise	Schmidt Calculator, KEMET	Add heatsinking area, not just core dissipation
Creepage/Isolation	UL's Pathfinder, IEC Wizard	Check for slot/vent edge cases

16.2 DESIGN SHORTCUTS

- Sheet shortcut: Calculate all losses, divide by output power - If >0.12, redesign.
- Winding ratio estimate: $N_{pri}/N_{sec} = V_{pri}/V_{sec}$ - rounds up for margin.
- Measure wire pack width, multiply by thickness; divide by bobbin area.
- If the design needs more than two winding fixes, re-spec the core.
- Compare datasheet area product vs. calculated required A_p . Must exceed by 10%.
- Wind one test transformer with 20% more leakage, test peak volt at probe. If lower, rerun EMI sim.

16.3 SMART SYSTEM HABITS

- Build your own mini database - save all test results by core type.
- When a prototype fails, record both fix and reason in review table.
- Always tag sample with build date and iteration count; helps trace issues.
- Group datasheets by material, not just part number.
- For large OEM projects, request manufacturer's application notes for similar builds.
- Capture test results with phone photo - visual logs catch future issues.
- Re-measure winding resistance after soldering, not just winding.

16.4 MATERIAL SELECTION & BOM OPTIMIZATION

- Use a shared spreadsheet for BOM tracking—flag substitutions and shortages early.
- Always check cross-references for core and wire; flexibility kills line stops.
- Track lead times on specialty insulation—supply chain delays can halt projects.
- Prefer materials stocked locally for prototypes—saves weeks on re-builds.
- Log cost-per-unit for every design round—see the real impact of tool choices.