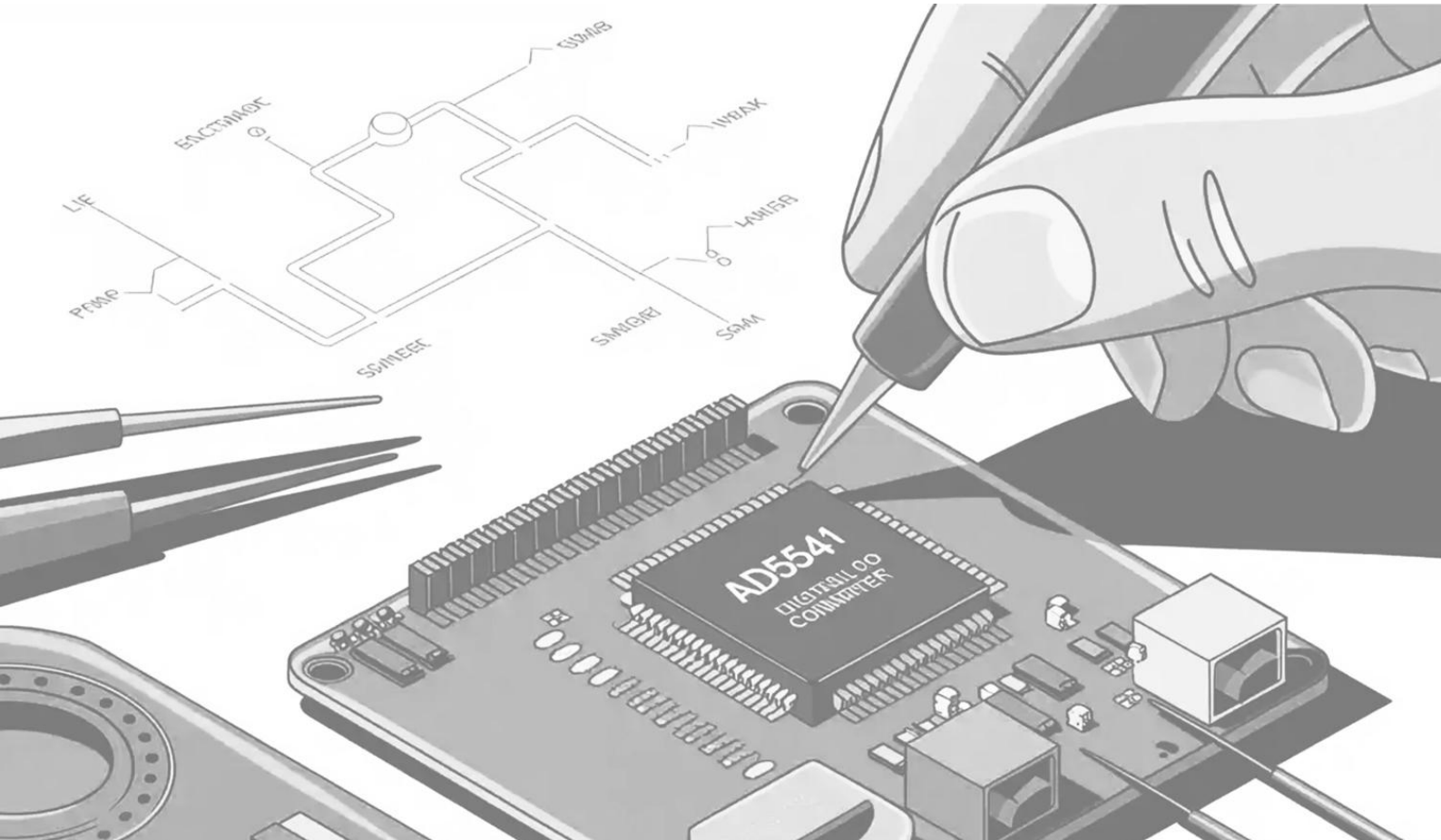
Hardware Engineer's Guide

TroubleShooting

By Shimi Cohen



INTRODUCTION

1.1 BOOK PURPOSE

This guide provides systematic approaches to troubleshooting assembled PCBs. It targets board designers who need practical solutions for common and complex hardware failures.

1.2 HOW TO USE THIS GUIDE

Start with Chapter 3 for immediate symptom identification. Use Chapter 4 for specific debug flows based on your symptoms. Reference Chapter 6 for advanced isolation techniques when standard approaches fail.

EACH SECTION INCLUDES:

- Real-world examples
- Step-by-step procedures
- Tool requirements
- Expected results

1.3 PCBA STAGES

Prototype

First PCBAs to arrive after new design. These boards should be tested comprehensively against the spec and components datasheet. Most issues should be found in this stage

First Batch

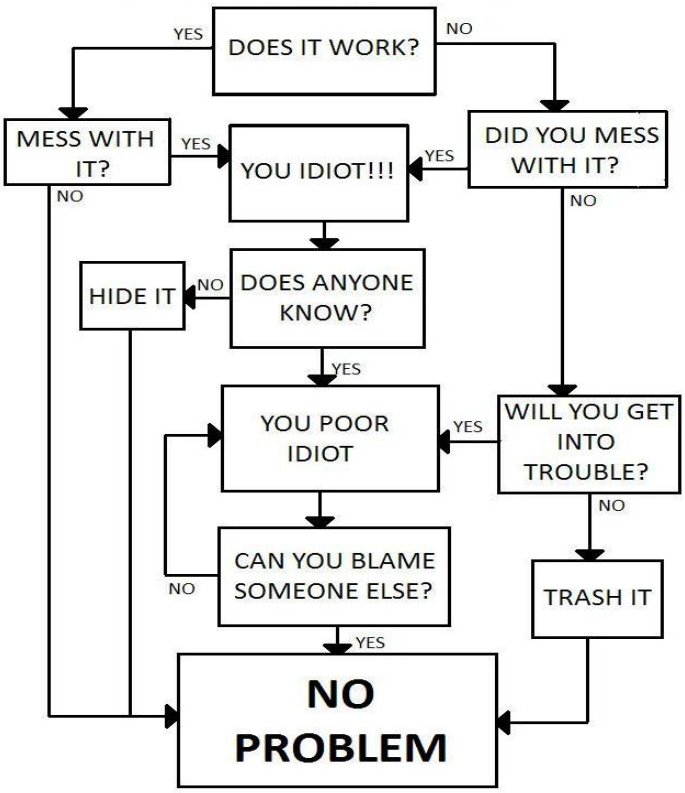
This spin should mitigate all problems found in prototypes. To reduce risks small batch is produced before mass production. These boards should be tested for corners and functional problem.

This phase require a deeper test including modes, scenarios and Environmental tests.

Production

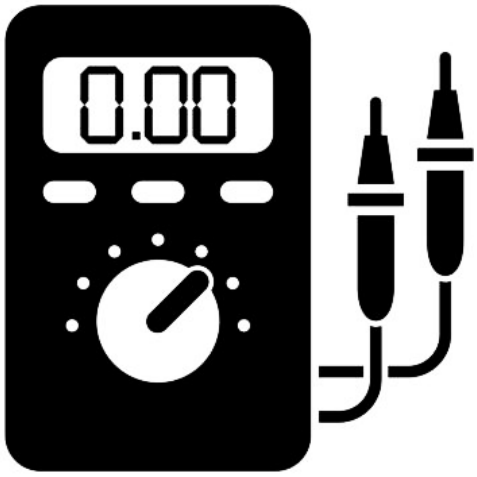
End of Line tests are done by percentage because most major issues should be resolved already.

This phase allows comparing different systems and using Goldens for reference.



PREPARING FOR DEBUG

2.1 TOOLS & EQUIPMENT



Essential Tools for Basic Debugging

Every troubleshooting session requires a core set of instruments.

MULTIMETER REQUIREMENTS:

- True RMS capability for AC measurements
- 10A current measurement range
- Continuity beeper with <50Ω threshold

OSCILLOSCOPE SPECIFICATIONS:

- Minimum 100MHz bandwidth for digital circuits
- 4 channels for complex signal analysis
- 1GSa/s sample rate minimum
- Math functions for power calculations

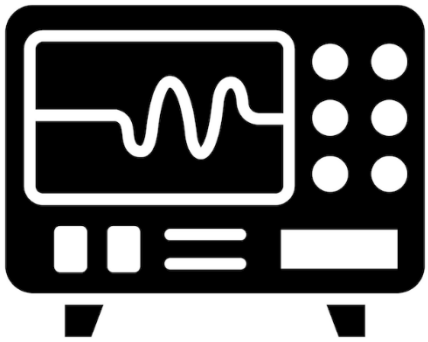
Advanced Debug Equipment

LOGIC ANALYZER SETUP:

- 16+ channels for bus analysis
- Protocol decode capability (SPI, I2C, UART)
- Saleae Logic Pro 16 recommended for mixed-signal work

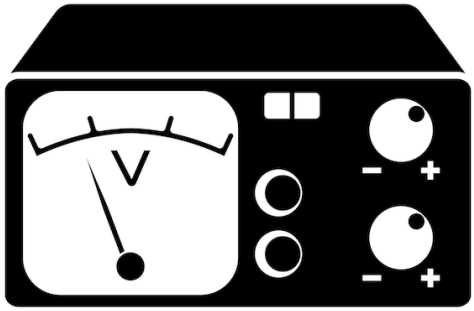
POWER SUPPLY REQUIREMENTS:

- Variable voltage 0-30V, 3A minimum
- Current limiting with 1mA resolution
- Keysight E3631A or Rigol DP832A suitable options



THERMAL IMAGING:

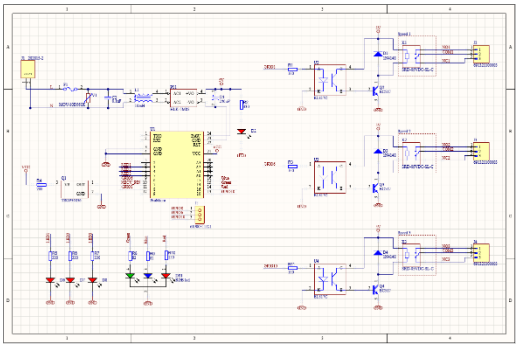
- FLIR E8-XT for component-level thermal analysis
- 0.1°C temperature resolution
- Essential for power dissipation troubleshooting



2.2 SCHEMATICS & DATASHEETS

Schematic Analysis Fundamentals

Before touching the board, understand the design intent. Identify critical paths and potential failure.



POWER DISTRIBUTION ANALYSIS:

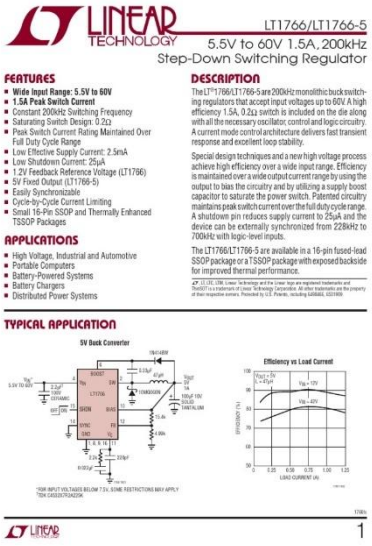
- Trace power flow from input to each IC
- Identify switching regulators vs linear regulators
- Note power sequencing requirements

SIGNAL PATH VERIFICATION:

- Follow clock distribution networks
- Identify critical timing paths
- Note impedance-controlled signals

Datasheet Critical Parameters

Focus on parameters that directly relate to failure modes.


LINEAR TECHNOLOGY

LT1766/LT1766-5

5.5V to 60V 1.5A, 200kHz Step-Down Switching Regulator

FEATURES

- Wide Input Range: 5.5V to 60V
- 1.5A Peak Switch Current
- Constant 200kHz Switching Frequency
- Saturating Switch Design: 0.2Ω
- Peak Switch Current Rating Maintained Over Full Duty Cycle Range
- Low Effective Supply Current: 2.5mA
- Low Shutdown Current: 25μA
- 1.2V Feedback Reference Voltage (LT1766)
- 5V Fixed Output (LT1766-5)
- Easily Synchronizable
- Cycle-by-Cycle Current Limiting
- Small 16-Pin SSOP and Thermally Enhanced TSSOP Packages

DESCRIPTION

The LT®1766/LT1766-5 are 200kHz monolithic buck switching regulators that accept input voltages up to 60V. A high efficiency 1.5A, 0.2Ω switch is included on the die along with all the necessary oscillator, control and logic circuitry. A current mode control architecture delivers fast transient response and excellent loop stability.

Special design techniques and a new high voltage process achieve high efficiency over a wide input range. Efficiency is maintained over a wide output current range by using the output to bias the circuitry and by utilizing a supply boost capacitor to saturate the power switch. Patented circuitry maintains peak switch current over the full duty cycle range. A shutdown pin reduces supply current to 25μA and the device can be externally synchronized from 228kHz to 700kHz with logic-level inputs.

The LT1766/LT1766-5 are available in a 16-pin fused-lead SSOP package or a TSSOP package with exposed backside for improved thermal performance.

APPLICATIONS

- High Voltage, Industrial and Automotive
- Portable Computers
- Battery-Powered Systems
- Battery Chargers
- Distributed Power Systems

TYPICAL APPLICATION

5V Buck Converter

Efficiency vs Load Current

1

FOR MICROCONTROLLERS:

- Absolute maximum ratings (especially VDD, input voltages)
- Power consumption specifications (active, sleep modes)
- I/O characteristics (VOH, VOL, IIH, IIL)
- Reset and clock requirements

FOR POWER MANAGEMENT ICS:

- Output voltage accuracy and regulation
- Current limit thresholds
- Thermal shutdown temperature
- Enable/disable logic levels

2.3 SAFETY AND HANDLING

ESD Protection Protocols

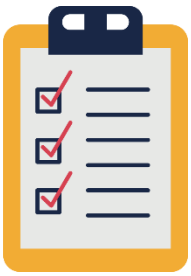
ESD damage often creates intermittent failures that are difficult to diagnose.

REQUIRED PRECAUTIONS:

- Wrist strap connected to earth ground
- ESD mat rated for electronics work
- Ionizing fan for sensitive component areas
- Humidity control 40-60% RH when possible

Power Safety Considerations

High-current circuits pose safety risks and can cause additional damage if handled improperly.



SAFETY CHECKLIST:

- Power off before making connections
- Use insulated probes rated for circuit voltages
- Implement current limiting during initial power-up
- Keep fire extinguisher (Class C) accessible for electrical fires

INITIAL INSPECTION

3.1 VISUAL INSPECTION TECHNIQUES

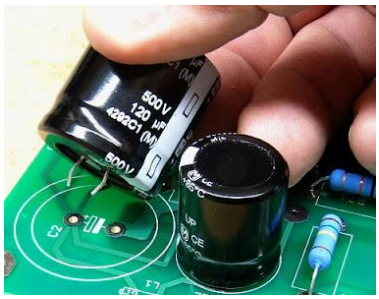
Visual inspection reveals 60% of assembly defects. Systematic examination prevents time wasted on complex measurements when simple assembly errors exist.

Component Placement Verification

Check component orientation before applying power. Reversed ICs often create permanent damage.

CRITICAL COMPONENTS TO VERIFY:

- Electrolytic capacitors (polarity markings)
- Diodes and LEDs (cathode band orientation)
- ICs (pin 1 indicators and dot markings)
- Connectors (keying and pin assignments)

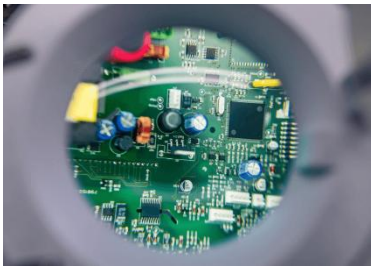


Solder Joint Quality Assessment

Poor solder joints cause 40% of field failures. Recognize good vs problematic joints before electrical testing.

GOOD SOLDER JOINT CHARACTERISTICS:

- Concave fillet shape
- Shiny, smooth finish
- Complete wetting to both pad and component
- No excess solder creating bridges



PROBLEMATIC JOINT INDICATORS:

- Dull, grainy appearance (cold joint)
- Excessive solder creating bridges
- Insufficient solder (partial wetting)
- Component lifted off pads (tombstoning)

Component Damage Assessment

Look for obvious physical damage that indicates handling problems or design stress issues.

DAMAGE INDICATORS:

- Cracked ceramic capacitors
- Bent or missing component leads
- Burned components (brown/black discoloration)
- Bulging electrolytic capacitors

3.2 RECOGNIZING EARLY FAILURE SIGNS

VCC and GND Shorts

Before power-up it is fundamental to check if VCC and GND are properly separated.

NO-POWER SHORT TESTS

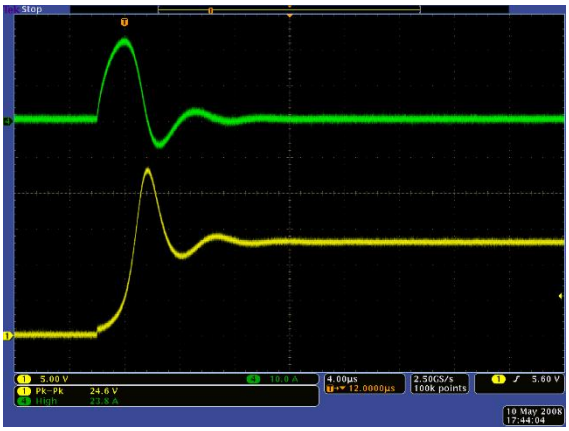
- Find all VCC and GND vias and conductors
- Check for resistance between them
- VCC and GND resistance must be high (>hundreds Ohm)
- Check resistance between different VCCs (not shorts between different rail)
- If GNDs should be separated – check resistance between them

Current Draw Analysis

Abnormal current consumption indicates design problems or component failures.

CURRENT ANALYSIS METHOD:

- Measure total system current
- Compare to design calculations
- Identify high-current subsystems
- Look for current spikes during operation



Thermal Indicators

Component overheating often precedes complete failure. Early thermal detection prevents permanent damage.

TEMPERATURE MONITORING:

- Touch test for excessive heat (>65°C feels hot)
- Thermal imaging for precise measurements
- Monitor ambient vs component temperature rise

NORMAL OPERATING TEMPERATURES:

Component Type	Maximum Safe Temperature
Linear regulators	85°C case temperature
Switching regulators	100°C case temperature
Microcontrollers	75°C case temperature
Power MOSFETs	125°C junction (calc from case temp)

3.3 FUNCTIONAL POWER AND SIGNAL CHECKS

Initial Power-Up Sequence

Never apply full power immediately. Use current-limited supply to prevent damage from shorts or design errors.

POWER-UP PROTOCOL

- Set current limit to 50mA initially
- Apply power and monitor current draw
- Check for immediate current limiting
- Measure key voltage rails before increasing current limit

EXPECTED RESULTS:

- Current should stabilize below limit
- Primary voltage rails should reach target values
- No components should become warm immediately

Voltage Rail Verification

Verify power rails reach correct voltages under no-load conditions. This isolates P.S issues from load-related.

MEASUREMENT POINTS:

- Power supply outputs (at regulator pins)
- Load points (at IC power pins)
- Reference voltages (at precision components)

TOLERANCE GUIDELINES:

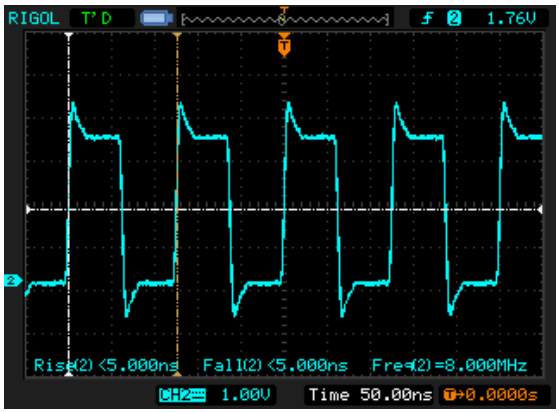
Rail Type	Acceptable Tolerance
Digital logic (3.3V, 5V)	±5%
Analog references	±1%
Power amplifier supplies	±10%

Clock Signal Verification

Clock failures prevent all digital operation. Check clock signals early in the debug process.

CLOCK VERIFICATION STEPS:

- Measure frequency with frequency counter
- Check signal amplitude (should reach logic levels)
- Verify duty cycle (typically 50% ±10%)
- Look for jitter using oscilloscope persistence mode



DEBUG FLOWS

4.1 BOARD NOT FUNCTIONAL

Power Supply and Voltage Verifications

When a board shows no signs of life, start with power supply analysis.

STEP 1: INPUT POWER VERIFICATION

- Measure input voltage at connector
- Verify polarity matches schematic
- Measure input current with known good supply

STEP 2: POWER SUPPLY IC ANALYSIS

- Check enable signals (logic levels)
- Verify reference voltages (typically 1.2-2.5V)
- Check feedback network resistor values

STEP 3: LOAD ANALYSIS

- Measure power supply output with no load
- Gradually reconnect loads
- Identify which load causes power supply failure

Clock Signal Debug Flow:

CRYSTAL OSCILLATOR CIRCUITS

- Measure crystal resistance (typically 10-100Ω)
- Check load capacitor values against Datasheet
- Look for excessive loading on clock output

EXTERNAL CLOCK SOURCES

- Verify clock source power supply
- Check clock enable/disable controls
- Test for clock signal integrity issues

RESET SIGNAL ANALYSIS

- Measure reset assertion time during power-up
- Check for reset supervisor IC proper operation
- Test manual reset button functionality

Common Fault Sources and Resolutions

ASSEMBLY ERRORS:

- Wrong component values (especially crystals, resistors)
- Reversed polarity components (diodes, electrolytic caps)
- Missing components (often small value resistors)
- Bridged pins on fine-pitch ICs

DESIGN ISSUES:

- Insufficient power supply current capability
- Incorrect power sequencing
- Missing pull-up/pull-down resistors
- Crystal load capacitor mismatch

COMPONENT FAILURES:

- Defective power management ICs
- Non-programmed MCU
- Damaged MCU (ESD or overvoltage)
- Open fuses or protection devices

4.2 OVERHEATING COMPONENT

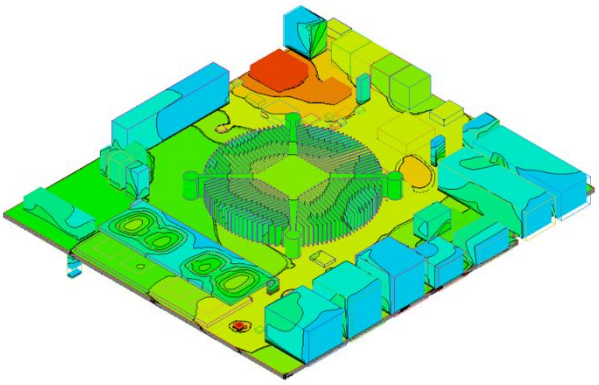
Diagnosing Short Circuits and Overcurrent

Component overheating typically indicates excessive current flow. Identify the current path causing the problem.

Systematic Overcurrent Analysis:

STEP 1: POWER SUPPLY CURRENT MONITORING

- Measure current on each power rail separately
- Compare to design calculations
- Look for current spikes during operation
- Use current probe for high-frequency current measurement



STEP 2: THERMAL MAPPING

- Use thermal camera to identify hot spots
- Check component temperatures under no-load
- Monitor temperature vs time during operation
- Compare similar components for temperature differences

STEP 3: SHORT CIRCUIT LOCALIZATION

- Power down and measure resistance between power rails
- Use low-voltage ohmmeter (avoid forward-biasing semiconductors)
- Apply voltage limiting (0.5V max) during resistance measurement
- Check for shorts at connector pins

Example:

STM32F103 microcontroller overheating during normal operation

INITIAL SYMPTOMS:

- MCU case temperature >85°C after 30 seconds
- System operates normally for 60-90 seconds before failure
- No obvious visual damage to components

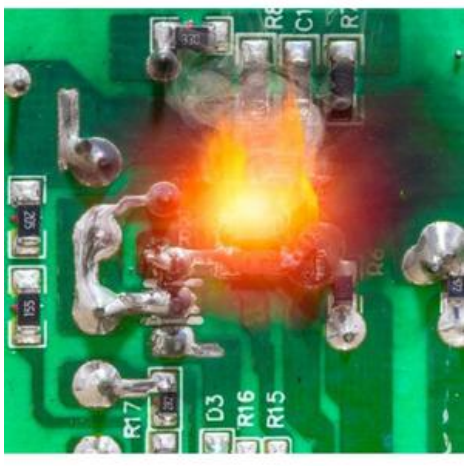
Debug Process:

STEP 1: POWER SUPPLY ANALYSIS

- 3.3V rail measured 3.31V (within tolerance)
- MCU current draw: 150mA (expected: 25mA max)
- Other components on 3.3V rail: 15mA total

STEP 2: PIN-BY-PIN ANALYSIS

- GPIO pins A0-A7 (5V tolerant) configured as outputs in software
- Hardware schematic shows PA4 connected to external 5V logic
- PA4 driving against 5V creates ~50mA current through protection diode



STEP 3: RESOLUTION

- Modified software to configure PA4 as open-drain output
- Added external pull-up resistor to 5V rail
- MCU current reduced to 28mA, temperature normal

LESSONS LEARNED:

- Always verify I/O voltage compatibility
- Consider protection diode current paths
- Use open-drain outputs for mixed voltage interfacing

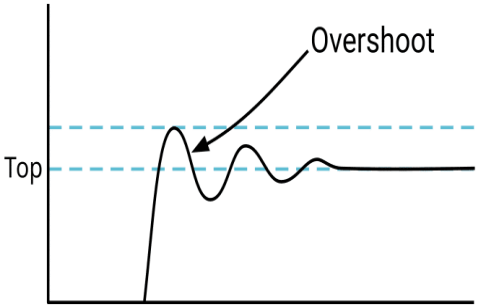
4.3 COMMUNICATION PROBLEMS

Signal Integrity and Interface Testing

Communication failures often result from signal integrity issues, Test physical layer before analyzing protocols.

VOLTAGE LEVEL CHECKING:

- Measure logic high and low voltages
- Compare to receiver input thresholds
- Check for proper termination on differential signals
- Verify common-mode voltage on differential pairs



SIGNAL QUALITY ASSESSMENT:

- Rise/fall time measurement
- Overshoot and undershoot analysis
- Jitter measurement on clock signals
- Eye diagram analysis for high-speed signals

COMMON SIGNAL INTEGRITY PROBLEMS:

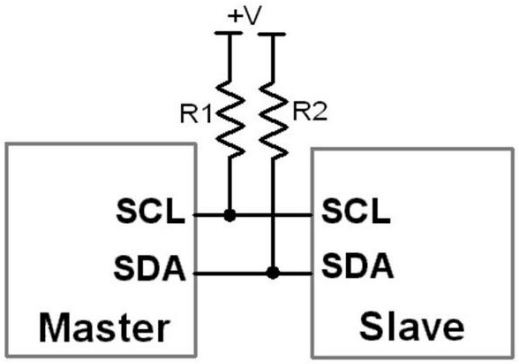
Issue	Symptoms	Measurement	Solution
Excessive ringing	Data errors at high speed	>20% overshoot	Add damping resistor
Slow edges	Setup/hold violations	Rise time >10% bit period	Reduce load capacitance
Ground bounce	Intermittent errors	Ground noise >0.5V	Improve ground planes
Crosstalk	Data-dependent errors	Adjacent line coupling	Increase spacing

I2C common problem

I2C like other comm protocols, requires a PU resistor. It is important to pick the right resistors.

LOW PULL-UP RESISTORS:

- Low values resistors selected (< 2.2kΩ)
- SDA and SCL both get the same resistor
- The current on the comm line is high
- Under and Overshoot may appear on SDA/SCL

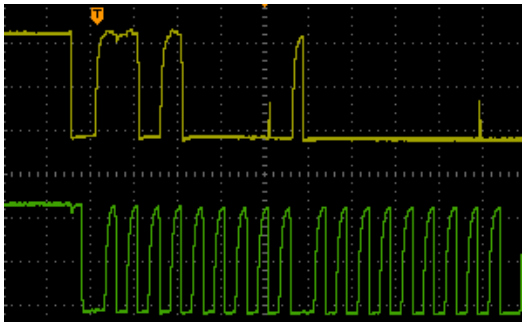


HIGH PULL-UP RESISTORS:

- High values resistors selected (< 10kΩ)
- SDA and SCL both get the same resistor
- The current on the comm line is low
- PU is not strong enough
- Logic levels will be too low and '1' will be interpreted as '0'

IDENTIFY I2C COMM PROBLEMS

- Check both SCL/SDA with scope
- perform the test while line is active
- check the level of '1' (should be very close to VCC e.g. 3.3V)
- Check Under and overshoots
- Check for ringing on the line
- Check if the signal is not too slow (capacitance problem)



Oscilloscope and Logic Analyzer Usage

Use appropriate tools for different communication debug scenarios.

OSCILLOSCOPE APPLICATIONS:

- Single-ended signal amplitude measurement
- Differential signal analysis (use math functions)
- Clock signal quality assessment
- Power supply noise correlation with communication errors

LOGIC ANALYZER APPLICATIONS:

- Protocol decode (I2C, SPI, UART, CAN)
- Bus timing analysis
- State machine debugging
- Multi-device communication sequence analysis

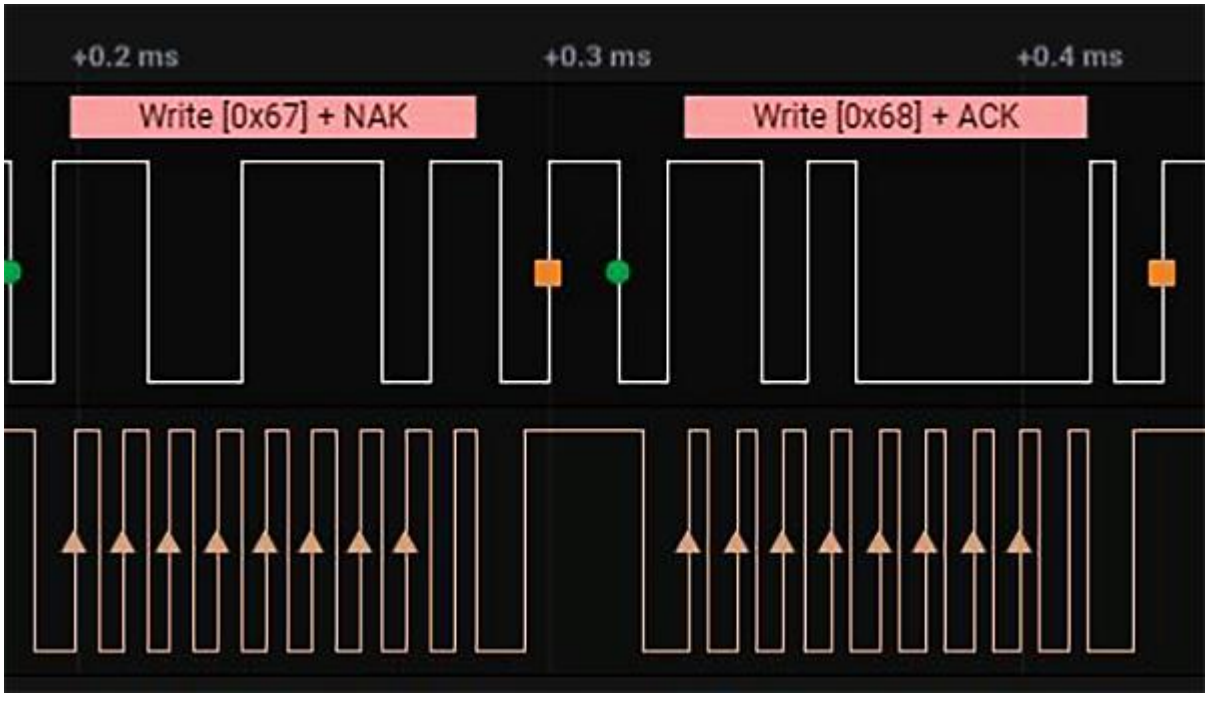
Measurement Setup Guidelines:

FOR HIGH-SPEED SIGNALS (>10MHZ):

- Use 50Ω probes with proper grounding
- Minimize probe ground lead length (<1 inch)
- Set oscilloscope bandwidth appropriately (5x signal frequency)
- Use differential probes for differential signals

FOR PROTOCOL ANALYSIS:

- Connect logic analyzer ground to circuit ground
- Use appropriate threshold voltages for logic family
- Set sample rate 10x higher than maximum data rate
- Configure protocol decoders before starting capture



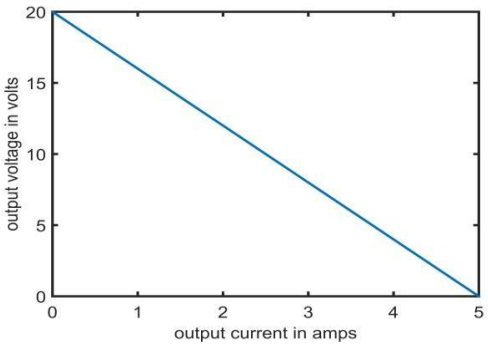
4.4 POWER SUPPLY ISSUES

Power Supply Instability and Voltage Droop

Poor power supply performance affects all circuit operation. Identify and correct power delivery problems.

LOAD REGULATION TESTING:

- Measure output voltage vs load current
- Calculate regulation: (VNL - VFL)/VFL × 100%
- Acceptable regulation: <5% for most digital circuits
- Test at maximum rated load current



LINE REGULATION TESTING:

- Vary input voltage across specified range
- Monitor output voltage stability
- Acceptable line regulation: <1% for most applications
- Test with realistic load conditions

RIPPLE AND NOISE MEASUREMENT:

- Use oscilloscope with 20MHz bandwidth limit
- Measure peak-to-peak ripple voltage
- Acceptable ripple: <50mV for 3.3V digital, <10mV for analog
- Check correlation between switching frequency and ripple

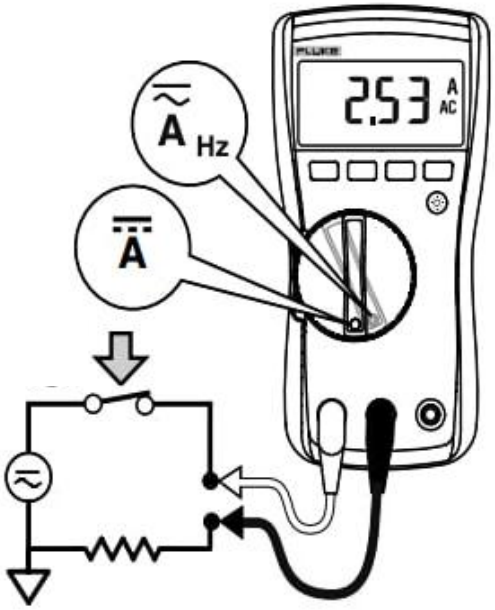
High Current Draw and Shorts Identification

Excessive current draw indicates component failures or design problems. Isolate high-current paths.

Current Path Analysis Method:

STEP 1: SECTION ISOLATION

- Identify major circuit sections
- Disconnect non-essential loads
- Measure current for each section separately
- Use fuses or removable links where possible



STEP 2: COMPONENT-LEVEL ANALYSIS

- Remove ICs from sockets (if socketed)
- Measure current with ICs removed
- Replace ICs one at a time
- Identify which IC causes high current

STEP 3: SHORT CIRCUIT LOCALIZATION

- Use thermal camera to find hot spots
- Apply limited current (100mA) and follow heat
- Check for shorts between power planes
- Use current injection and voltage measurement

4.5 MECHANICAL AND SOLDER DEFECTS

Cold Solder Joints, Bridges, Tombstoning

Mechanical defects create both immediate failures and long-term reliability problems. Identify and correct assembly issues.

COLD SOLDER JOINT CHARACTERISTICS:

- Dull, granular appearance
- Poor mechanical strength
- High electrical resistance
- Temperature-dependent contact

SOLDER BRIDGE DETECTION:

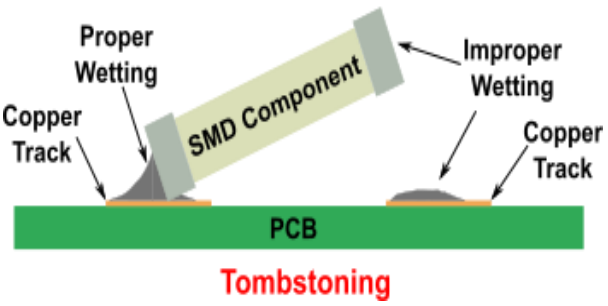
- Visual inspection under magnification (10-20x)
- Electrical continuity testing between adjacent pins
- In-circuit testing for short circuits
- X-ray imaging for hidden bridges (BGA, QFN)

TOMBSTONE DEFECT ANALYSIS:

Tombstoning occurs when one end of a component lifts during reflow. Common on small passive components.

TOMBSTONE CAUSES:

- Unequal pad sizes creating unequal thermal mass
- Paste volume imbalance between pads
- Component placement offset
- Reflow profile with excessive ramp rate



Tombstoning

Component Misplacement and Replacement

Wrong components often pass visual inspection but cause functional failures.

Component Verification Process:

PASSIVE COMPONENTS:

- Measure resistance values in-circuit (consider parallel paths)
- Use LCR meter for capacitor and inductor values
- Check voltage ratings on capacitors
- Verify tolerance markings match requirements

ACTIVE COMPONENTS:

- Check part number markings against schematic
- Verify pin configuration matches footprint
- Test basic functionality (voltage levels, current draw)
- Compare with known good reference parts

COMPONENT SELECTION:

- Match or exceed voltage ratings
- Verify temperature ratings for application
- Check package compatibility (footprint, height)
- Ensure equivalent electrical characteristics

TROUBLESHOOTING TECHNIQUES

5.1 DIVIDE AND CONQUER

Complex PCBs require systematic approaches to isolate problems efficiently.

System Partitioning Strategy

IDENTIFY MAJOR FUNCTIONAL BLOCKS:

- Power supply sections (input, regulation, distribution)
- Processing sections (CPU, DSP, FPGA)
- Interface sections (communication, I/O, connectors)
- Support sections (clock generation, reset, monitoring)

POWER DOMAIN ANALYSIS:

- Create power distribution tree diagram
- Identify all voltage rails and their sources
- Map which circuits depend on each power rail
- Test power rails independently before applying loads

SIGNAL FLOW MAPPING:

- Trace critical signals from input to output
- Identify signal processing stages
- Document signal levels and timing requirements
- Create test points for signal monitoring

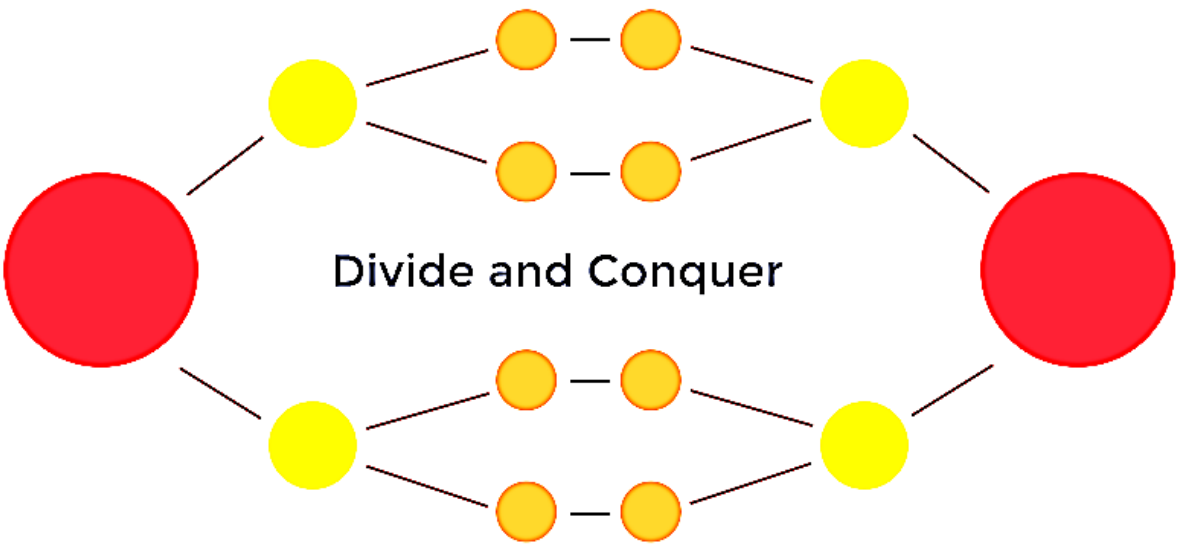
Isolation Testing Procedures

SEQUENTIAL POWER-UP METHOD:

1. Apply only input power, verify input protection
2. Enable primary power supplies, measure no-load voltages
3. Enable secondary supplies in dependency order
4. Apply loads gradually, monitor current and voltage
5. Enable active circuits last, verify functionality

LOAD ISOLATION TECHNIQUE:

- Remove or disconnect major load sections
- Start with minimum configuration for basic operation
- Add load sections one at a time
- Identify which section causes problems



5.2 THE SPLIT-HALF METHOD

The split-half method reduces problem space exponentially.

Implementation Strategy

BINARY SEARCH APPROACH:

- Identify midpoint of suspected problem area
- Test functionality at midpoint
- If midpoint works, problem is in second half
- If midpoint fails, problem is in first half
- Repeat process on remaining half

SIGNAL PATH SPLITTING:

- Inject known good signals at circuit midpoints
- Monitor outputs for correct response
- Work backward from outputs when signals are corrupted
- Work forward from inputs when no signals present

POWER DISTRIBUTION SPLITTING:

- Test power rails at distribution points
- Isolate power sections using jumpers or switches
- Measure current consumption of individual sections
- Identify sections with excessive current draw

Practical Application Examples

DIGITAL CIRCUIT DEBUG:

1. Test clock signals at source, middle, and destination
2. If clock good at middle but bad at destination, problem in second half
3. If clock bad at middle, problem in first half
4. Continue splitting until single component identified

ANALOG CIRCUIT DEBUG:

1. Inject test signal at input, measure at each amplifier stage
2. Find last stage with correct signal amplitude and frequency
3. Problem located between last good stage and first bad stage
4. Focus debug efforts on identified stage

5.3 ELIMINATION TECHNIQUES

Systematic elimination prevents overlooking simple causes.

Component Elimination Process

REMOVABLE COMPONENT STRATEGY:

- Remove socketed ICs systematically
- Test basic functionality with each IC removed
- Identify which IC removal restores normal operation
- Focus detailed analysis on problematic IC and supporting circuits

POWER SECTION ELIMINATION:

- Disable non-essential power sections
- Verify core functionality with minimum power configuration
- Re-enable power sections individually
- Identify which power section introduction causes problems

INTERFACE ELIMINATION:

- Disconnect external interfaces and cables
- Test internal functionality without external influences
- Reconnect interfaces individually
- Identify problematic interface or cable

Software vs Hardware Isolation

HARDWARE-ONLY TESTING:

- Load minimal software (hardware initialization only)
- Test hardware functionality without complex software algorithms
- Use built-in self-test features where available
- Apply external stimulus and measure responses

KNOWN GOOD SOFTWARE TESTING:

- Use previously validated software version
- Test with reference software from vendor
- Compare behavior with and without suspect software features
- Isolate software-dependent vs hardware-dependent issues

5.4 FISHBONE (ISHIKAWA) DIAGRAM

Fishbone diagrams help identify all possible causes systematically. Particularly useful for intermittent problems.

Diagram Construction Process

MAIN CATEGORIES FOR PCB PROBLEMS:

- Materials (components, PCB substrate, solder)
- Methods (assembly process, test procedures, handling)
- Machines (assembly equipment, test equipment)
- Environment (temperature, humidity, vibration, EMI)
- People (training, procedures, workmanship)
- Measurements (calibration, accuracy, precision)

SYSTEMATIC CAUSE INVESTIGATION:

1. Define the problem clearly (effect)
2. List all possible causes in each category
3. Investigate most likely causes first
4. Use data to validate or eliminate causes
5. Focus on causes with supporting evidence

Troubleshooting Example:

RS-485 communication fails randomly during operation

MATERIAL CAUSES:

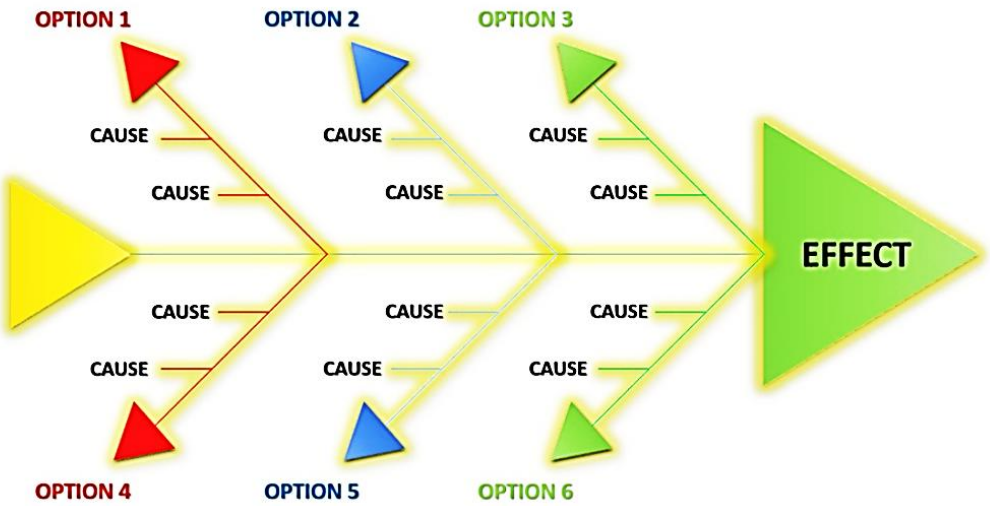
- Defective transceiver IC
- Wrong termination resistor values
- Poor quality cable
- Connector contact problems

METHOD CAUSES:

- Incorrect cable routing near power circuits
- Improper grounding technique
- Missing common-mode chokes
- Inadequate surge protection

ENVIRONMENTAL CAUSES:

- Electrical noise from motors/relays
- Temperature variations affecting timing
- Vibration causing intermittent connections
- EMI from nearby radio frequency sources



5.5 A-B-A SWAP TECHNIQUE

Component swapping determines whether problems are component-related or PCB-related.

Swap Testing Protocol

COMPONENT SWAP PROCESS:

1. Identify suspected component on failing board (Board A)
2. Remove suspect component, install known good component
3. Test for problem resolution
4. Install original component on known good board (Board B)
5. Test if problem moves to Board B

INTERPRETATION OF RESULTS:

Board A Result	Board B Result	Conclusion
Problem fixed	Problem appears	Component defective
Problem persists	No problem	Board defective
Problem fixed	No problem	Component marginal
Problem persists	Problem appears	Multiple issues

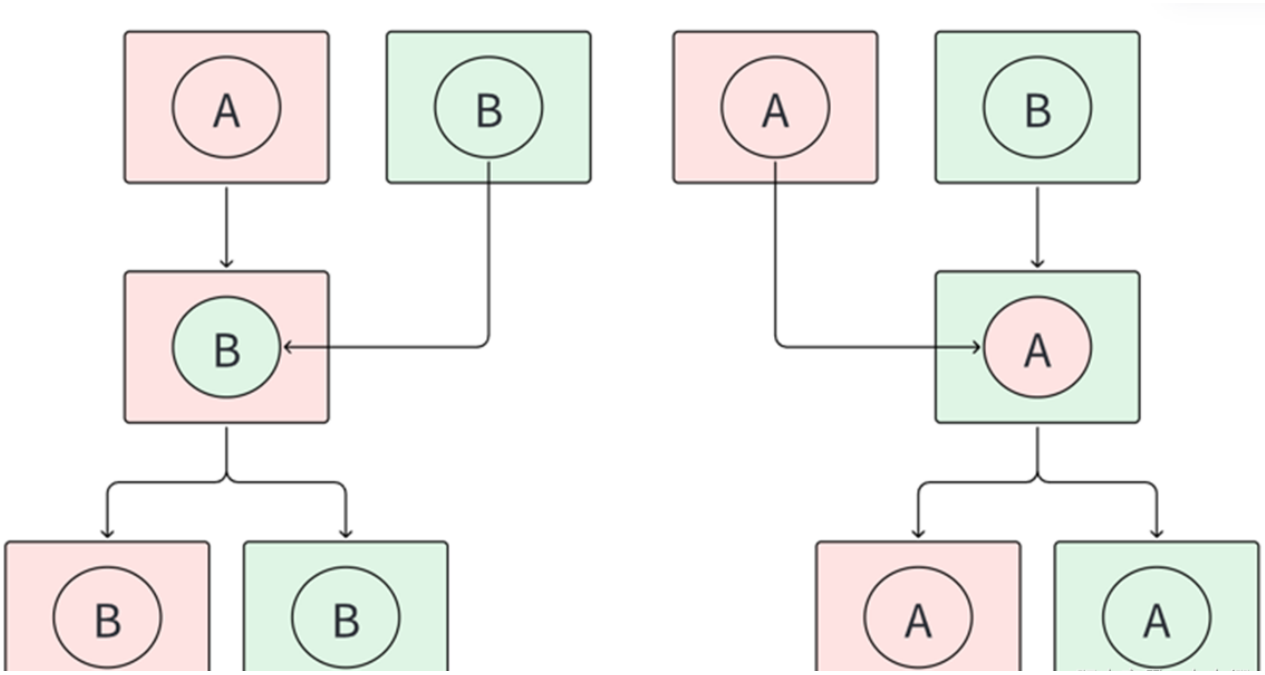
Advanced Swapping Techniques

PROGRESSIVE COMPONENT SWAPPING:

- Start with most likely suspect components
- Swap components in order of suspicion
- Document results for each swap
- Continue until root cause identified

SECTION SWAPPING:

- Swap entire functional sections when possible
- Use modular designs to facilitate section swapping
- Compare identical boards for population differences
- Identify systematic vs random problems



5.6 USING KNOWN GOOD PARTS

Reference standards accelerate problem identification and provide confidence in measurements.

Reference Standard Requirements

KNOWN GOOD BOARD CRITERIA:

- Identical PCB revision and assembly lot
- Verified functional operation under all conditions
- Same component population and values
- Documented performance measurements for comparison

GOLDEN UNIT ESTABLISHMENT:

- Select board that meets all specifications
- Document all critical measurements and waveforms
- Store in controlled environment to prevent degradation
- Re-verify periodically to ensure continued validity

Comparison Testing Methods

SIDE-BY-SIDE MEASUREMENT:

- Measure same points on good and suspect boards
- Use identical test setup and procedures
- Compare waveforms, voltages, currents, and timing
- Look for subtle differences that indicate problems

SIGNAL SUBSTITUTION TESTING:

- Use known good board to generate reference signals
- Inject reference signals into suspect board
- Verify suspect board responds correctly to known good inputs
- Isolate input vs output problems

5.7 LOGICAL DEBUG FLOWS

Logical progression prevents wasted time on complex tests when simple problems exist.

Debug Complexity Hierarchy

LEVEL 1 - VISUAL AND BASIC ELECTRICAL:

- Component presence and orientation
- Solder joint quality and bridges
- Power supply voltages and currents
- Basic continuity testing

LEVEL 2 - FUNCTIONAL TESTING:

- Clock signals and frequencies
- Reset and enable signals
- Communication interface loopback tests
- Simple stimulus/response testing

LEVEL 3 - PERFORMANCE ANALYSIS:

- Signal integrity and timing analysis
- Power supply regulation and ripple
- Temperature and thermal analysis
- EMI and susceptibility testing

LEVEL 4 - ADVANCED CHARACTERIZATION:

- Protocol analysis and compliance testing
- Reliability testing and stress analysis
- Statistical analysis of multiple units
- Root cause failure analysis

Decision Tree Methodology

PROBLEM SYMPTOM ASSESSMENT:

- Complete failure: Start with power and basic connectivity
- Intermittent operation: Focus on environmental and mechanical factors
- Performance degradation: Analyze specifications and tolerances
- Compatibility issues: Verify protocol compliance and timing

TEST RESULT INTERPRETATION:

- Pass result: Move to next complexity level
- Fail result: Focus debugging on current level
- Marginal result: Investigate specification limits and tolerances
- Intermittent result: Add environmental stress during testing

CASE STUDIES

6.1 RESISTOR VALUE DRIFT

Background:

Industrial sensor board intermittently reports incorrect readings after 6 months of operation.

Problem Description

System: 4-20mA current loop sensor interface

Components: Precision current sense resistors (0.1% tolerance)

Symptoms: Output readings drift +15% from calibrated values

Environment: 85°C ambient, high humidity industrial setting

Debug Process

STEP 1: SYMPTOM REPRODUCTION

- Measured actual sensor output: 3.45V (expected: 3.00V)
- Calculated current sense voltage: 0.234V (expected: 0.200V)
- Resistance measurement of sense resistor: 1.15Ω (marked: 1.00Ω)

STEP 2: ROOT CAUSE ANALYSIS

- Removed resistor from circuit for accurate measurement
- Out-of-circuit resistance: 1.16Ω (+16% drift)
- Visual inspection revealed brown discoloration
- Other identical resistors on same board: 1.02-1.05Ω

STEP 3: ENVIRONMENTAL ANALYSIS

- PCB temperature measurement: 92°C @ resistor location
- Power dissipation calculation: $I^2R = (0.02A)^2 \times 1\Omega = 0.4mW$
- Resistor power rating: 0.125W (adequate for calculated power)
- Moisture absorption suspected due to high humidity

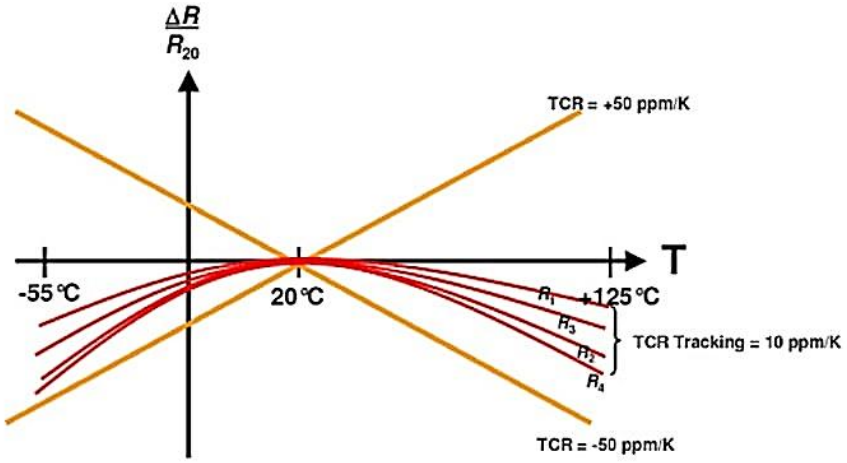
Resolution and Prevention

IMMEDIATE FIX:

- Replaced all current sense resistors with fresh parts
- Applied conformal coating to protect from moisture
- Recalibrated system after repairs

LONG-TERM PREVENTION:

- Specified resistors with better moisture resistance
- Added temperature compensation in software
- Implemented periodic calibration check procedure



6.2 BROKEN / CUT PCB TRACES

Background:

Automotive ECU fails intermittently after vibration testing.

Problem Description

System: Engine control unit with mixed digital/analog circuits

Failure Mode: Loss of throttle position sensor signal

Symptoms: Engine runs rough, error codes stored

Trigger: Occurs after temperature cycling and vibration

Debug Process

STEP 1: SIGNAL PATH ANALYSIS

- Throttle position sensor provides 0.5-4.5V signal
- Signal travels through connector, PCB trace, to ADC input
- Oscilloscope shows intermittent signal dropouts
- Signal present at connector, absent at MCU pin

STEP 2: TRACE CONTINUITY TESTING

- Visual inspection reveals no obvious damage
- Multimeter continuity test: intermittent open circuit
- Flexing PCB reproduces the open circuit
- Thermal cycling makes problem worse

STEP 3: DETAILED TRACE INSPECTION

- 10x magnification reveals hairline crack in trace
- Crack located near large capacitor (thermal stress point)
- Crack propagates with thermal cycling
- Multiple boards show similar cracks in same location

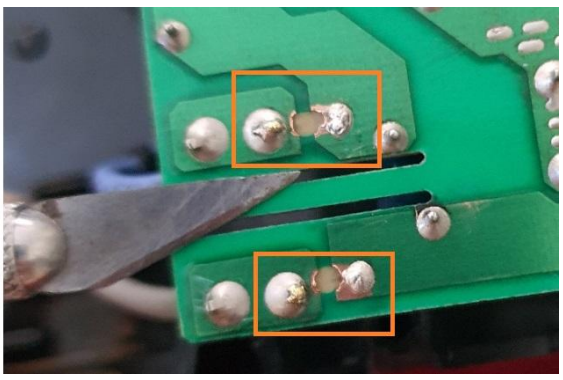
Repair Techniques

PERMANENT FIX:

- Route jumper wire on component side
- Use 30AWG wire-wrap wire for flexibility
- Secure with UV-cure solder mask
- Test repair under thermal cycling

PCB LAYOUT CHANGES:

- Added stress relief slots around large components
- Increased trace width for critical signals
- Changed to 2oz copper for better durability
- Added redundant traces for critical signals



6.3 UNSTABLE VOLTAGE

Background:

Switch-mode power supply exhibits output voltage oscillation in battery-powered device.

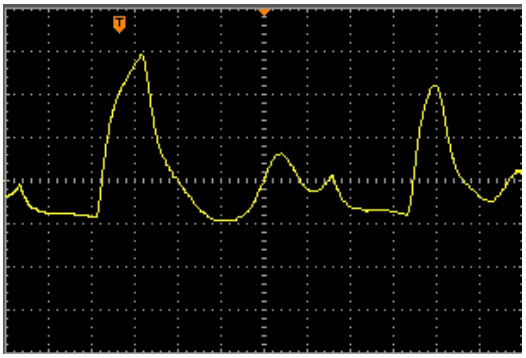
Problem Description

System: Portable medical device with 12V to 3.3V buck converter

Components: TI TPS54531 switching regulator

Symptoms: 3.3V output oscillates between 2.8V and 3.8V at 20kHz rate

Load: 500mA average, varying from 100mA to 1A



Debug Process

STEP 1: OSCILLATION CHARACTERIZATION

- Scope measurement shows 1Vpp oscillation at output
- Switching node shows irregular switching pattern
- Feedback voltage oscillates around 0.8V reference
- Current limit LED flickers during oscillation

STEP 2: LOOP STABILITY ANALYSIS

- Removed output capacitor: oscillation frequency increases
- Added additional 100µF: oscillation amplitude decreases
- Changed feedback resistor values: oscillation frequency changes
- Suspected feedback network instability

STEP 3: COMPONENT VERIFICATION

- Output inductor measured: 4.7µH (specified: 4.7µH)
- Output capacitor ESR measured: 45mΩ (specified: <100mΩ)
- Feedback resistor values correct
- Input capacitor ESR high: 200mΩ (should be <50mΩ)

Root Cause and Solution

High ESR input capacitor created input impedance that interacted with control loop.

ANALYSIS:

- High input impedance caused input voltage variation
- Input voltage variation coupled to output through poor PSRR
- Created positive feedback loop causing oscillation
- Problem worse at high load current

SOLUTION:

- Replaced input capacitors with low-ESR types
- Added ceramic bypass capacitors in parallel with electrolytics
- Adjusted compensation network for improved phase margin
- Added input EMI filter to reduce conducted emissions

COMPONENT CHANGES:

Function	Original	Replacement	Improvement
Input cap	220µF Electrolytic	220µF + 22µF ceramic	Lower ESR
Output cap	470µF	470µF + 47µF ceramic	Better transient response
Compensation	10nF	15nF	Improved phase margin

6.4 BULGING CAPACITOR

Background:

Power amplifier board shows distortion and instability after 18 months operation.

Problem Description

System: Audio power amplifier, 100W per channel

Environment: Rack-mounted in hot equipment room

Symptoms: Audio distortion, DC offset at outputs, occasional shutdown

Visual: Several electrolytic capacitors show bulging tops

Detection and Analysis

VISUAL INSPECTION RESULTS:

- 4 of 12 electrolytic capacitors show dome-shaped bulging
- No visible electrolyte leakage yet
- Bulged capacitors located near heat-generating components
- PCB shows brown discoloration around hot components

ELECTRICAL TESTING:

- ESR measurement using dedicated ESR meter
- Normal 1000µF/25V capacitor ESR: 0.02-0.05Ω
- Bulged capacitors ESR: 0.15-0.3Ω (3-15x higher than normal)
- Capacitance measurement: 650-800µF (should be 1000µF ±20%)

ROOT CAUSE ANALYSIS:

- High ambient temperature (45°C in equipment rack)
- Ripple current heating accelerated electrolyte evaporation
- Original capacitors rated for 85°C operation
- Actual component temperature measured at 95°C during operation

6.5 STARVED THERMAL PADS

Background:

LED driver circuit experiences thermal shutdown during normal operation.

Problem Description

System: High-power LED driver, 50W output

Components: Power MOSFET in DPAK package with thermal pad

Symptoms: Thermal shutdown after 2-3 minutes of operation

Design: MOSFET mounted on 4-layer PCB with thermal vias

Thermal Analysis

TEMPERATURE MEASUREMENTS:

- MOSFET case temperature: 145°C (Tj max = 150°C)
- PCB temperature under MOSFET: 130°C
- Ambient temperature: 25°C
- Expected case temperature: <100°C with proper thermal design

THERMAL RESISTANCE CALCULATIONS:

- Junction-to-case: 0.5°C/W (datasheet value)
- Case-to-ambient measured: 2.8°C/W
- Case-to-ambient expected: 1.2°C/W
- Thermal resistance 2.3x higher than designed

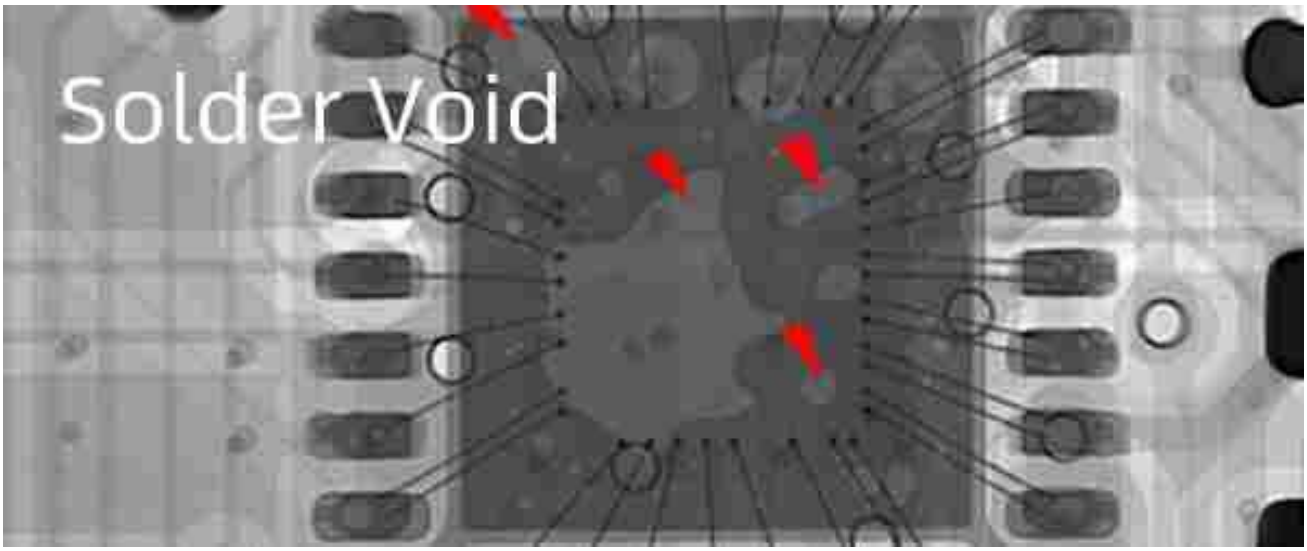
Root Cause Investigation

SOLDER JOINT ANALYSIS:

- X-ray inspection reveals voids in thermal pad solder
- Thermal pad coverage: ~40% (should be >80%)
- Voids created during reflow due to trapped air/flux
- Insufficient solder paste volume on thermal pad

THERMAL VIA ANALYSIS:

- Thermal vias partially filled with solder mask
- Via drill size: 0.2mm (too small for effective heat transfer)
- Via spacing: 1.27mm (adequate)
- Number of vias: 16 (adequate if properly implemented)



6.6 INACCURATE ADC READING

Background:

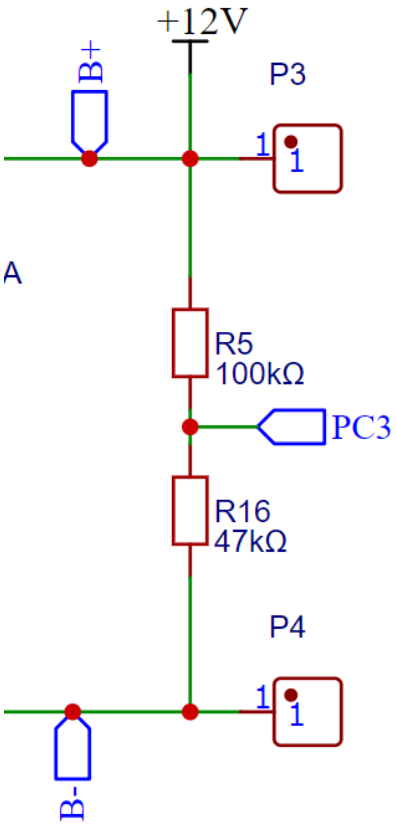
Supply Voltage levels are monitored via ADC as part of Multidisciplinary system.

Problem Description

System: Multidisciplinary board connecting to PC

ADC: 12-bit ADC (inherent in MCU), monitoring the voltage levels.

Symptoms: Voltage readings from PC far from expected level



Debug Process

STEP 1: INTIAL VALIDATION

- Measure MCU analog reference voltage
- Check if any voltage drops on filters in the measured path
- Measure the resistors in the voltage divider.
- Measure the voltage before division
- Measure the ADC input

STEP 2: CONDITIONING ANALYSIS

- Check how stable the voltage in each point
- Observe what happens in power-up
- Use different modes to check if the problem is related to specific scenario

STEP 3: ADC PERFORMANCE VERIFICATION

- DNL (Differential Non-linearity)
- INL (Integral Non-linearity)
- Noise floor measurement
- Saturation level check

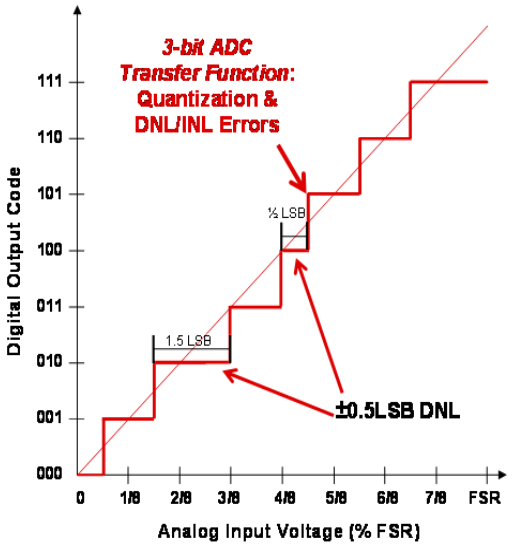
Root Causes

COMMON PROBLEMS:

- Wrong voltage division
- Low resistors values (Ignoring the input resistance of ADC input)
- Parasite resistance in the measured path

COMPLEX PROBLEMS:

- The monitored voltage rail is low (not an ADC problem)
- The wrong rail is connected to the input
- The FW interpreting the level is wrong
- The input level is saturated or buried in Noise (near GND)



6.7 NON-COMMUNICATIVE BOARDS (PC)

Background:

Industrial data logger stops responding to host PC commands after firmware update, preventing data retrieval from field installations.

Problem Description

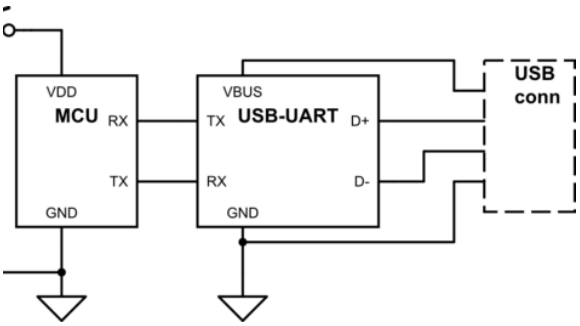
System: USB-connected data acquisition module with STM32F4 MCU

Interface: UART over USB using FTDI FT232R USB-to-serial converter

Symptoms: Device enumerates in Windows Device Manager but no data transmission

Environment: Field installation with 50+ units affected simultaneously

Debug Process

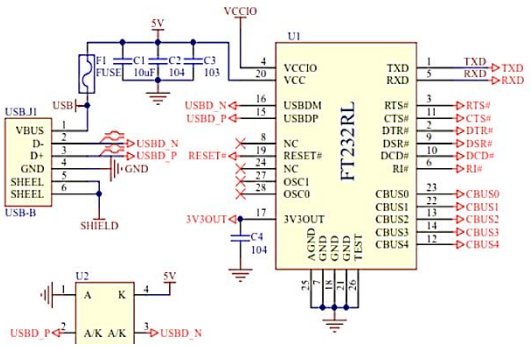


STEP 1: USB ENUMERATION ANALYSIS

- Windows Device Manager shows "USB Serial Port (COM3)"
- Device descriptor reads correctly with USB tools
- VID/PID matches expected values: 0403:6001 (FTDI standard)
- Driver installation successful, no yellow warning indicators

STEP 2: UART SIGNAL LAYER TESTING

- UART RX pin shows proper signal levels from FTDI chip
- Baud rate verified: 115200 8N1 matches PC configuration
- Hardware handshaking disabled on both ends as designed

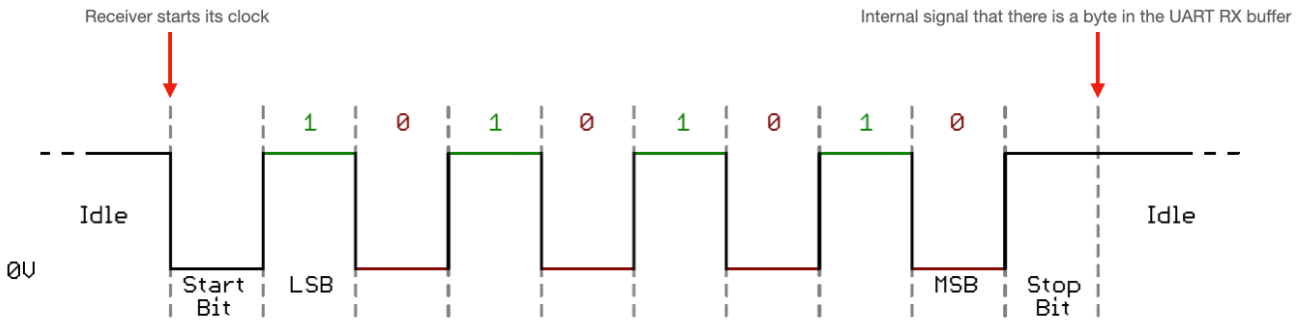


STEP 3: FIRMWARE COMMUNICATION STACK ANALYSIS

- UART peripheral registers show correct configuration
- Interrupt service routine never executes (confirmed with debug LED)
- MCU UART RX pin floating - internal pullup not enabled
- GPIO alternate function mapping incorrect after firmware update

STEP 4: HARDWARE LAYER VERIFICATION

- FTDI chip RXD/TXD signals present and correct polarity
- MCU power supply stable at 3.28V
- Crystal oscillator running at 8.000MHz (verified with scope)
- Reset line shows proper power-on sequence



6.8 NO MOTION FAULT

Background:

Robotic arm positioning system fails to respond to motion commands, with motor remaining stationary despite control signals being present.

Problem Description

System: Step motor drive for precision positioning application

Motor: 10W Step Nema23 motor with encoder feedback

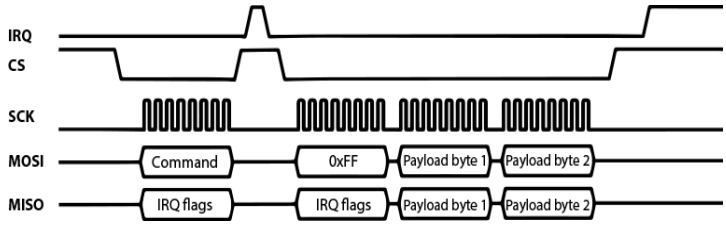
Symptoms: Motor shows no rotation, no audible switching noise, encoder position unchanged

Control: Step motor driver via SPI

Debug Process

STEP 1: COMMAND SIGNAL VERIFICATION

- Check SPI command Checked: ensure Proper packets are sent
- Validate Clean SPI signal with clear Pulses
- Measure Enable signal if implemented



STEP 2: POWER STAGE INVESTIGATION

- Check DC voltage to motor
- Measure Driver supply voltages
- Check Driver output levels

STEP 3: PROTECTION CIRCUIT ANALYSIS

- Ensure overcurrent comparators all showing normal state
- Validate that DC overvoltage protection not active
- Check Temperature sensors reading

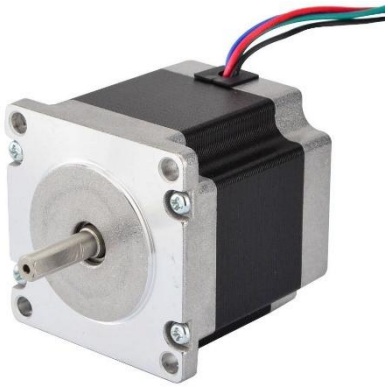
STEP 4: CONTROL LOOP FEEDBACK VERIFICATION

- Current feedback signal: Reading 0A (no motion)
- Check Encoder power supply: present and stable
- Ensure Encoder signals A/B: Present and toggling during manual motor rotation
- Check Position feedback to controller

Possible Root Causes

COMMAND:

- SPI Logic Levels are low
- Capacitance problem delaying the signal (not reaching '1')
- SPI is not produced at all (to Motor Driver)
- Wrong MOSI / MISO / CLOCK / CS activity
- Wrong Packets are sent



POWER:

- Driver Voltage problem
- Motor Voltage Issue
- Encoder Supply is low or not provided

CONTROL

- False Overvoltage indication
- Overcurrent protection activated
- Encoder Feedback problem
- FW Problem with data parsing