

# Towards Multi-Level Arithmetic Optimizations



#### The Real Number Illusion

- Most numerical code is written with real numbers in mind.
- Yet, compilers only obey low-level machine numbers: floats and ints.
- This discourages ("unsafe-math") or misses many optimization opportunities, especially in machine learning, linear algebra, or signal processing.

# **Arithmetic Optimizations**

- ... beyond existing low-level rewrites in current compilers:
- Operator specialization: squarers, constant multipliers
- Expression fusion:  $\frac{1}{\sqrt{x^2+y^2}}$  or  $\sin(\omega t + \phi)$
- Optimizations tailored to target semantics Useful when compiling to hardware [Lah+18; Ugu+20; For+22; DK24], but not only.

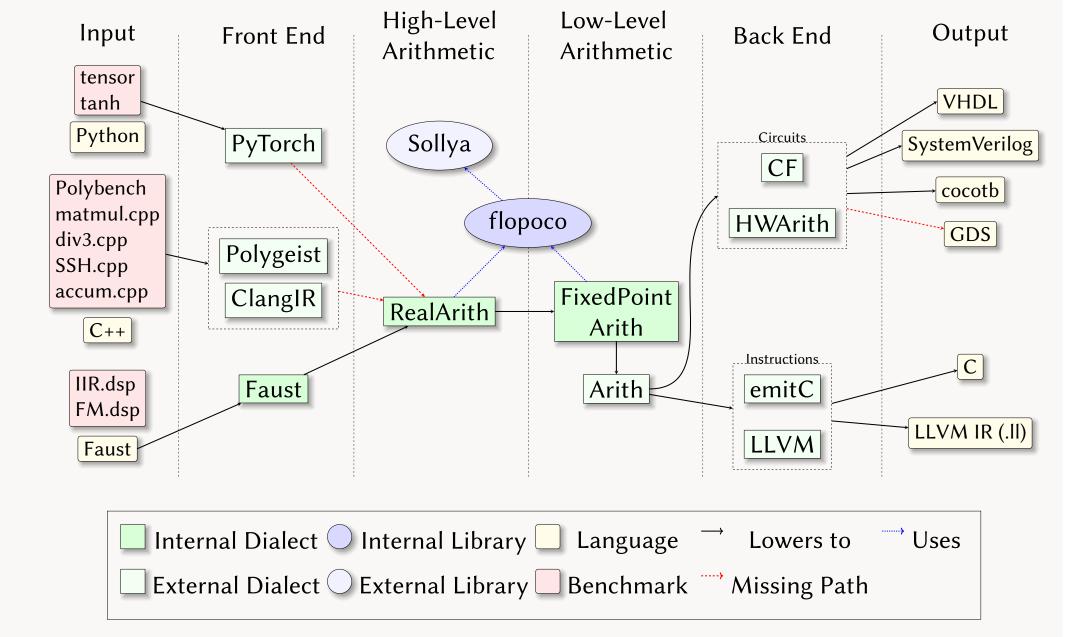
## Semantics First, Bits Later

#### **Separation of concerns** thanks to MLIR:

- Higher levels capture "mathematical intent",
- Lower levels deal with "machine numbers".

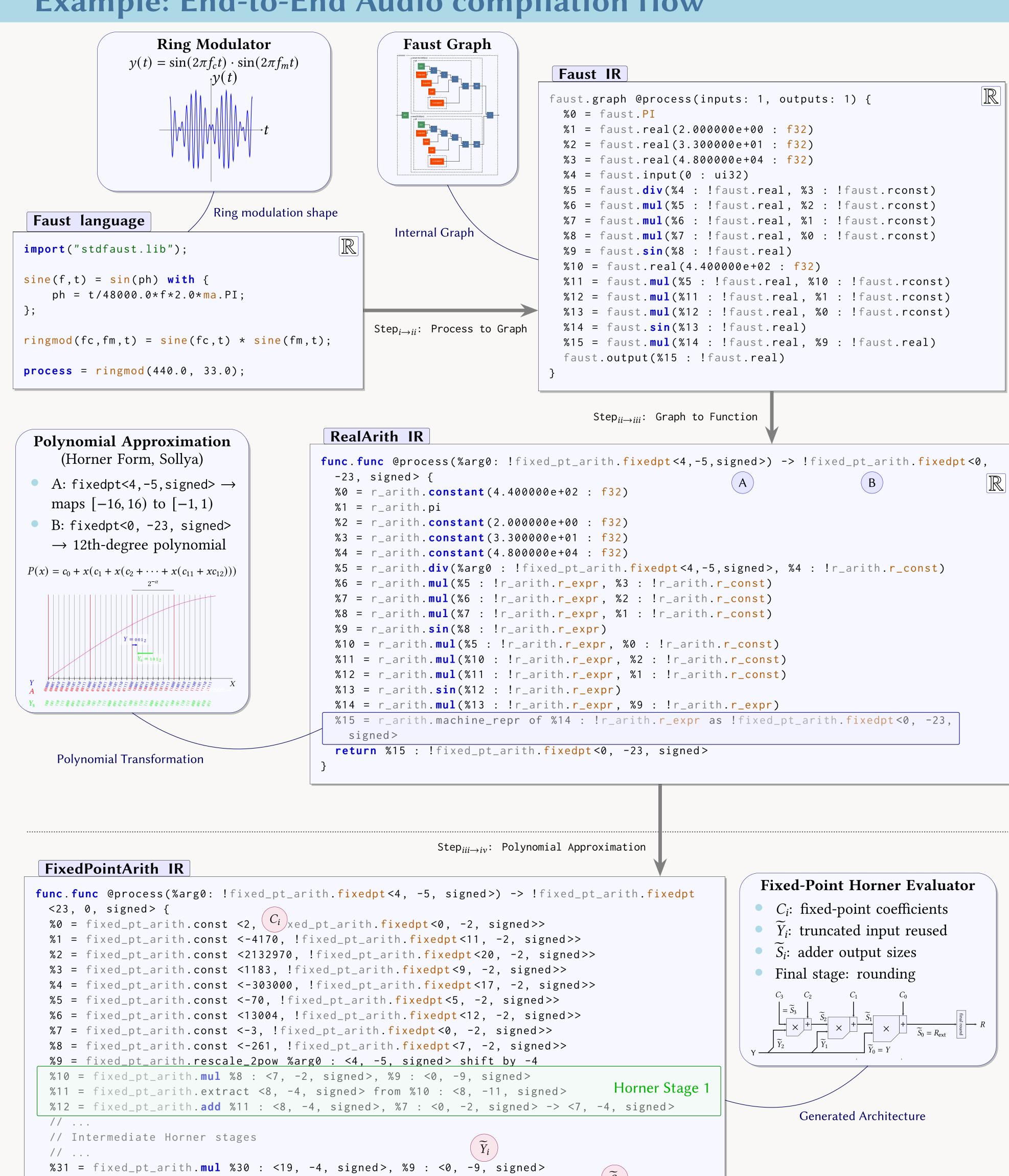
#### Our contributions:

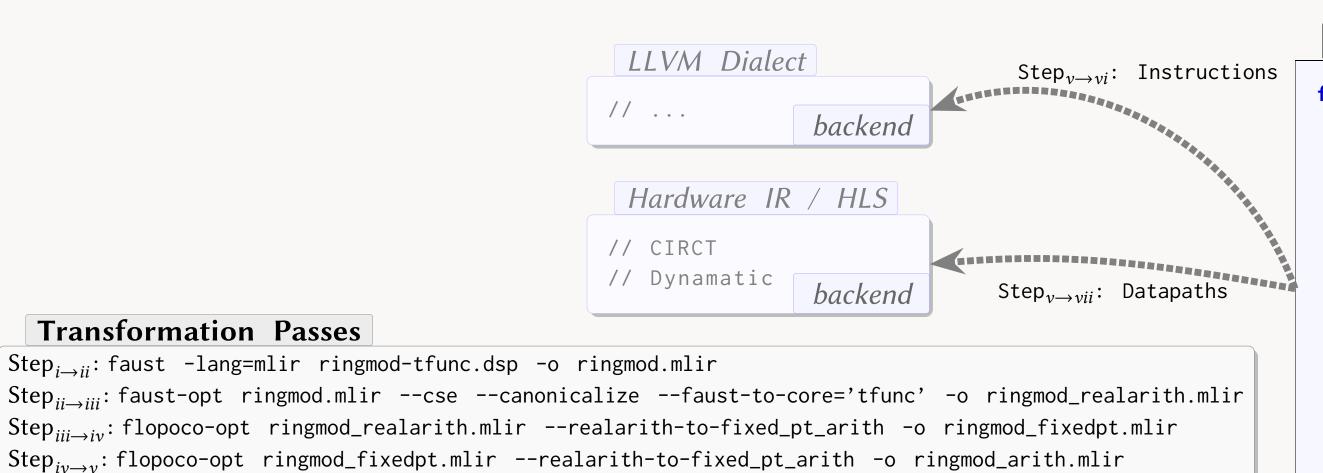
- real\_arith and fixed\_pt\_arith dialects
- Polynomial approximation lowering from real expressions
- Precision-tuned Horner architecture derived from dialect-level ops
- End-to-end MLIR flow evaluated on signal processing workloads



Overall contribution: proposed dialects (in dark green), integrated in a High-Level Synthesis ecosystem.

# **Example: End-to-End Audio compilation flow**





%33 = fixed\_pt\_arith.add %32 : <20, -4, signed>, %0 : <0, -2, signed> -> <20, -4, signed>

%32 = fixed\_pt\_arith.extract <20, -4, signed> from %31 : <20, -13, signed>

%34 = fixed\_pt\_arith.extend %33 : <20, -4, signed> to <23, -4, signed>

return %35 : !fixed\_pt\_arith.fixedpt<23, 0, signed>

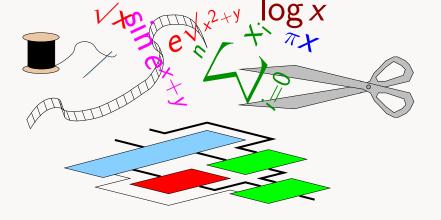
%35 = fixed\_pt\_arith.extract <23, 0, signed> from %34 : <23, -4, signed>

Arith IR (simplified) func.func @process(%arg0: i10) -> i24 {  $%c2_i3 = arith.constant 2 : i3$  $%c-4170_{i14} = arith.constant -4170 : i14$ %0 = arith.extsi %arg0 : i10 to i20  $%1 = arith.muli %0, %c-261_i20 : i20$  $%c7_i20 = arith.constant 7 : i20$ %2 = arith.shrsi %1, %c7\_i20 : i20 %3 = arith.trunci %2 : i20 to i13 %4 = arith.extsi %3 : i13 to i14 %65 = arith.trunci %64 : i28 to i24 **return** %65 : i24

 $Step_{iv \rightarrow v}$ : Fixed-Point scaling

### **Open-Source Tools**

- Sollya [SMC10]
- ScaleHLS [Ye+22]
- Dynamatic [Che+22],
- https://dynamatic.epfl.ch/
- SODA-OPT [Ago+22],
- https://github.com/pnnl/soda-opt **CIRCT** https://circt.llvm.org/
- Faust https://faust.grame.fr
- FloPoCo https://www.flopoco.org



#### Bibliography

N. B. Agostini et al. "An MLIR-based compiler flow for system-level design and hardware acceleration". In: 41st IEEE/ACM International [Ago+22] Conference on Computer-Aided Design. 2022, pp. 1–9.

J. Cheng, L. Josipović, G. A. Constantinides, and J. Wickerson. "Dynamic Inter-Block Scheduling for HLS". In: Field Programmable Logic and Applications. 2022.

F. de Dinechin and M. Kumm. *Application-Specific Arithmetic*. Springer, 2024. [DK24]

 $Step_{v \to vi}$ : flopoco-opt ringmod\_arith.mlir --arith-to-llvmir -o ringmod\_llvm.mlir

 $Step_{v \to vii}$ : flopoco-opt ringmod\_arith.mlir --arith-to-hw -o ringmod\_hw.mlir

L. Forget, G. Harnisch, R. Keryell, and F. De Dinechin. "A single-source C++20 HLS flow for function evaluation on FPGA and beyond.". [For+22] In: Highly Efficient Accelerators and Reconfigurable Technologies. ACM, 2022.

S. Lahti, P. Sjövall, J. Vanne, and T. D. Hämäläinen. "Are we there yet? A study on the state of High-Level Synthesis". In: Transactions on [Lah+18] Computer-Aided Design of Integrated Circuits and Systems 38.5 (2018), pp. 898–911.

S. Chevillard, M. Joldes, and C. Lauter. "Sollya: An Environment for the Development of Numerical Codes". In: *International Congress on* [SMC10] Mathematical Software. 2010.

Y. Uguen, F. de Dinechin, V. Lezaud, and S. Derrien. "Application-Specific Arithmetic in High-Level Synthesis Tools". In: Transactions on [Ugu+20] Architecture and Code Optimization 17.1 (2020).

H. Ye et al. "ScaleHLS: A new scalable High-Level Synthesis framework on Multi-Level Intermediate Representation". In: High Performance [Ye+22] Computer Architecture. 2022.