UCI University of California, Irvine

MCA Daemon

Hybrid Throughput Analysis Beyond Basic Blocks

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Keynote, EuroLLVM 2022

Outline

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Motivation

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MCA Daemon (MCAD)

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Future Plans

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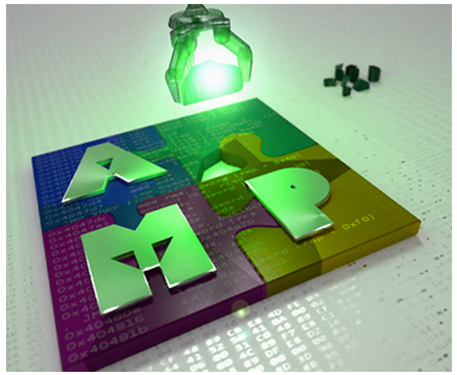

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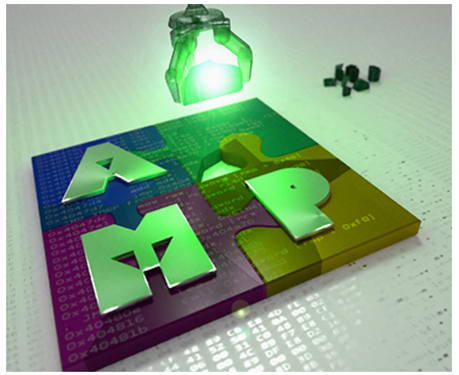

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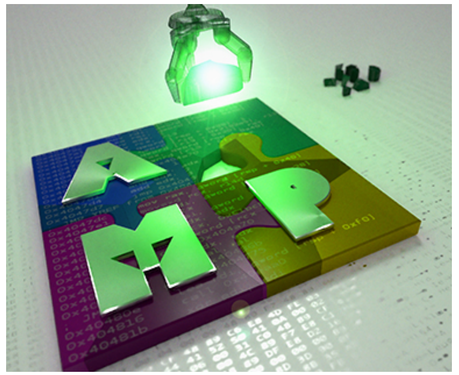

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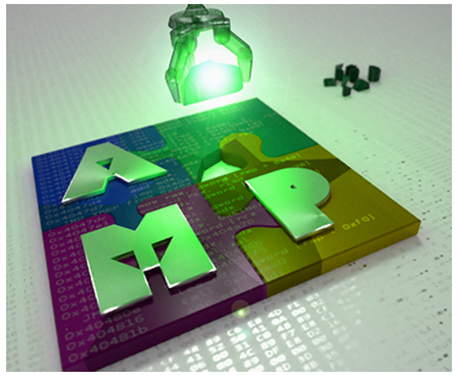

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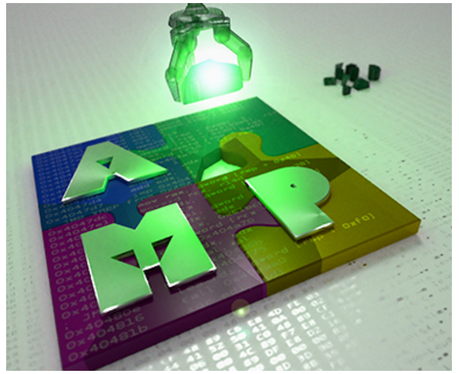

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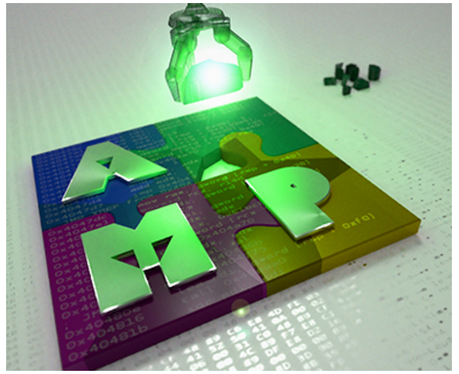
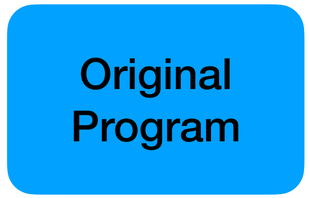


- UCI was studying the timing impacts of binary patches
  - Example: After the firmware on a truck is binary-patched to prevent brakes from locking up, we need to make sure **latencies** do not degrade terribly

Timing impacts of binary patches

Problem definition



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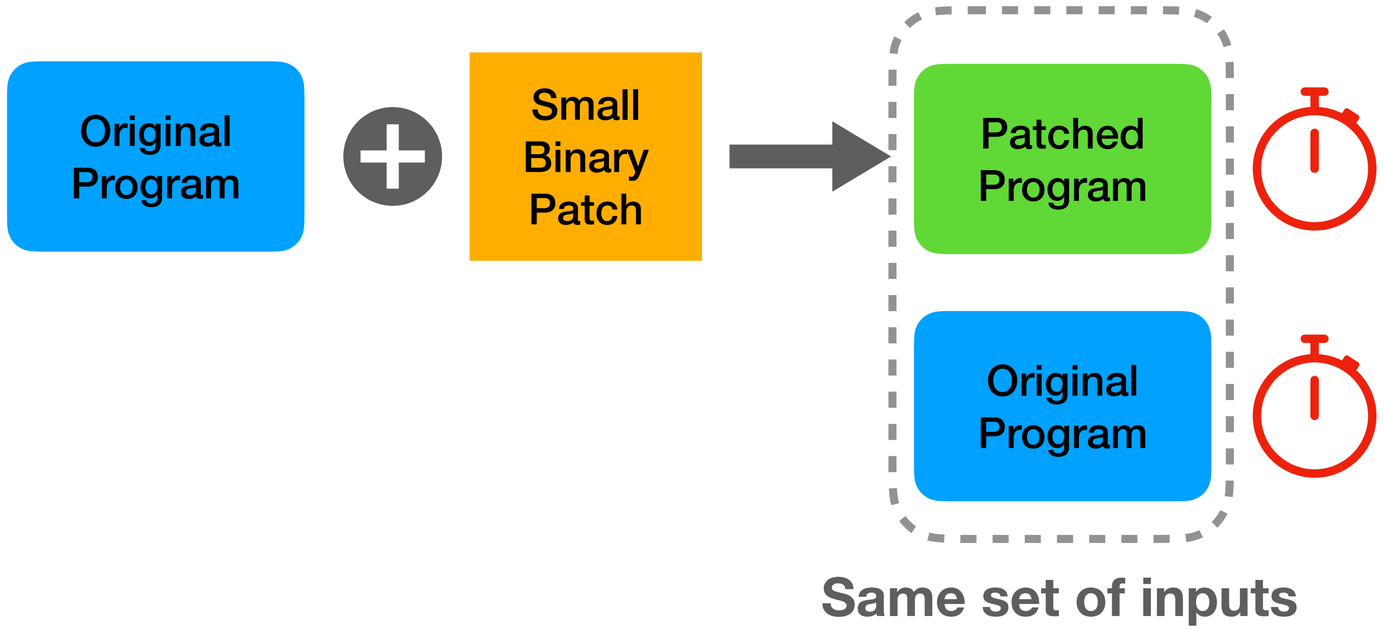

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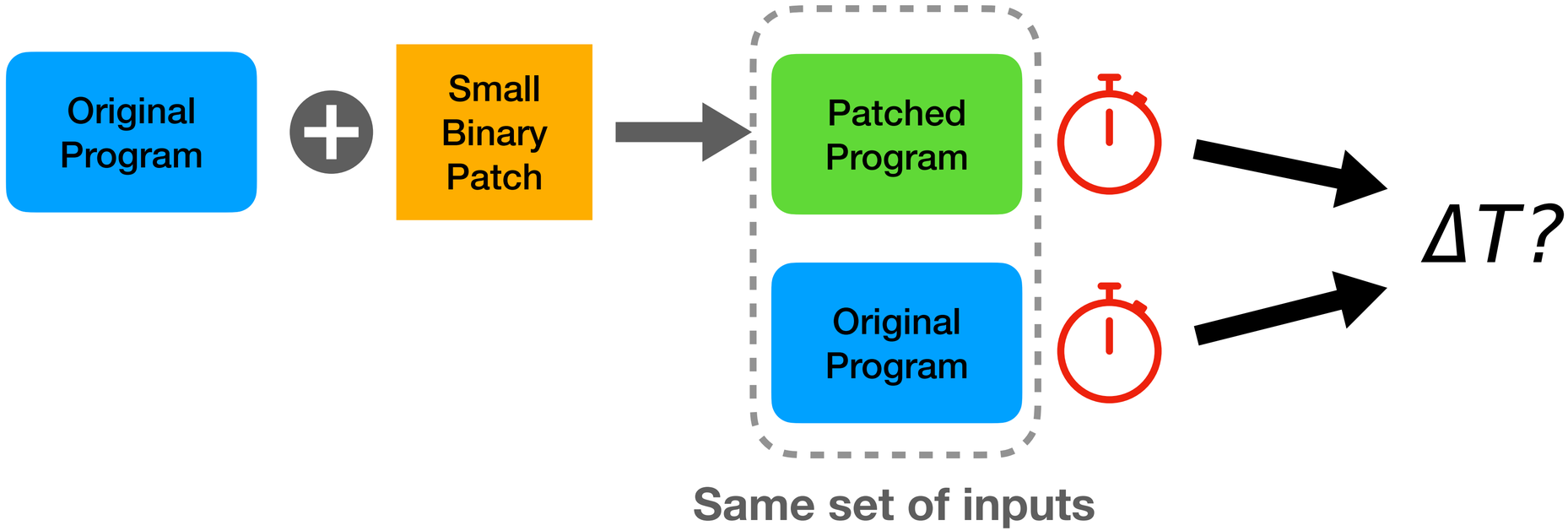
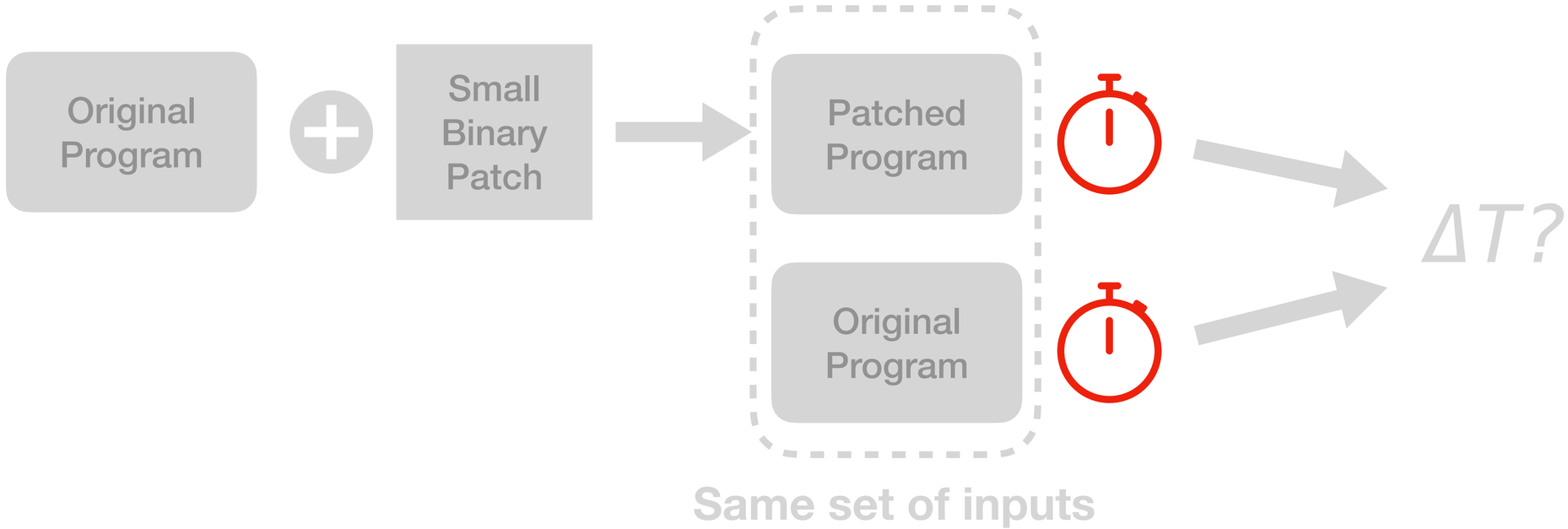


Execution time assessment



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- Performance analysis
  - **Insights** into performance bottlenecks
    - Examples: Potential CPU pipeline stalling, GPU memory bank conflicts

Execution time assessment

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    - Examples: gem5, gpgpu-sim

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- Higher fidelity on hardware details

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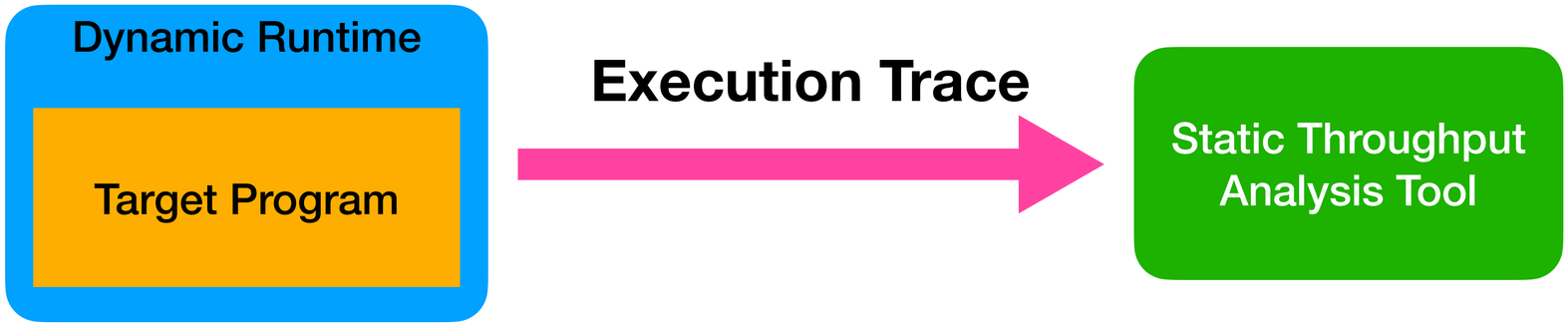
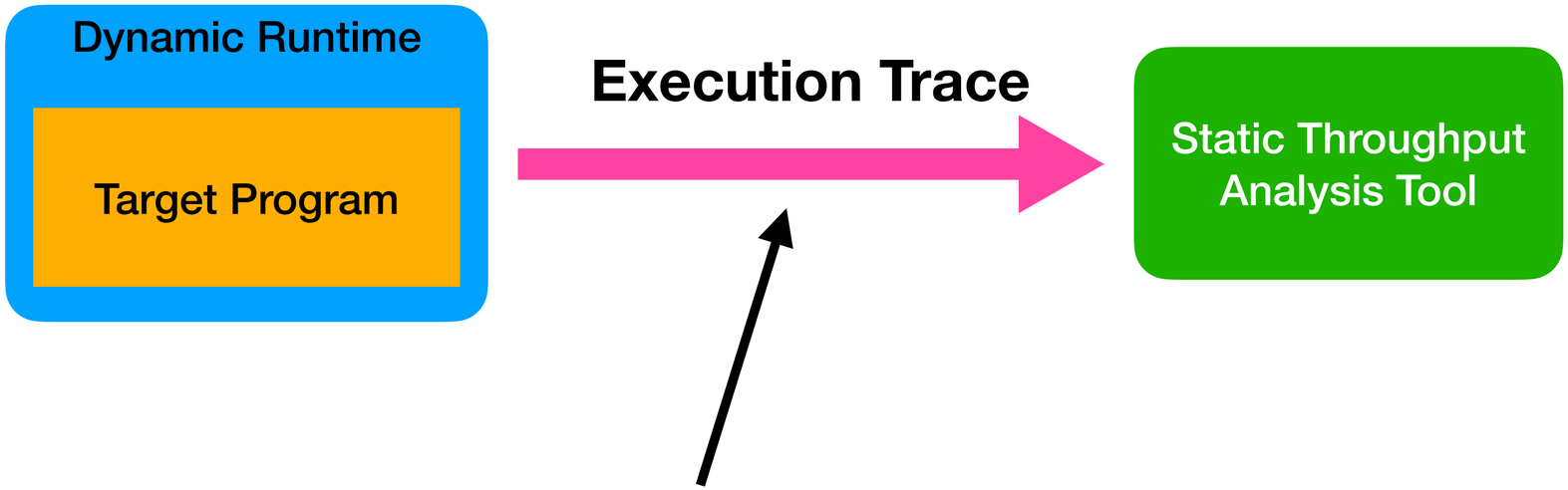


MCA Daemon (MCAD)

High-level concept



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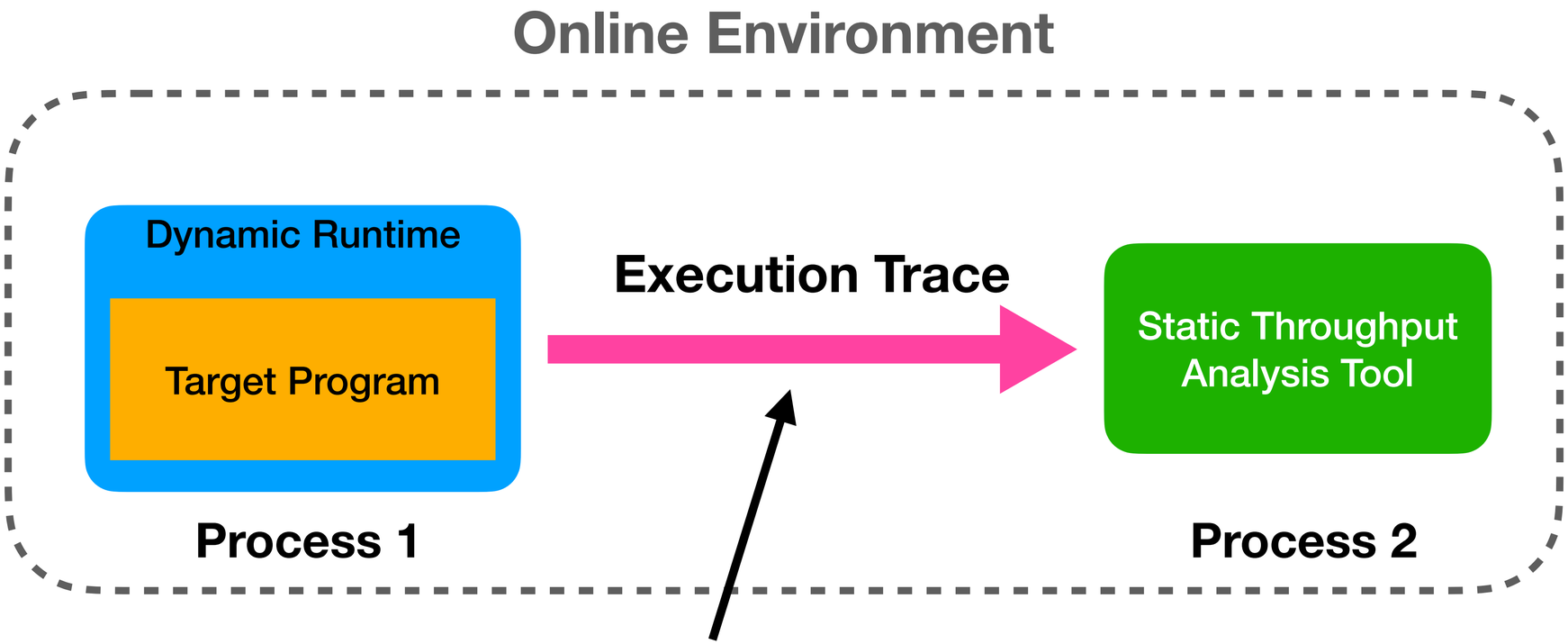

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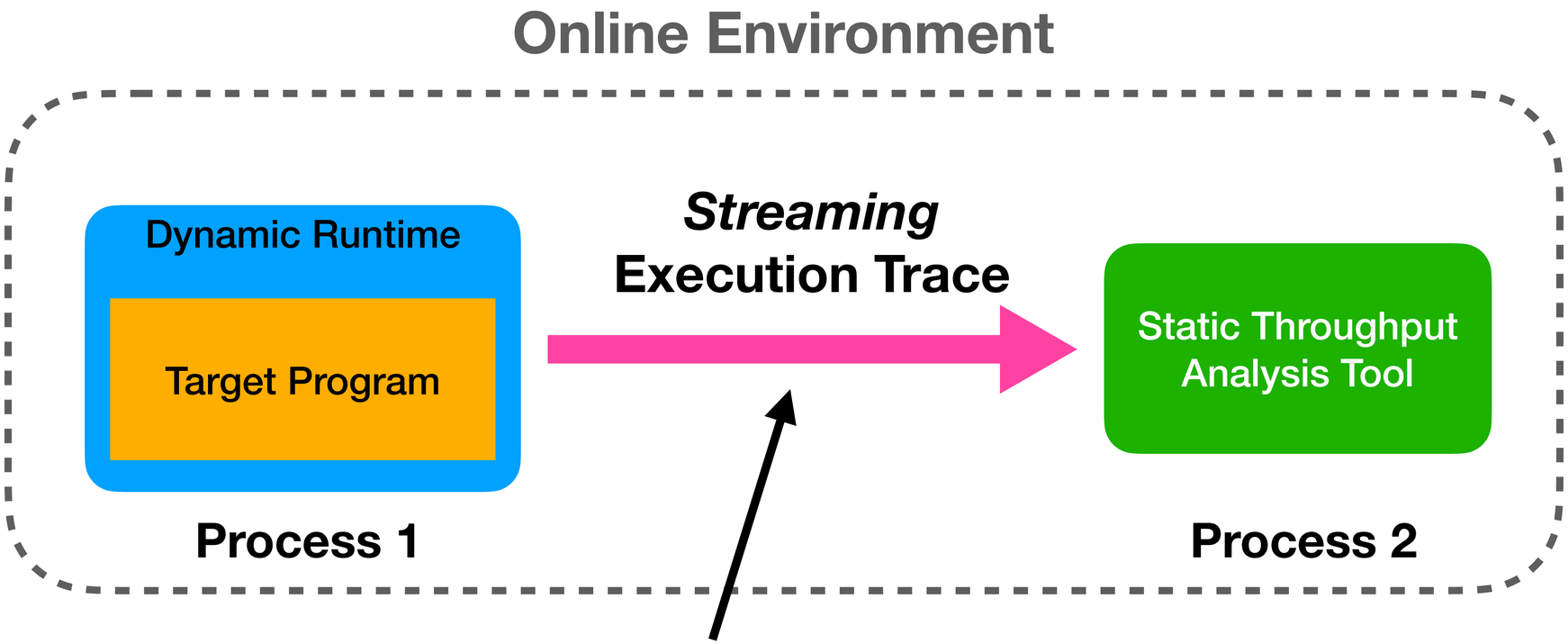

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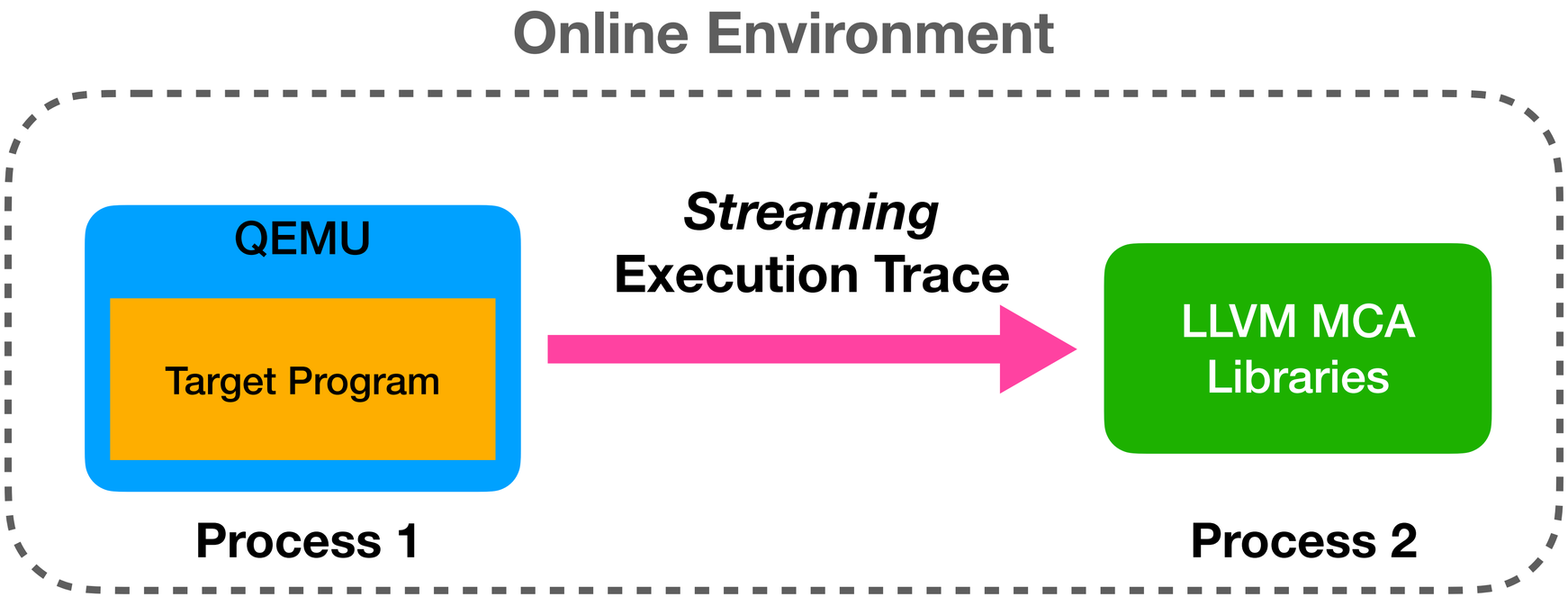

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  - New ISA (with proper scheduling info) can be supported *out of the box*
- Accounting for modern processor features: super scalar, out-of-order etc.
- Implemented via lightweight simulation
  - Abstract real CPU pipeline stages into a small handful of stages

Introduction to MCA

An example

test/tools/llvm-mca/X86/BtVer2/dot-product.s

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Summary

```
Iterations:          300
Instructions:        900
Total Cycles:        610
Total uOps:          900

Dispatch Width:      2
uOps Per Cycle:      1.48
IPC:                 1.48
Block RThroughput:   2.0
```

llvm-mca

MCAD

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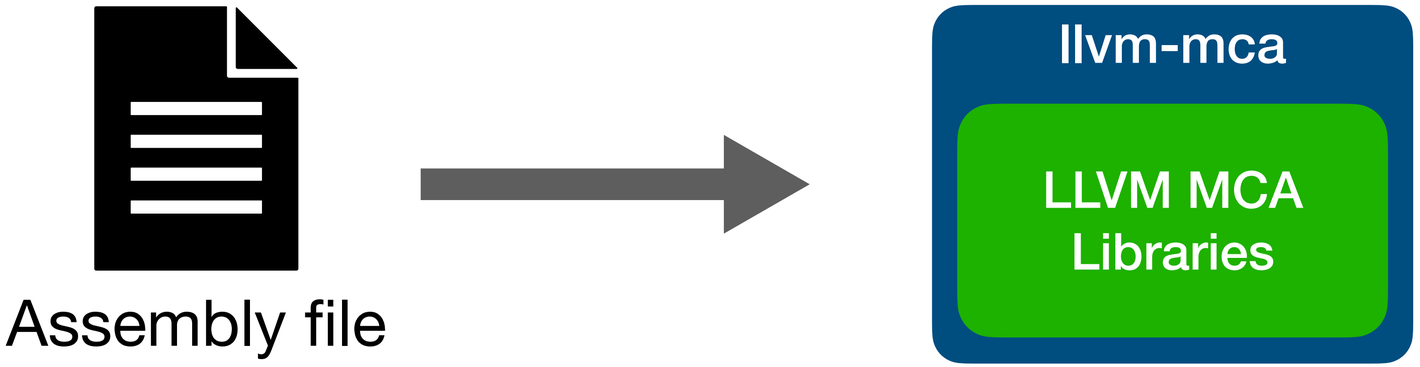
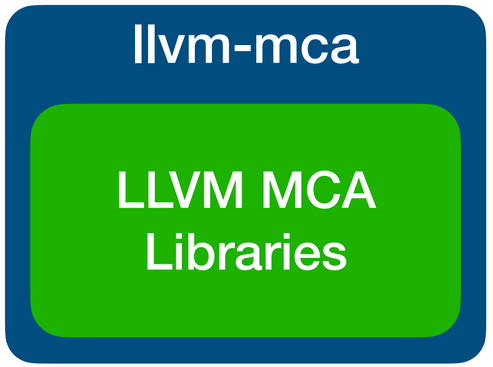


MCAD

llvm-mca

Assembly file



MCAD

Process 1

Streaming
Execution Trace

Process 2

MCA Daemon (MCAD)

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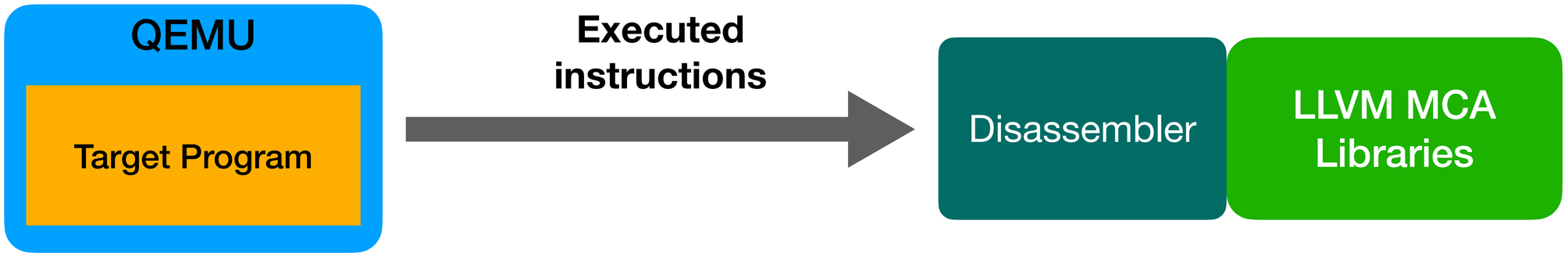
- Augment the analysis region *beyond* basic blocks
  - MCAD is able to analyze the **entire** program execution trace
- Throughput analysis is happening **in parallel** / **on-the-fly** with the target program execution

Implementation

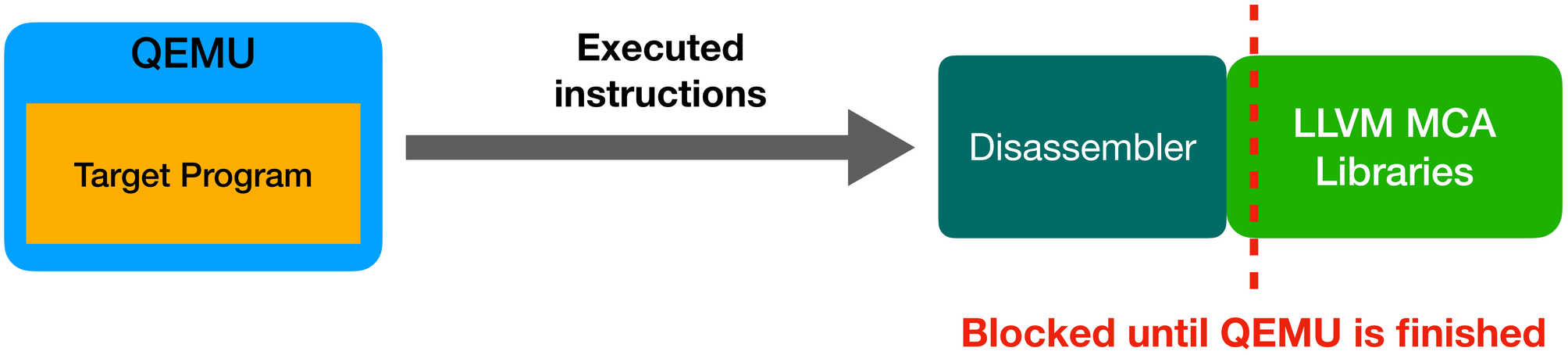
Analyze execution traces using MCA

Using unmodified MCA libraries



Analyze execution traces using MCA

Challenge: Sequential workflow



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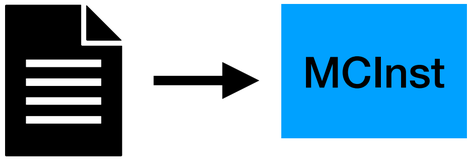

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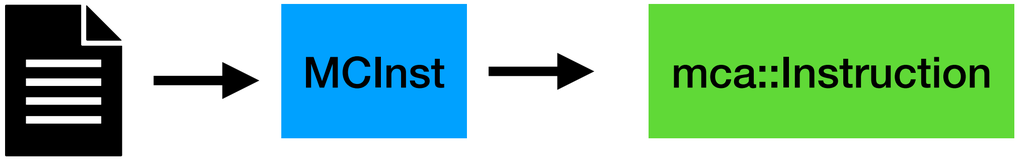

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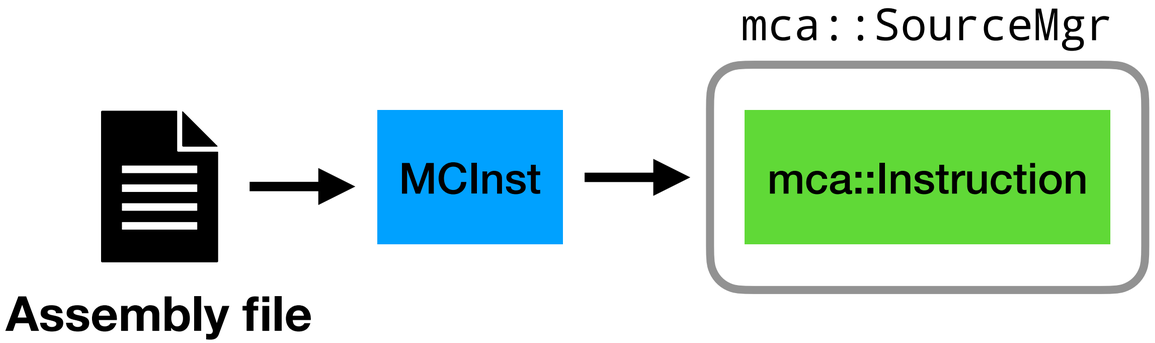

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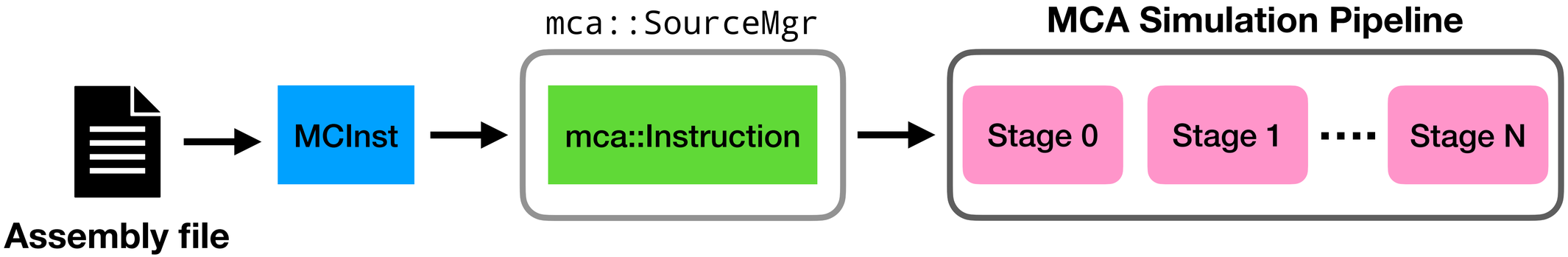

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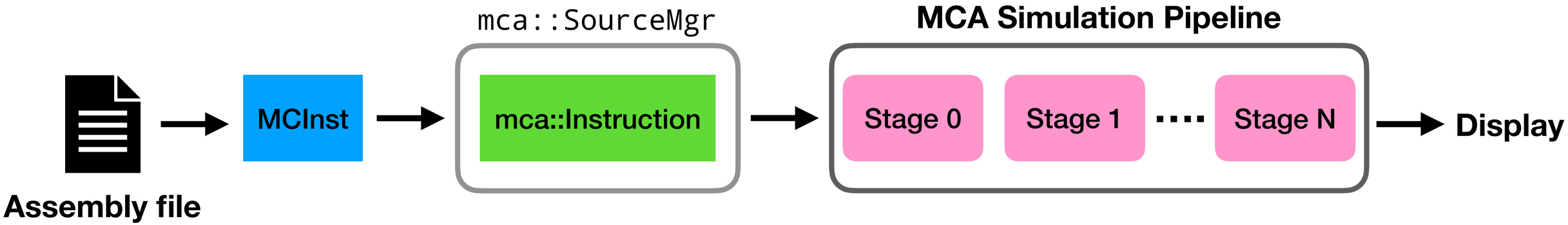
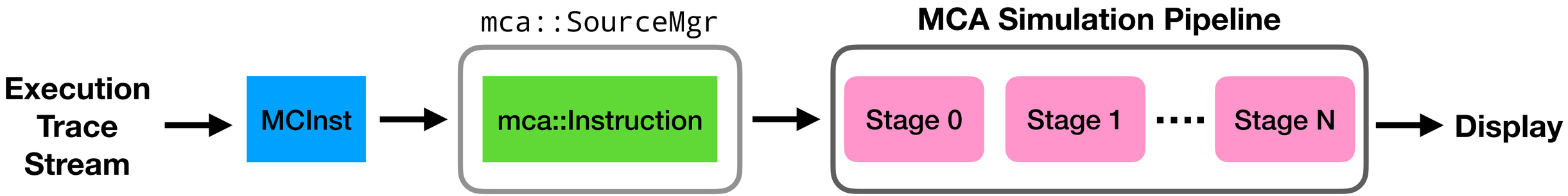


MCA with execution trace stream as input



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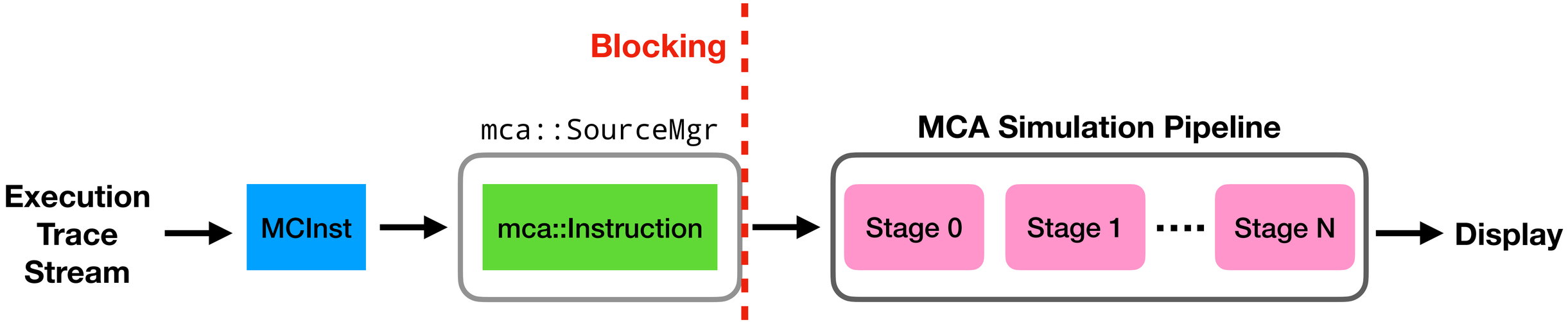
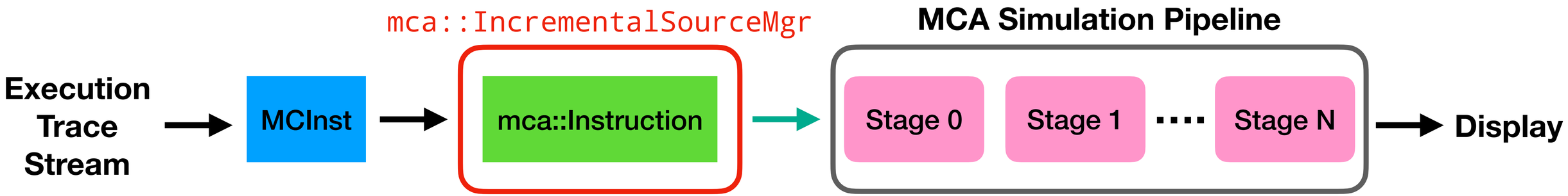


Incremental SourceMgr



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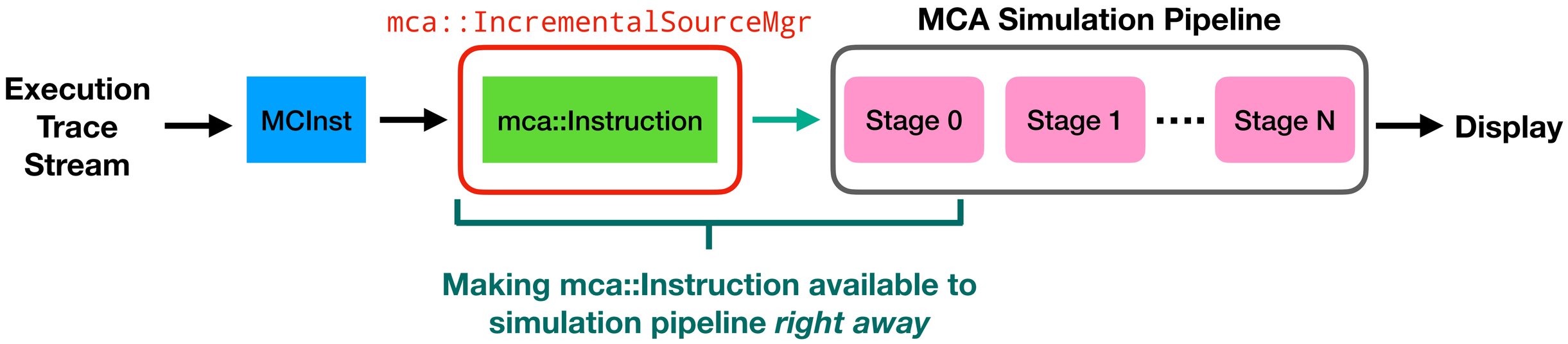

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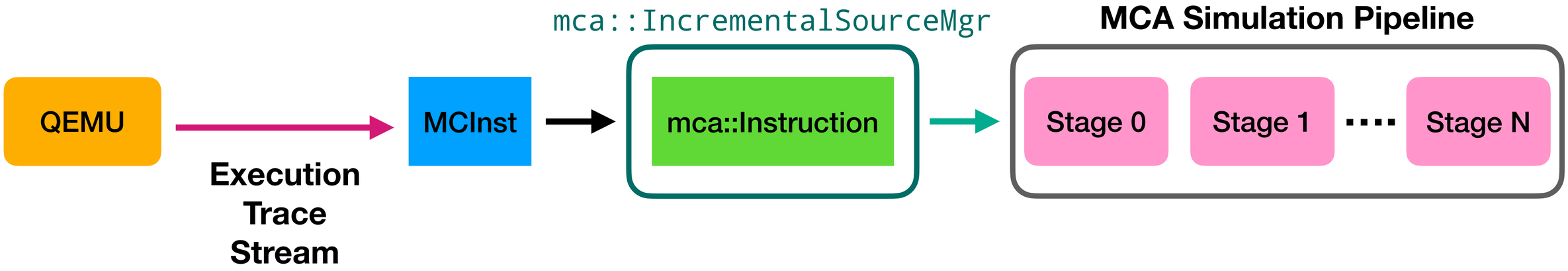

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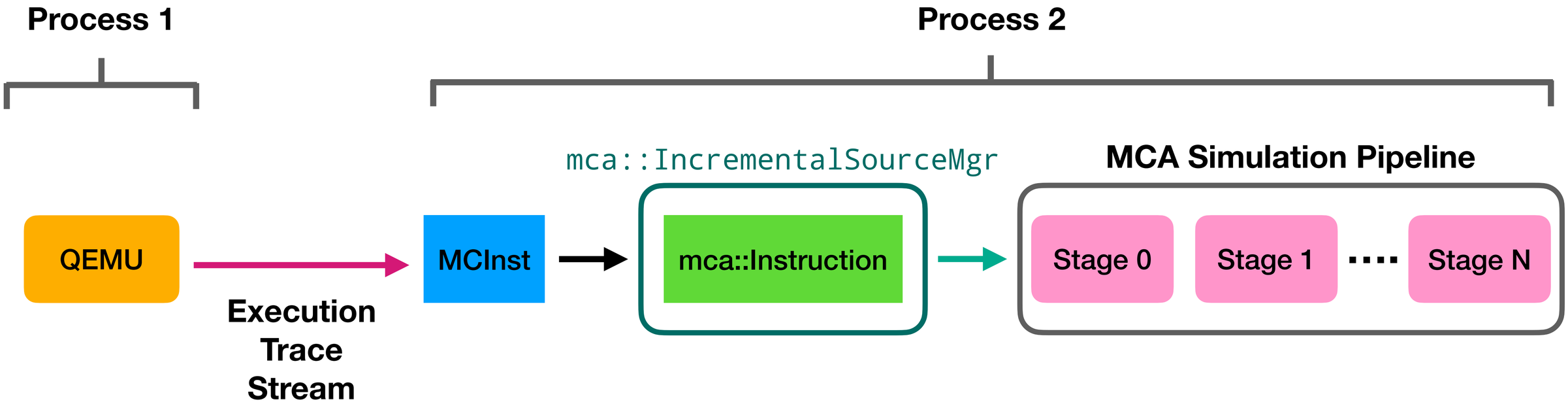

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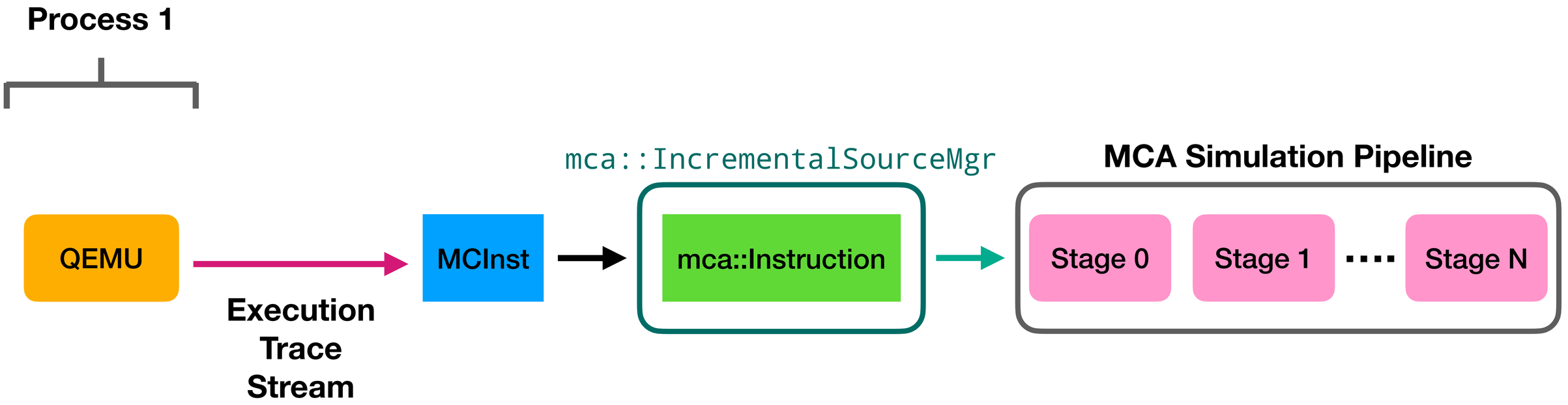
Implement with threads



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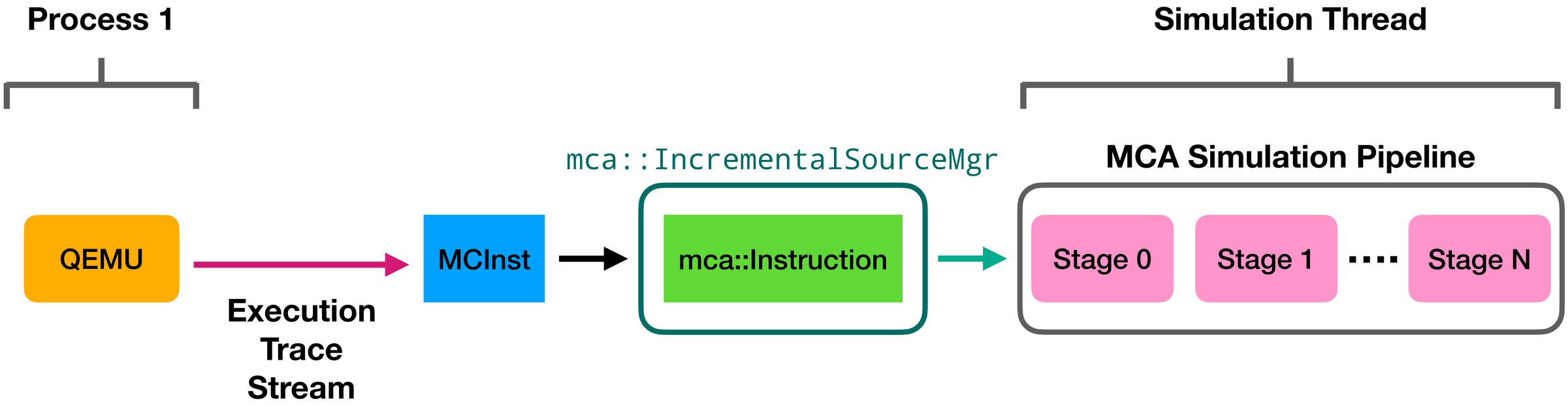

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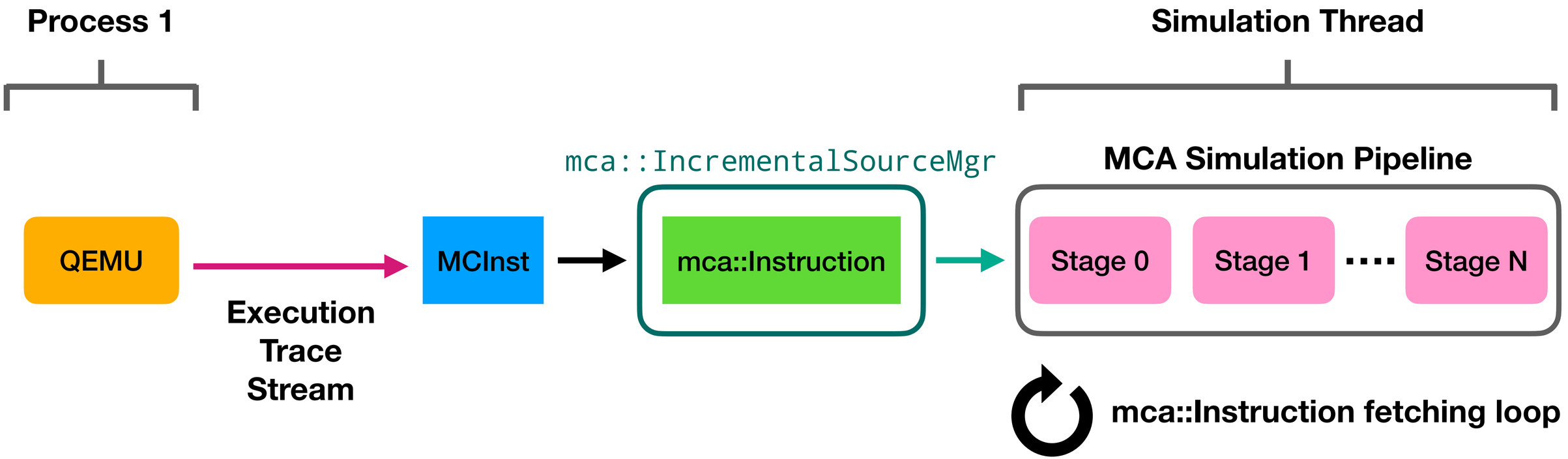

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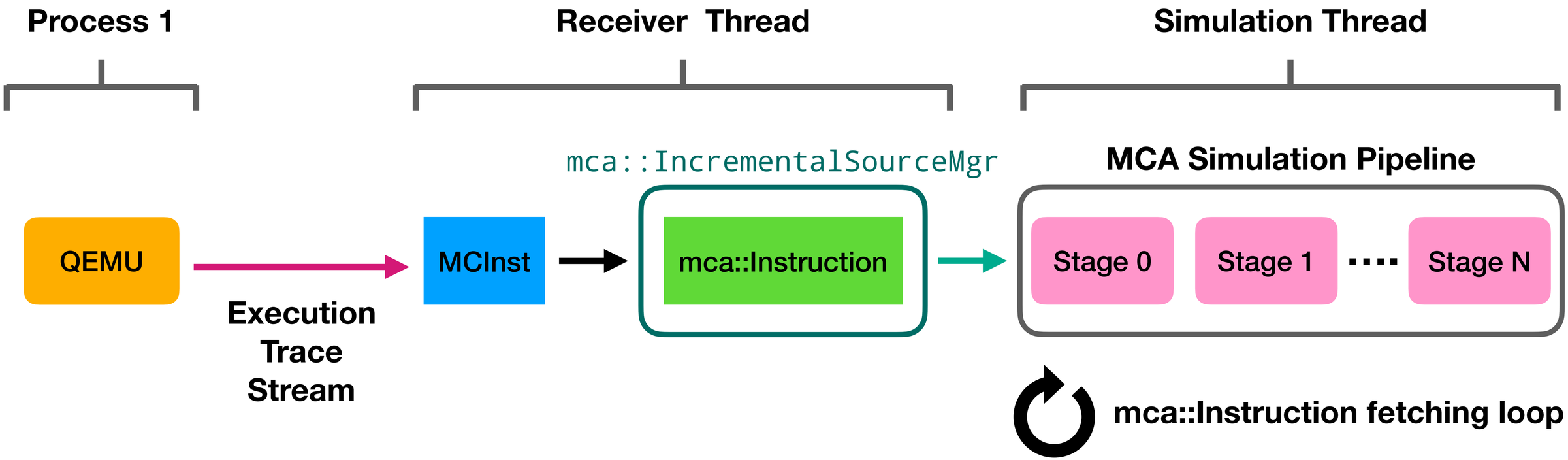
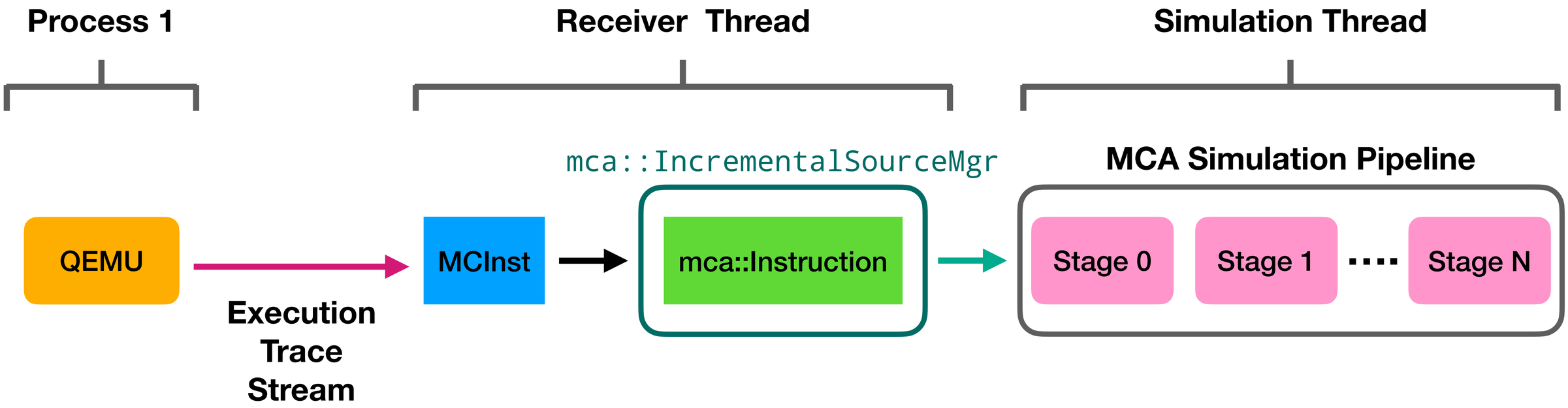


Incremental SourceMgr

Implement with threads: Pros & Cons



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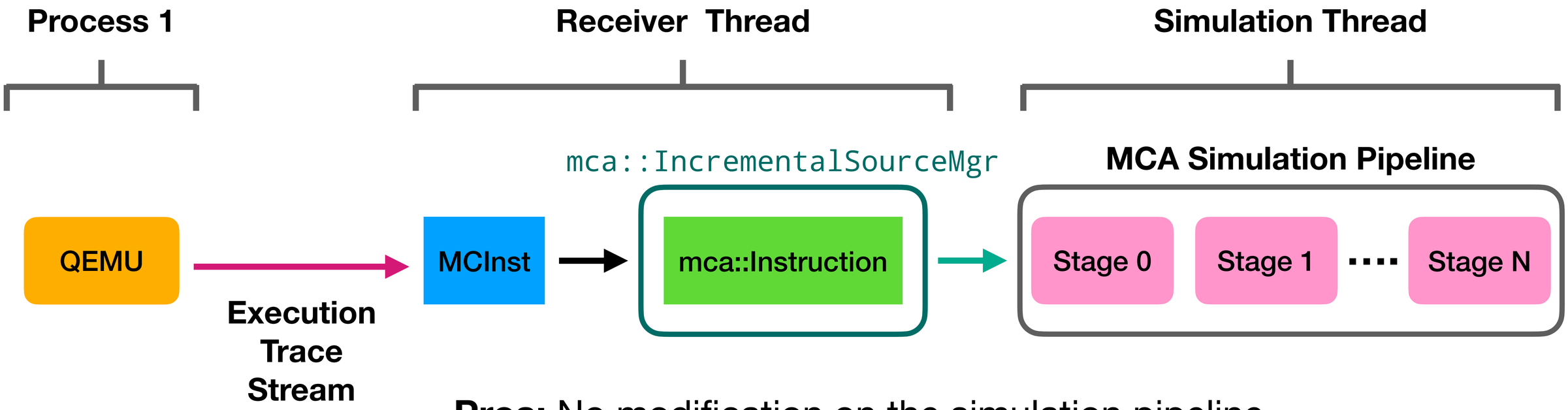

Pros: No modification on the simulation pipeline

Incremental SourceMgr

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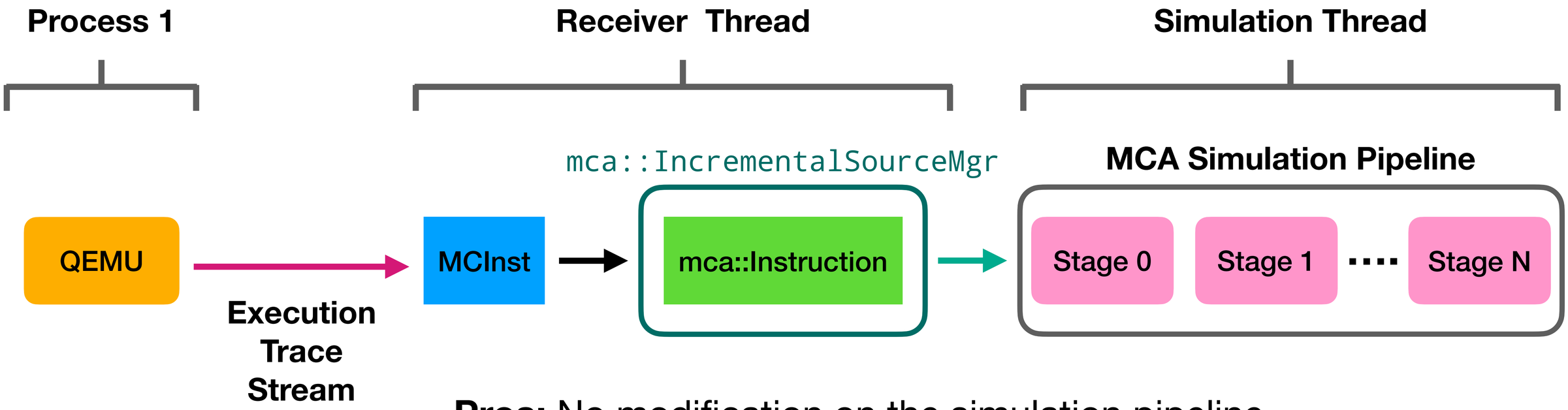
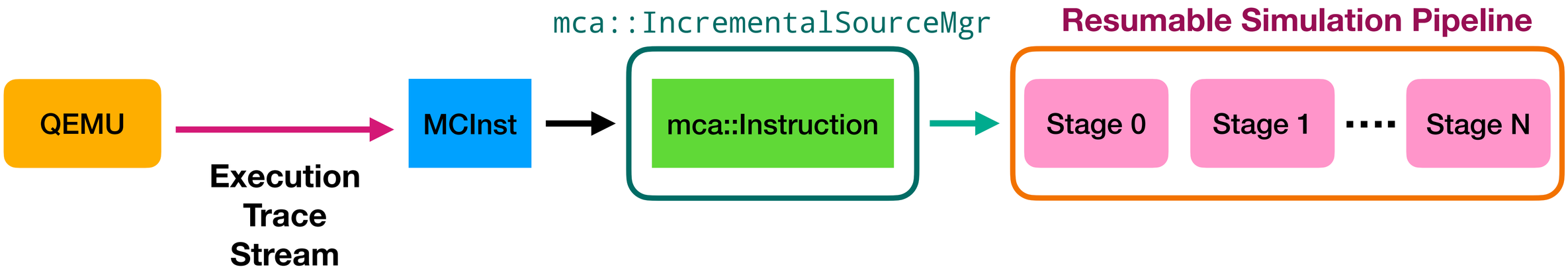


Pros: No modification on the simulation pipeline

Cons: To use IncrementalSourceMgr, you *have to* use threads

Incremental SourceMgr

Better solution: Resumable simulation pipeline



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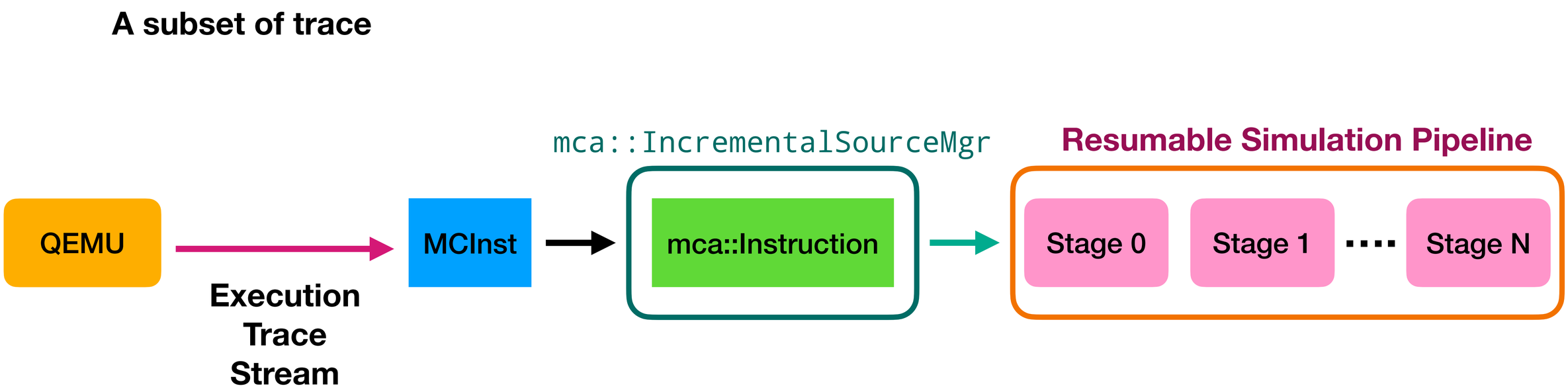

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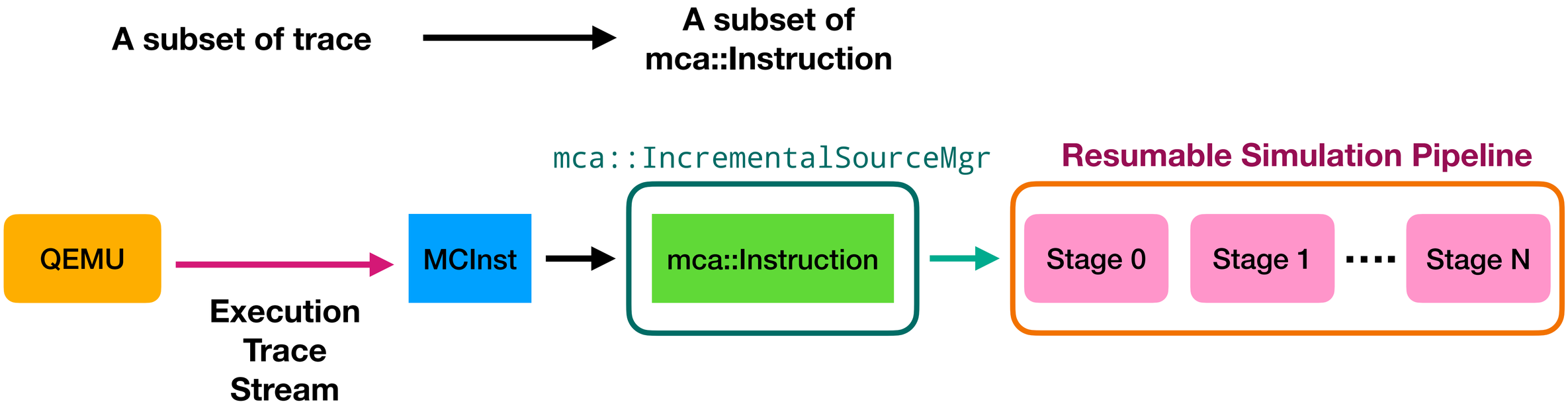

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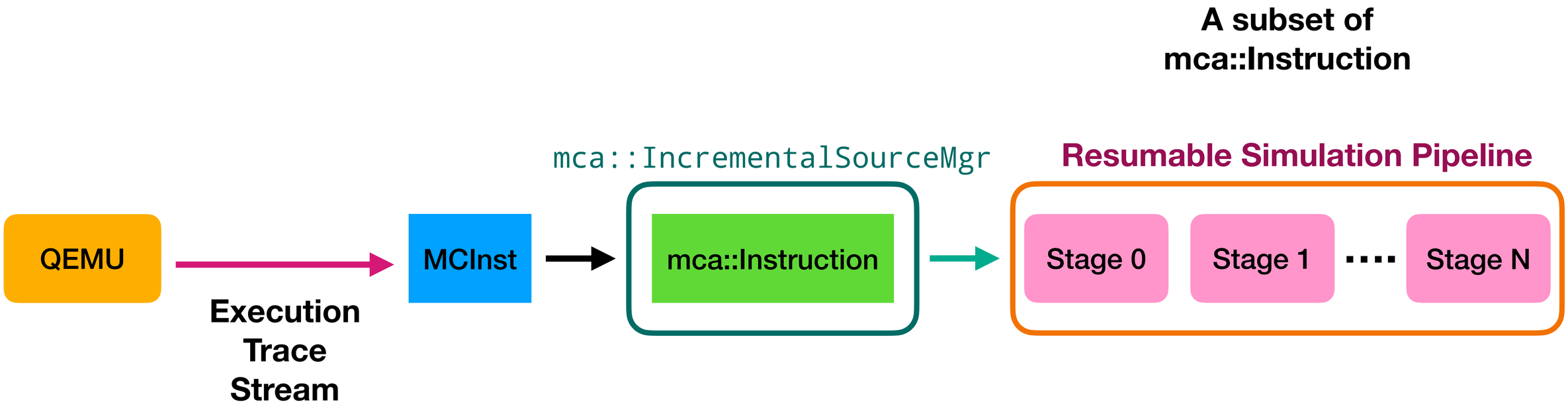

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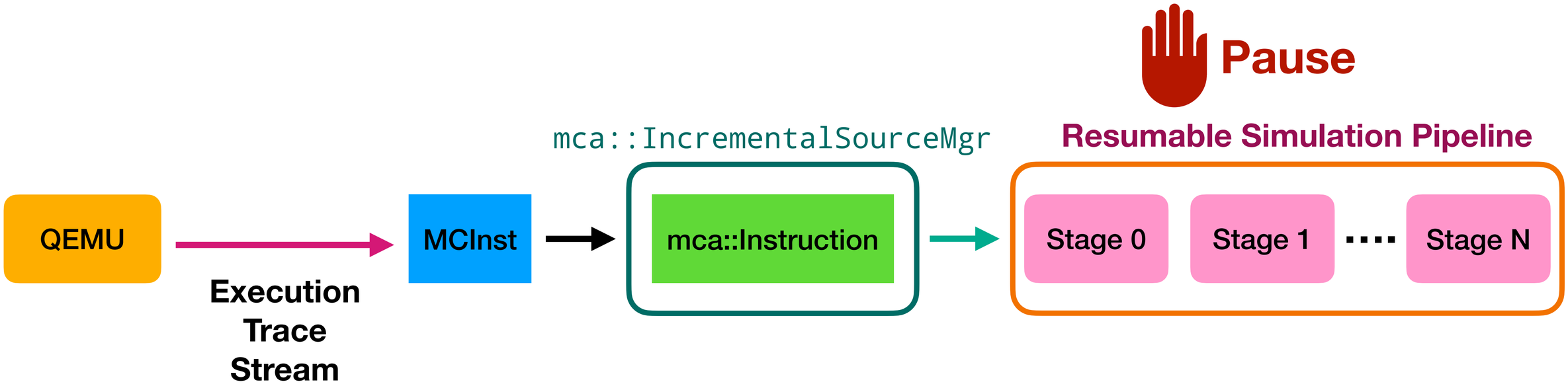

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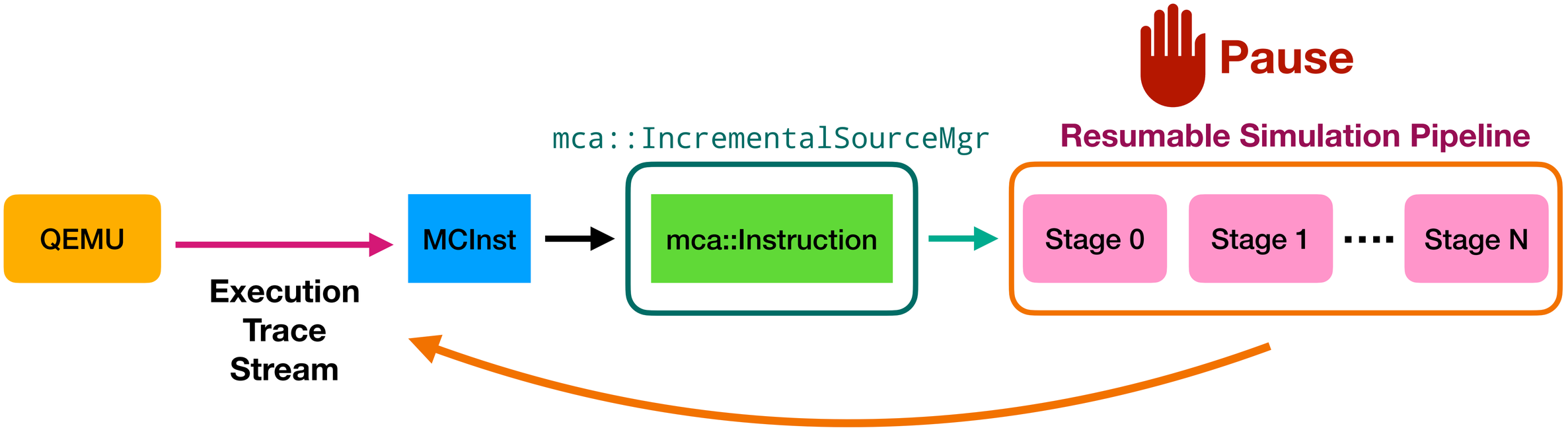

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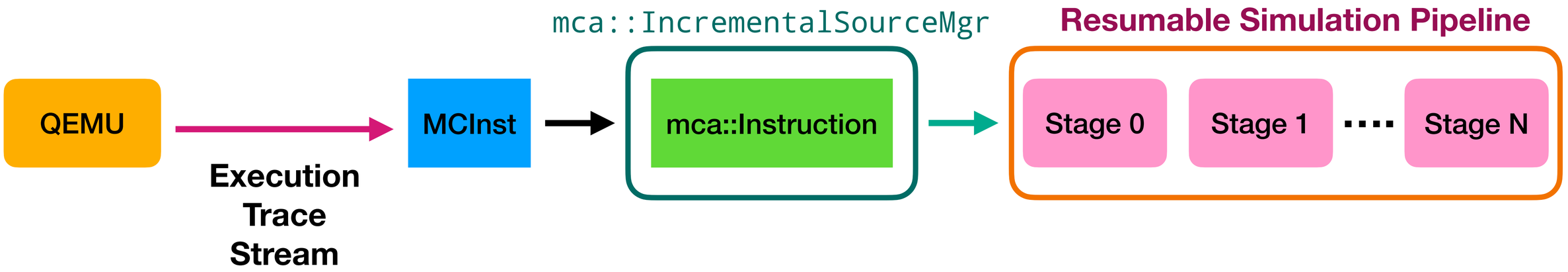
- Minor downside: Modifications on the simulation pipeline

Incremental SourceMgr + Resumable pipeline

Put into real actions



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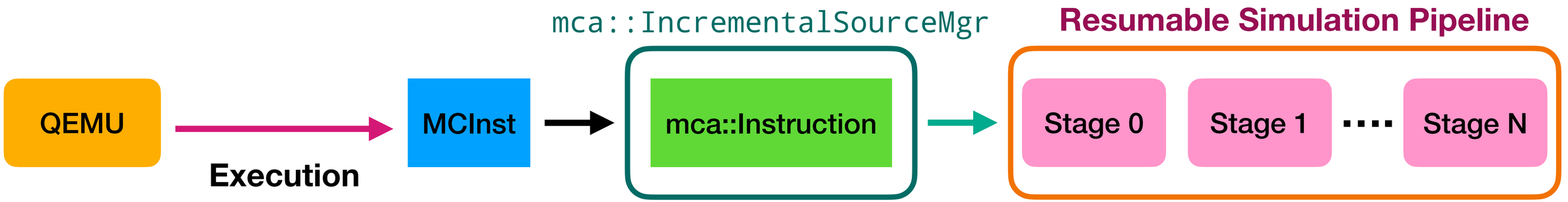

- A program that continuously reads from an I/O device

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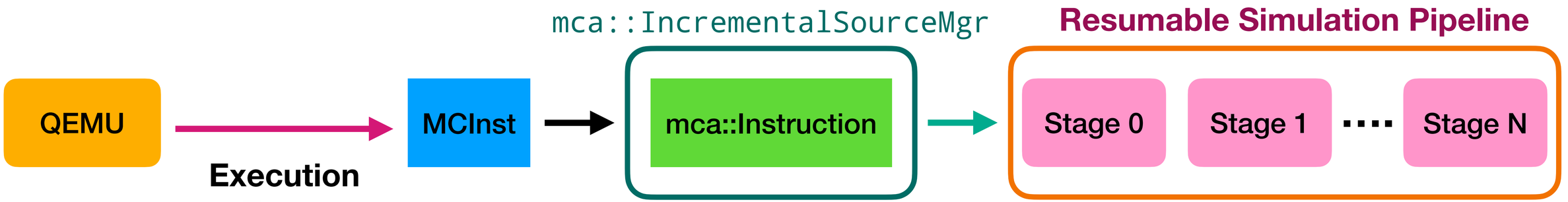

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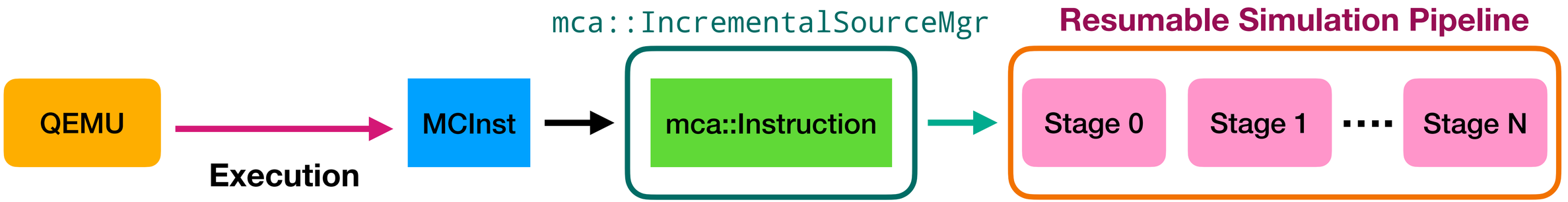

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- Collected **~1 million** instructions

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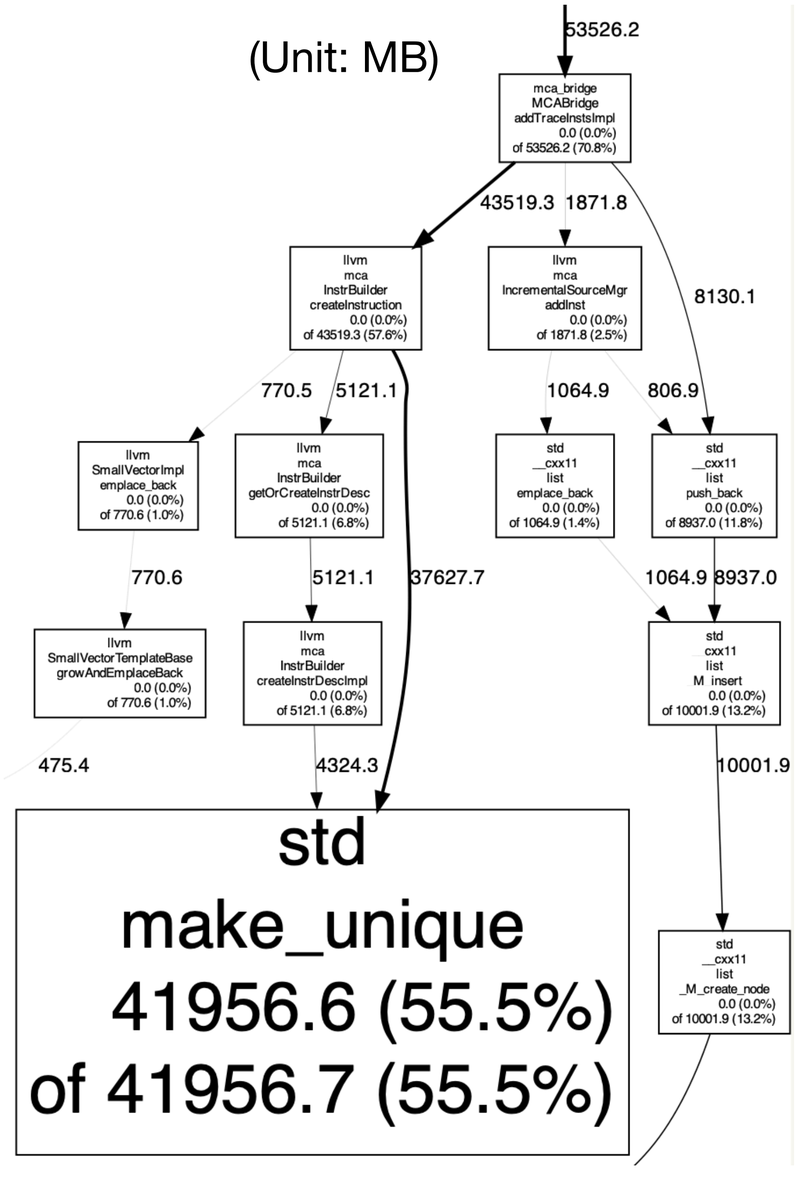

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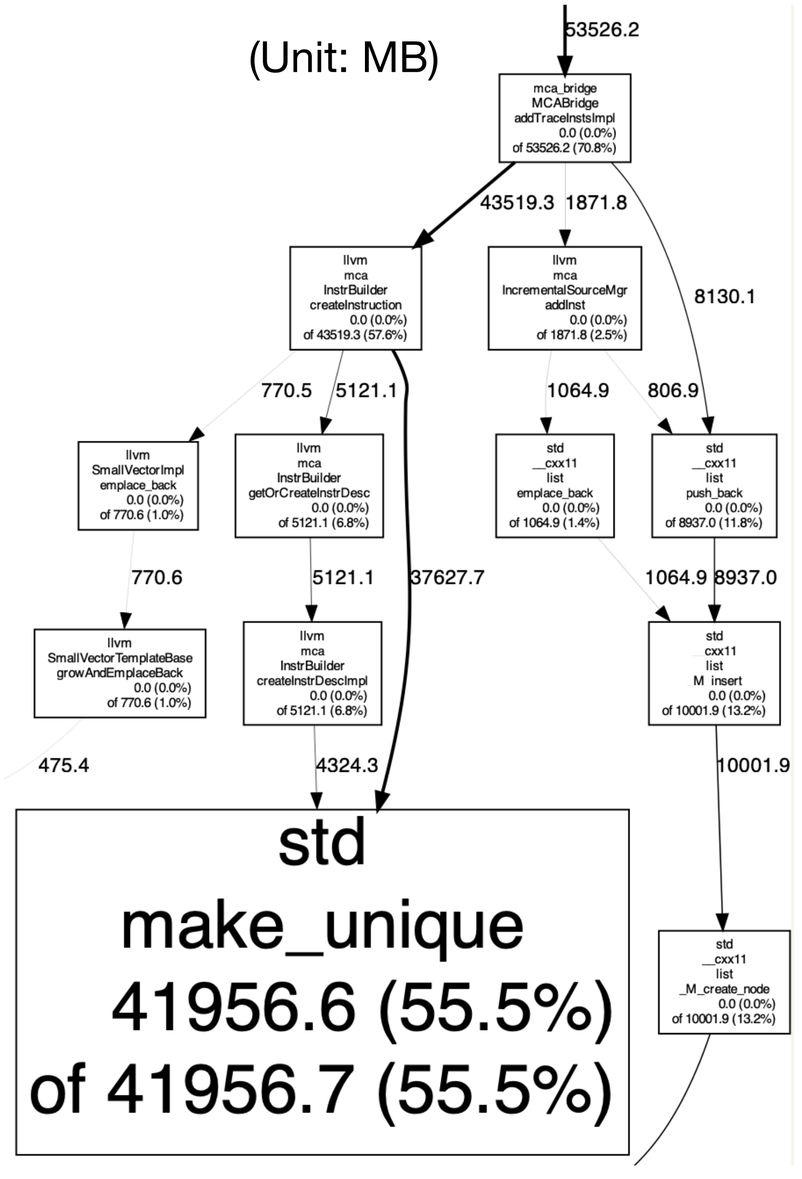

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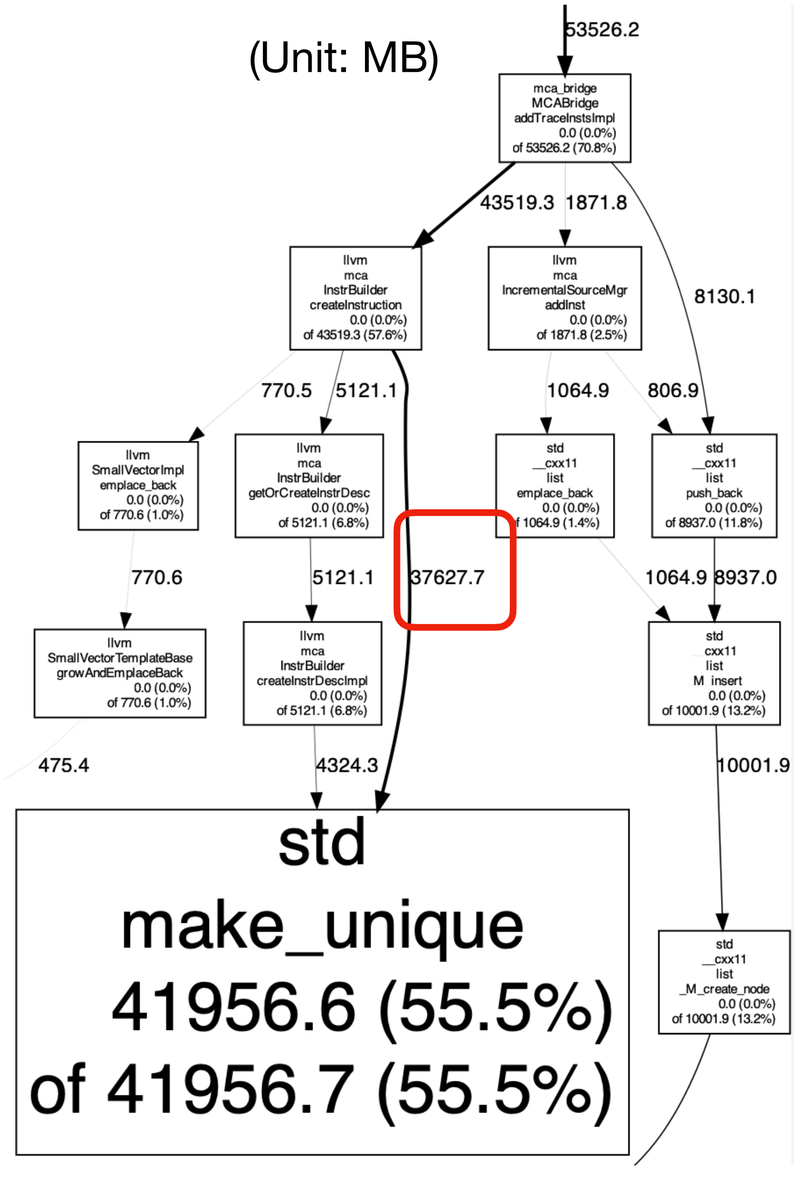

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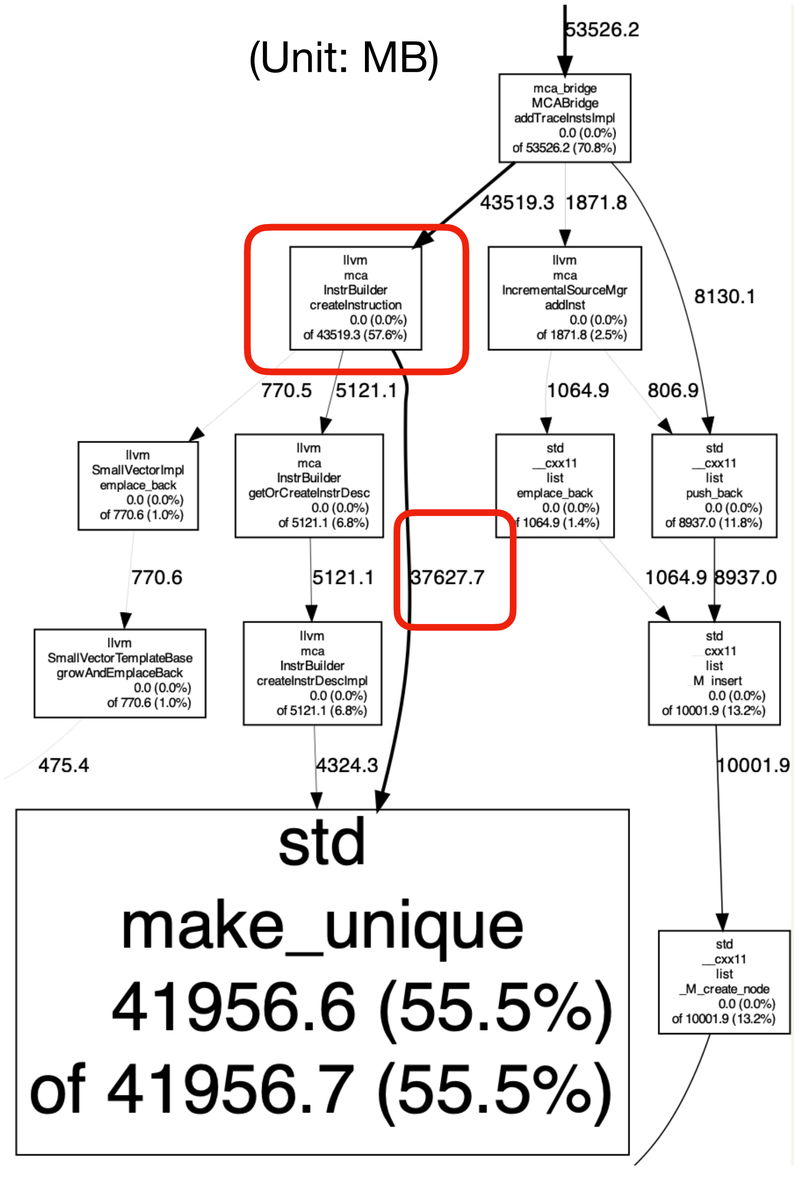

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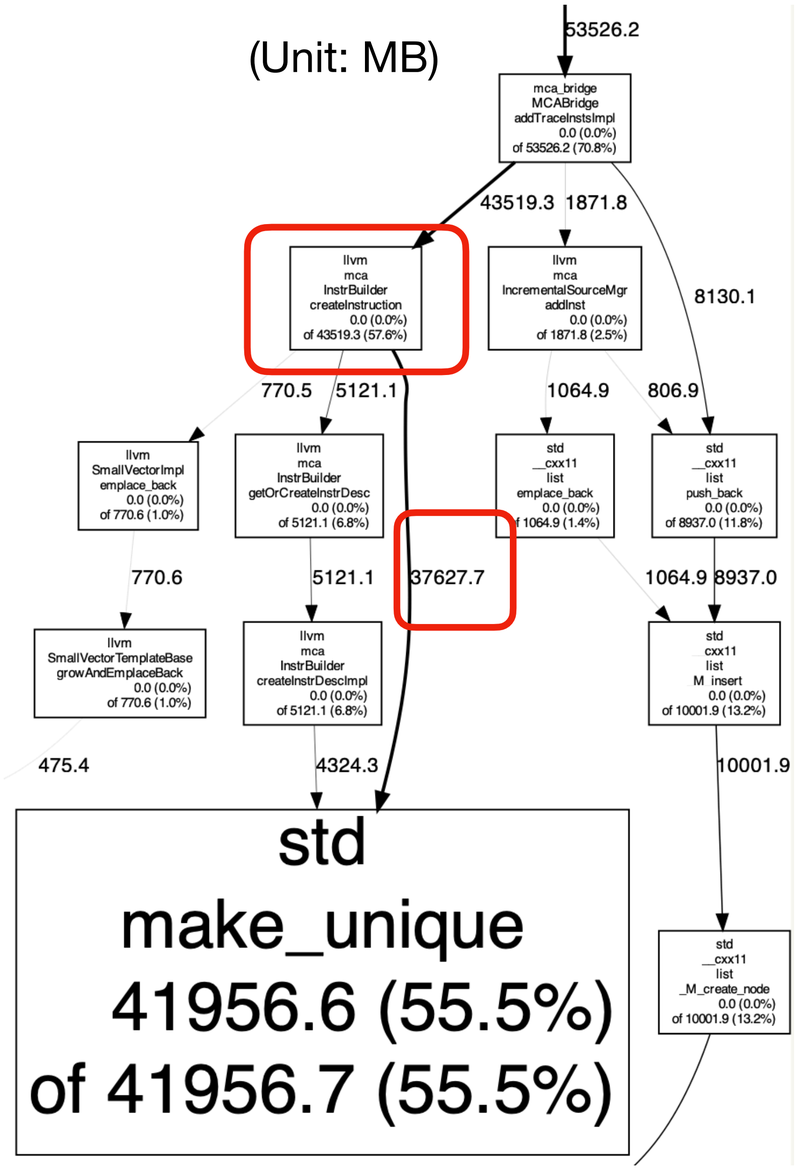

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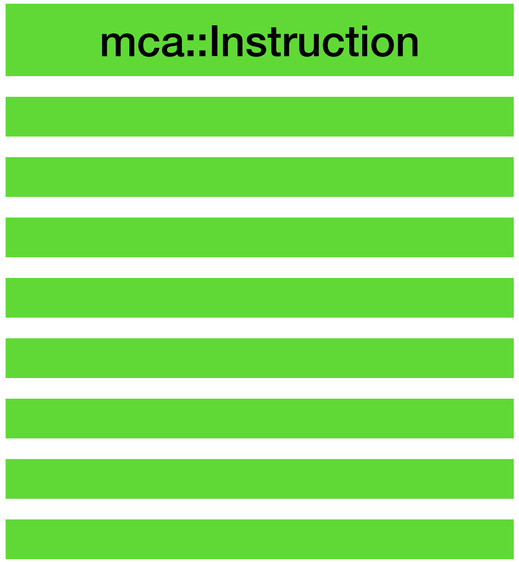
- `mca::Instruction` is also used for tracking simulation state, so it's hard to make it immutable
- Doesn't scale really well with large input (recall: ~1 million instructions)

Large memory footprint

Observation

`mca::IncrementalSourceMgr`



Resumable Simulation Pipeline

Large memory footprint

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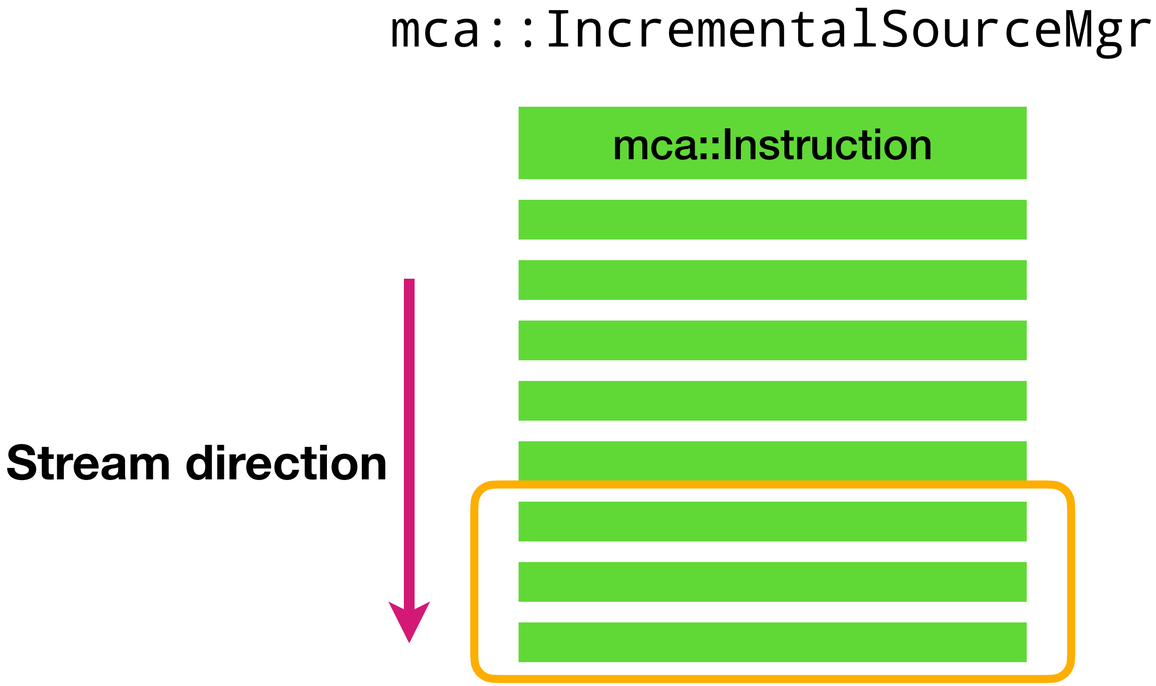

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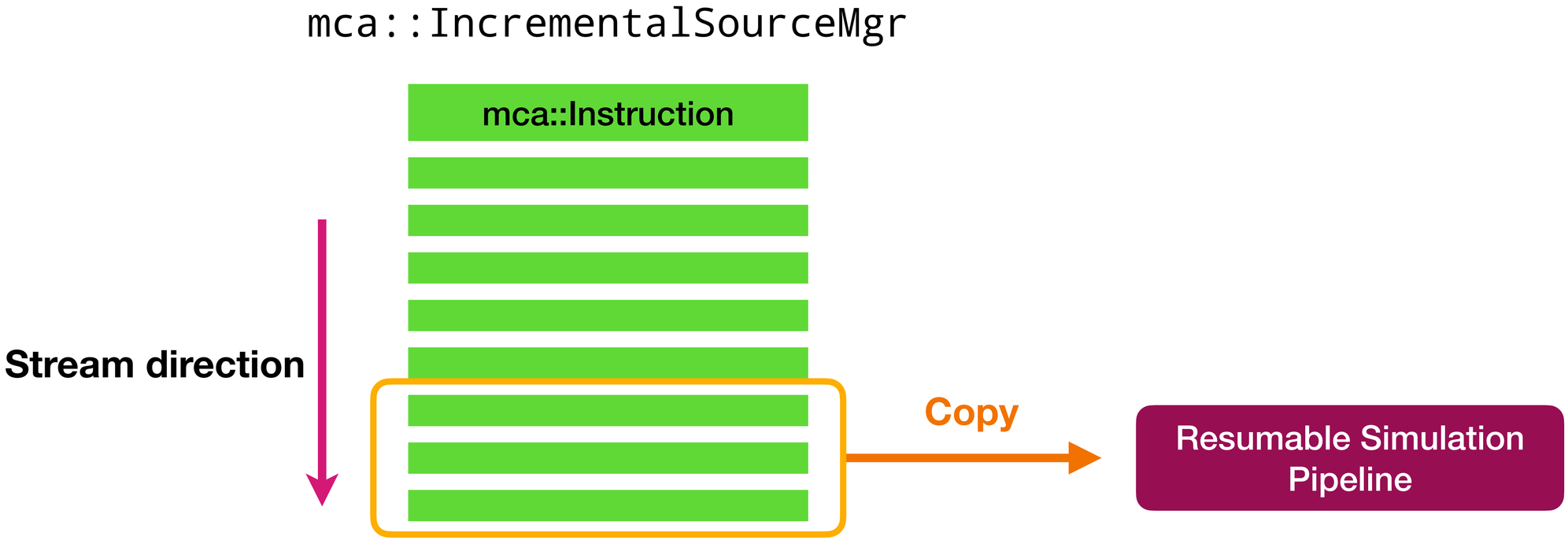

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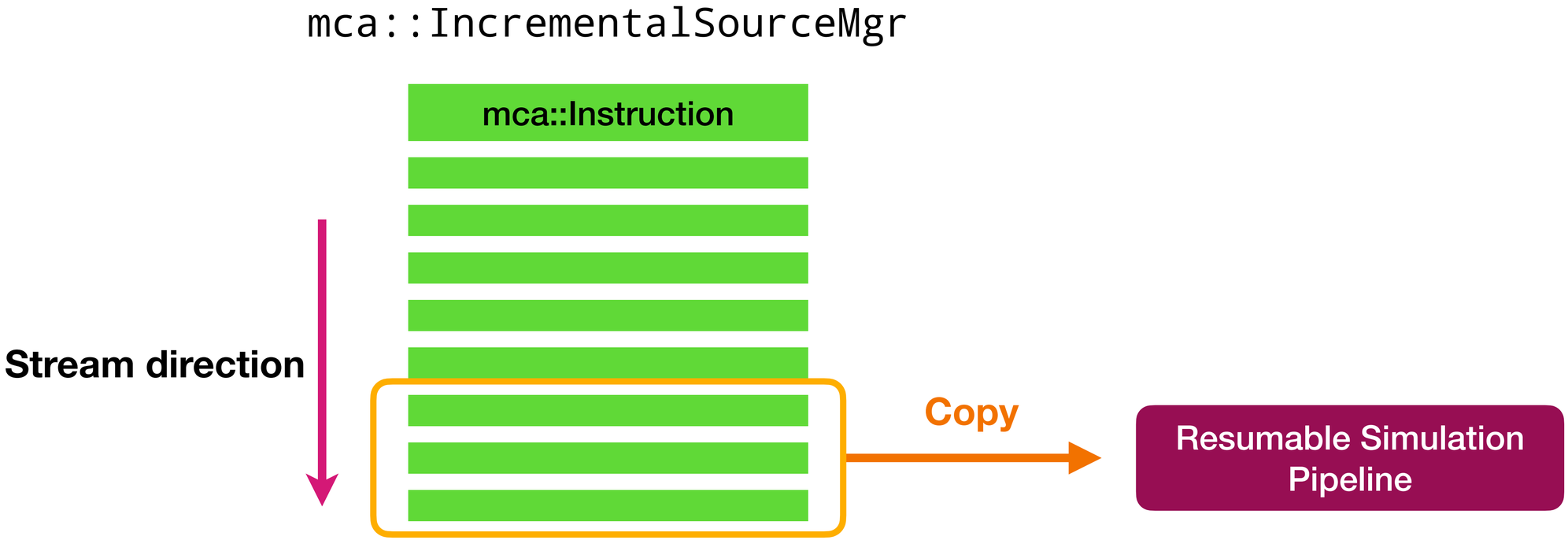

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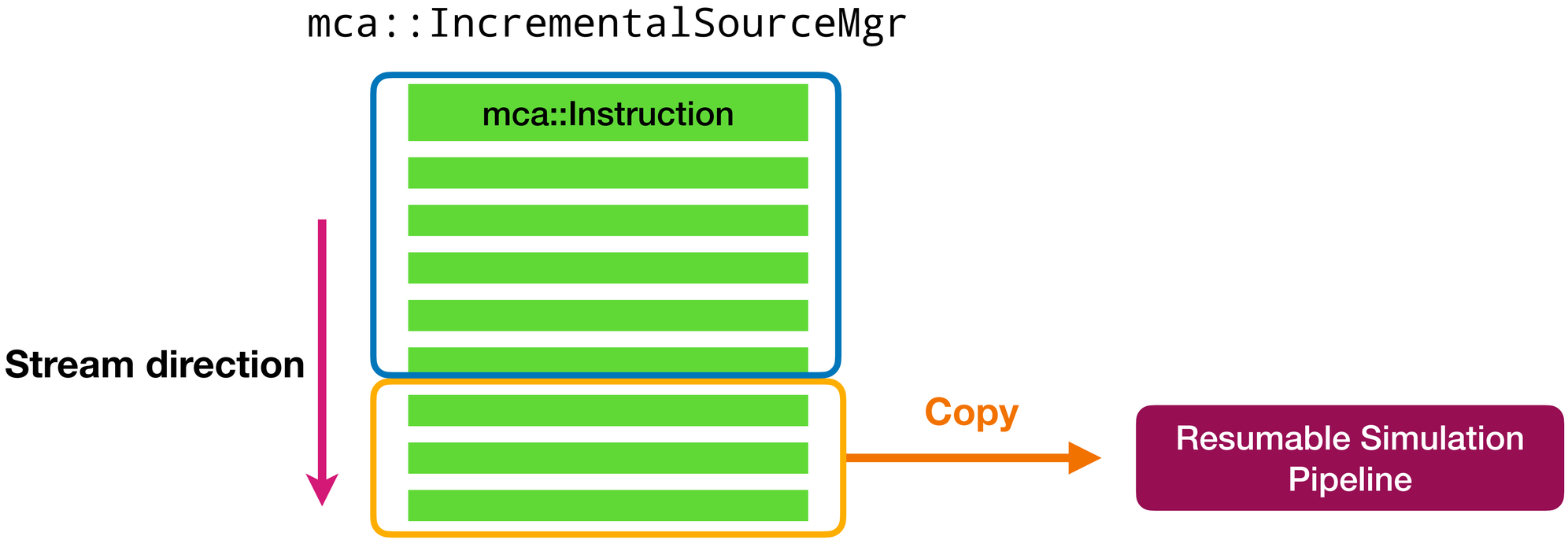

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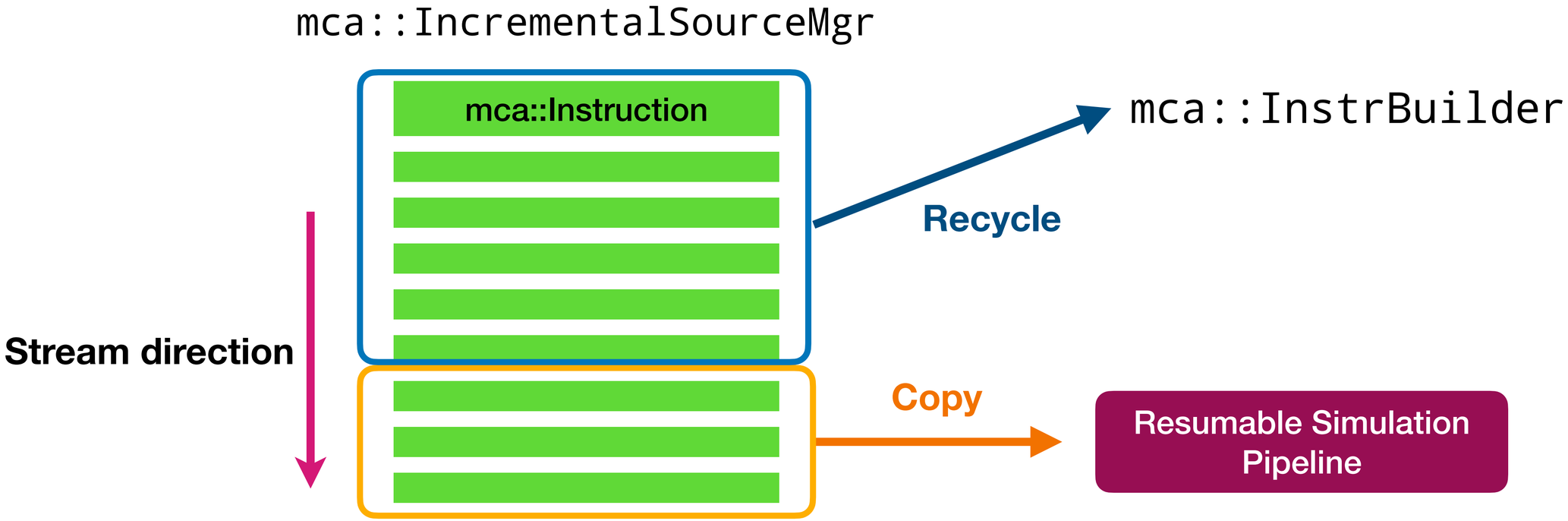


67%

improvement on accumulated memory consumption

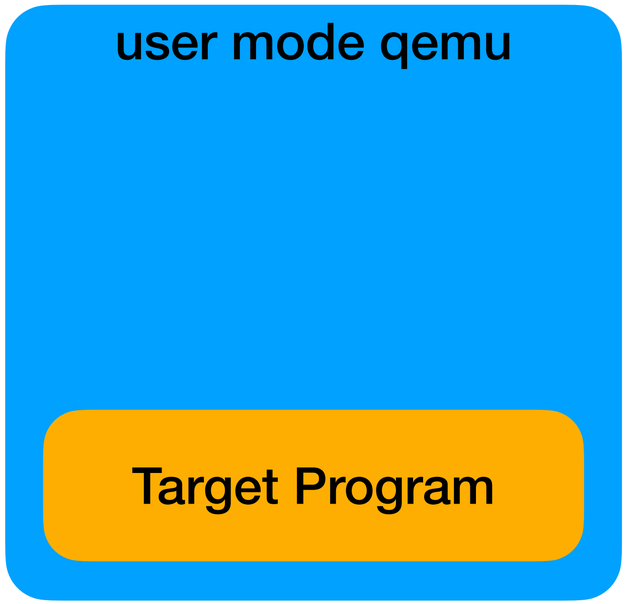
~70%

of the mca::Instruction objects are recycled

Collecting execution traces via QEMU

QEMU

MCAD



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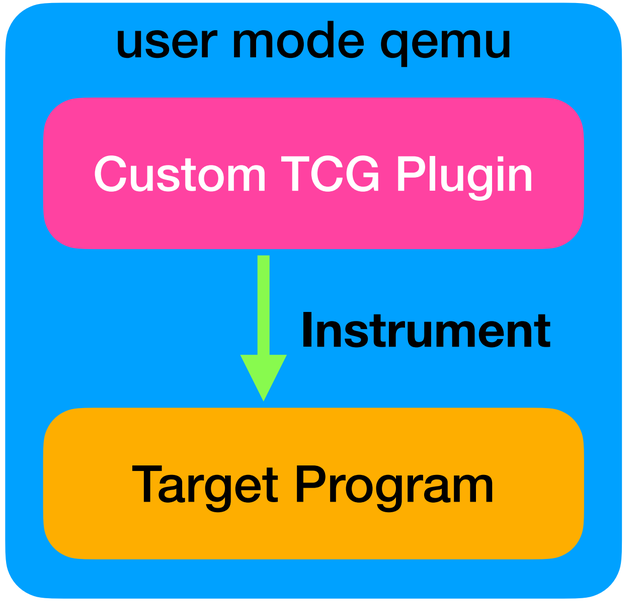

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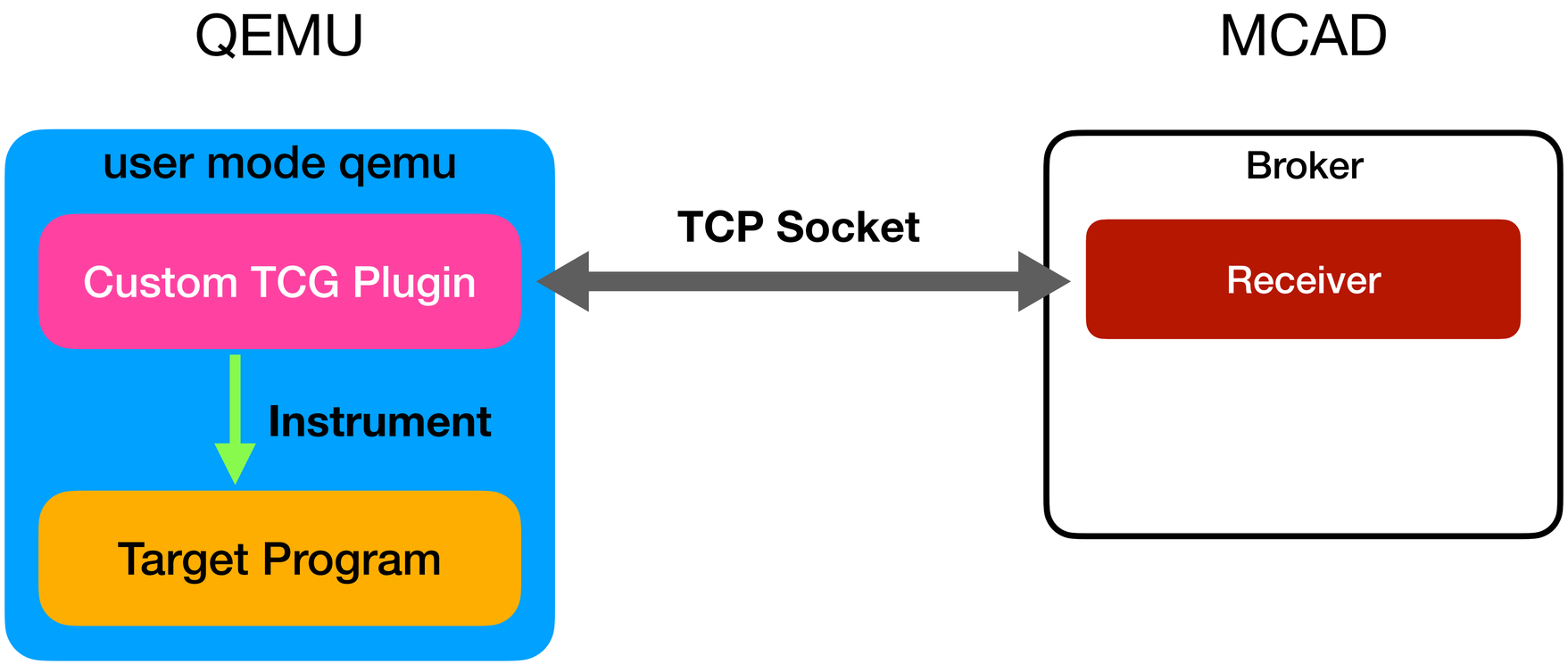

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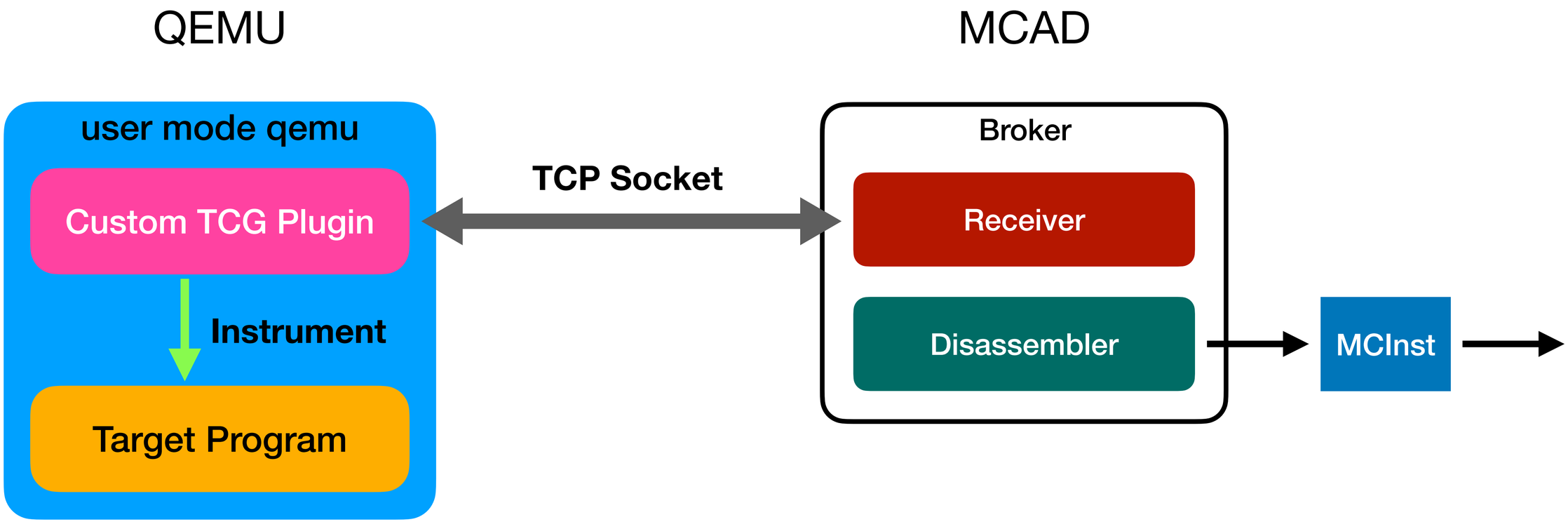

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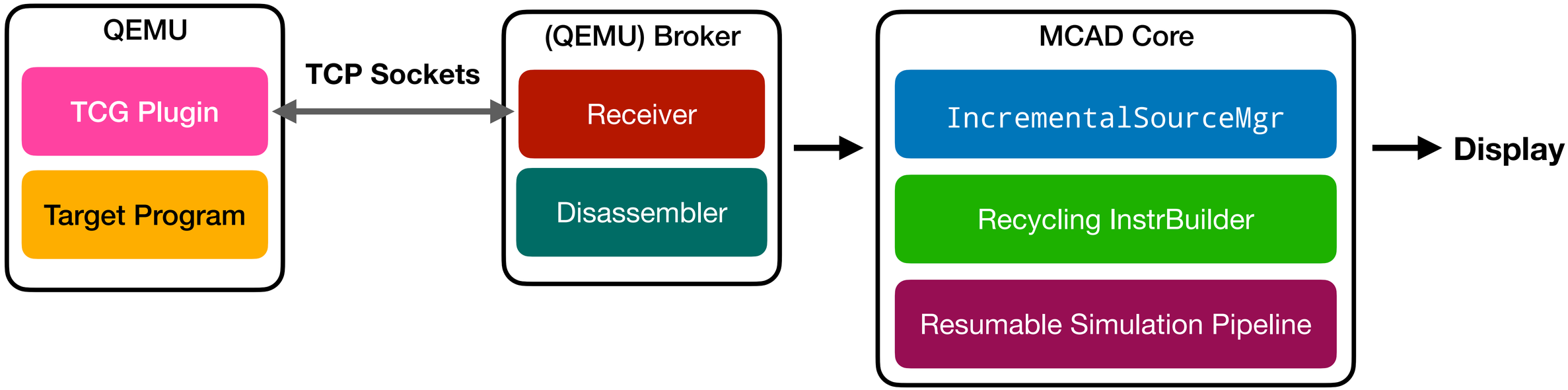
- Sending raw binary instructions* through TCP sockets

Complete structure of MCAD



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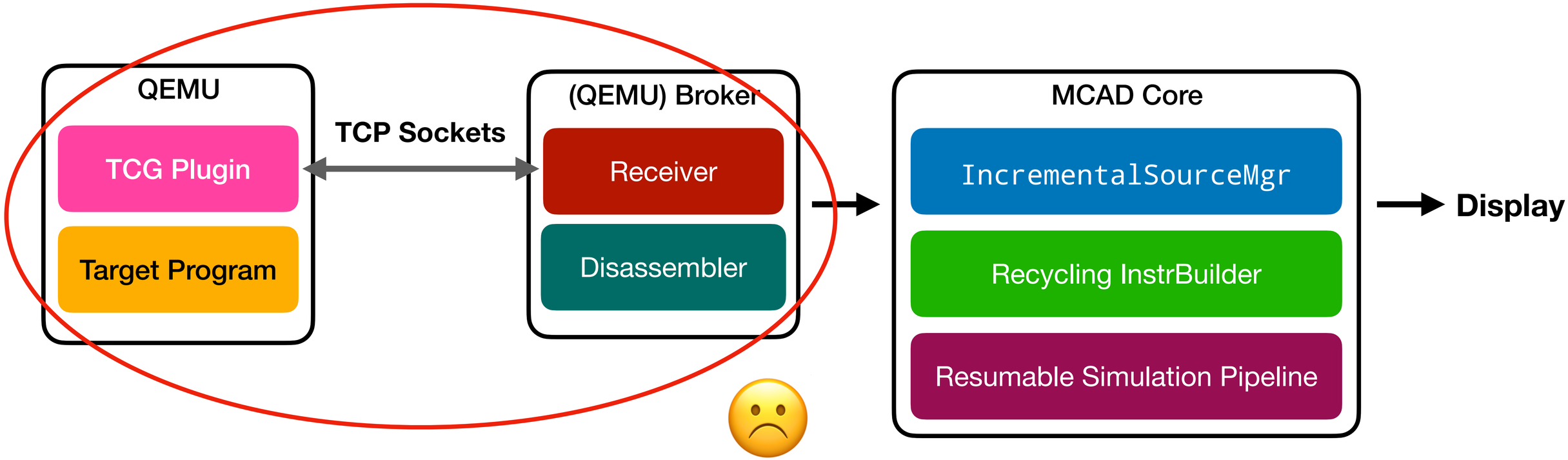

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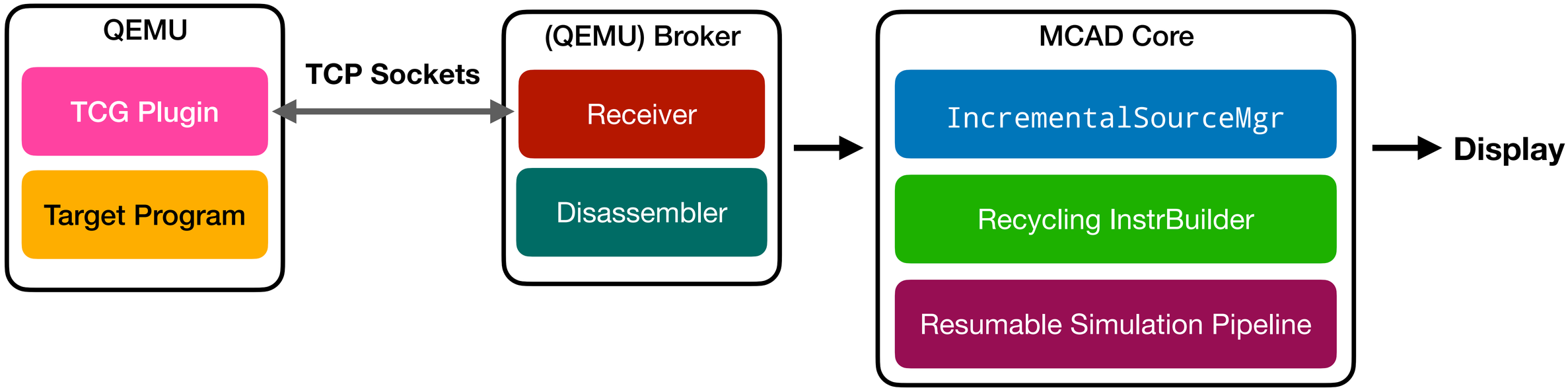
A modular design



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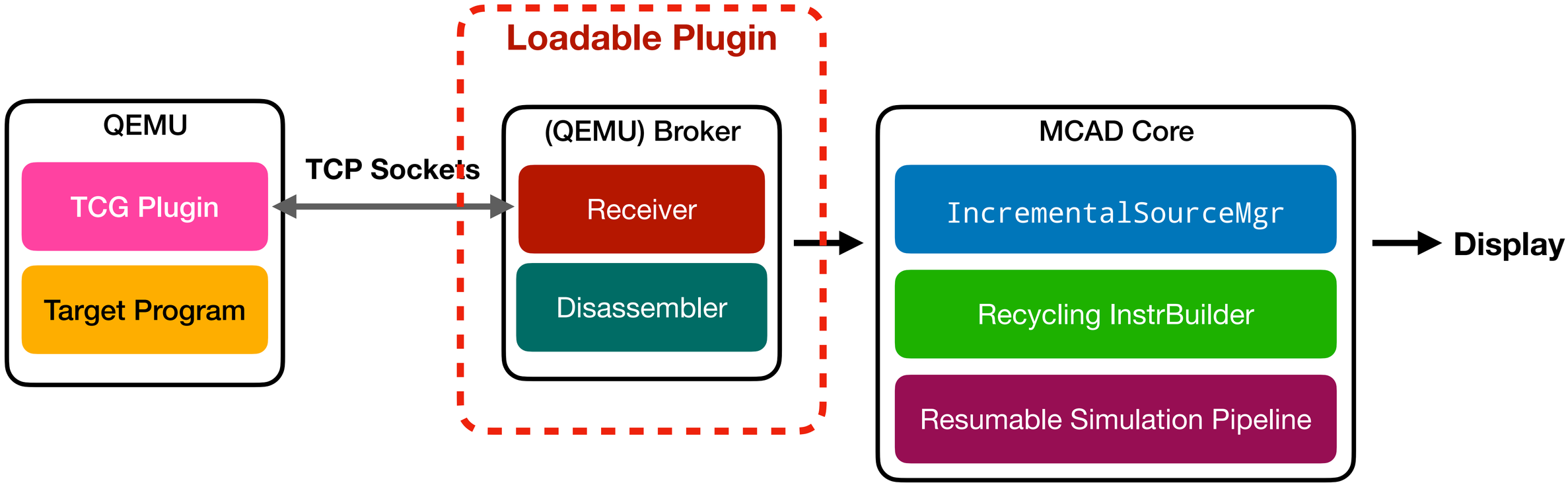
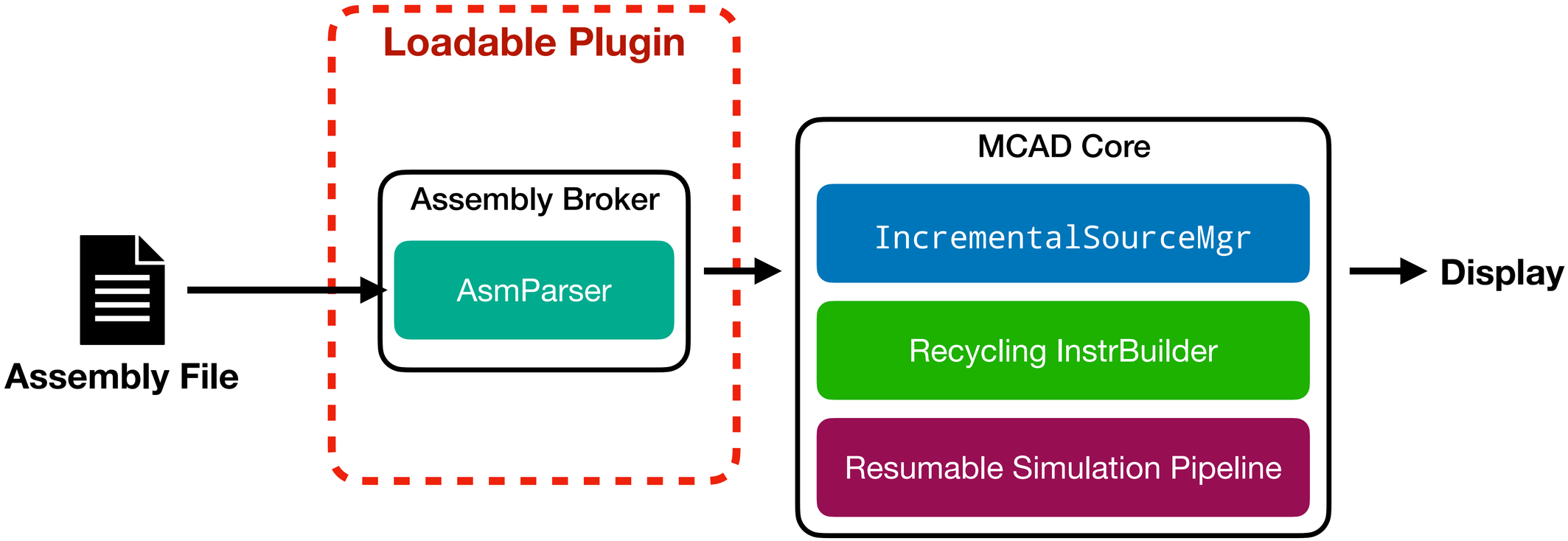


Complete structure of MCAD

Example: Assembly broker plugin



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- For baseline, we dump the execution trace (assembly instructions) to a file before feeding into llvm-mca
  - Time measurement on baseline only accounts for llvm-mca's run time. **Excluding** the trace collection time.

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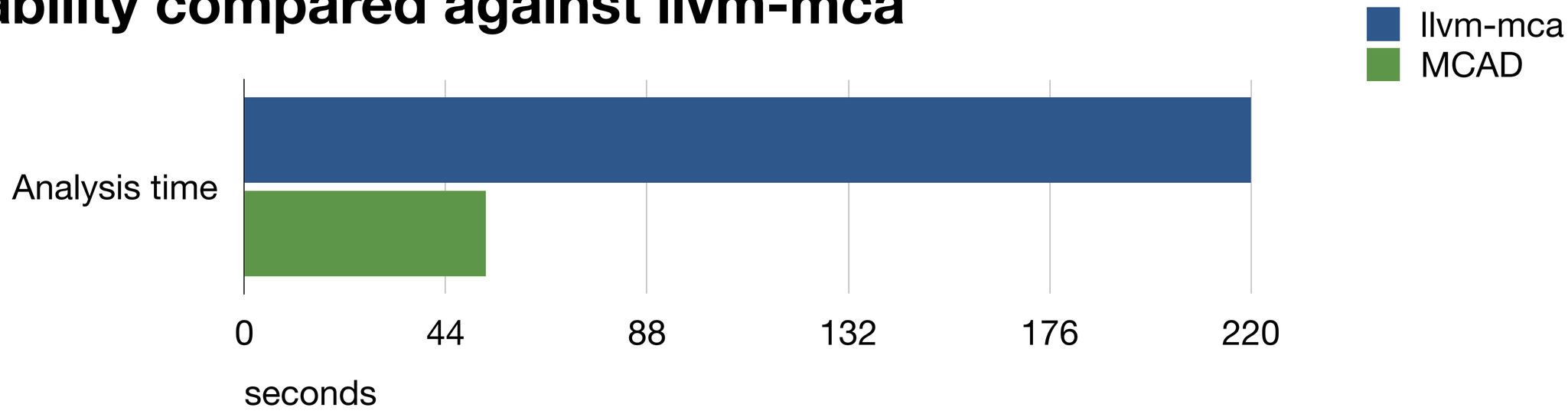

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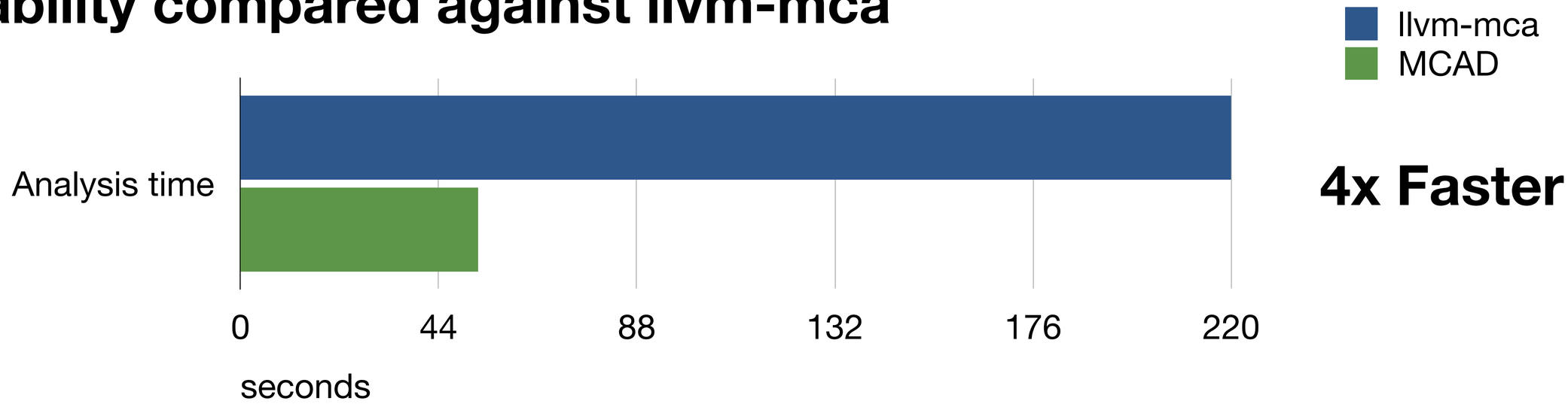

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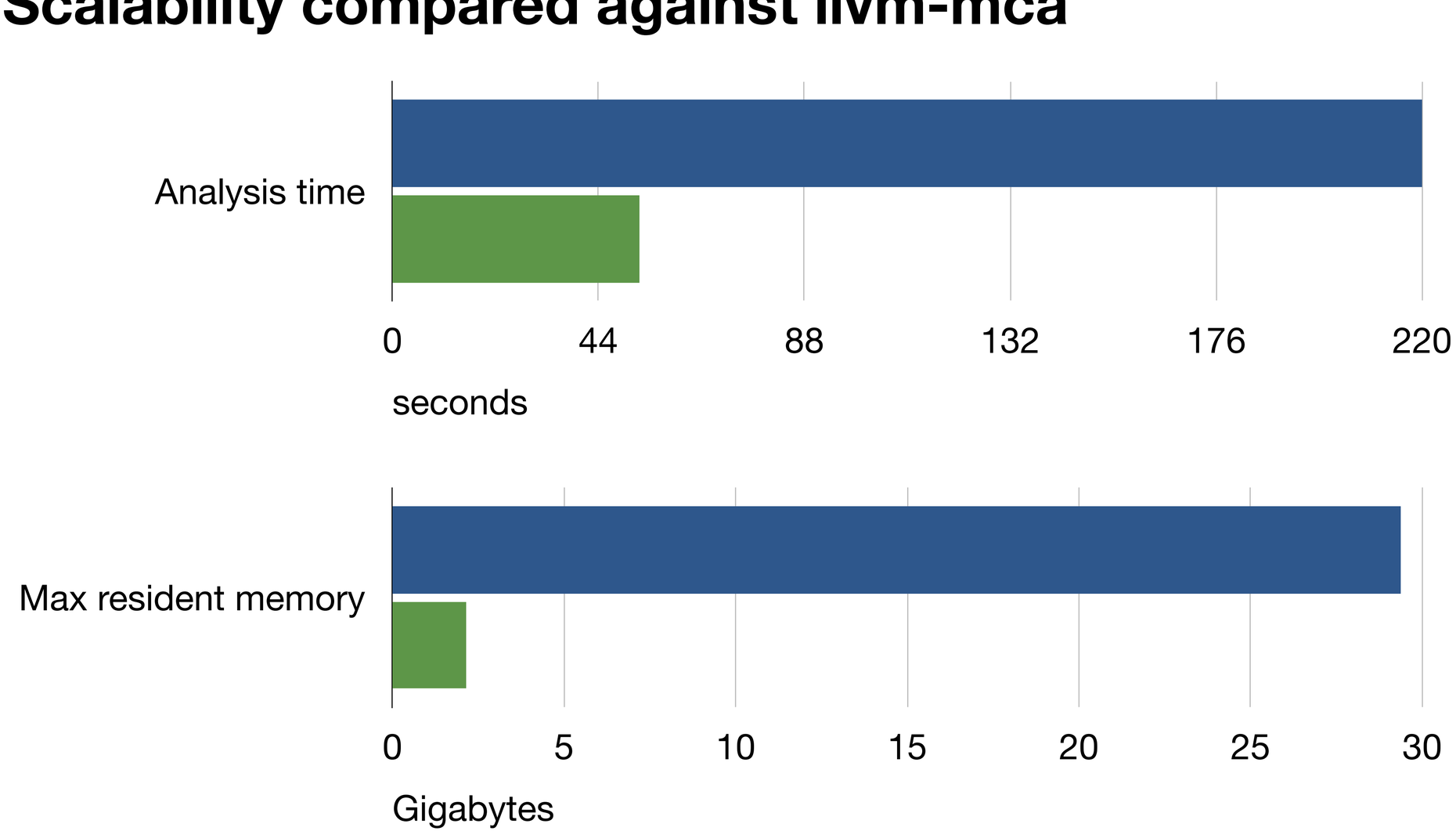

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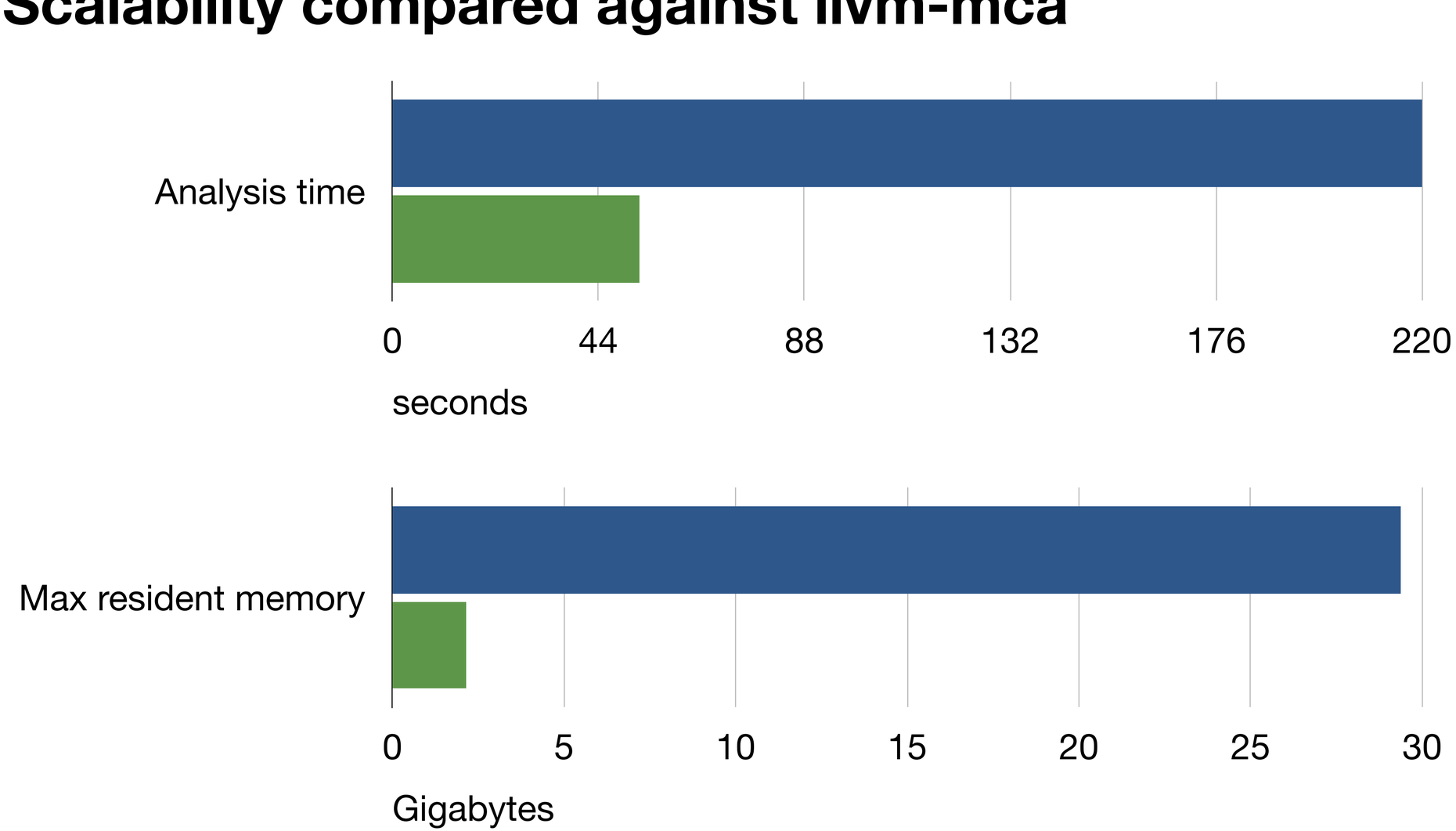

4x Faster

13x Less

Evaluation

Scalability compared against other static throughput analysis tools

	Analysis Time	Max Resident Memory
uiCA	Timeout after 48h	113 GB
OSACA	Exit w/ error after 24h	N/A
Ithemal	Exit w/ error after 2m	N/A
MCAD	**52.69s**	**2.16 GB**

Outline

Motivation

MCA Daemon (MCAD)

Future Plans

Epilogue

// TODO

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- Going upstream: QEMU & LLVM

Going upstream: LLVM

The plan

Going upstream: LLVM

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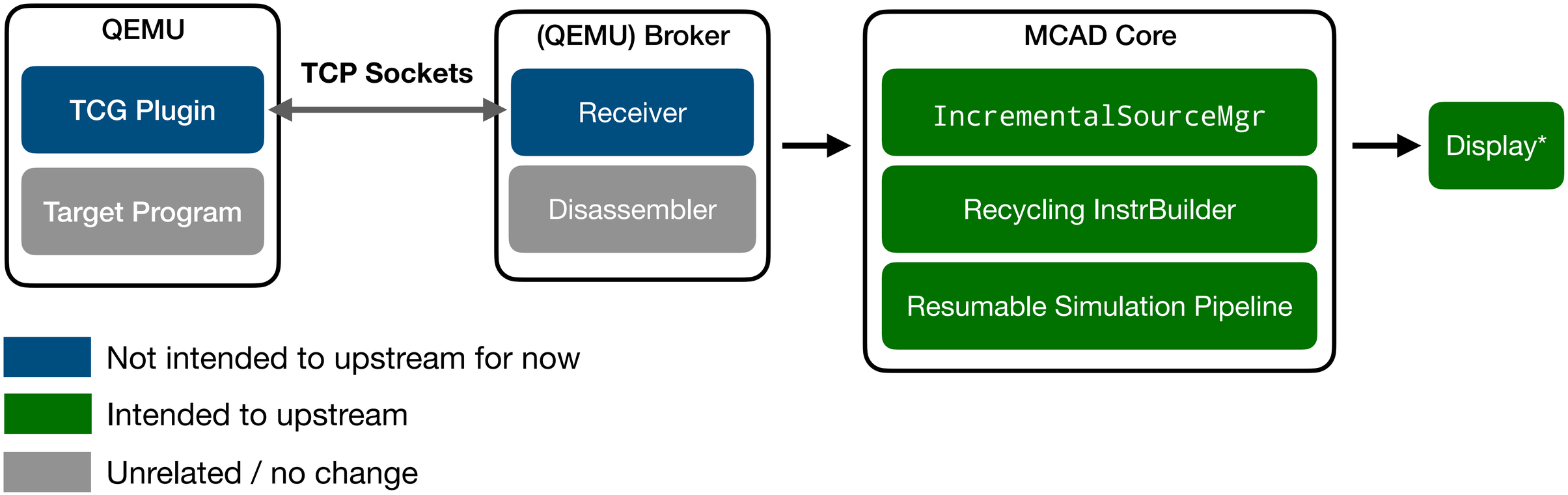
- We would like to upstream components that are beneficial to the **core MCA libraries** first

Going upstream: LLVM

The plan: components to upstream



Going upstream: LLVM

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  - Some of the (advanced) interfaces in broker plugin are only used by QEMU broker. So, without the latter, it's not well tested.

Outline

Motivation

MCA Daemon (MCAD)

Future Plans

Epilogue

Summary

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- We improved the performance & flexibility of core MCA libraries
  - We would like to merge these changes upstream to benefit the wider community

Source code

https://github.com/securesystemslab/LLVM-MCA-Daemon

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Thank You!
Q&A
Me
Aldrich Park @ UC Irvine, California

Appendix

Introduction to MCA

An example

test/tools/llvm-mca/X86/BtVer2/dot-product.s

```
vmulps    %xmm0, %xmm1, %xmm2
vhaddps   %xmm2, %xmm2, %xmm3
vhaddps   %xmm3, %xmm3, %xmm4
```

```
llvm-mca -mtriple=x86_64 -mcpu=btver2 \
         -iterations=300 dot-products.s
```

Timeline

```
                    012345
Index     0123456789

[0,0]     DeeER.    .    .   vmulps
[0,1]     D==eeeER  .    .   vhaddps
[0,2]     .D====eeeER    .   vhaddps
[1,0]     .DeeE-----R    .   vmulps
[1,1]     . D=eeeE---R   .   vhaddps
[1,2]     . D====eeeER   .   vhaddps
[2,0]     .   DeeE-----R .   vmulps
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[2,0]     .   DeeE-----R .  vmulps
[2,1]     .   D====eeeER .  vhaddps
[2,2]     .    D======eeeER vhaddps
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