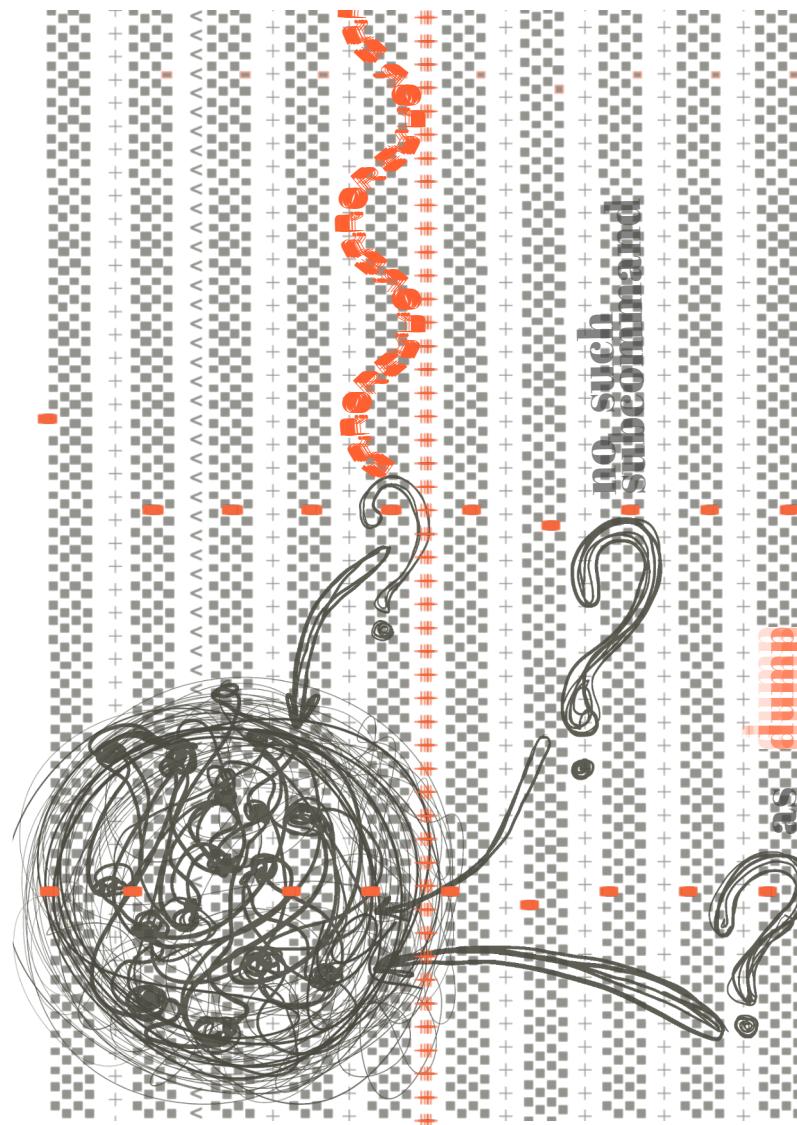
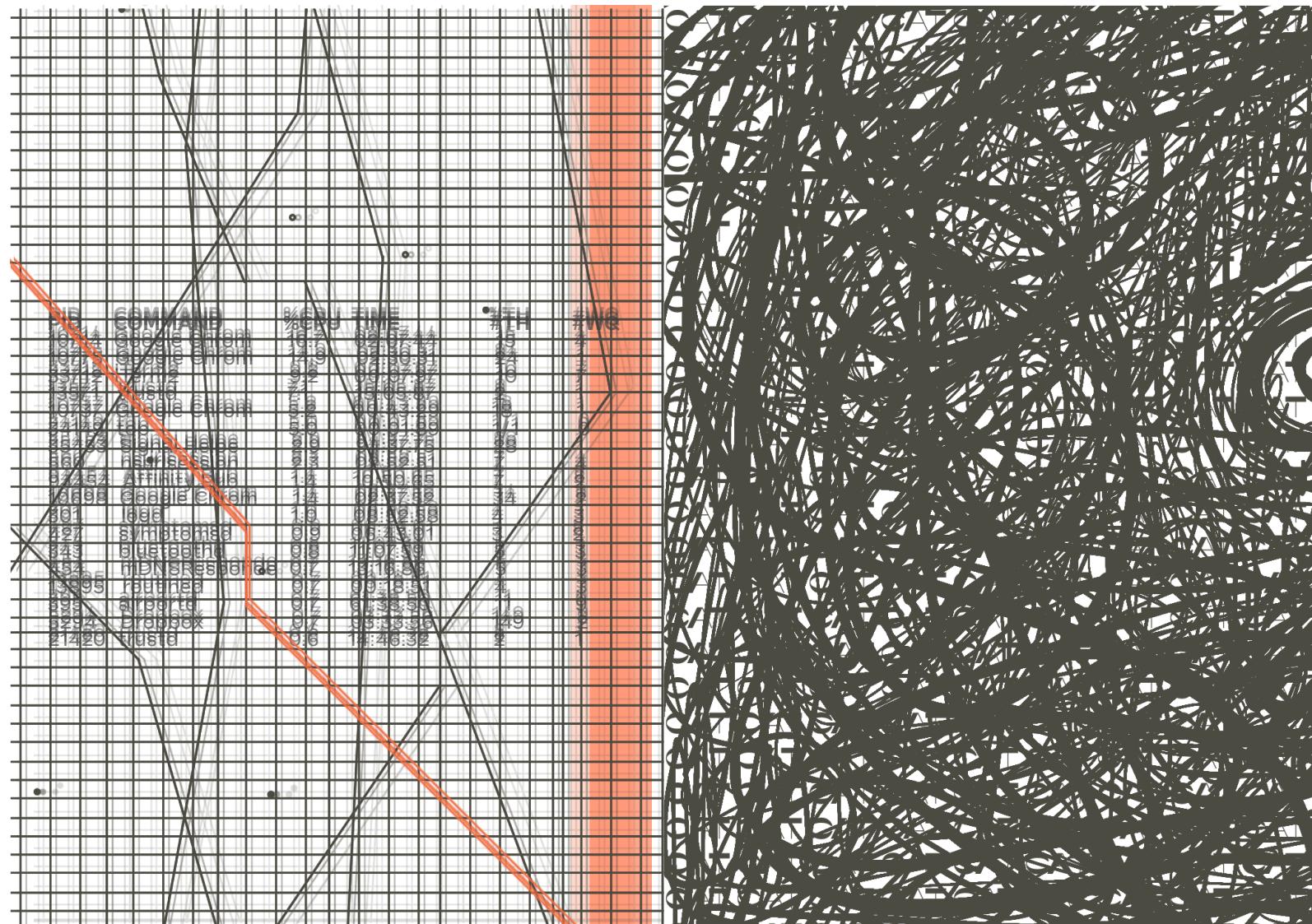
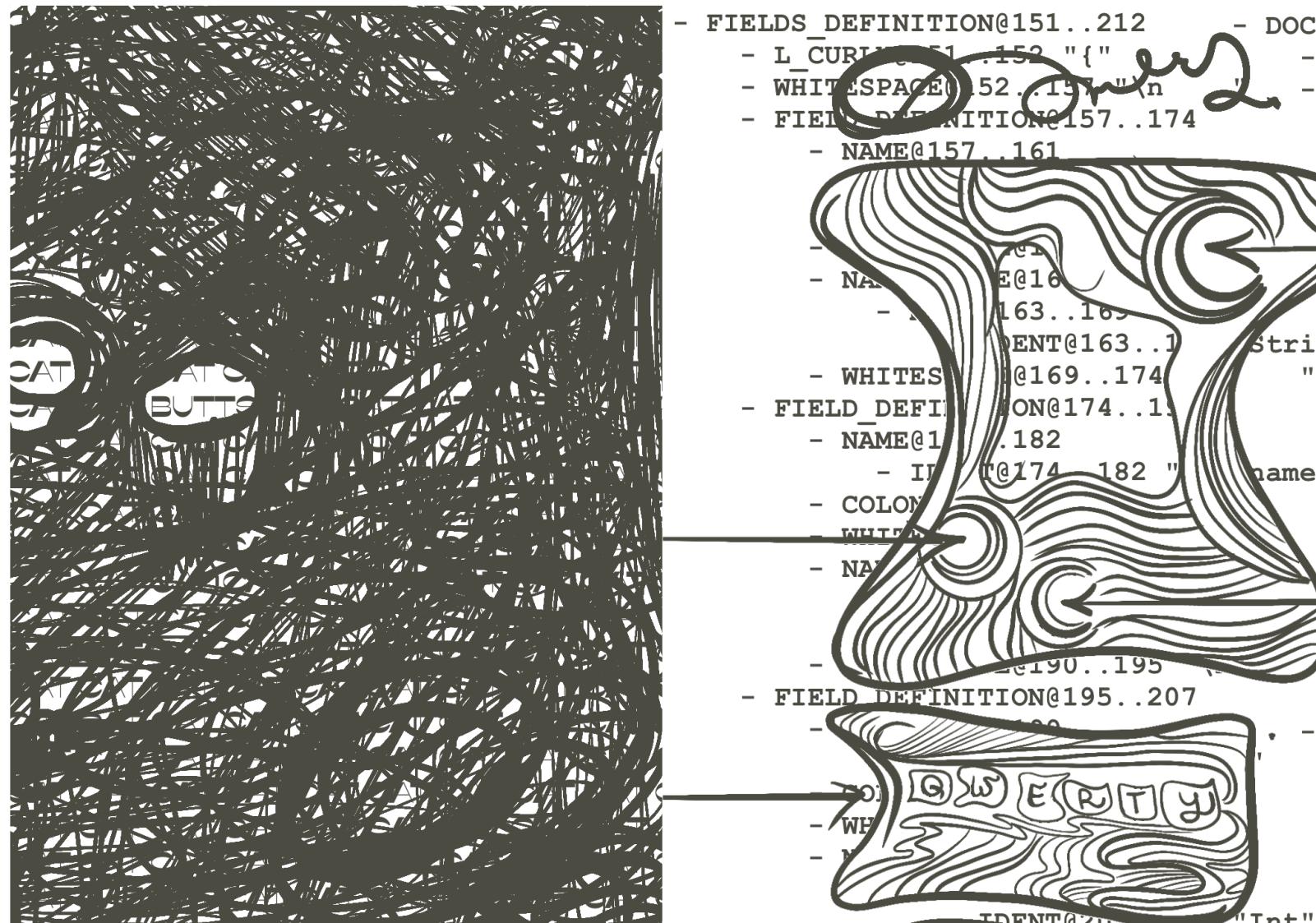


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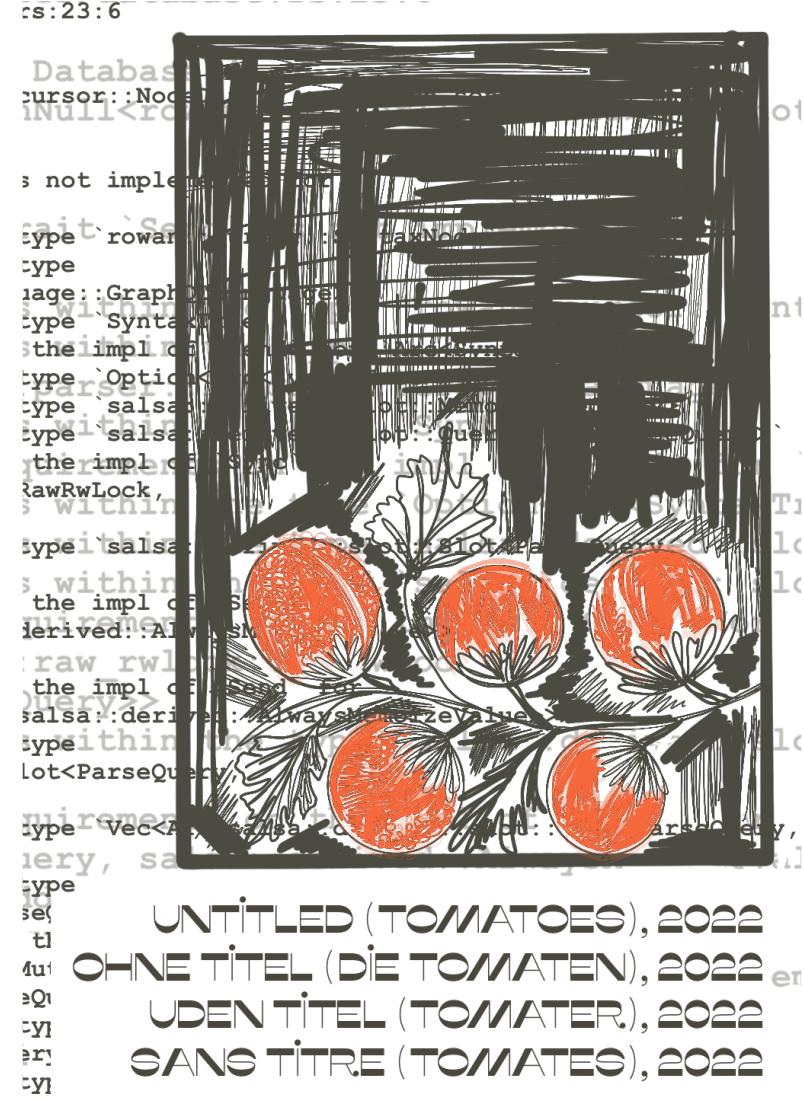


Table 25. Character Codes (cont.)

KEY #	BASE CASE	OTHER CASE	BUTTS	LF	ALT
28	28 CTAB	CTAB	CTAB	CTAB	CTAB
30	30 CTAB	CTAB	CTAB	CTAB	CTAB
32	32 CTAB	CTAB	CTAB	CTAB	CTAB
34	34 CTAB	CTAB	CTAB	CTAB	CTAB
36	36 CTAB	CTAB	CTAB	CTAB	CTAB
38	38 CTAB	CTAB	CTAB	CTAB	CTAB
40	40 CTAB	CTAB	CTAB	CTAB	CTAB
42	42 CTAB	CTAB	CTAB	CTAB	CTAB
44	44 CTAB	CTAB	CTAB	CTAB	CTAB
46	46 CTAB	CTAB	CTAB	CTAB	CTAB

SIGNAL	DESCRIPTION (AREA)	PAGE
28MHz	28.63636 MHz Mostar Clock	2
7MHz	7.15909 MHz Processor Clock	2.5
A[23:1]	Processor Address Bus (68000)	2.3
ACK	Data Acknowledge (Parallel Port)	6
AS	Address Strobe (68000)	2.7
AUDI	Audio Input (RS232 Port)	1.5
AUDOUT	Audio Output (RS232 Jack)	1.5
BEFR	Bus Error (68000)	2
BG	Bus Grant (68000)	2
BGACK	Bus Grant Acknowledge (68000)	2
BLISS	Blitter Shutdown (Chips)	2
B.LT	Chip Memory Access (Chips)	2
BR	Bus Request (68000)	2
BUSY	Device Busy (Parallel Port)	6
CASL/U	Column Address Strobe (DRAM)	2.2
CCK/CCKD	Color Clock / Quadrature (Chips)	2.4
CDAC	7.15909 MHz Quadrature Clock (Chips)	2.5
CHNG	Media Change (Floppy)	6.1
CLKR0/WR	Read-Time Clock Read / Write (RT)	2.9
COMP	Monochrome Composite Video (Video)	5
CSYNC	Composite Sync (Video)	2.5
CTS	Clear to Send (RS232 Port)	6
D11S:01	Processor Data Bus (68000)	2.2
D1R	Step Direction (Floppy)	8.1
DKRD	Disk Read Data (Floppy)	4.1
DKWD	Disk Write Data (Floppy)	4.1
DKWE	Disk Write Enable (Floppy)	4.1
DMAL	Chip DMA Request Line (Chips)	2.1
DRAB:01	DRAM Address Bus (DRAM)	2.1
DRDI5:01	DRAM Data Bus (DRAM)	2.1
DSR	Data Set Ready (RS232 Port)	6
DTACK	Data Transfer Acknowledge (68000)	2.1
DTR	Data Terminal Ready (RS232 Port)	6
E	Peripheral Enable Clock (68000)	2.1
EXRAM	Expansion Memory Present	2.1
F0I2:01	Function Code (68000)	2.1
FIRE0/1	Fire Button 0/1 (Joysticks)	2.1
HLT	Processor Halt (68000)	2.1
HSYNC	Horizontal Sync (Video)	2.1
INDEX	Index Pulse (Floppy)	6.1
INT(2,3,5)	Interrupt Request (Chips)	6.1
IORESET	I/O Reset	6
IPU(2:01)	Interrupt Priority Level (68000)	2.1
KBCLOCK	Keyboard Clock (Keyboard)	2
KADATA	Keyboard Data (Keyboard)	2
KBRESET	Keyboard Reset (Keyboard)	2
LDS/UDS	Upper / Lower Data Strobes (68000)	2
LED	Power On LED / Audio Filter Disable	4.1

RUNNING CI TESTS
T E S T TEST:TEC0000.INPUT_OBJECT_FIELD_TYPEO_DIRECTIVE_NAME
NE OX
TEST:TEC0000.INPUT_OBJECT_DEFINITION_OX
TEST:TEC0000.ACCESSO_DIRECTIVE_DEFINITION_OX
TEST:TEC0000.INTERFACE_DEFINITION_OX
TEST:TEC0000.FIELD_DEFINITION_OX
TEST:TEC0000.ENUM_DEFINITION_OX
T E S T TEST:TEC0000.FIELD_DEFINITION_FROM_OPERATION_DEFINITION_OX
TEST:TEC0000.FIELD_DEFINITION_NAME_OX
TEST:TEC0000.FIELD_DEFINITION_TYPE_OX
TEST:TEC0000.FIELD_DEFINITION_OPERATION_OX
TEST:TEC0000.FIELD_DEFINITION_INTERFACE_OX
TEST:TEC0000.FIELD_DEFINITION_PARTS_OX
T E S T TEST:TEC0000.INPUT_OPERATION_FIELD_OX
VALIDATION:INTERFACE:TEST:IT_FAILE_VALIDATION_WITH_DUPLICATE_OPERATION_FIELDS_OX
T E S T TEST:TEC0000.INPUT_OPERATION_FIELD_OX
VALIDATION:INTERFACE:TEST:IT_FAILE_VALIDATION_WITH_DUPLICATE_INTERFACE_DEFINITION_OX
TEST:TEC0000.UNION_DEFINITION_OX
T E S T TEST:TEC0000.INPUT_OPERATION_FIELD_OX
VALIDATION:INTERFACE:TEST:IT_FAILE_VALIDATION_WITH_NONNULL_TRANSITIVE_INTERFACE_OX
T E S T TEST:TEC0000.INPUT_OPERATION_FIELD_OX
VALIDATION:INTERFACE:TEST:IT_FAILE_VALIDATION_WITH_INCOMPLETE_INTERFACE_DEFINITION_OX
TEST:TEC0000.OBJECT_DEFINITION_OX
T E S T TEST:TEC0000.INPUT_OPERATION_FIELD_OX
VALIDATION:INTERFACE:TEST:IT_FAILE_VALIDATION_WITH_UNDEFINED_INTERFACE_DEFINITION_OX
T E S T TEST:TEC0000.INPUT_OPERATION_FIELD_OX
VALIDATION:INTERFACE:TEST:IT_GENERATE_DIALECTICS_FOR_NON_OUTPUT_FIELD_TYPEO_OX
T E S T TEST:TEC0000.INPUT_OPERATION_FIELD_OX
VALIDATION:OPERATIONS:TEST:IT_VALIDATE_UNIQUE_OPERATION_NAME_OX

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thanks for
reading!!

