RISC-V Workshop
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# Performance Enhancement of RISC-V cores through Value Prediction based on Dynamic Data Flow Analysis

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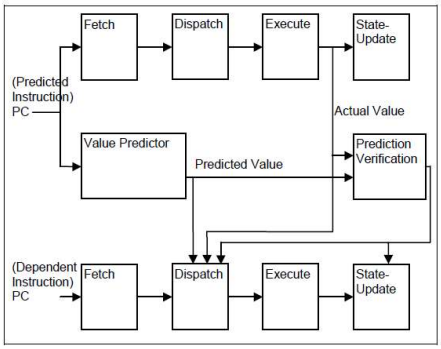
The effective performance of wide-issue superscalar processors depends on many parameters, such as branch prediction accuracy, available instruction-level parallelism, and instruction-fetch bandwidth.

True-data dependent instructions cannot be executed in parallel and the dataflow-graph of a sequential application decides the limits of the maximum instruction level parallelism that can be exploited.

```
I1 : e = a + b
I2 : f = c + d
I3 : m = e * f
```

In such cases prediction of the outcome of the instruction based on the context derived from the history of occurrences and executing dependent instructions earlier using the predicted value can help avoid stalls in dynamic context.

Without using Value prediction (VP), the third instruction can be dispatched only after the first and seconds instructions have been executed since its result becomes available only at this point.




*Hardware Value Speculation Mechanism for Flow dependent Instructions*

**Value locality (VL)**

- Recurrence of values in a memory structure OR
- Some correlation/pattern in the output produced by different dynamic instances of the static instructions.

**Value prediction (VP) :**

Value prediction is a technique capable of pushing the upper bound on Instruction Level Parallelism (ILP), predicting the outcome of an instruction and executing dependent instructions earlier using the predicted value, by exploiting Value Locality.

## Kinds of Patterns in outcome

Constant(C): 5 5 5 5 5 5 5...
Stride(S): 1 2 3 4 5 6 7 8...
Non-Stride(NS) : 28 -13 -99 107 23 456...
Repeated Stride(RS): 1 2 3 1 2 3 1 2 3...
Repeated Non-Stride(RNS): 1-13 -99 7 1-13 -99 7...
Could be others:.....

## Categorization of Value Predictors

**Based on Operation:**

- Computational Based: Register Value, Last Value, Stride
- Context Based: FCM, DFCM

**Based on Number:**

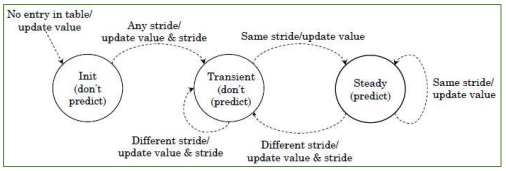
- Solo
- Hybrid

**Based on Dependency considered:**

- Local Value
- Global Value

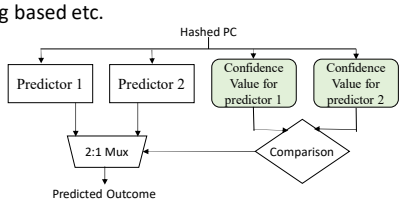
## Confidence estimation scheme

Whether the outcome of the predictor should be considered for consumption or not: : e.g. State based, Counter based, SAg based etc.




*← Example of a State based confidence estimation scheme*

*Hybrid Predictor with a confidence estimation scheme →*




## Challenges in Value Prediction

- Low Accuracy: predicting larger no. of bits as compared to branch predictor
- High Recovery Penalty: For Performance improvement need high accuracy or aggressive recovery scheme.
- Hardware overhead and complexity: prediction tables
- Energy Penalty: Not useful for power constraint systems
- Limitations due to finite resources

## Potential and Scope of Value Prediction

Potential of VP is limited by instruction-fetch bandwidth and instruction issue rate.
Fetch bandwidth is constrained by:

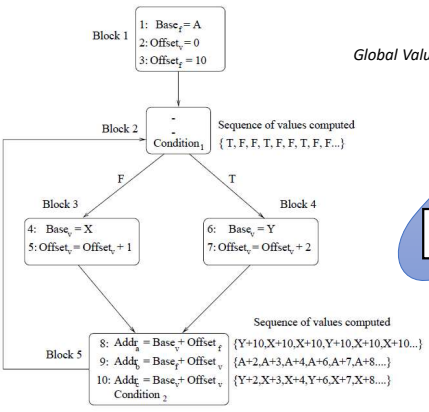
- I-cache hit rate,
- branch prediction accuracy,
- misprediction overhead

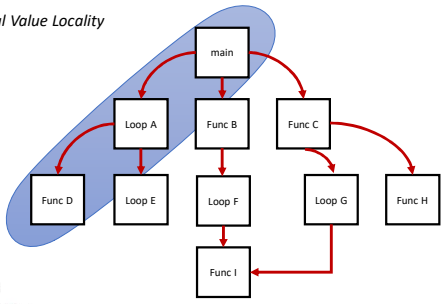
Scope of VP depends on the distance between Producer and Consumer (in terms of number of instructions, compared to fetch-rate):

- Far Distant
- Short Distant

## Motivation and Focus of Work

- Highly accurate data value prediction methods are required to boost processor performance by overcoming the trade-off between increased parallelism and misprediction penalty.
- As hardware resources are limited, challenge includes identifying new variables in dynamic context & storing only the ones more valuable for successive predictions.
- Focus of research is to carry out value prediction, by doing hardware-based real time & on the fly Dynamic Data Flow Analysis (DDFA) of application programs by exploiting Global Value Locality.
- Explore the possibility of using Multiple Input Linear Feedback Shift Registers as new structures for confidence estimation to enable identification of variables having high accuracy predictability.




## Scope of Work

Scope of DDFA includes dynamic value prediction & hence its possible incorporation into some of the high-end multiple core server processors intended for cloud applications in Data Centres. From current literature it is evident that for performance enhancements, value prediction will be needed across all categories of processor designs (RISC, GPUs, etc.).

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**References** [1] M. M. K. Martin, D. J. Sorin, H. W. Cain, M. D. Hill and M. H. Lipasti, "Correctly Implementing Value Prediction in Microprocessors that Support Multithreading and Multiprocessing", 34th Annual ACM/IEEE International Symposium on Microarchitecture, Austin, Texas, 2001.
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