

به نام خدا

آشنایی با زبان اسمبلی AVR

دستورات پایه

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Comment

- Use “ ; ” to write a comment in Assembly language
 - Like “//” in C language
- To present number
 - In hex
 - \$ or 0x LDI R16,\$50 LDI R16,0x50
 - Decimal
 - No thing LDI R16, 50
 - Binary
 - 0b LDI R16,0b00110010

NOP – No Operation

- This instruction performs a single cycle No Operation

Operation:

(i) No

Syntax:

Operands:

Program Counter:

(i) NOP

None

$PC \leftarrow PC + 1$

16-bit Opcode:

0000	0000	0000	0000
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	–	–	–	–	–	–

Words 1 (2 bytes)

Cycles 1

ADC – Add with Carry

- Adds two registers and the contents of the C Flag and places the result in the destination register Rd

Operation:

$$(i) \quad Rd \leftarrow Rd + Rr + C$$

Syntax:

Operands:

Program Counter:

(i) ADC Rd,Rr

$0 \leq d \leq 31, 0 \leq r \leq 31$

$PC \leftarrow PC + 1$

16-bit Opcode:

0001	11rd	dddd	rrrr
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow

Words 1 (2 bytes)

Cycles 1

SUB – Subtract Without Carry

- Subtracts two registers and places the result in the destination register Rd

Operation:

(i) $Rd \leftarrow Rd - Rr$

Syntax:

(i) SUB Rd,Rr

Operands:

$0 \leq d \leq 31, 0 \leq r \leq 31$

Program Counter:

$PC \leftarrow PC + 1$

16-bit Opcode:

0001	10rd	dddd	rrrr
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow

Words 1 (2 bytes)

Cycles 1

SUB – Subtract Without Carry

H $\overline{Rd3} \cdot Rr3 + Rr3 \cdot R3 + R3 \cdot \overline{Rd3}$

Set if there was a borrow from bit 3; cleared otherwise.

S $N \oplus V$, for signed tests.

V $Rd7 \cdot \overline{Rr7} \cdot \overline{R7} + \overline{Rd7} \cdot Rr7 \cdot R7$

Set if two's complement overflow resulted from the operation; cleared otherwise.

N $R7$

Set if MSB of the result is set; cleared otherwise.

Z $\overline{R7} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}$

Set if the result is \$00; cleared otherwise.

C $\overline{Rd7} \cdot Rr7 + Rr7 \cdot R7 + R7 \cdot \overline{Rd7}$

Set if the absolute value of the contents of Rr is larger than the absolute value of Rd; cleared otherwise.

SBC – Subtract with Carry

- Subtracts two registers and subtracts with the C Flag, and places the result in the destination register Rd.

Operation:

(i) $Rd \leftarrow Rd - Rr - C$

Syntax:

Operands:

Program Counter:

(i) SBC Rd,Rr

$0 \leq d \leq 31, 0 \leq r \leq 31$

$PC \leftarrow PC + 1$

16-bit Opcode:

0000	10rd	dddd	rrrr
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow	\Leftrightarrow

Words 1 (2 bytes)

Cycles 1

AND – Logical AND

- Performs the logical AND between the contents of register Rd and register Rr, and places the result in the destination register Rd

Operation:

(i) $Rd \leftarrow Rd \cdot Rr$

Syntax:

Operands:

Program Counter:

(i) AND Rd,Rr

$0 \leq d \leq 31, 0 \leq r \leq 31$

$PC \leftarrow PC + 1$

16-bit Opcode:

0010	00rd	dddd	rrrr
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	–	\Leftrightarrow	0	\Leftrightarrow	\Leftrightarrow	–

Words 1 (2 bytes)

Cycles 1

AND – Logical AND

S $N \oplus V$, for signed tests.

V 0

Cleared.

N R7

Set if MSB of the result is set; cleared otherwise.

Z $\overline{R7} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}$

Set if the result is \$00; cleared otherwise.

OR – Logical OR

- Performs the logical OR between the contents of register Rd and register Rr, and places the result in the destination register Rd

Operation:

(i) $Rd \leftarrow Rd \vee Rr$

Syntax:

Operands:

Program Counter:

(i) OR Rd,Rr

$0 \leq d \leq 31, 0 \leq r \leq 31$

$PC \leftarrow PC + 1$

16-bit Opcode:

0010	10rd	dddd	rrrr
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	–	\Leftrightarrow	0	\Leftrightarrow	\Leftrightarrow	–

Words 1 (2 bytes)

Cycles 1

EOR – Exclusive OR

- Performs the logical EOR between the contents of register Rd and register Rr and places the result in the destination register Rd

Operation:

(i) $Rd \leftarrow Rd \oplus Rr$

Syntax:

Operands:

Program Counter:

(i) EOR Rd,Rr

$0 \leq d \leq 31, 0 \leq r \leq 3$

$PC \leftarrow PC + 1$

16-bit Opcode:

0010	01rd	dddd	rrrr
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	–	\Leftrightarrow	0	\Leftrightarrow	\Leftrightarrow	–

Words 1 (2 bytes)

Cycles 1

Summary

ALU Instructions Using Two GPRs

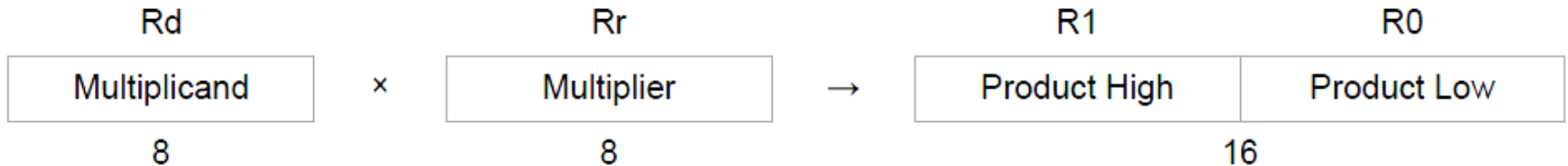
Instruction		
ADD	Rd, Rr	ADD Rd and Rr
ADC	Rd, Rr	ADD Rd and Rr with Carry
AND	Rd, Rr	AND Rd with Rr
EOR	Rd, Rr	Exclusive OR Rd with Rr
OR	Rd, Rr	OR Rd with Rr
SBC	Rd, Rr	Subtract Rr from Rd with carry
SUB	Rd, Rr	Subtract Rr from Rd without carry

ADD	Rd, Rr	ADD Rd and Rr
ADC	Rd, Rr	ADD Rd and Rr with Carry
AND	Rd, Rr	AND Rd with Rr
EOR	Rd, Rr	Exclusive OR Rd with Rr
OR	Rd, Rr	OR Rd with Rr
SBC	Rd, Rr	Subtract Rr from Rd with carry
SUB	Rd, Rr	Subtract Rr from Rd without carry

Rd and Rr can be any of the GPRs.

MUL – Multiply Unsigned

- This instruction performs 8-bit \times 8-bit \rightarrow 16-bit unsigned multiplication



- The multiplicand Rd and the multiplier Rr are two registers containing unsigned numbers. The 16-bit unsigned product is placed in R1 (high byte) and R0 (low byte). Note that if the multiplicand or the multiplier is selected from R0 or R1 the result will overwrite those after multiplication.

MUL – Multiply Unsigned

Operation:

- (i) $R1:R0 \leftarrow R_d \times R_r$ (unsigned \leftarrow unsigned \times unsigned)

Syntax:

Operands:

Program Counter:

- (i) MUL R_d, R_r

$0 \leq d \leq 31, 0 \leq r \leq 31$

$PC \leftarrow PC + 1$

16-bit Opcode:

1001	11rd	dddd	rrrr
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	–	–	–	–	\Leftrightarrow	\Leftrightarrow

C R15

Z $\overline{R15} \cdot \overline{R14} \cdot \overline{R13} \cdot \overline{R12} \cdot \overline{R11} \cdot \overline{R10} \cdot \overline{R9} \cdot \overline{R8} \cdot \overline{R7} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}$

Set if the result is \$0000; cleared otherwise.

MULS – Multiply Signed

- This instruction performs 8-bit × 8-bit → 16-bit signed multiplication

Operation:

- (i) $R1:R0 \leftarrow R_d \times R_r$ (signed ← signed × signed)

Syntax:

Operands:

Program Counter:

- (i) MULS R_d, R_r

$16 \leq d \leq 31, 16 \leq r \leq 31$

$PC \leftarrow PC + 1$

16-bit Opcode:

0000	0010	dddd	rrrr
------	------	------	------

Status Register (SREG) and Boolean Formula

I	T	H	S	V	N	Z	C
–	–	–	–	–	–	⇔	⇔

C R15

Z $\overline{R15} \cdot \overline{R14} \cdot \overline{R13} \cdot \overline{R12} \cdot \overline{R11} \cdot \overline{R10} \cdot \overline{R9} \cdot \overline{R8} \cdot \overline{R7} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}$

Set if the result is \$0000; cleared otherwise.

پایان

موفق و پیروز باشید