AXI4 W Pattern Trigger V1.1
IP User Guide

1 Description
The AXI4 W Pattern Trigger is an FPGA IP Core for debugging purposes. It monitors an AXI4 write channel and triggers if it contains a user configured data pattern. The data pattern is configured through an AXI Lite interface.

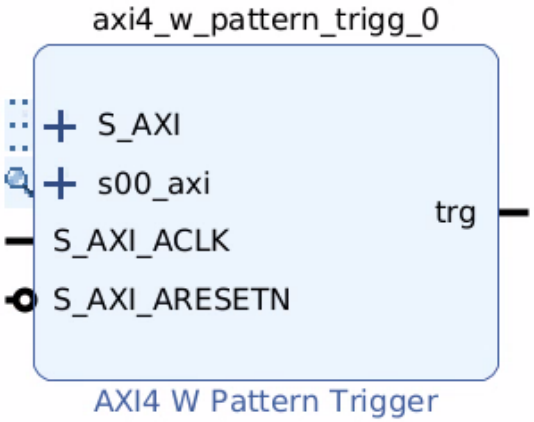

Figure 1: AXI4 W Pattern Trigger Block IP

2 Applications
- Performance Measurements
- Latency Measurement

3 Features
- AXI Lite register interface
- Compares 4 bytes to variable WDATA width

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4 Designing with the Core

Clocking

The IP core is clocked through the S_AXI_ACLK clock which needs to match the clock frequency of the monitored AXIS interface. Use the Xilinx AXI Interconnect IP to perform clock domain crossing for the AXI Lite interface.

Table 1: Signal Descriptions

Signal Name		Direction	Clock Domain	Description
S_AXI_*		AXI Lite bus	s_axi_aclk	AXI Lite interface to access the internal register space.
S00_AXI_*		AXI Stream	s_axi_aclk	AXI4 monitor interface.
trg		output	s_axi_aclk	Counter start trigger. Uses double flip-flop synchronization to synch to s_axi_aclk domain.

5 Comparison Principle

This IP Core will compare the bit-pattern configured in the PATTERN register against the data appearing at the AXI4_WDATA signal. If the pattern appears at least once inside WDATA, the output trg will ouput a high-level pulse of 1 clock cycle length. See Figure 2 for an illustration of the comparison.

Note that C_S_AXI_DATA_WIDTH is greater or equal to C_S_AXI_DATA_WIDTH.

Note that the comparison is byte-aligned and that patterns that are not byte aligned will not be detected.

Note that endianness is relevant for matching byte patterns. Ethernet packets are BIG_ENDIAN and Microblaze designs are typically LITTLE_ENDIAN.

Note that the IP core always compares the pattern. If the PATTERN register is left unconfigured, it will trigger on any occurrence of zeroes in the AXIS data stream.

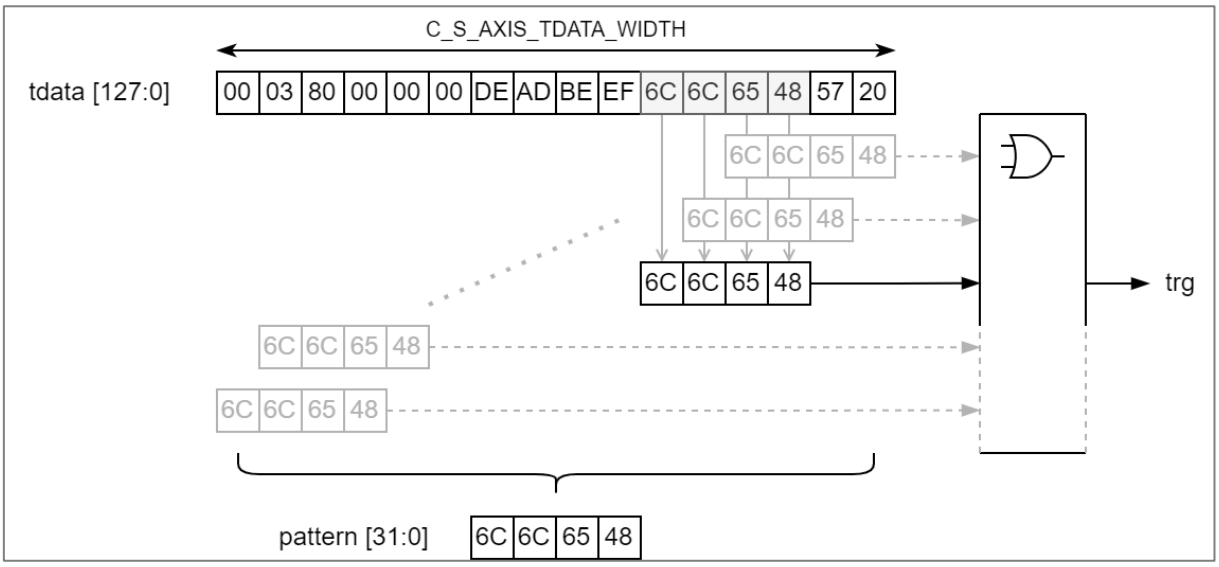

Figure 2: Pattern Comparison Principle

6 Software Flow

The IP is programmed through the AXI Lite interface. Table 2 shows the available registers and functions.

Table 2: Configuration Registers

Address Offset	Name	Access	Description
0x00	PATTERN	RW	Contains the 4-byte pattern that should be compared to WDATA.
0x04 – 0x08	reserved	RW	–
0x0C	reserved	RO	Reads as ‘1’s

Configuration Steps

1. Write the desired target pattern into the PATTERN register