Multiply units

3.5 Control registers

4.3 Interrupts

All interrupts are effectively treated by the ST220 as an exception of type **EXTERN_INT**. Individual interrupt lines are indicated by registers in the Interrupt Controller, *Chapter 11: Interrupt controller on page 67*.

4.4 Exception types and priorities

The table below shows the possible exceptions and the bit number in the EXCEPT_CAUSE control register that each corresponds to. Since only one exception is raised at a time, simultaneous exceptions are prioritised. The table is listed in exception priority order starting with the highest priority.

4.5 Speculative load cons0 l ierations

SIeculative (or dismissable) loads are defined such that they execute as normal loa943.63 loa9430l

1 Misaligned implementation

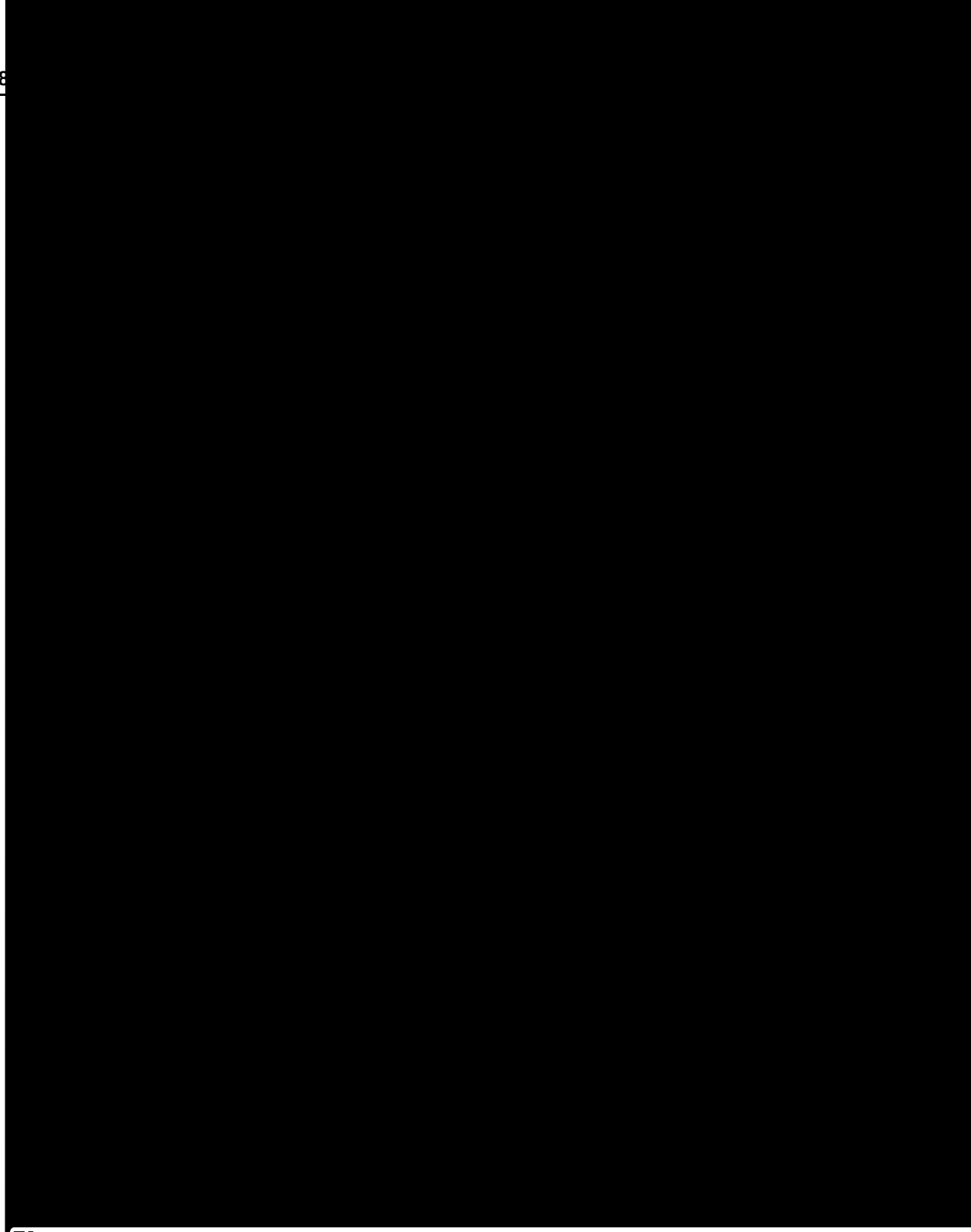
execution by stalling the entire processor. No execution proceeds until the channel becomes ready for the requested communication or a timeout exception is taken.

Interrupts can also be taken while waiting on the SDI.

7.2.1 Data width

The Se wa41 interface is 32-bits wide.

	SAVED_SAVED_PSW	0xffc0	RO/RW	PSW saved by debug unit inter-rupt.
RO/RW	PC saved by debug unit interrupt.			



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