NOT FOR EXTERNAL USE

2 Frequency

2.1 Core Frequency

NOT FOR EXTERNAL USE

3 Latency Changes

5   Instruction Changes

5.1   SIMD

Today no SIMD instructions are proposed.

5.2   Prefetch (pft)

The prefetch instruction is currently a NOP instruction, which consumes a load/store instruction slot. The ST220 will implement the prefetch instruction. This is dealt with in more details in the Chapter : *Data Prefetch* on page 13

5.3   Shift Distance (shr, shru, shl)

It is suggested that the shift distance for all shift instructions be changed to include the next two bits of the opcode. i.e. bits 5-7. Such that shifts of >31 and <=255 will produce the value zero. This will help in a number of bit

Data cache instructions

Instruction Encodings

mullhu	s						
mulhh	s						
mulhhu	s						
mulhs	s						
capeq	s	00	010	0000	dest	src2	src664(s)12(r)5(c2)-56666(s)349(

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Instruction Encodings

6   **Data Prefetch**

Thereoe1(etce(r)-543(i4(cs)-247(d)-3(signeM)13dr)-569(t49(o)-569ro)11(duce4)-240(t)85(h)9(e)-07aovh)9(rallY)-249stllYfective

EXCEPT_CAUSE

11 Addresses & Booting

11.1 Boot Addrs

The ST220 will support the configuration of the boot address. After power on rset the ST220 jumps to the boot

12   Control Registers

12.1   Address range

The address range of the control registers is extended to 8k bytes. This increase allows the incorporatn°ł(2d)-256(o)-3(f)-242(t)4(he

Control Register Addresses

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