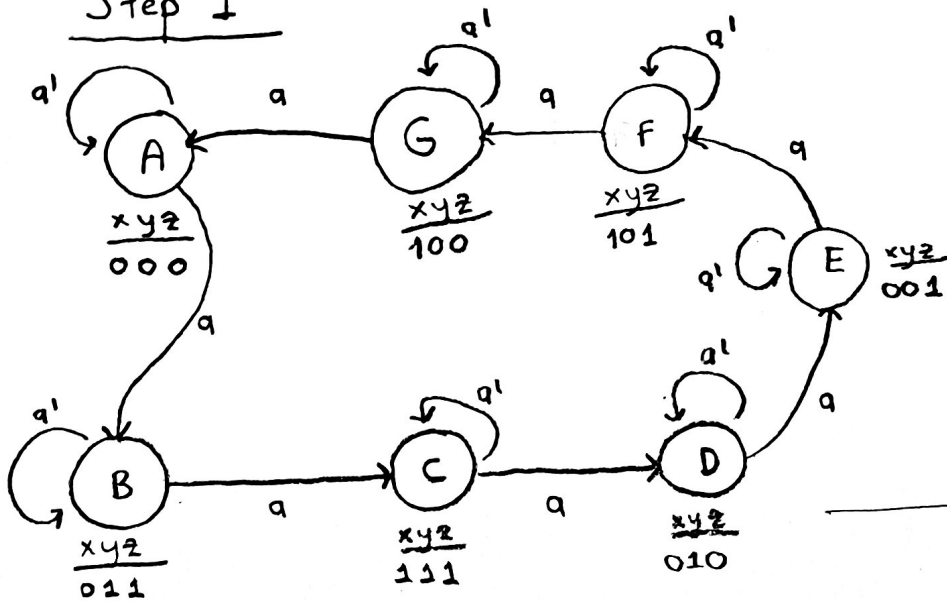


Step 1



Step 3

A : 000
 B : 001
 C : 010
 D : 011
 E : 100
 F : 101
 G : 110

Step 2

- 7 states (3 bits register, s_2, s_1, s_0)
- 3 bits for next states (n_2, n_1, n_0)
- a is input
- x, y, z are outputs

Step 4

	s_2	s_1	s_0	a	x	y	z	n_2	n_1	n_0
A	0	0	0	0	0	0	0	0	0	0
A	0	0	0	1	0	1	1	0	0	1
B	0	0	1	0	0	1	1	0	0	1
B	0	0	1	1	1	1	1	0	1	0
C	0	1	0	0	1	1	1	0	1	0
C	0	1	0	1	0	1	1	0	1	1
D	0	1	1	0	0	0	1	1	0	0
D	0	1	1	1	0	0	1	1	0	1
E	1	0	0	0	0	0	1	1	0	1
E	1	0	0	1	1	0	1	1	0	1
F	1	0	1	0	1	0	1	1	1	0
F	1	0	1	1	1	0	0	1	1	0
G	1	1	0	0	1	0	0	0	0	0
G	1	1	0	1	0	0	0	0	0	0
	1	1	1	0	0	0	0	0	0	0
	1	1	1	1	0	0	0	0	0	0

Step 5

$s_2 s_1 \backslash s_0 a$	00	01	11	10
00	0	0	1	0
01	1	0	0	0
11	1	0	X	X
10	0	1	1	1

$$X = s_1 s_0' a' + s_2 s_1' a + s_1' s_0 a + s_2 s_0$$

$s_2 s_1 \backslash s_0 a$	00	01	11	10
00	0	1	1	1
01	1	1	0	1
11	0	0	X	X
10	0	0	0	0

$$Y = s_2' s_1 s_0' + s_2' s_0' a + s_2' s_1' a + s_2' s_0 a'$$

$S_2 S_1 \backslash S_0 a$	00	01	11	10
00	0	1	1	1
01	1	0	1	0
11	0	0	X	X
10	1	1	0	1

$$Z = S_2' S_1 S_0' a' + S_2 S_1' S_0' + S_2' S_1' a + S_2' S_0 a + S_2' S_1' S_0 + S_2 S_0 a'$$

$S_2 S_1 \backslash S_0 a$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	1	0	X	X
10	1	1	1	1

$$n_2 = S_2 a' + S_2 S_1' + S_1 S_0 a$$

$S_2 S_1 \backslash S_0 a$	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	1	0	X	X
10	0	0	1	0

$$n_1 = S_2' S_1 S_0' + S_1 a' + S_1' S_0 a$$

$S_2 S_1 \backslash S_0 a$	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	0	X	X
10	0	1	0	1

$$n_0 = S_1' S_0' a + S_2' S_0' a + S_0 a'$$