Homework 3

CSE 232

May 2021

Draw a state diagram for an FSM with an input a and three outputs, x, y and z. The xyz outputs generate a sequence in order 000, 011, 111, 010,001,101, 100, repeat. The output should change only on a rising clock edge when the input a = 1. Make the initial state 000.
Design your solution in five steps

Step 1: Create FSM
Step 2: Obtain architecture
Step 3: Encode states
Step 4: Generate state table
Step 5: Obtain Boolean expressions and draw controller

(Hint, at Step 5, you may use K-maps for simplifications)