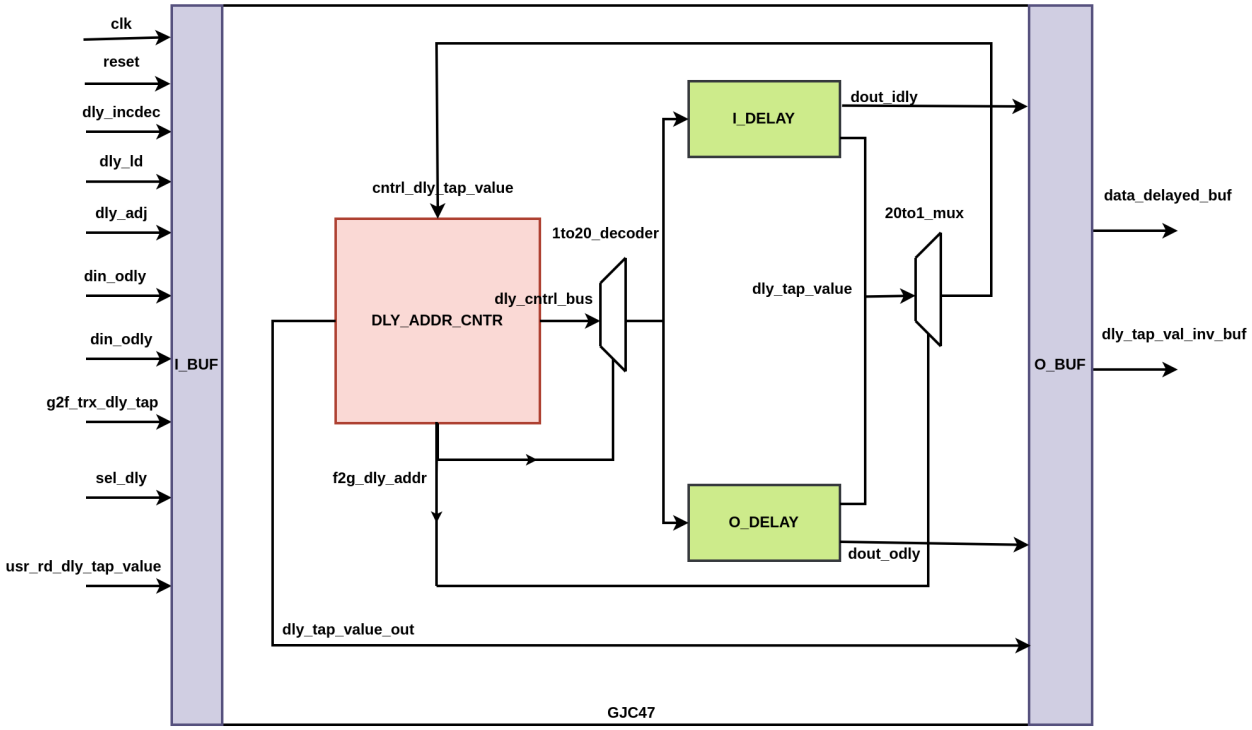
GJC-47



Description: -

The top module that instantiates the address controller (DLY_ADDR_CNTR) and the mux (20to1) and the decoder (1to20) as well. The controller is responsible for generating the addresses for the locations of the I_DELAYs and O_DELAYs corresponding to where they are connected defined by the DELAY_LOC parameter. This address controller also makes use of the above mentioned mux and decoder to form this address as well as the delay_tap_output.
There are two more modules instantiated inside the GJC47 top module. These are named **one_hot_to_output** and **slice_assignment_with_addr**. The “one_hot_to_output” is responsible for taking the 20 bit one-hot encoded bus input and generating an output bus whose width is equal to the number of I_DELAYs and O_DELAYs together so it can be connected directly to these modules carrying the correct addresses. Now the delay_tap outputs from these *_DELAY modules is appended onto adjacent bits on the bus, whereas we require this output to be on the slices governed by the address generated by the address controller. This is where the “slice_assignment_with_addr” comes into play. This module takes input and then reshuffles all the bits in it and place them at slices governed by the address generated and the sel_dly input from the top level.

Keeping in mind that the mux and decoder work as one-hot encoded, so the address output from the address controller has to be converted into one-hot encoded values as select lines to the mux and decoder.

DELAY_LOC parameter tells the addresses where the *_DELAYs are to be connected. These addresses are find out in the address_controller and then passed on to the muxes and decoders in their one-hot encoded format. Since the bus width from the mux and decoder is 20 bits at least, there could be less number of *_DELAYs, hence these are mapped onto smaller width buses via the use of **one_hot_to_output** and **slice_assignment_with_addr** modules.

The DELAY parameter is loaded onto the specified *_DELAY module. This is selected on the basis of the value of sel_dly input. sel_dly input specifies which of the *_DELAYs connected at the specific addresses should be loaded. The dly_ld signal is kept high for 2 clock cycles for the value to be loaded. dly_adj and dly_incdec inputs are responsible for incrementing and decrementing the loaded value. Finally the outputs from these *_DELAYs are driven through a mux, of which the select line is the one-hot encoded address from the address controller. The output is fed back to the address controller through which, the final output comes out based on the values of the input dly_ld, dly_adj and dly_incdec signals.