CSE/EEE230 Exam 2 Review (Spring 2021)

IMPORTANT NOTE:
**You will not be allowed to start the exam later than 15 minutes
after the exam starting time.**
You must start the exam on time.

- You will be taking the exam on Canvas, and you will be required to use Respondus
Lockdown browser (installation needed) and Monitor, using a webcam. Please take the
Practice exam on Canvas to ensure that you have a correct setting.
- You need to have your ASU photo ID to take the exam. You will need to show your
picture ID to your webcam before taking the exam (the system will ask you to take a
picture of your ID).
- You will also need to show your cheat sheet, front and back to the webcam before the
exam start.
- You will be asked to use your webcam to show your surroundings including what you
have in front of your compute on your table.
- Your face must be on webcam at all times.
- You may not leave the camera view during the exam (no bathroom break).
- You may not have anyone else in the room with you during the exam. You are not
allowed to use any virtual background.
- You may not browse other websites during the exam.
- You need to make sure that you have a secure Internet connection for each exam.
Turning on your mobile phone hotspot to have your mobile connection as a backup might
be an option.
- You should ensure that you are in a location where you won't be interrupted.
- Turn off all other devices (e.g. tablets, phones, second computers,) and place them
outside of your reach. You can not use earphones, headphones either.
- You should clear your desk or workspace of all external materials not permitted - books,
papers, other devices.
- To produce a good webcam video, do the following:
   * Avoid wearing baseball caps or hats with brims.
   * Ensure your computer or device is on a firm surface (a desk or table). Do NOT have
the computer on your lap, a bed, or other surface where the device (or you) are likely to
move.
   * If using a built-in webcam, avoid readjusting the tilt of the screen after the webcam
setup is complete.
   * Take the exam in a well-lit room, but avoid backlighting (such as sitting with your
back to a window).
- Remember that LockDown Browser will prevent you from accessing other websites or
applications.
- Closed notes, closed books.
- Two cheat sheets of the size of **8.5 in by 11 in** is allowed. Both sides of sheets can be
used. You will be need to show your cheat sheets at the beginning of the testing time.
You can also choose them to use as your scrap paper. Thus if you need some space to do
your calculation, etc., then you might not want to leave some empty space in your 8.5 in
by 11 in cheat sheet and not fill it up with other information.

- You can also have a greensheet (MIPS reference sheet), printed in a double sided sheet or single sided sheets.
-You can also have one sheet containing the single cycle datapath.
-You may not wear any kind of watch.
-You can bring a calculator. You may not share a calculator with anyone. TI-Nspires are not allowed.

Violating any of the rules stated above might result in a grade of E or XE in this course.

Topics to be covered:

Section 1.6 – Performance

-CPU time (seconds, picoseconds), Execution Time
-Performance = 1 / Execution time
-Performance Ratio
-Clock Cycles
-Clock Cycle time (period)
-Clock rate (Hz, GHz) = 1 / Clock Cycle time
-CPI (cycles per instruction)
-MIPS (millions of instructions per second)

Chapter 4 – Processor

-Single Cycle Datapath & Control (lw, sw, R-type (add, sub, and, or, slt), bne, j)
    -which paths in the datapath rs, rt, rd, and shamt data are using? Op and funct code are used for controls. Be familiar with all paths in the datapath and control signals.

R-type/format

op	rs	rt	rd	shamt	funct
31:26	25:21	20:16	15:11	10:6	5:0

I-type/format

op	rs	rt	immediate
31:26	25:21	20:16	15:0

J-type/format

| op	address
31:26	25:0

    -be able to add datapath(s) and control(s) to the single cycle datapath for a given
      Instruction.
    -Control Signals – RegDst, RegWrite, ALUSrc, PCSrc, MemRead, MemWrite,
      MemtoReg, Branch ALUOp (ALUOp1 and ALUOp0)
 -Compute CPI, IPS (instructions per second), cycle numbers, etc.

Chapter 4 – Pipelining

Steps to execute an instruction in the pipelined datapath:
1. IF: Instruction Fetch
2. ID: Instruction Decode and Register File Read
3. EX/ALU: Execution or Address Calculation
4. MEM: Data Memory Access
5. WB: Write Back
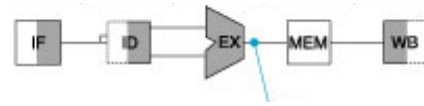
- What are structural hazards, data hazards, and control hazards?
- What are forwarding and stalling?
- How does the forwarding detection unit check if it can resolve data hazards using forwarding?
- How does the hazard detection unit check if the pipeline needs to stall?
- Know the structure of pipelined datapath with its control (pipeline registers – IF/ID, ID/EX, EX/MEM, MEM/WB – are added to the single cycle datapath, etc.)
- Control Hazards/Branch Hazards handling
    2 ways to improve branch performance:
    o To predict the branch decision with a high probability.
    o To reduce the cost of the taken branch, by moving the branch decision in the earlier cycle (reduce to penalty of one cycle):
        ▪ Moving the branch target address calculation to the ID stage from the EX stage.
        ▪ Evaluating the branch decision (check the equality) during the ID stage by adding a new unit to check the equality. – First exclusive ORing their respective bits, and then ORing all the result bits.
    • IF.Flush signal is added to make control values zero in IF
- Exception handling
        o The signals IF.Flush, ID.Flush, and EX.Flush are used to make control values in IF, ID, and EX zero.

Chapter 5 – Memory Hierarchy

-Know Cache, block, cache miss, cache hit, miss rate, hit rate, miss penalty, tag, valid bit,
- 32-bit address consists of bits used for tags, bits for block indices, bits for block offset and bytes off set (2 bits).
- Compute the number of bits for tags, the number of bits for block indices, the number of bits for block offset. Compute the total number of bits used for a cache.
- How to deal with read hits, read misses, write misses, and write hits.
        Know Write-through, Write-back, write buffer
-How to compute the CPI or the CPU execution time using cache with its miss penalty.
-How to compute AMAT (average memory access time) = time for a hit + miss rate x miss penalty

- Cache structures
    - Direct mapped with one word blocks
    - Direct mapped with multi-word blocks
    - N-way Set Associative
    - Fully Associative
-Which structure has less miss rate compared to others?
-Which structure needs to use more bits for tags?
- LRU (Least Recently Used) Scheme

-Multi-Level Caches (L1 cache, L2 cache)
    -Be able to compare CPI, miss penalty (clock cycles) for just one level cache and
2 level caches.

- Virtual Memory, what is it?
- Two major motivations for Virtual Memory?
- Know pages, page fault
- Relocation
- It uses Write-back. And it uses Dirty-Bit to track whether page has been written since it
was read into the memory.
- Know Page Table, Page Table Register.
- Reference Bit, what is it for? How is it used?
- Know TLB (translation-lookaside buffer, a.k.a. translation cache)