CO Lab Assignment-2

---------- **Report**----------

CO215, CO Lab 2021, Assignment 2

Roll number: CSB19057

Name: PRASANJIT DUTTA

Objectives: To understand the working of a data path by integrating a minimal set of components in a simulation environment.

Exercises:

a. Integrate the already designed ALU (Assignment-1) into a data-path as shown in the diagram below in a logic simulator environment

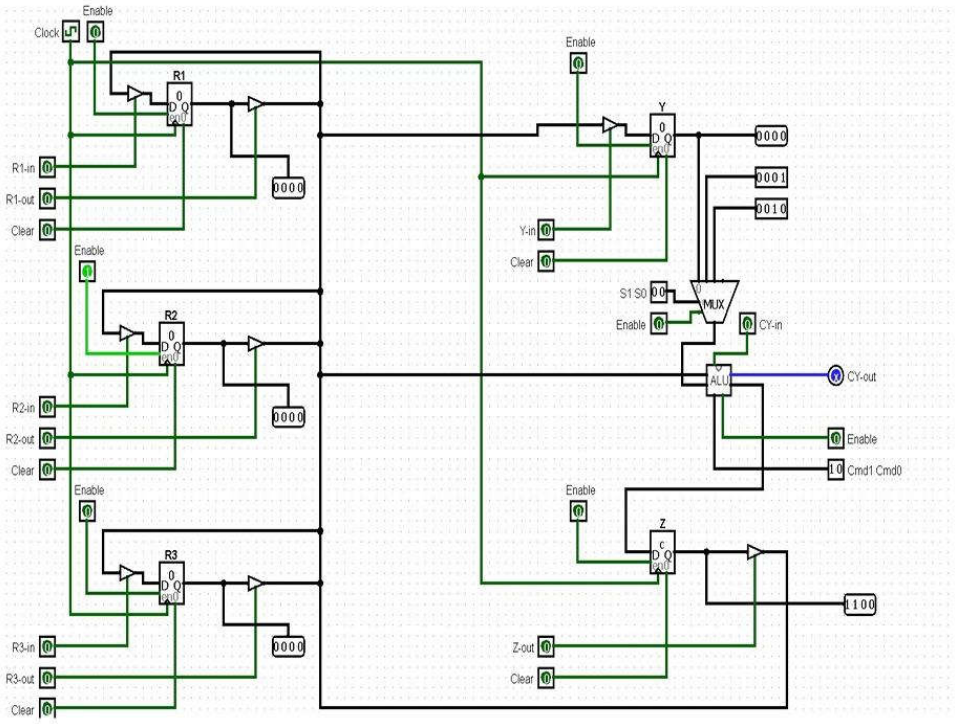
b. Write down the steps required to be issued for the operations:
   1. R3 <-R1
   2. R3 <-R1 + R2
   3. R3 <-R1 AND R2

c. Carryout the operations for at least three different values in R1, R2, R3 and make your observations.

d. Demonstrate the results.

e. Prepare a report containing the Objectives, Exercise Details, the Observations and the Learnings.

Details of work:



Observation Table: (include the filled in observation table below)

1. R3<-R1

Obs.	CLK	R1in	R1out	R1	R2in	R2out	R2	R3in	R3out	R3	Yin	Y	S1	S2	Cmd	Cyin	Cyout	Z	Zout
1	**0**	0	1	4	**0**	**0**	**0**	0	0	0	0	0	**1**	**1**	0	0	0	**0**	**0**
	1	0	1	4	**0**	**0**	**0**	0	0	0	0	0	**1**	**1**	0	0	0	**0**	**0**
2	**0**	0	0	3	**0**	**0**	**0**	0	0	4	1	0	**1**	**1**	0	0	0	**0**	**0**
	1	0	0	3	**0**	**0**	**0**	1	0	3	1	3	**1**	**1**	0	0	0	**0**	**0**
3	**0**	0	1	2	**0**	**0**	**0**	1	0	3	1	3	**1**	**1**	0	0	0	**0**	**0**
	1	0	1	2	**0**	**0**	**0**	1	0	2	1	2	**1**	**1**	0	0	0	**0**	**0**

2. R3<-R1+R2

Obs.	CLK	R1in	R1out	R1	R2in	R2out	R2	R3in	R3out	R3	Yin	Y	S1	S2	Cmd	S	Cyin	Cyout	Z	Zout
1	**0**	0	0	5	**0**	**0**	**4**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	5	**0**	**0**	**4**	0	0	0	1	5	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	0	5	**0**	**1**	**4**	0	0	0	0	5	**0**	**0**	01	0	0	0	**4**	**0**
	1	0	0	5	**0**	**0**	**4**	0	0	0	0	5	**0**	**0**	01	1	0	0	**4**	**9**
	1	0	0	5	**0**	**0**	**4**	0	0	0	0	5	**0**	**0**	01	1	0	0	**4**	**9**
	1	0	0	5	**0**	**0**	**4**	1	0	9	0	5	**0**	**0**	01	1	0	0	**4**	**9**
2	**0**	0	0	6	**0**	**0**	**2**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	6	**0**	**0**	**2**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	6	**0**	**0**	**2**	0	0	0	1	6	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	0	6	**0**	**1**	**2**	0	0	0	0	6	**0**	**0**	01	0	0	0	**0**	**0**
	1	0	0	6	**0**	**1**	**2**	0	0	0	0	6	**0**	**0**	01	1	0	0	**2**	**8**
	1	0	0	6	**0**	**0**	**2**	1	0	8	0	6	**0**	**0**	01	1	0	0	**2**	**8**
3	**0**	0	0	7	**0**	**0**	**3**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	7	**0**	**0**	**3**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	7	**0**	**0**	**3**	0	0	0	1	7	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	0	7	**0**	**1**	**3**	0	0	0	0	7	**0**	**0**	01	0	0	0	**0**	**0**
	1	0	0	7	**0**	**1**	**3**	0	0	0	0	7	**0**	**0**	01	1	0	0	**3**	**10**
	1	0	0	7	**0**	**0**	**3**	1	0	10	0	7	**0**	**0**	01	1	0	0	**3**	**10**

3. R3<-R1 AND R2

Obs.	CLK	R1in	R1out	R1	R2in	R2out	R2	R3in	R3out	R3	Yin	Y	S1	S2	Cmd	S	Cyin	Cyout	Z	Zout
1	**0**	0	0	5	**0**	**0**	**4**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	5	**0**	**0**	**4**	0	0	0	1	5	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	0	5	**0**	**1**	**4**	0	0	0	0	5	**0**	**0**	10	0	0	0	**4**	**0**
	1	0	0	5	**0**	**0**	**4**	0	0	0	0	5	**0**	**0**	10	1	0	0	**4**	**1**
	1	0	0	5	**0**	**0**	**4**	0	0	0	0	5	**0**	**0**	10	1	0	0	**4**	**1**
	1	0	0	5	**0**	**0**	**4**	1	0	4	0	5	**0**	**0**	10	1	0	0	**4**	**1**
2	**0**	0	0	6	**0**	**0**	**2**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	6	**0**	**0**	**2**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	6	**0**	**0**	**2**	0	0	0	1	6	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	0	6	**0**	**1**	**2**	0	0	0	0	6	**0**	**0**	10	0	0	0	**0**	**0**
	1	0	0	6	**0**	**1**	**2**	0	0	0	0	6	**0**	**0**	10	1	0	0	**2**	**1**
	1	0	0	6	**0**	**0**	**2**	1	0	2	0	6	**0**	**0**	10	1	0	0	**2**	**1**
3	**0**	0	0	7	**0**	**0**	**3**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	7	**0**	**0**	**3**	0	0	0	0	0	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	1	7	**0**	**0**	**3**	0	0	0	1	7	**1**	**1**	00	0	0	0	**0**	**0**
	1	0	0	7	**0**	**1**	**3**	0	0	0	0	7	**0**	**0**	10	0	0	0	**0**	**0**
	1	0	0	7	**0**	**1**	**3**	0	0	0	0	7	**0**	**0**	10	1	0	0	**3**	**1**
	1	0	0	7	**0**	**0**	**3**	1	0	3	0	7	**0**	**0**	10	1	0	0	**3**	**1**

Learnings:

The assignment gave a good insight into how the GPRs and ALU work together to perform the basics operation in a CPU. From this assignment, we got to learn about how the fetch and store operations are carried out in CPU.