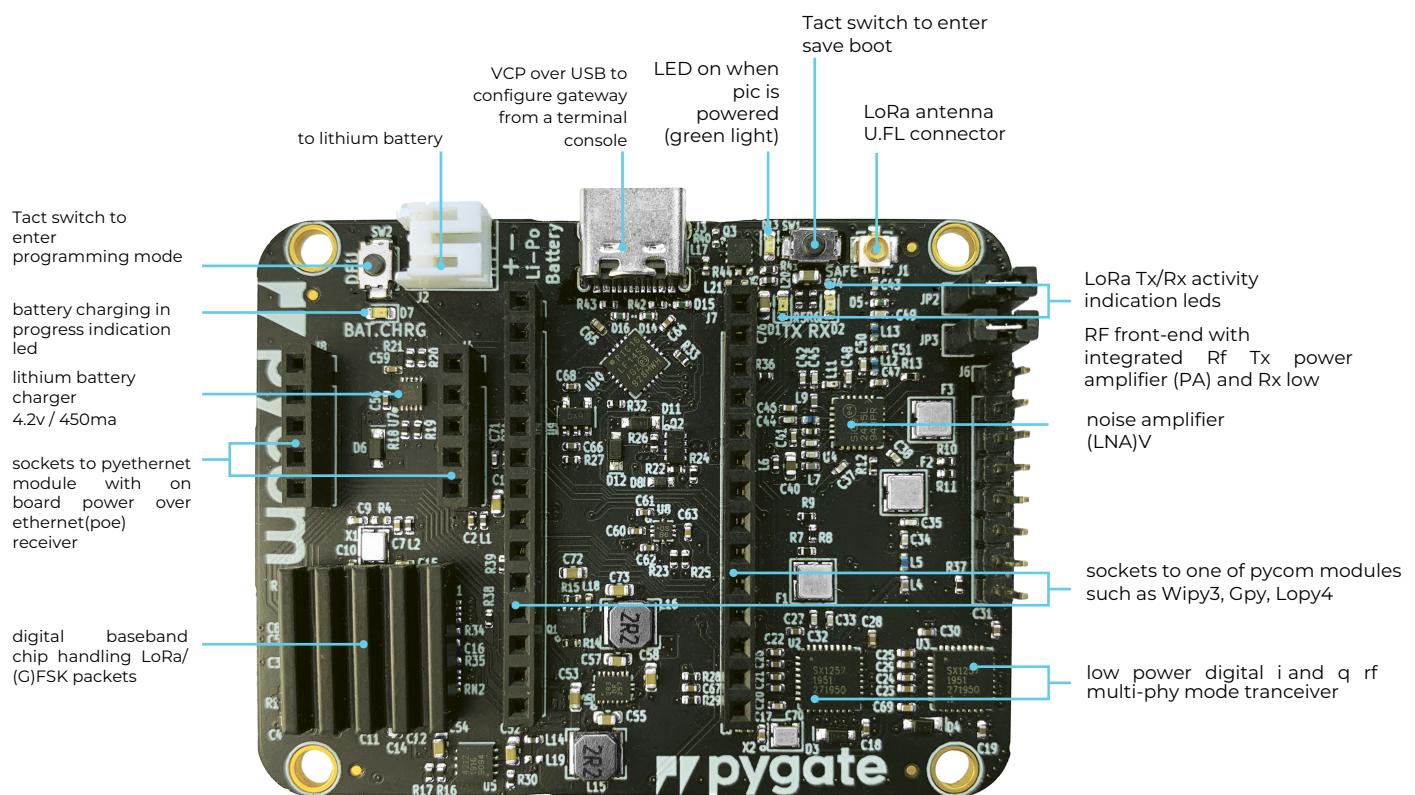




Datasheet
Version 1.0



1.0	Overview	03	12.0	Mechanical Specifications	24
2.0	Features	04	13.0	Ordering information	25
3.0	Specifications	04	13.1	Bundles	25
3.1	Hardware configuration	04	14.0	Packaging	25
3.2	Power supply options	04	15.0	Certification	26
3.3	Available signals on headers	04	15.1	EU Regulatory Conformance	26
3.4	Wireless connectivity options	04	15.2	Federal Communication Commission Interference Statement	26
3.5	Absolute maximum ratings	04	15.2.1	RF Warning Statement	26
4.0	Block Diagram	05	15.2.2	OEM integrator conditions	26
5.0	Pinout	06	15.2.3	End Product Labelling	27
5.1	PyEthernet socket pinout	07	15.2.4	Manual Information to the End User	27
5.2	Lithium battery connector pinout	07	16.0	Revision History	28
5.3	Module (WiPy3, GPy or LoPy4) socket pinout	08			
5.4	POWER and UART from/to the Pycom module header pinout	08			
6.0	Pin Details	09			
6.1	PyEthernet socket pin details	09			
6.2	Lithium battery connector pinout	09			
6.3	Module (WiPy3,GPy or LoPy4) socket pinout	10			
6.4	POWER and UART from/to the module header pinout	12			
6.5	Synchronization signal from a GPS receiver.	12			
7.0	API overview	13			
8.0	Configuring PyGate	13			
9.0	Programming the device	14			
10.0	Power	14			
11.0	Memory Map	14			
11.1	Supported features	14			
11.2	Reception Paths Characteristics	14			
11.3	Packet Engine and Data Buffers	15			
11.3.1	Receiver Packet Engine	15			
11.4	Transmitter Packet Engine	17			
11.5	Receiver IF Frequencies Configuration	21			
11.5.1	PyGate Using 2 x SX1257 Radios	21			



Size: 42mm x 20mm x 3.5mm

1.0 Overview

The Pygate is a super low-cost 8-channel LoRaWAN gateway that comes in the shape of a shield. It's got the well-known form factor from our other shields and you can connect your much loved WiPy3, LoPy4 or a GPy to it. Hook in your Pycom development boards up and you have yourself a nifty little decentralized IoT network in one go. Pygate also fits inside the Universal IP67 Case so you don't have to limit yourself to indoors.

2.0 Features

- Dual SX1257 transceivers for a total of 8 channels support simultaneously
- Ability to work in hostile RF environments such as close to mobile phones, Wi-Fi Routers and Bluetooth devices.
- Frequencies: 863-870 MHz and 902-928 MHz
- Baseband processor: SX1308
- Compatible with WiPy3, GPy and LoPy4
- Ultra-low power standby mode
- Ethernet with PoE via the optional daughter board
- Powered via USB, LiPo Battery and Power over Ethernet (PoE) injector via the optional daughter board
- 2mm pitch JST header for PHR-2 battery connector (pin 1 [+], pin 2 [-])
- LiPo battery charging (BQ24040) via the USB port or Ethernet PoE daughter board
- USB to serial connection for the Pycom module with auto programming features
- Same form factor as the Expansion Board v3.x
- Dimensions: 65mm (L) x 50mm (W) x 16mm (H)
- Fits the universal IP67 Case for outdoor use

3.0 Specifications

3.1 Hardware configuration:

- Transceivers: Dual Semtech SX1257 transceivers for a total of 8 channels support.
- Baseband processor: Semtech SX1308 running @ 133MHz.
- Frequency range: 863-870 MHz and 902-928 MHz
- LoRaWAN regions: EU868, US915, AU915, AS923, IN865
- Ultra low power standby mode allows backup battery operation.
- Same form factor as the expansion board.
- Compatible with WiPy3, GPy and LoPy4.
- USB to serial connection for the Pycom module with auto-programming features.

3.2 Power supply options:

- Micro USB.
- PoE (Power Over Ethernet) via the optional adapter board.
- LiPo or Li-Ion battery.
- LiPo battery charging via the USB or the PoE ports.

3.3 Available signals on headers:

- VCC supply.
- 3.3V from the Pycom module.
- VCC supply that goes off when the system enters sleep mode.
- 3V3 from the Gateway subsystem.
- UART Tx and UART Rx.
- GPS PPS input for adding an external GPS
- GND

3.4 Wireless connectivity options:

- WiFi: In combination with the WiPy3, LoPy4 or the GPy.
- Ethernet: In combination with the Ethernet adapter board. This also requires a Pycom module to provide the TCP stack.
- LTE: In combination with the GPy.
- Bluetooth.

3.5 Absolute maximum ratings:

- Operating temperature range depends on edition (please check with your distributor):
- Commercial temperature range: 0 to 70 °C
- Industrial temperature range: -40 to +85 °C
- Maximum RF Input Level: -10 dBm (0.1 mW)

4.0 Block Diagram

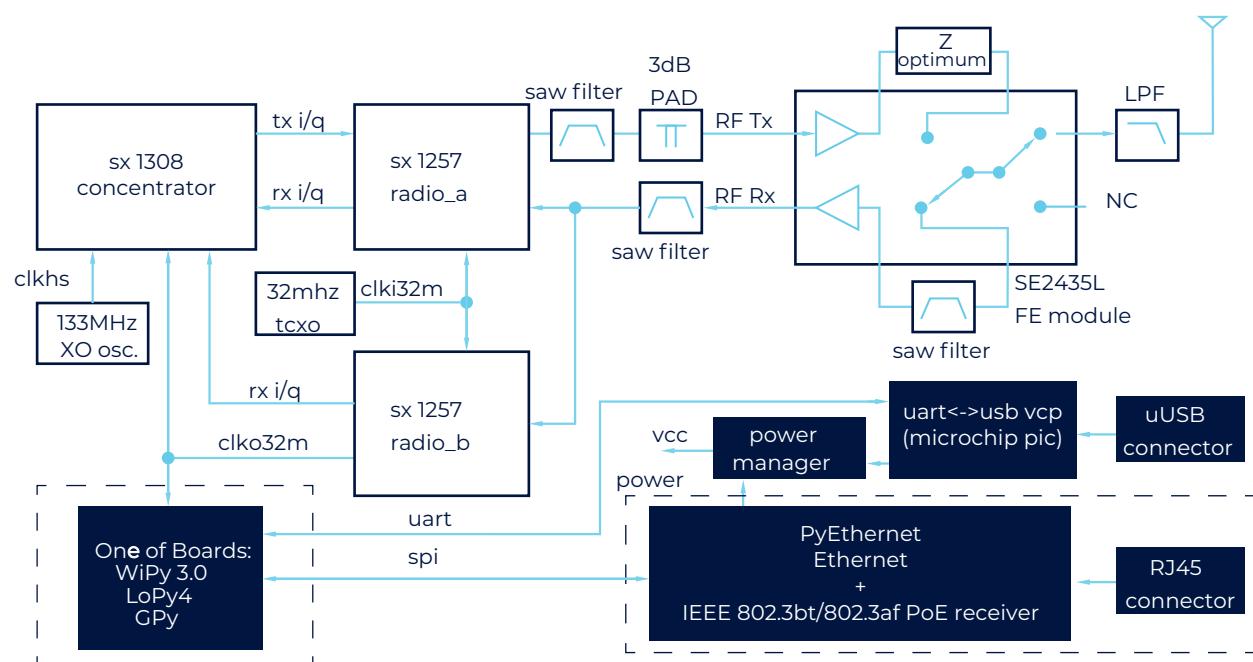


Figure 1 - Pygate Block Diagram

* blocks shown with a dashed outline are modules that are plugged into the Pygate

** PyEthernet module is not mandatory for the gateway operation, but recommended when Ethernet connectivity or Power over Ethernet functionality needed.

5.0 Pinout

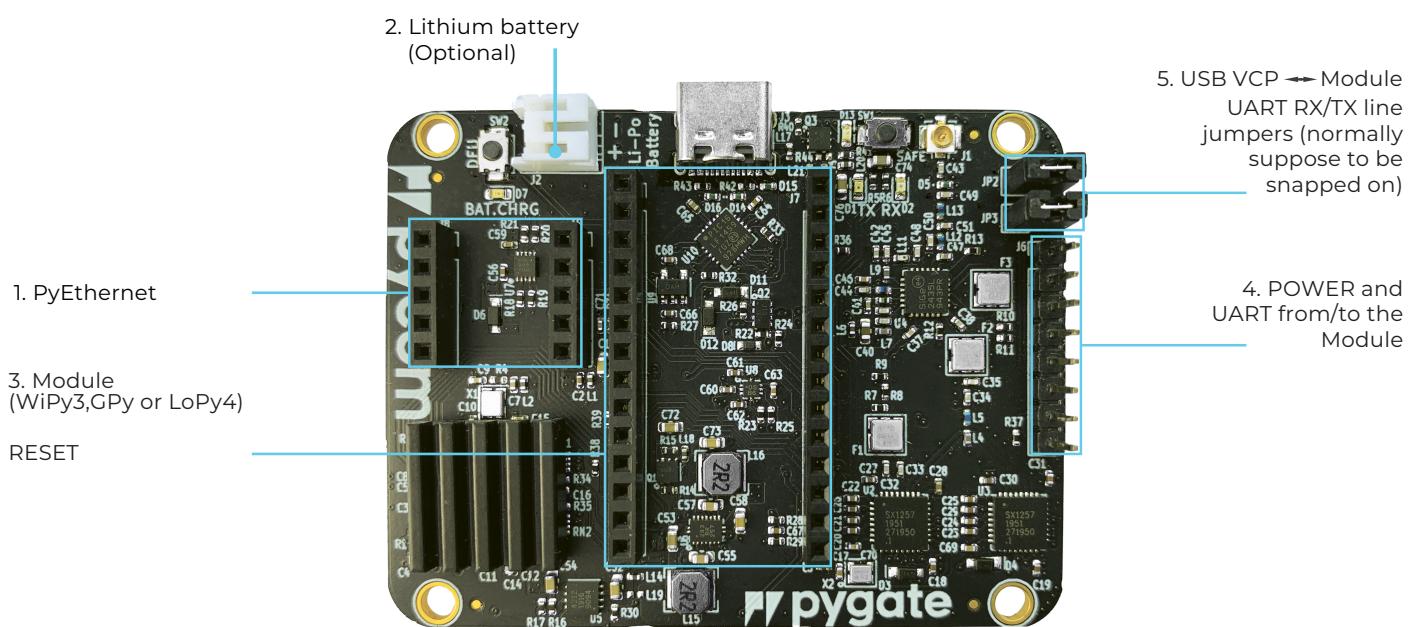


Figure 2 – Pygate pins and connectors

5.1 PyEthernet socket pinout

PyEthernet shield with
PoE(Power over
Ethernet)

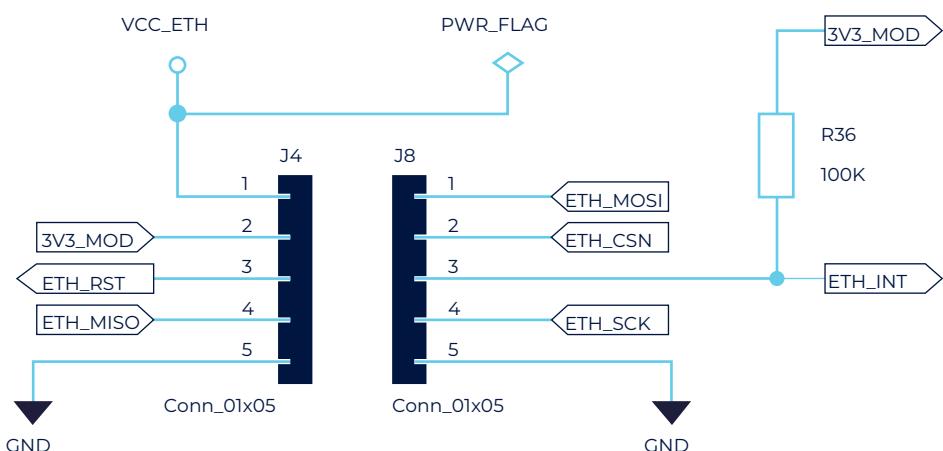


Figure 3 – Socket to PyEthernet

5.2 Lithium battery connector pinout

BATTERY
LiPo
3.6...4.2V

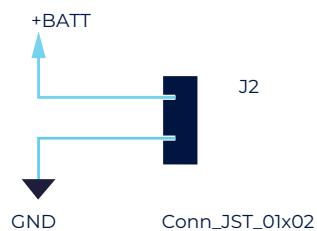


Figure 4 – JST (S2B-PH-K-S) Header to Lithium battery

5.3 Module (WiPy3, GPy or LoPy4) socket pinout

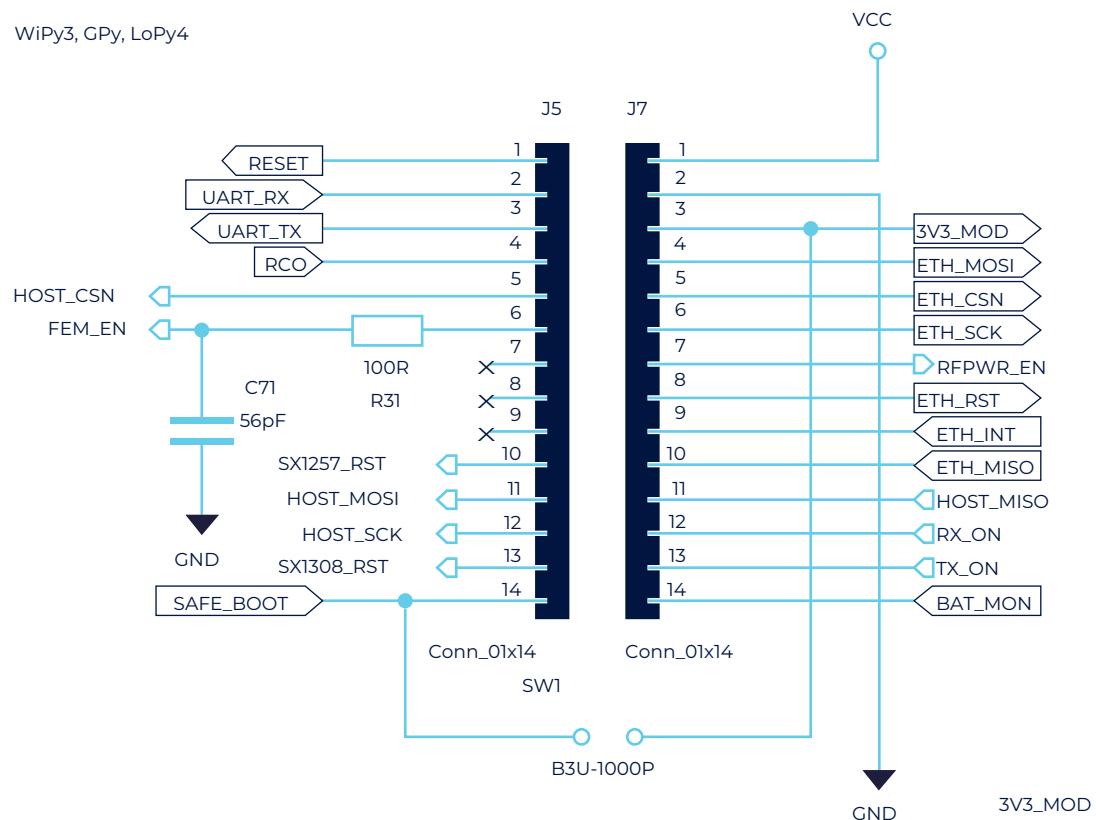


Figure 5 – Socket to Pycom module

5.4 POWER and UART from/to the Pycom module header pinout

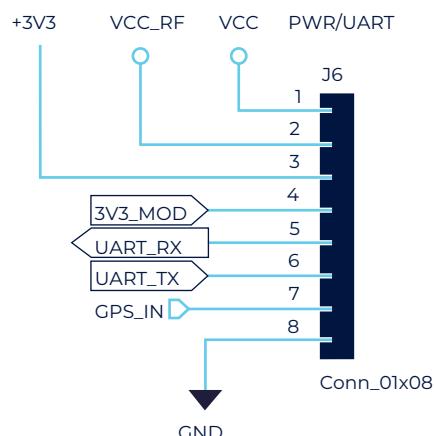


Figure 6 – Header with Power, UART, Sync from a GPS signals

6.0 Pin details

The tables below provide description of the pins. Pin direction given from Pygate board point of view.

6.1 PyEthernet socket pin details

Table 1 - J4 socket to a PyEthernet shield

Pin	Pin Name	Type	Description
1	VCC_ETH	Power In (+5V)	Power coming from PoE of PyEthernet
2	3V3_MOD	Power Out (+3.3V)	Power to PyEthernet from a Pycom module
3	ETH_RST	Output	Ethernet PHY reset
4	ETH_MISO	Input	Ethernet PHY SPI MISO
5	GND	Power (GND)	Ground

Table 2 - J8 socket to a PyEthernet shield

Pin	Pin Name	Type	Description
1	ETH_MOSI	Output	Ethernet PHY SPI MOSI
2	ETH_CSN	Output	Ethernet PHY SPI chip select
3	ETH_INT	Input	Ethernet PHY interrupt line
4	ETH_SCK	Output	Ethernet PHY SPI clock
5	GND	Power (GND)	Ground

6.2 Lithium battery connector pinout

Table 3 - J2 Battery connector pins

Pin	Pin Name	Type	Description
1	+BATT	Power In (+3.7V)	Power coming from Lithium Polymer battery
2	GND	Power (GND)	Ground

6.3 Module (WiPy3, GPy or LoPy4) socket pinout

Table 4 - J5 socket to a Pycom module

Pin	Pin Name	Type	Description
1	RESET	Output	Pycom Module reset, active low
2	UART_RX	Output	Module UART RX used for communication with PC and to program module in bootloader mode.
3	UART_TX	Input	Module UART TX used for communication with PC and to program module in bootloader mode.
4	RC0	Input/Output	If tied to GND during boot, the device will enter bootloader mode. Connected to the on-board RGB LED
5	HOST_CSN	Input	LoRa packets processor SPI chip select
6	FEM_EN	Input	Power enable of RF Front-End Module
7	NC	Floating	Reserved
8	NC	Floating	Reserved
9	NC	Floating	Reserved
10	SX1257_RST	Input	Reset of IQ RF Transceivers
11	HOST_MOSI	Input	LoRa packets processor SPI Master Output Slave Input
12	HOST_SCK	Input	LoRa packets processor SPI clock
13	SX1308_RST	Input	LoRa packets processor RESET
14	SAFE_BOOT	Output	To make Pycom module to enter the safe boot mode.

Table 5 - J7 socket to a Pycom module

Pin	Pin Name	Type	Description
1	VCC	Power Out (+VCC)	VCC is combined power from three sources, USB, Power-over-Ethernet or Lithium battery. Once USB and PoE power is not available lithium battery will supply the Pygate, else the battery will be charged with charging current 450mA.
2	GND	Power (GND)	Ground
3	3V3_MOD	Power Input (+3.3V)	+3.3V power coming from the Pycom module voltage regulator
4	ETH_MOSI	Input	PyEthernet shield SPI Master Output Slave Input
5	ETH_CSN	Input	PyEthernet shield SPI Chip Select
6	ETH_SCK	Input	PyEthernet shield SPI Clock
7	RFPWR_EN	Input	RF power ON/OFF control signal
8	ETH_RST	Input	PyEthernet shield reset
9	ETH_INT	Output	PyEthernet shield interrupt line
10	ETH_MISO	Output	PyEthernet shield SPI Master Input Slave Output
11	HOST_MISO	Output	LoRa packets processor SPI Master Input Slave Output
12	RX_ON	Output	LoRa RX activity signal (RX LED)
13	TX_ON	Output	LoRa TX activity signal (TX LED)
14	BAT_MON	Output	VCC Voltage Monitor (100k + 100k voltage divider)

6.4 POWER and UART from/to the Module header pinout

Table 6 - J6 header pins

Pin	Pin Name	Type	Description
1	VCC	Power Out (+VCC)	VCC is combined power from three sources, USB, Power-over-Ethernet or Lithium battery.
2	VCC_RF	Power Out (+VCC_RF)	VCC power controlled by RFPWR_EN signal
3	+3V3	Power Out (+3V3)	+3.3V coming form voltage regulator supplied by VCC_RF
4	3V3_MOD	Power Out (+VCC_MOD)	+3.3V power coming from the Pycom module voltage regulator
5	UART_RX	Input	See J5 pin 2 description
6	UART_TX	Output	See J5 pin 3 description
7	GPS_IN	Input	*Optional 1 pulse-per-second synchronization signal from a GPS receiver.
8	GND	Power (GND)	Ground

6.5 Synchronization signal from a GPS receiver

Figure 7 – 1 pulse-per-second synchronization signal from a GPS receiver



7.0 API overview

For details about software please visit:

[https://docs.pycom.io/firmwareapi/pycom/
machine/pygate/](https://docs.pycom.io/firmwareapi/pycom/machine/pygate/)

8.0 Configuring Pygate

For details about configuration please
visit:

<https://docs.pycom.io/tutorials/all/pygate/>

9.0 Programming the device

Refer to WiPy3, Gpy or LoPy module users manual

10.0 Power

AVG (no radio) 45mA
AVG (TTN gateway) 565mA
MIN (TTN gateway) 220mA
MAX (TTN gateway) 750mA

11.0 LoRa

11.1 Supported features Table 15 - J2 Battery connector pins

11.2 Reception Paths Characteristics

The SX1308/ SX1301 digital baseband chip contains 10 programmable reception paths. Those paths have differentiated levels of programmability and allow different use cases. It is important to understand the differences between those demodulation paths to make the best possible use from the system.

IF8 LoRa Channel

This channel can be connected to Radio A or B using any arbitrary intermediate frequency within the allowed range. This channel is LoRa only. The demodulation bandwidth can be configured to be 125, 250 or 500 kHz. The data rate can be configured to any of the LoRa available data rates (SF7 to SF12) but, as opposed to IF0 to 7, ONLY the configured data rate will be demodulated. This channel is intended to serve as a high speed backhaul link to other gateways or infrastructure equipment. This demodulation path is compatible with the signal transmitted by the SX1272 & SX1276 chip family.

IF9 (G)FSK Channel

Same as previous except that this channel is connected to a GFSK demodulator. The channel bandwidth and bitrate can be adjusted. This demodulator offers a very high level of configurability, going well beyond the scope of this document. The demodulator characteristics are essentially the same than the GFSK demodulator implemented on the SX1232 and SX1272 Semtech chips.

This demodulation path can demodulate any legacy FSK or GFSK formatted signal.

IF0 to IF7 LoRa Channels

Those channels can be connected individually to Radio A or B. The channel bandwidth is 125 kHz and cannot be modified or configured. Each channel IF frequency can be individually configured. On each of those channels any data rate can be received without prior configuration. Several packet using different data rates may be demodulated simultaneously even on the same channel. Those channels are intended to be used for a massive asynchronous star network of 10000's of sensor nodes. Each sensor may use a random channel (amongst IF0 to 7) and a different data rate for any transmission. Typically sensor located near the gateway will use the highest possible data rate in the fixed 125kHz channel bandwidth (e.g. 6 kbit/s) while sensors located far away will use a lower data rate down to 300 bit/s (minimum LoRa data rate in a 125 kHz channel). The SX1308/ SX1301 digital baseband chip scans the 8 channels (IF0 to IF7) for preambles of all data rates at all times. The chip is able to demodulate simultaneously up to 8 packets. Any combination of up to 8 packets is possible (e.g. one SF7 packet on IF0, one SF12 packet on IF7 and one SF9 packet on IF1 simultaneously). The SX1308/ SX1301 can detect simultaneously preambles corresponding to all data rates on all IF0 to IF7 channels. However it cannot demodulate more than 8 packets simultaneously. This is because the SX1308/ SX1301 architecture separates the preamble detection and acquisition task from the demodulation process. The number of simultaneous demodulation (in this case 8) is an arbitrary system parameter and may be set to any value for a customer specific circuit. The unique multi data-rate multi-channel demodulation capacity of channels 0 to 7 allow innovative network architecture to be implemented:

- End-point nodes can change frequency with each transmission in a random pattern. This provides vast improvement of the system in term of interferer robustness and radio channel diversity
- End-point nodes can dynamically perform link rate adaptation based on their link margin without adding to the protocol complexity. There is no need to maintain a table of which end point uses which data rate, because all data rates are demodulated in parallel.
- True antenna diversity can be achieved on the gateway side. Allows better performance for mobile nodes in difficult multi-path environments.

Packet Engine and Data Buffers

11.3 Packet Engine and Data Buffers

11.3.1 Receiver Packet Engine

Each time any of the demodulators decodes a packet, it is tagged with some additional information and stored in a shared data buffer (the data buffer size is 1024 bytes). For this purpose a specific data buffer management block reserves a segment with the necessary length in the data buffer and at the same time, stores the start address and the length of the packet field in a small FIFO type structure (named the access FIFO). The FIFO can contain up to 16 (start_addr, length) pairs.

A status register contains at any moment the number of packets currently stored in the data buffer (and in the access FIFO).

To retrieve a packet, Pycom module (host) first advances 1 step in the access FIFO by writing 1 to the 'next' bit. Then reads the (start_addr, length) information. Now Pycom module can retrieve in one SPI burst operation the entire packet and associated meta-data by reading 'length'+16 bytes starting at address 'start_addr' in the data buffer .. To do so, first position the HOST address pointer to 'start_addr', then read 'length' + 16 bytes from the 'packet_data' register. At the end of each byte the HOST address pointer is automatically incremented.

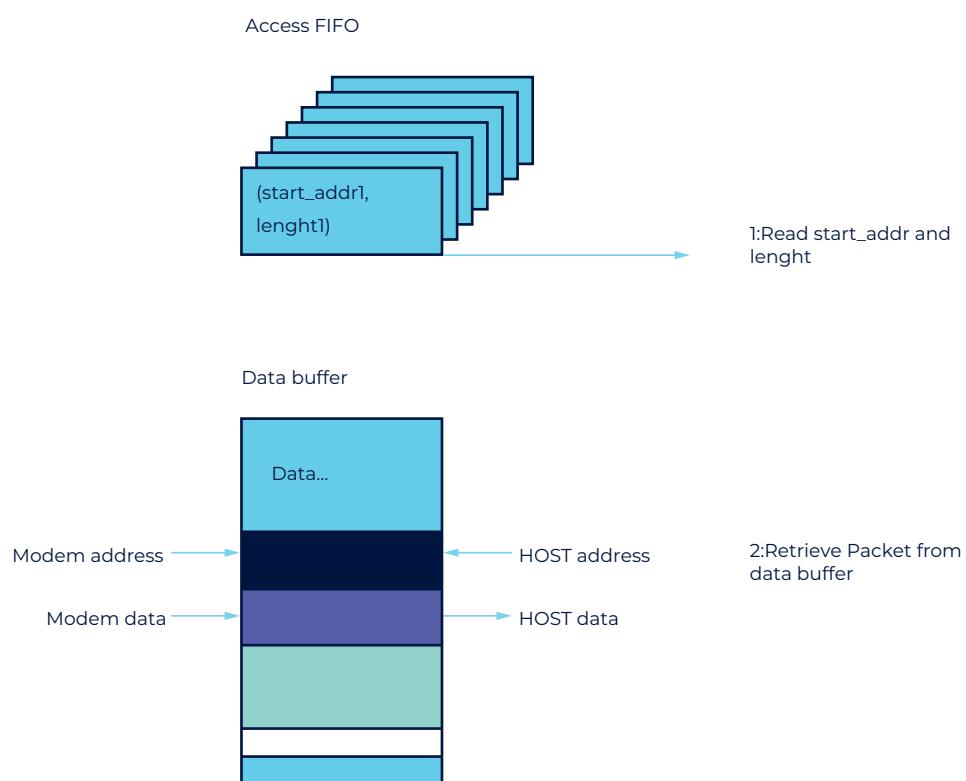


Figure 8 – Access FIFO and Data Buffer

The packet data is organized as follows:

Table 7 – LoRa Packet data fields

Packet Buffer data organization		
Offset from start pointer	Data stored	Comment
0		
...		
...	PAYLOAD	PAYLOAD DATA
...		
...		
...		
payload size -1		
payload size	CHANNEL	1 to 10 as described by block diagram
+1 payload size	SF[3:0],CR[2:0],CRC_EN	
+2 payload size	SNR Average	averaged SNR in dB on the packet lenght
+3 payload size	SNR MIN	minimum SNR (dB) recorded during packet lenght
+4 payload size	SNR MAX	maximum SNR recorded during packet lenght
+5 payload size	RSSI	Channel signal strengthin dB averaged during packet
+6 payload size	TMESSAMP[7:0]	
+7 payload size	TMESSAMP[15:8]	31 bit time stamp, 1 us step
+8 payload size	TMESSAMP[23:16]	
+9 payload size	TMESSAMP[31:24]	
+10 payload size	CRC Value[7:0] CRC	Value of the computet CRC 16
+11 payload size	Value[15:8]	
+12 payload size	MODEM ID	
+13 payload size	RX MAX BIN POS[7:0] RX	Correaltion peak position
+14 payload size	MAX BIN POS[15:8]	

+15 payload size	RX CORP SNR	Detection correlation SNR
+16 payload size	RESERVED	
+17 payload size	RESERVED	

This means that the host has to read 16 additional bytes on top of each packet to have access to all the meta-data. If the host is only interested in the payload itself + the channel and the data rate used, then payload + 2bytes is enough.

11.4 Transmitter Packet Engine

The Pygate transmitter can be used to send packets. The following parameters can be dynamically programmed with each packet:

- Radio channel
- FSK or LoRa modulation
- Bandwidth, data rate, coding rate (in LoRa mode), bit rate and Fdev (in FSK mode)
- RF output power
- Time of departure (immediate or differed based on the gateway hardware clock with 1us accuracy)

All those dynamic parameter fields are sent alongside the payload in the same data buffer. The data buffer can only hold a single packet at a time (next packet to be sent). The scheduling and ordering task is let to the host micro-processor. The host micro-processor can program the exact time of departure of each packet relative to the gateway hardware clock. The same clock is used to tag each packet received with a 32bits timestamp. The same 32bits time stamp principle is used in TX mode to indicate when to transmit exactly. This removes the real time constraint from the host micro-processor and allows very precise protocol timing.(For example, if the protocol running on the end point expects an acknowledgement exactly one sec after the end of each packet of its uplink). The host micro-processor pulls the uplink packet from the RX packet engine, realizes that it must send an acknowledgement, takes the uplink packet time stamp, simply increments it by 1 sec and uses that value to program the time of departure of the acknowledgement packet. Exactly one second (+/- 1us) after the uplink packet was received, the gateway will transmit the

desired acknowledgement packet. This allows very tight reception interval windows on the battery powered end points hence improved battery life.

The packet structure for transmission is as follow:

Table 8 - Packet structure for transmission

Byte	Subfield	Description	Comment
0	23:16		
1	15:8	Channel Frequency	$F_{chan}/32MHz \times 2^{19}$
2	7:0		
3	31:24		
4	23:16	Start Time	Value at the timer at which the modem has to start (in us)
5	15:8		
6	7:0		
	7:6	Reserved	
7	5:5	Radio select	Select radio A (0) or B (1)
	4:4	Modulation Type	0:LoRa, 1: FSK
	3:0	Tx power	>7:20dBm, otherwise 14dBm
8		Reserved	

LoRa:

Byte	Subfield	Description	Comment
	7:7	Payload CRC16 enable	Enables CRC16
9	6:4	Coding Rate	Coding Rate = $4/(4+CR)$
	3:0	SF	6 to12
10	7:0	Payload lenght	numbers of bytes
	7:3	Reserve	
11	2:2	Implicit header enable	
	1:0	Modulation Bandwidth	2:500, 1:250, 0:125 kHz
12	15:8	Preamble symbol number	Number of symbols in the preamble
13	7:0		
14		Reserved	
15		Reserved	

FSK:

Byte	Subfield	Description	Comment
9	7:0	FSK frequency deviation	Frequency deviation in kHz
10	7:0	Payload length	Number of bytes
0		Packet mode	0-> fixed lenght 1->variable lenght
1		CRC enable	0-> No CRC 1->CRC
11	3:2	Dcfree ENC	00-> DC free encoding off 01->Manchester encoding 10-> Whitening encoding 1->Reserved
4		Crc IBM	0-> CCITT CRC 1->IBM CRC
12	15:8	FSK Preamble Size	
13	7:0	FSK Preamble Size	The number of preamble bytes send over the air before the sync pattern
14	15:8	FSK Bit Rate	bit rate=32e6/(FSK bit rate)
15	7:0	FSK Bit Rate	
16		Payload first byte	up to 128 bytes

For words of more than 1 byte, MSBs are sent first.

Bytes 9 to 15 vary depending whether the FSK or the LoRa TX modem is being used.

The user payload starts at byte 16. This is the first byte that will be received by the end point. Bytes 0 to 15 are not transmitted and are just used to dynamically configure the gateway prior to emission.

where:

- Radio A PLL is set to 867.0 MHz
- Radio B PLL is set to 868.4 MHz
- The system uses 8 separate 125 kHz LoRa channels for star connection to sensors
- One high speed 250 kHz LoRa channel for connection to a relay
- One high speed 200 kHz GFSK channel for meshing

11.5

Receiver IF Frequencies Configuration

Each IF path intermediate frequency can be programmed independently from -2 to +2 MHz. The following sections give a few programming examples for various use cases.

11.5.1 PyGate Using 2 x SX1257 Radios

The SX1257 RX PLLs can be configured to any frequency inside the 868/900 MHz ISM band with a 61 Hz step. The SX1257 streams I/Q samples through a 2 wire digital interface. The bits stream corresponds directly to the I/Q sigma delta ADCs outputs sampled at 32 MSps. This delta sigma stream must be low-passed and decimated to recover the available 80dB dynamic of the ADCs. After decimation the usable spectrum bandwidth is ± 400 kHz centered on the RX PLL carrier frequency.

The following plot gives the spectral power content of the I/Q bit stream.

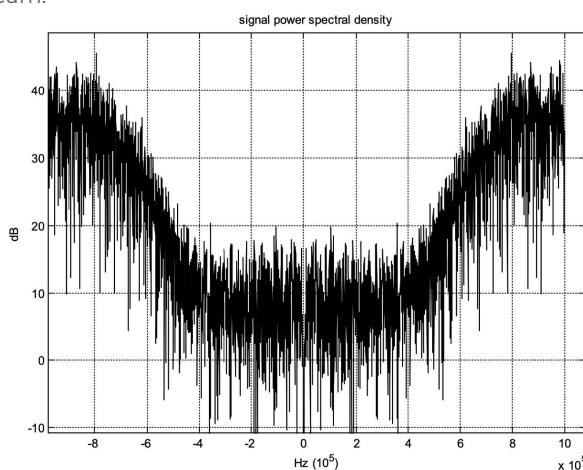


Figure 9 - SX1257 Digital I/Q Power Spectral Density

The quantization noise raises sharply outside the -400 to +400 kHz range. For more details on the SX1257 radio specifications please consult the specific product datasheet.

The following plot represents a possible use case

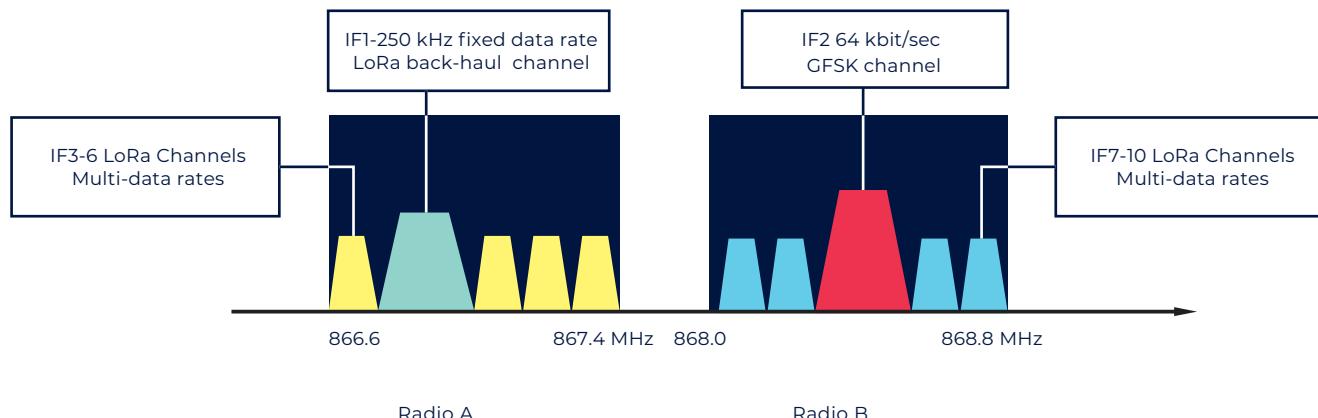


Figure 10 - Radio Spectrum

In the previous example the various IF frequencies would be set as follow:

Table 9 – IF Frequency Set

IF8	A: -125 kHz	LoRa backhaul, fixed data-rate
IF9	B: 0 kHz	GFSK backhaul
IFO	A: -312.5 kHz	LoRa multi-data rate channel
IF1	A: 62.5 kHz	
IF2	A: 187.5 kHz	
IF3	A: 312 kHz	
IF4	B: -312 kHz	
IF5	B: -187 kHz	
IF6	B: 187.5 kHz	
IF7	B: 312.5 kHz	

If for example, 8 contiguous 125 kHz LoRa channels are desired the following configuration may be used:

- Radio A PLL is set to 867 MHz
- Radio B PLL is set to 876.5 MHz

The two radio baseband spectrum overlap a little bit.

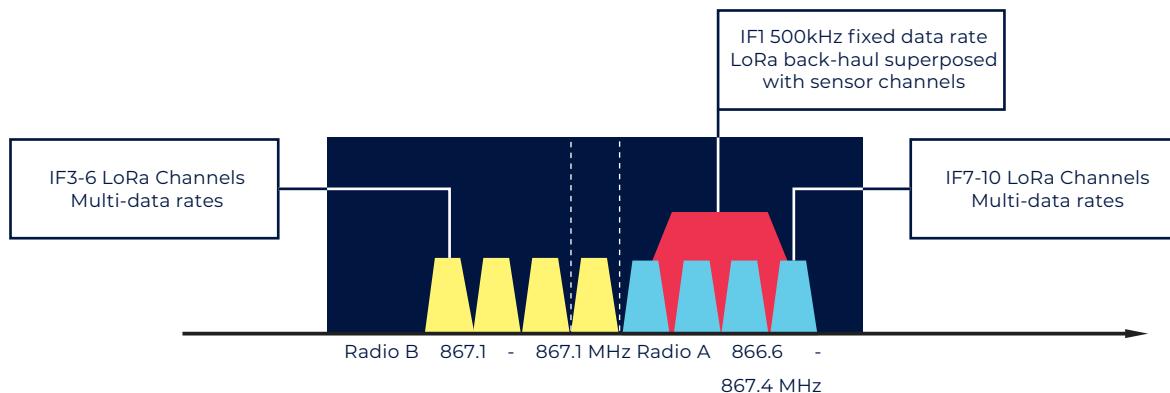


Figure 11 - Radio Spectrum

The following IF frequencies are used:

Table 10 – IF Frequency Used

IF8	A: 0 kHz	LoRa backhaul, fixed data-rate
IF9	Not used	GFSK backhaul
IFO	B: -187.5 kHz	LoRa multi-data rate channel
IF1	B: -62.5 kHz	
IF2	B: 62.5 kHz	
IF3	B: 187.5 kHz	
IF4	A: -187.5 kHz	
IF5	B: -187 kHz	
IF6	A: 62.5 kHz	
IF7	A: 187.5 kHz	

Note : As shown in this example the 500 or 250 kHz IF1 LoRa channel may overlap with the multidata rate IF3 to 10 channels. Transmissions happening in the IF7 to 10 channels will be noise like for the IF1 LoRa demodulator and reciprocally. It is however better from a performance point of view to separate as much as

possible different channels mainly when the associated signal powers are very different (like between a backhaul link which usually enjoys line-of-sight attenuation and sensor link with very low signal levels).

12.0 Mechanical Specifications

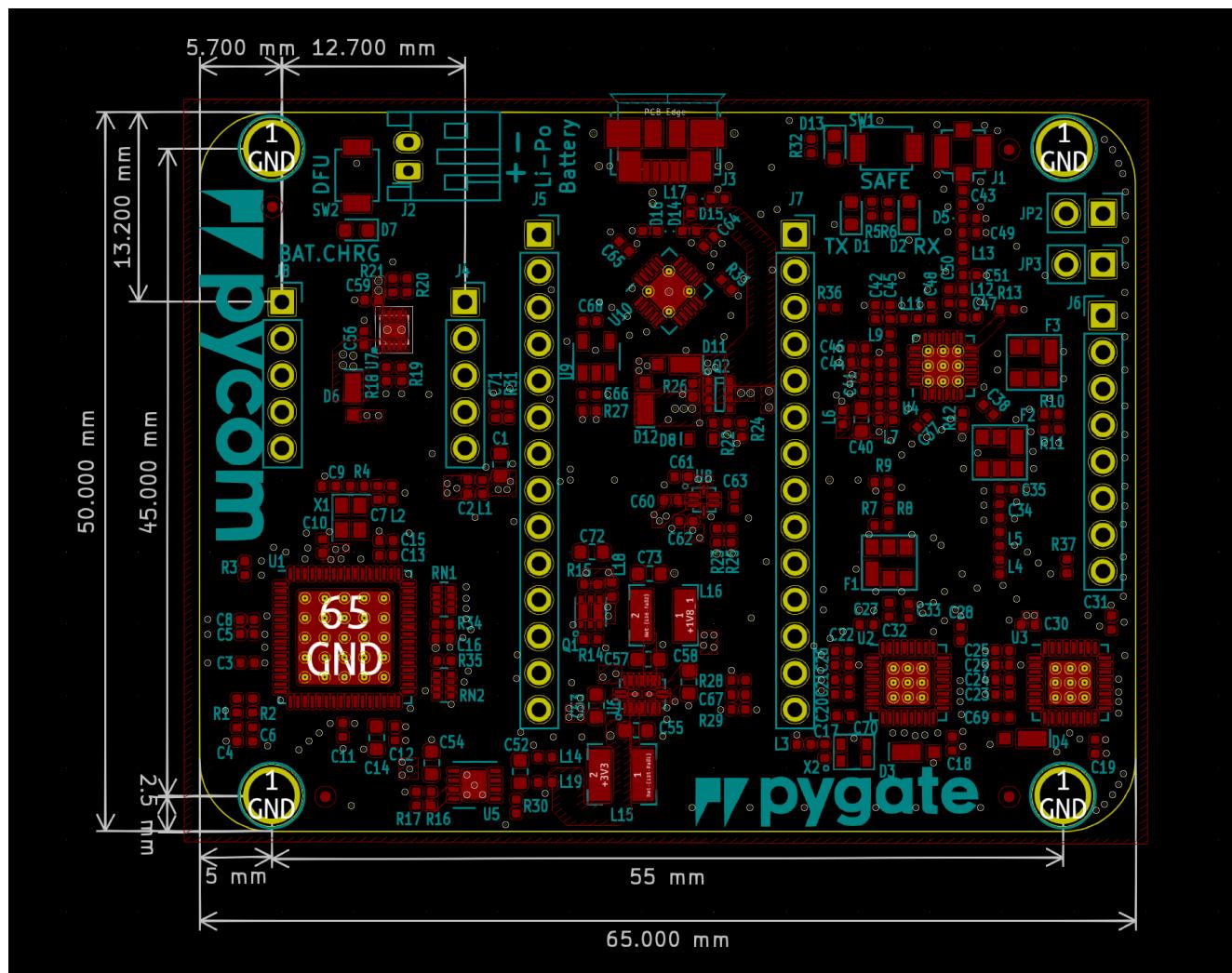


Figure 12 - Mechanical drawing (top down view) – Units: mm

* Tallest component: 12 mm

13.0 Ordering information

Table 1- Ordering information

Product EAN	Description
604565285904	PyGate 868 Mhz
604565285973	PyGate 915 Mhz
604565285911	PoE Adapter for PyGate

13.1 Bundles

Table 12 -Bundles

Description	Contents
PyGate 868 Mhz with PoE	PyGate 604565285904 and PoE 604565285911
PyGate 915 Mhz with PoE	PyGate 604565285973 and PoE 604565285911

14.0 Packaging

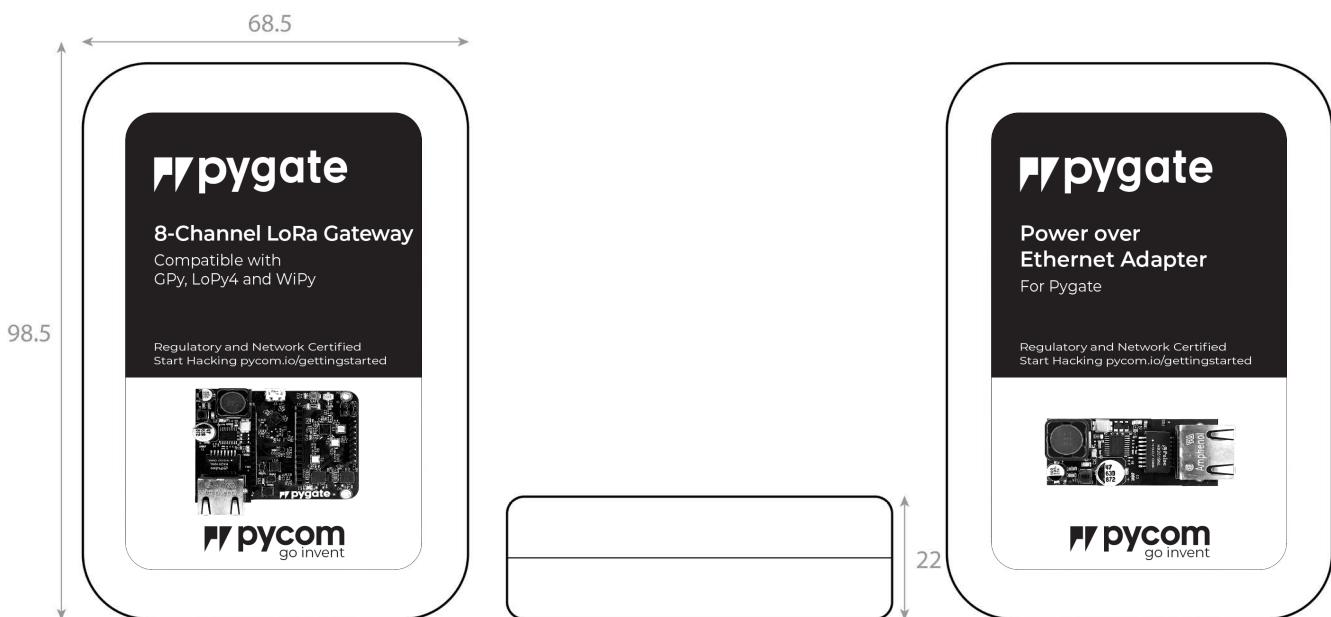


Figure 10 – Mechanical drawing of packaging – Units: mm

The module will come inside a reusable anti-static bag. If the module has headers it will also be inserted into anti-static foam.

Total weight inc. packaging (with headers): __g Total weight inc. packaging (without headers): __g

15.0 Certification

Certification of Pygate is ongoing.
Please contact Pycom Sales for more details.

15.2.1 RF Warning Statement

To comply with FCC RF exposure compliance requirements, the antennas used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Regulatory Information

15.1 EU Regulatory Conformance

Hereby, Pycom Ltd declares that this device is in compliance with the essential requirements and other relevant provisions of Directive 1999/5/EC

15.2 Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

CAUTION: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

15.2.2 OEM integrator conditions

This device is intended only for OEM integrators under the following conditions:

- The antenna must be installed such that 20 cm is maintained between the antenna and users and
- The transmitter module may not be co-located with any other transmitter or antenna.
As long as the two conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed. To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.
The module is limited to OEM installation ONLY. The module is limited to installation in mobile or fixed application. We hereby acknowledge our responsibility to provide guidance to the host manufacturer in the event that they require assistance for ensuring compliance with the Part 15 Subpart B requirements. **IMPORTANT NOTE:** In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

15.2.3 End Product Labelling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following:
"Contains FCC ID: 2AJMTPYGATE01". The grantee's FCC ID can be used only when all FCC compliance requirements are met. The following FCC part 15.19 statement has to also be available on the label:

This device complies with Part 15 of FCC rules.
Operation is subject to the following two conditions:

- this device may not cause harmful interference and
- this device must accept any interference received, including interference that may cause undesired operation.

15.2.4 Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

In the user manual of the end product, the end user has to be informed that the equipment complies with FCC radio-frequency exposure guidelines set forth for an uncontrolled environment.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

The end user manual shall include all required regulatory information/warning as show in this manual.

The maximum operating ambient temperature of the equipment declared by the manufacturer is **0 – 70 C** Receiver category 3

16.0 Revision History

Table 12– Document revision history

Revision / Date	Description
Rev 0.1 / 11.11.2019	First DRAFT release