Justification for GPIO

Four, non-adjacent register bits must be written to put pin in GPIO mode. Beforehand, the pin is configured in a multiplexing receive mode (UART) that is inherently pulled LOW.

- For a single burn-wire circuit to be enabled, four register bits would have to be flipped to enable the relay GPIO pin and hold it HIGH. That pin would have to be held high (and not be flagged as a misconfigured register during routine software checks), and then an additional four non-adjacent register bits flipped on the GPIO pin controlling the burn-wire MOSFET.

Example SEU

SAMD21 SEU cross-section hasn't been measured. Use educated guess of an ST-16 supervisor processor (3.27e-14 cm2) for 105 MeV protons. SPENVIS simulated about 100 protons/cm2 per second hitting SAMD21. Assuming energy invariant cross-section: **that's about one upset every 3e11 seconds**.

- 86400/3e11 = 2.88e-7 (1 in 3.4e6) probability of bit flip in a day
- number required bit flips for deployment = 4+3(4) = 16
  (2.88e-7)^16 = 2.24e-105 (1 in 4.46e106) chance of SEU-induced burn-wire actuation. (it's actually an even smaller chance since there's also a chance of flipping the bit BACK to it's original state)