CLC430

CLC430 General Purpose 100MHz Op Amp with Disable

Literature Number: SNOS823B

National Semiconductor

January 2001

CLC430
General Purpose 100MHz Op Amp with Disable

General Description

The CLC430 is a low cost, wideband monolithic amplifier for general purpose applications. The CLC430 utilizes National's patented current feedback circuit topology to provide an op amp with a slew rate of 2000V/µs, 100MHz unity-gain bandwidth and fast output disable function. Like all current feedback op amps, the CLC430 allows the frequency response to be optimized (or adjusted) by the selection of the feedback resistor. For demanding video applications, the 0.1dB bandwidth to 20MHz and differential gain/phase of 0.03%/0.05˚ make the CLC430 the preferred component for broadcast quality NTSC and PAL video systems.

The large voltage swing (28V_{PP}) , continuous output current (85mA) and slew rate (2000V/µs) provide high-fidelity signal conditioning for applications such as CCDs, transmission lines and low impedance circuits. Even driving loads of 100Ω, the CLC430 provides very low 2nd and 3rd harmonic distortion at 1MHz (−76/−82dBc).

Video distribution, multimedia and general purpose applications will benefit from the CLC430's wide bandwidth and disable feature. Power is reduced and the output becomes a high impedance when disabled. The wide gain range of the CLC430 makes this general purpose op amp an improved solution for circuits such as active filters, differential-to-single-ended drivers, DAC transimpedance amplifiers and MOSFET drivers.

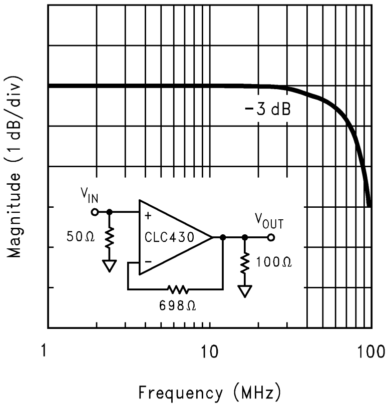
Features

- 0.1dB gain flatness to 20MHz (A_V = +2)
- 100MHz bandwidth (A_V = +1)
- 2000V/µs slew rate
- 0.03%/0.05˚ differential gain/phase
- ±5V, ±15V or single supplies
- 100ns disable to high impedance output
- Wide gain range
- Low cost

Applications

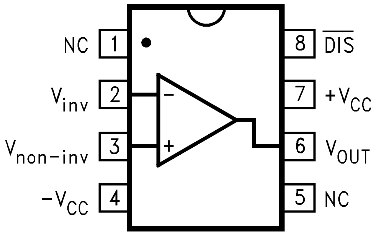
- Video distribution
- CCD clock driver
- Multimedia systems
- DAC output buffers
- Imaging systems

Unity-Gain Frequency Response



DS012711-1

Connection Diagram



DS012711-4

Pinout
DIP & SOIC

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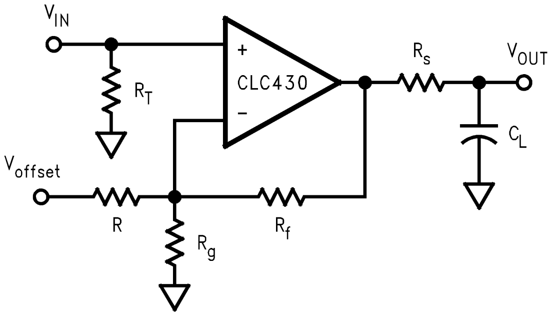
Typical Application


V_{IN}
R_T
+
CLC430
−
R_s
V_{OUT}
C_L
V_{offset}
R
R_g
R_f

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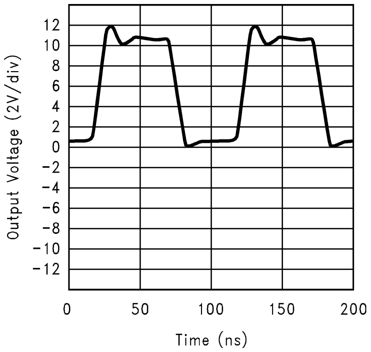


DS012711-3

CCD Clock Driver

Ordering Information

Package	Temperature Range Industrial	Part Number	Packaging Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC430AJP	CLC430AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC430AJE	CLC430AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±16.5V
Short Circuit Current	(see note 4)
Common-Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (soldering 10 sec)	+300˚C
ESD (human body model)	4000V

Operating Ratings

Thermal Resistance

Package	θ_{JC}	θ_{JA}
MDIP	60˚C/W	115˚C/W
SOIC	55˚C/W	135˚C/W

Electrical Characteristics

V_{CC} = ±15 V, A_V = +2V/V, R_f = 604Ω, R_L = 100Ω; unless specified

Symbol	Parameter	Conditions	V_{CC}	Typ	Min/Max Ratings (Note 2)			Units
	Ambient Temperature	CLC430AJ		+25˚C	+25˚C	0 to 70˚c	−40 to 85˚C	
Frequency Domain Response								
	Unity-Gain Bandwidth	$V_{OUT} < 1.0V_{PP}$	±15	100				MHz
	Small-Signal Bandwidth	$V_{OUT} < 1.0V_{PP}$	±15	75	50	45	42	MHz
		$V_{OUT} < 1.0V_{PP}$	±5	55	35			MHz
	0.1dB Bandwidth	$V_{OUT} < 1.0V_{PP}$	±15	20	7			MHz
		$V_{OUT} < 1.0V_{PP}$	±5	16				MHz
	Large-Signal Bandwidth	$V_{OUT} < 10V_{PP}$		30	22	20	19	MHz
	Gain Flatness	$V_{OUT} < 1.0V_{PP}$						
	Peaking	DC to 10MHz		0.0	0.1	0.2	0.2	dB
	Rolloff	DC to 20MHz		0.1	0.7	1.0	1.2	dB
	Linear Phase Deviation	DC to 20MHz		0.5	1.8	2.0	2.1	deg
	Differential Gain	4.43 MHz, R_L = 150Ω	±15	0.03	0.05	0.06	0.06	%
		4.43 MHz, R_L = 150Ω	±5	0.03	0.05			%
	Differential Phase	4.43 MHz, R_L = 150Ω	±15	0.05	0.09	0.12	0.13	deg
		4.43 MHz, R_L = 150Ω	±5	0.09	0.19			deg
Time Domain Response								
	Rise and Fall Time	2V Step		5	7	7	7	ns
		10V Step		10	14	14	14	ns
	Settling Time to 0.05%	2V Step		35	50	55	55	ns
	Overshoot	2V Step		5	15	15	15	%
	Slew Rate	20V Step		2000	1500	1450	1450	V/µs
Distortion And Noise Response								
	2nd Harmonic Distortion	$1V_{PP}$, 1MHz, R_L = 500Ω		−89				dBc
	3rd Harmonic Distortion	$1V_{PP}$, 1MHz, R_L = 500Ω		−92				dBc
	Input Voltage Noise	>1MHz		3.0	3.5	3.7	3.8	$nV/\sqrt{Hz}$
	Non-Inverting Input Current Noise	>1MHz		3.2	6.0	6.3	6.8	$pA/\sqrt{Hz}$
	Inverting Input Current Noise	> 1MHz		15	18	20	21	$pA/\sqrt{Hz}$
DC Performance								
	Input Offset Voltage (Note 3)		±15	1.0	7.5	9.0	10.0	mV
	Average Drift			25	-	50	50	µV/˚C
	Input Bias Current (Note 3)	Non-Inverting	±15, ±5	3	14	16	20	µA
	Average Drift		-	10	-	100	100	nA/˚C

Electrical Characteristics (Continued)

V_{CC} = ±15 V, A_V = +2V/V, R_f = 604Ω, R_L = 100Ω; unless specified

Symbol	Parameter	Conditions	V_{CC}	Typ	Min/Max Ratings (Note 2)			Units
DC Performance								
	Input Bias Current (Note 3)	Inverting	±15, ±5	3	14	15	17	µA
	average drift		-	10	-	60	90	nA/˚C
	Power-Supply Rejection Ratio	DC		62	56	54	53	dB
	Common-Mode Rejection Ratio	DC		62	54	53	52	dB
	Supply Current (Note 3)	$R_L = \infty$	±15, ±5	11, 8.5	12	13	14.5	mA
	Disabled (Note 3)	$R_L = \infty$	±15, ±5	1.5	2.0	2.2	2.4	mA
Switching Performance								
	Turn On Time			200	300	320	340	ns
	Turn Off Time	(Note 5)		100	200	200	200	ns
	Off Isolation	10MHz		59	56	56	56	dB
	High Input Voltage	V_{IH}	±15	11.8	12.5	12.7		V
			±5	1.8	2.5	2.7		V
	Low Input Voltage	V_{IL}	±15	10.8	10.5	10.0		V
			±5	0.8	0.6	0.1		V
Miscellaneous Performance								
	Non-Inverting Input Resistance			8.0	3.0	2.5	1.7	MΩ
	Non-Inverting Input Capacitance			0.5	1.0	1.0	1.0	pF
	Input Voltage Range	Common Mode	±5	±12.5	±12.3	±12.1	±11.8	V
		Common Mode	±5	±2.5	±2.3	±2.2	±1.9	V
	Output Voltage Range	$R_L = \infty$	±15	±14	±13.7	±13.7	±13.6	V
		$R_L = \infty$	±5	±4.0	±3.9	±3.8	±3.7	V
	Output Current			±85	±60	±50	±45	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

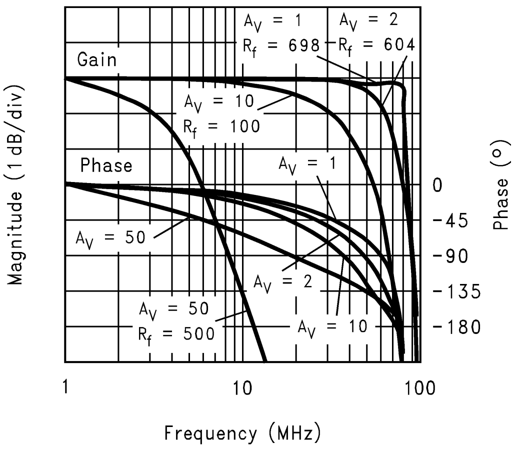
Note 3: AJ-level: spec. is 100% tested at +25˚C.

Note 4: Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 125mA.

Note 5: To <50dB attenuation @10MHz.

Typical Performance Characteristics (V_{CC} = ±15V, A_V = +2V/V, R_f = 640Ω, R_L = 100Ω; Unless Specified)

Non-Inverting Frequency Response



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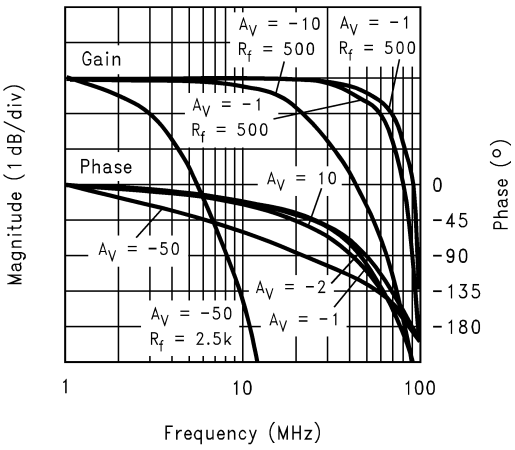
Inverting Frequency Response



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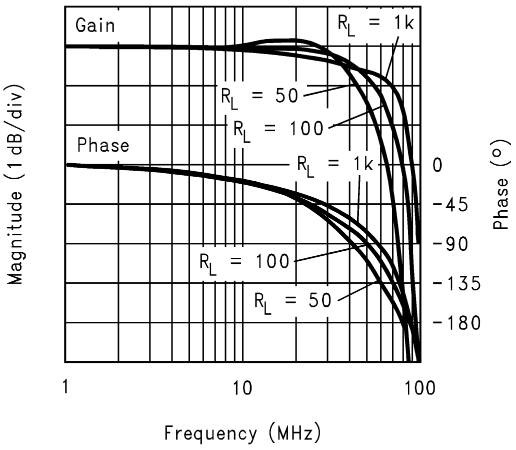
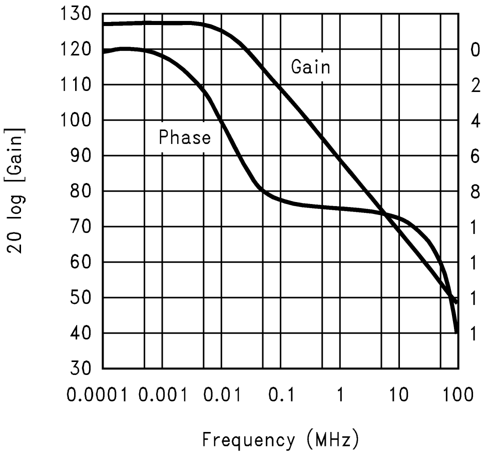
Frequency Response vs. Load



DS012711-8

Open-Loop Transimpedance Gain, Z(s)



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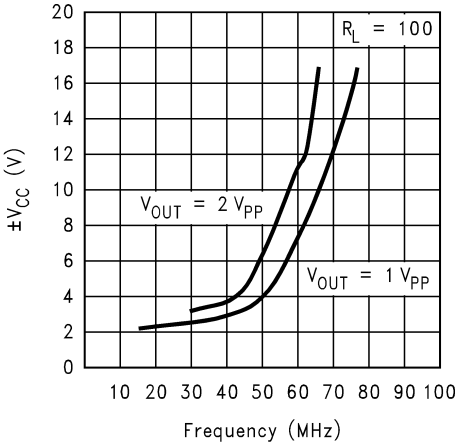
−3dB Bandwidth vs. V_{CC}



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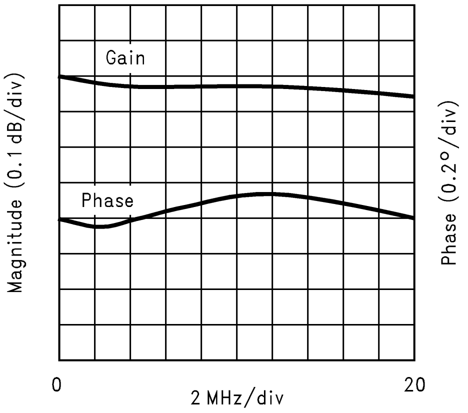
Gain Flatness and Linear Phase



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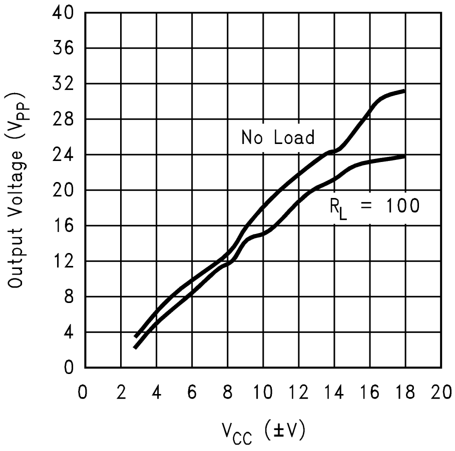
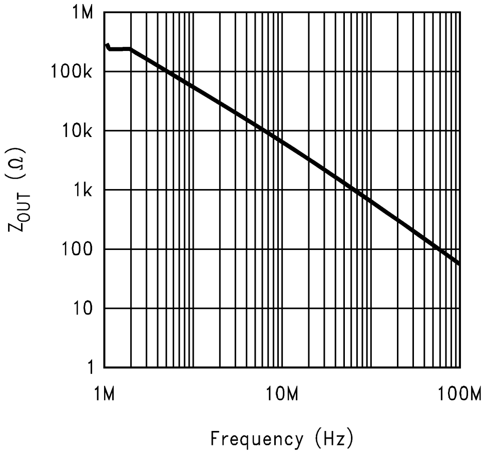
Typical Performance Characteristics (V_{CC} = ±15V, A_V = +2V/V, R_f = 640Ω, R_L = 100Ω; Unless Specified)) (Continued)

Maximum Output Voltage vs. V_{CC}



DS012711-12

Output Impedance, Disable Mode



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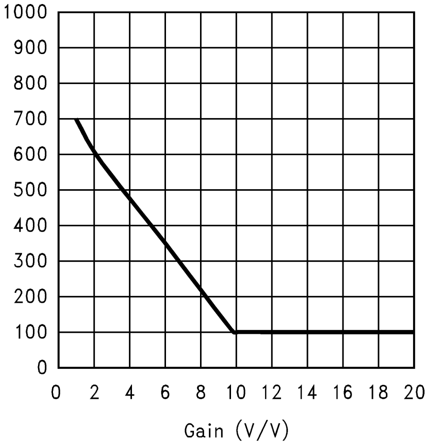
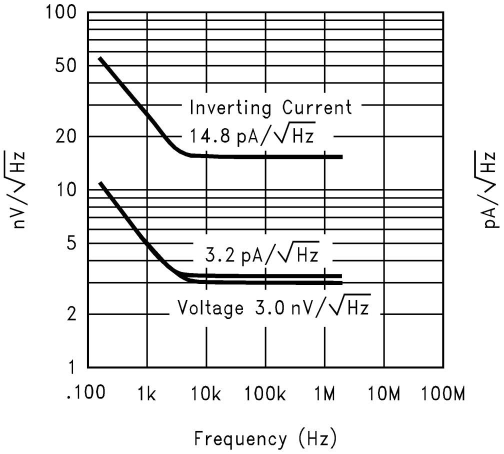
Recommended R_f vs. Gain



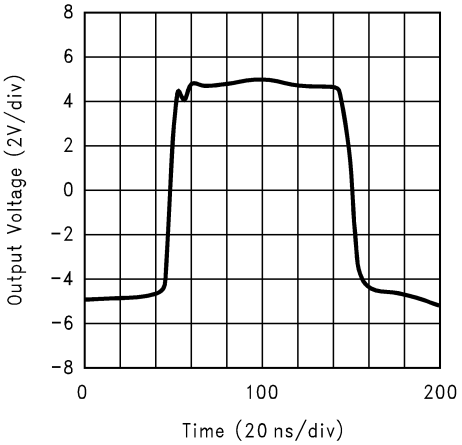
DS012711-14

Equivalent Input Noise



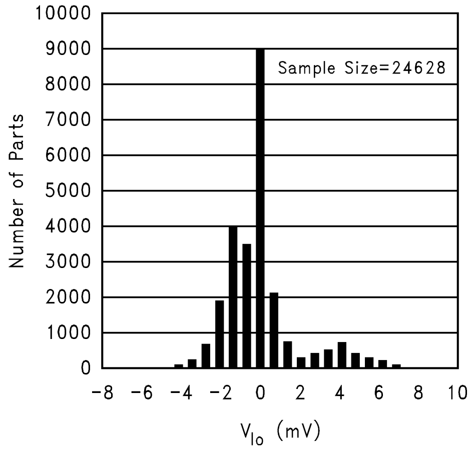
DS012711-15

Large Signal Pulse Response



DS012711-16

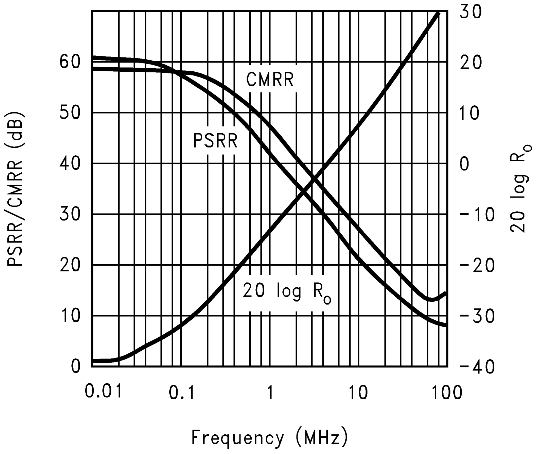
Histogram of Input Offset Voltage



DS012711-17

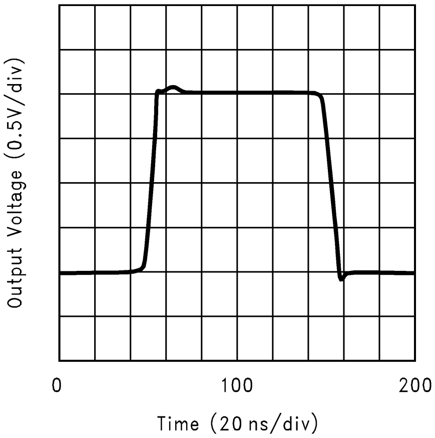
Typical Performance Characteristics (V_{CC} = ±15V, A_V = +2V/V, R_f = 640Ω, R_L = 100Ω; Unless Specified)) (Continued)

PSRR, CMRR and Closed Loop R_O



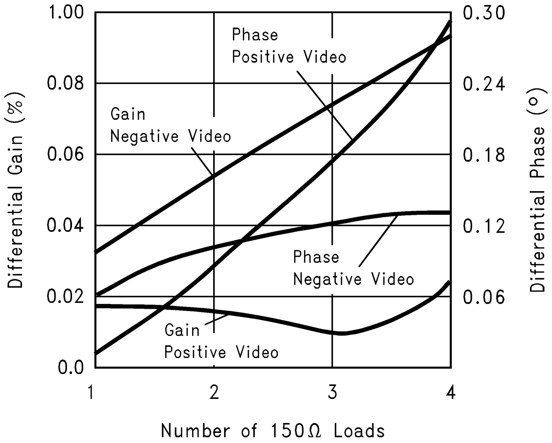
DS012711-18

Small Signal Pulse Response



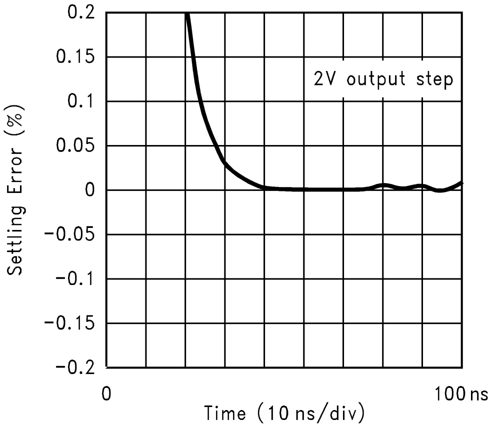
DS012711-19

Differential Gain and Phase (3.58MHz)



DS012711-20

Short Term Settling Time



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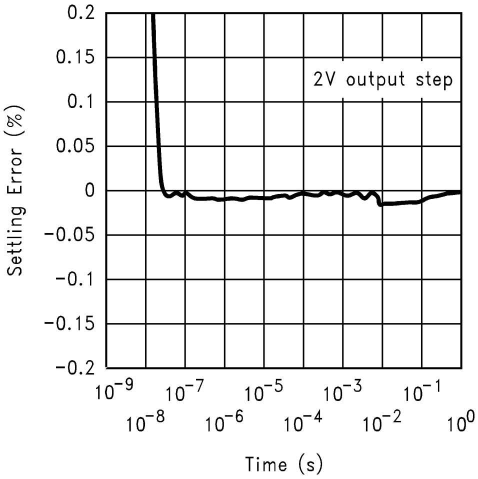
Long Term Settling Time



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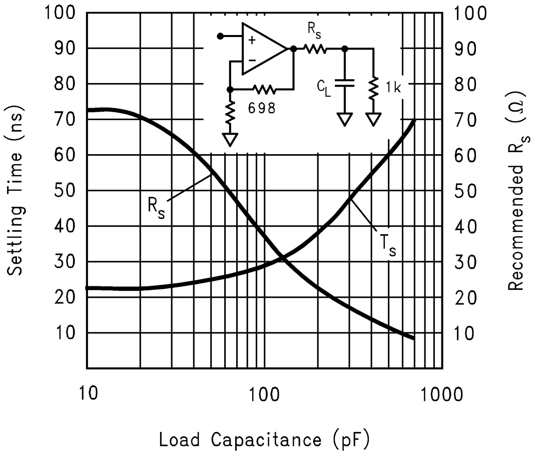
Settling Time vs. Capacitive Load



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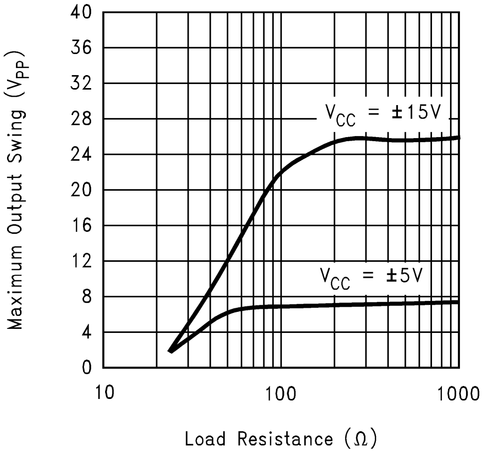
Typical Performance Characteristics (V_{CC} = ±15V, A_V = +2V/V, R_f = 640Ω, R_L = 100Ω; Unless Specified)) (Continued)

Output Voltage Swing vs. Load Resistance



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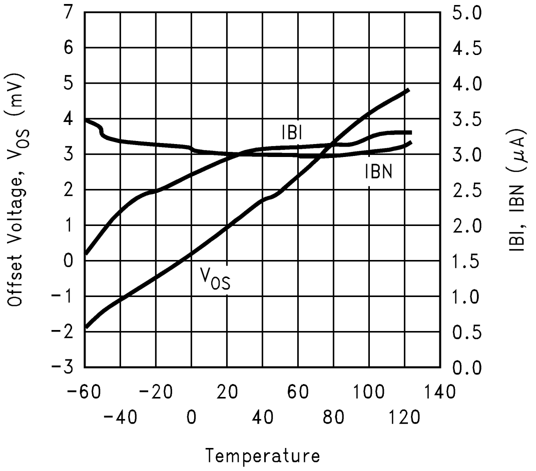
Typical IBI, IBN, VOS vs. Temperature



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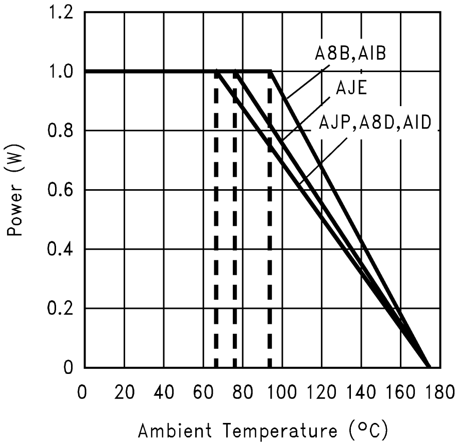
Power Derating Curves



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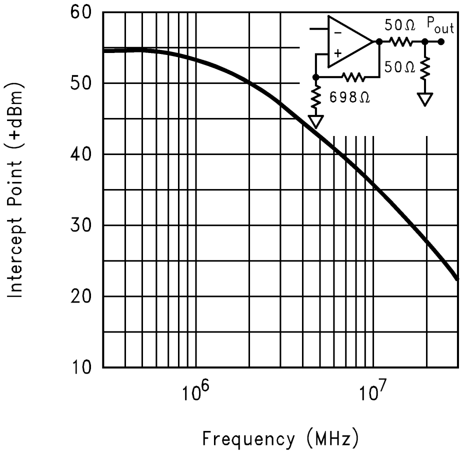
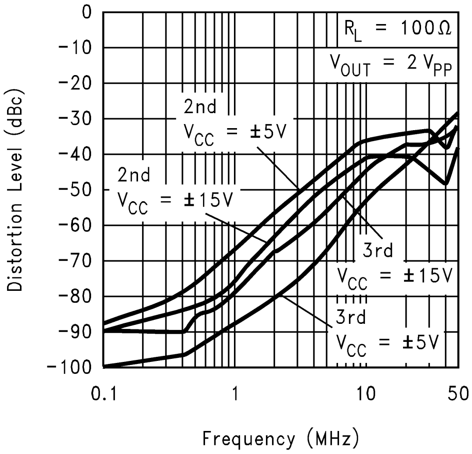
2-Tone, 3rd Order Intermodulation Intercept



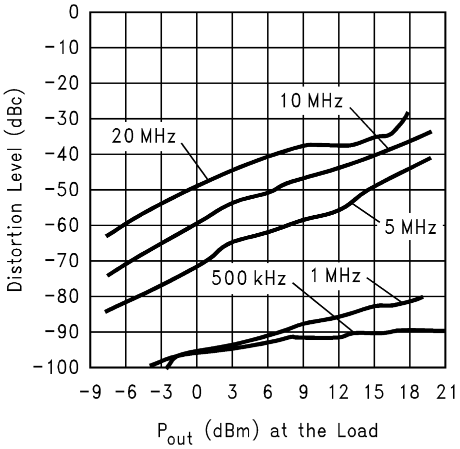
DS012711-27

Harmonic Distortion vs. Frequency



DS012711-28

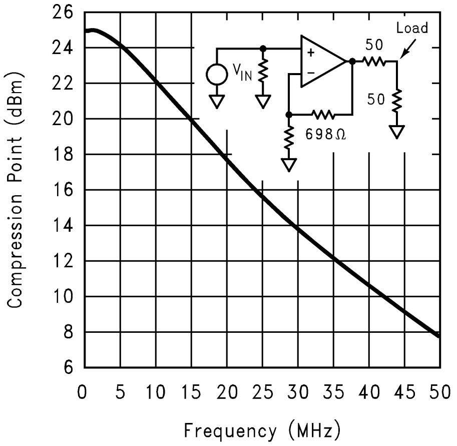
3rd Harmonic Distortion vs. P_{OUT}



DS012711-29

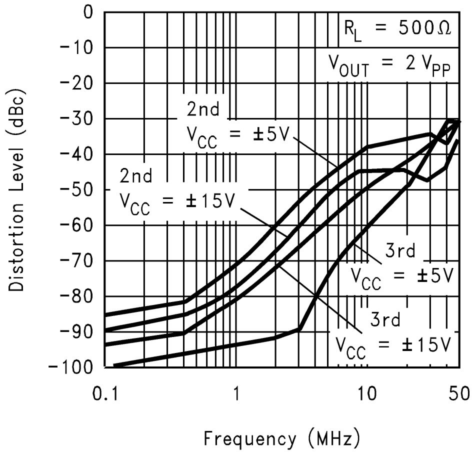
Typical Performance Characteristics (V_{CC} = ±15V, A_V = +2V/V, R_f = 640Ω, R_L = 100Ω; Unless Specified)) (Continued)

−1dB Compression to Load



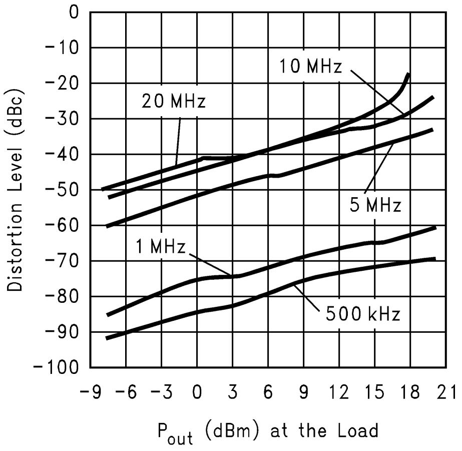
DS012711-30

Harmonic Distortion vs. Frequency



DS012711-31

2nd Harmonic Distortion vs. P_{OUT}



DS012711-32

Application Division

General Design Considerations

The CLC430 is a general purpose current-feedback amplifier for use in a variety of small and large signal applications. Use the feedback resistor to fine tune the gain flatness and −3dB bandwidth for any gain setting. National provides information for the performance at a gain of +2 for small and large signal bandwidths. The plots show feedback resistor values for selected gains.

Gain

Use the following equations to set the CLC430's non-inverting or inverting gain:

$$\text{Non-Inverting Gain} = 1 + \frac{R_f}{R_g}$$

$$\text{Inverting Gain} = -\frac{R_f}{R_g}$$

Choose the resistor values for non-inverting or inverting gain by the following steps.

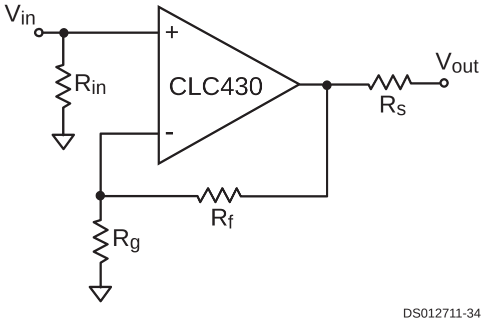


FIGURE 1. Component Identification

1) Select the recommended feedback resistor R_f (refer to plot in the plot section entitled R_f vs. Gain).

2) Choose the value of R_g to set gain.

3) Select R_s to set the circuit output impedance.

4) Select R_{in} for input impedance and input bias.

High Gains

Current feedback closed-loop bandwidth is independent of gain-bandwidth-product for small gain changes. For larger gain changes the optimum feedback resister R_f is derived by the following:

$$R_f = 724\Omega - 60\Omega \times (A_V).$$

As gain is increased, the feedback resistor allows bandwidth to be held constant over a wide gain range. For a more complete explanation refer to application note OA-25 Stability Analysis of Current-Feedback Amplifiers.

Resistors have varying parasitics that affect circuit performance in high speed design. For best results, use leaded metal-film resistors or surface mount resistors. A SPICE model for the CLC430 is available to simulate overall circuit performance.

Enable/Disable Function

The CLC430 amplifier features an enable/disable function that changes the output and inverting input from low to high impedance. The pin 8 enable/disable logic levels are as follows:

V_{CC}	±15V	±5V
Enable	>12.7V	>2.7V
Disable	<10.0V	<0.08

The amplifier is enabled with pin 8 left open due to the 2kΩ pull-up resistor, shown in *Figure 2*.

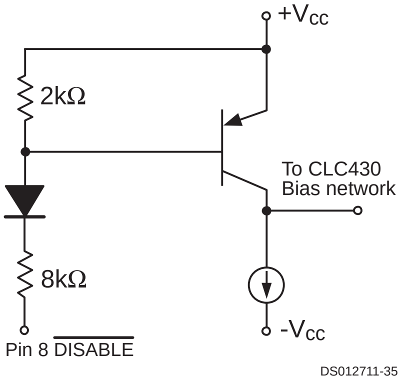


FIGURE 2. Pin 8 Equivalent Disable Circuit

Open-collector or CMOS interfaces are recommended to drive pin 8. The turn on and off time depends on the speed of the digital interface.

The equivalent output impedance when disabled is shown in *Figure 3*. With R_g connected to ground, the sum of R_f and R_g dominates and reduces the disabled output impedance. To raise the output impedance in the disabled state, connect the CLC430 as a unity-gain voltage follower by removing R_g. Current-feedback op-amps need the recommended R_f in a unity-gain follower circuit. For high density circuit layouts consider using the dual CLC431 (with disable) or the dual CLC432 (without disable).

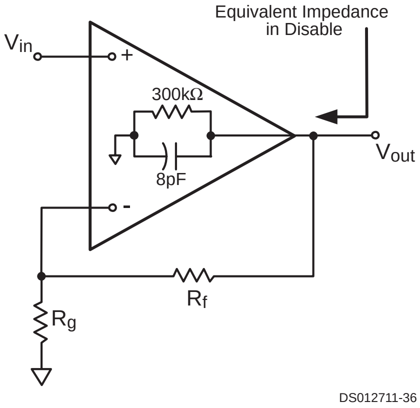


FIGURE 3. Equivalent Disabled Output Impedance

2nd and 3rd Harmonic Distortion

To meet low distortion requirements, recognize the effect of the feedback resistor. Increasing the feedback resistor will decrease the loop gain and increase distortion. Decreasing the load impedance increases 3rd harmonic distortion more than 2nd.

Application Division (Continued)

Differential Gain and Differential Phase

The CLC430 has low DG and DP errors for video applications. Add an external pulldown resistor to the CLC430's output to improve DG and DP as seen in *Figure 4*. A 604Ω R_P will improve DG and DP to 0.01% and 0.02˚.

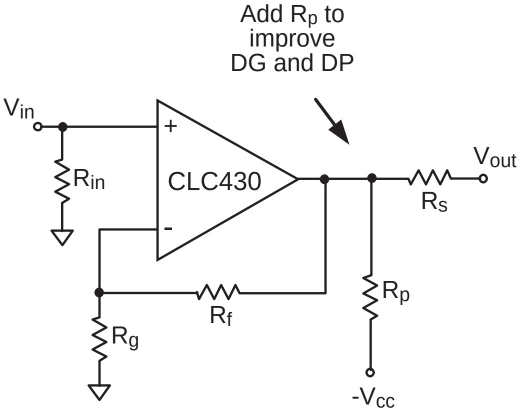


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FIGURE 4. Improved DG and DP Video Amplifier

Printed Circuit Layout

To get the best amplifier performance careful placement of the amplifier, components and printed circuit traces must be observed. Place the 0.1µF ceramic decoupling capacitors less than 0.1″ (3mm) from the power supply pins. Place the 6.8µF tantalum capacitors less than 0.75″ (20mm) from the power supply pins. Shorten traces between the inverting pin and components to less than 0.25″ (6mm). Clear ground plane 0.1″ (3mm) away from pads and traces that connect to the inverting, non-inverting and output pins. Do not place ground or power plane beneath the op-amp package. National provides literature and evaluation boards 730013 DIP or 730027 SOIC illustrating the recommended op-amp layout.

Applications Circuits

Level Shifting

The circuit shown in *Figure 5* implements level shifting by AC coupling the input signal and summing a DC voltage. The resistor R_{in} and the capacitor C set the high-pass break frequency. The amplifier closed-loop bandwidth is fixed by the selection of R_f. The DC and AC gains for circuit of *Figure 5* are different. The AC gain is set by the ratio of R_f and R_g. And the DC gain is set by the parallel combination of R_g and R_2.

$$V_{out} = V_{in_{ac}}\left(1+\left(\frac{R_f}{R_g \| R_2}\right)\right) - V_{in_{DC}}\left(\frac{R_f}{R_2}\right)$$

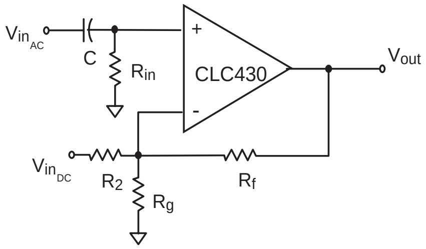

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FIGURE 5. Level Shifting Circuit

Multiplexing

Multiple signal switching is easily handled with the disable function of the CLC430. Board trace capacitance at the output pin will affect the frequency response and switching transients. To lessen the effects of output capacitance place a resistor (R_o) within the feedback loop to isolate the outputs as shown in *Figure 6*. To match the mux output impedance to a transmission line, add a resistor (R_s) in series with the output.

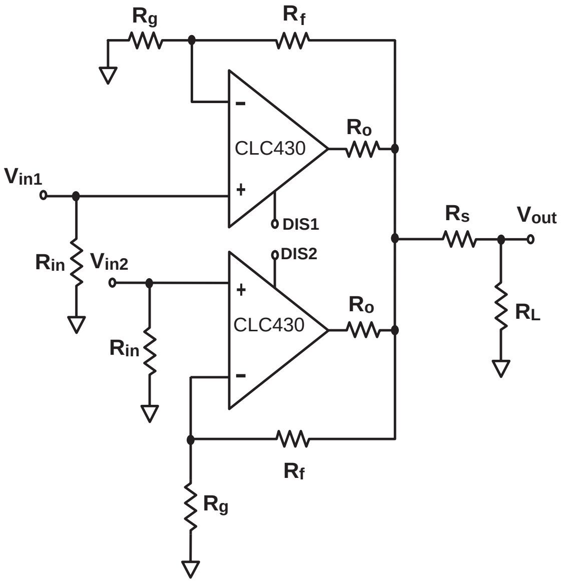

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FIGURE 6. Output Connection

Application Division (Continued)

Automatic Gain Control

Current-feedback amplifiers can implement very fast automatic-gain control circuits. The circuit shown in *Figure 7* shows an AGC circuit using the CLC430, a half-wave rectifier, an integrator and a FET. The CLC430 current-feedback amplifier maintains constant bandwidth and linear phase over AGC's gain range. This circuit effectively controls the output level for continuous signals.

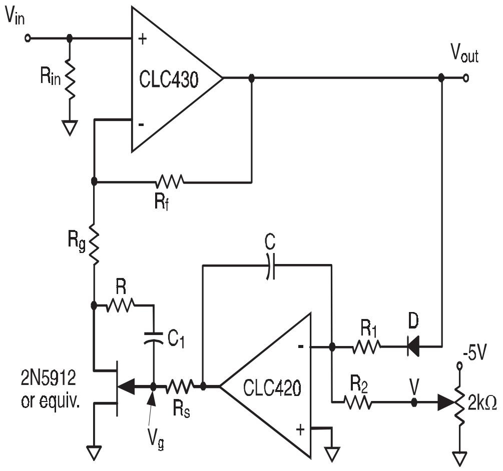

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FIGURE 7. AGC Circuit

The bandwidth of CLC430 AGC is limited by R_f, the feedback resistor. The FET gate voltage is limited to a range of:

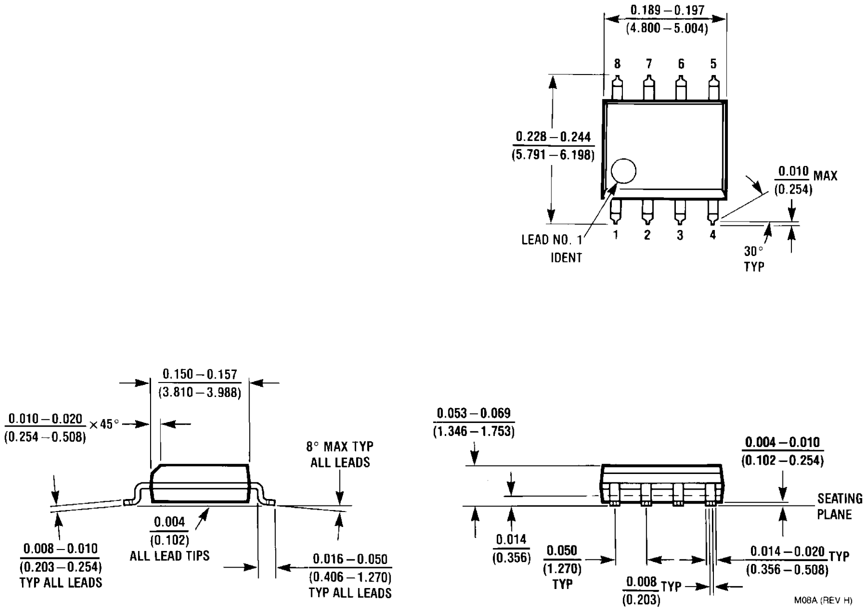
$$-2.5 < V_g < -1$$

R of 750Ω and C1 of 1.0µF gives a useful R_{ds} range of approximately 150 to 2kΩ. Scaling the integrator gain or adding attenuation before the diode D accommodates large signal swings. Determine the overall gain by:

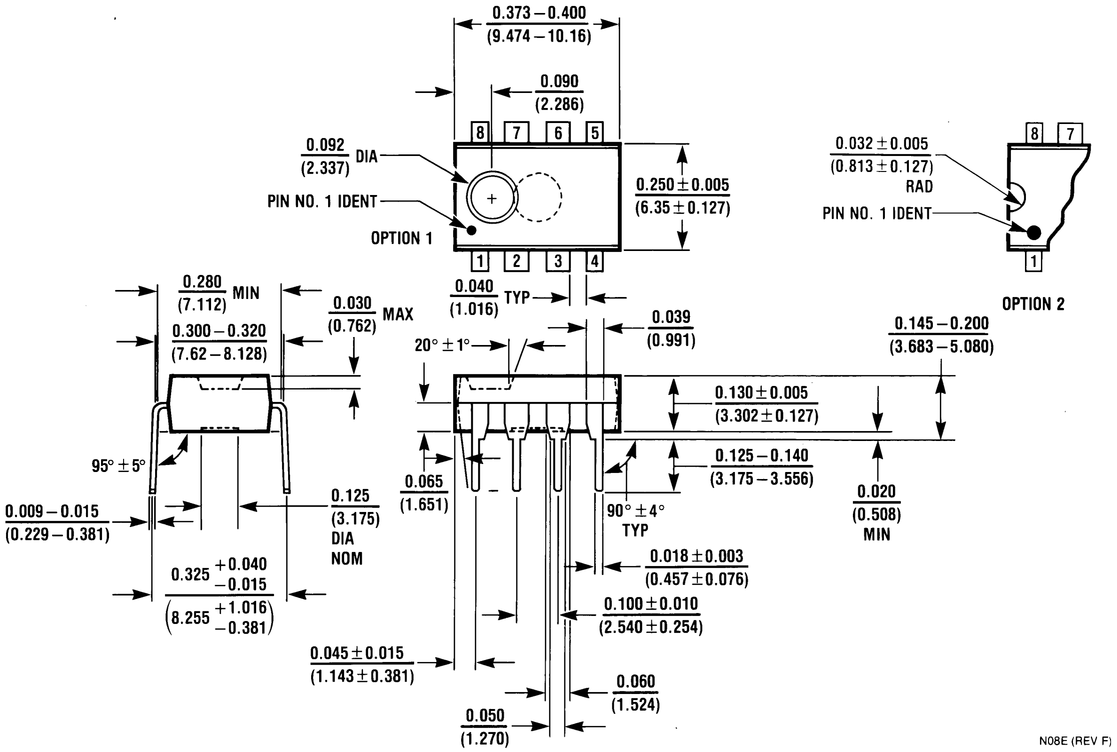
$$1+\frac{R_f}{R_g+R_{ds}}$$

The integrator sets the loop time constant.

Physical Dimensions inches (millimeters) unless otherwise noted


0.189 – 0.197
(4.800 – 5.004)
8 7 6 5
0.228 – 0.244
(5.791 – 6.198)
0.010 MAX
(0.254)
LEAD NO. 1
IDENT
1 2 3 4
30°
TYP
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020 × 45°
(0.254 – 0.508)
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.008 TYP
(0.203)
0.014 – 0.020 TYP
(0.356 – 0.508)
M08A (REV H)

8-Pin SOIC
NS Package Number M08A


0.373 – 0.400
(9.474 – 10.16)
0.090
(2.286)
8 7 6 5
0.092
(2.337) DIA
PIN NO. 1 IDENT
OPTION 1
0.250 ± 0.005
(6.35 ± 0.127)
1 2 3 4
0.032 ± 0.005
(0.813 ± 0.127)
RAD
PIN NO. 1 IDENT
8 7
1
OPTION 2
0.280
(7.112) MIN
0.300 – 0.320
(7.62 – 8.128)
0.030
(0.762) MAX
0.040
(1.016) TYP
0.039
(0.991)
20° ± 1°
0.145 – 0.200
(3.683 – 5.080)
0.130 ± 0.005
(3.302 ± 0.127)
95° ± 5°
0.065
(1.651)
0.125 – 0.140
(3.175 – 3.556)
0.020
(0.508)
MIN
90° ± 4°
TYP
0.009 – 0.015
(0.229 – 0.381)
0.125
(3.175)
DIA
NOM
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
0.045 ± 0.015
(1.143 ± 0.381)
0.060
(1.524)
0.050
(1.270)
N08E (REV F)

8-Pin MDIP
NS Product Number N08E

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