SHIBO CHEN

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EDUCATION

University of Michigan – Ann Arbor

Doctor of Philosophy in Engineering — Sept. 2019 to present

Bachelor of Science with High Distinction — Sept. 2016 to May. 2019

Major: Computer Science ***GPA:*** 3.92

M. Gallagher, L. Biernacki, **S. Chen**, Z. Aweke, S. Yitbarek, M. Aga, A. Harris, Z. Xu, B. Kasikci, V. Bertacco, S. Malik, M. Tiwari, T. Austin. "Morpheus: A Vulnerability-Tolerant Secure Architecture Based on Ensembles of Moving Target Defenses with Churn". Accepted for 24th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '19).

J. Erickson, **S. Chen**, M. Savich, S. Hu, M. Mao. "CommPact: Evaluating the Feasibility of Autonomous Vehicle Contracts". In Proceedings of IEEE Vehicular Networking Conference 2018 (VNC 18').

RESEARCH EXPERIENCE

Morpheus: A Vulnerability-Tolerant Secure Architecture Based on Ensembles of Moving Target Defenses with Churn — May 2018 to Jan.2019

University of Michigan – Ann Arbor

- Evaluated the robustness of a multi-layer moving target defense architecture.
- Implemented GCC support to tag memory during compile time.
- Implementing FPGA prototype to evaluate the defense on real hardware.

CommPact: A Feasibility Study for Platoon Contracts — Sept. 2017 to May 2018

University of Michigan – Ann Arbor

- Designed secure platoon joining and emergency termination protocol.
- Implemented communication functionality based on Dedicated Short Distance Communication Protocol.
- Worked on SGX Enclave Programming and traffic-network simulation.

PowerSpy Upgraded: Location Tracking using Mobile Device Power Analysis — Jan. 2018 to April 2018

University of Michigan - Ann Arbor

- Added support under wifi and mixed network conditions.
- Evaluated the feasibility of attacks with time-independent machine learning algorithm.
- Assessed different factors that are responsible for the attack.

PROJECTS

Alpha64 Out-of-Order Superscalar Processor Design — Sept. 2018 to Dec. 2018

University of Michigan – Ann Arbor

- Took charge of instruction fetch stage design, including but not limited to a 3-way instruction cache, tournament BTB, instruction fetch buffer and return address stack.
- Implemented Reorder Buffer based on a 3-way R10K architecture.
- Realized early branch resolution.

AWARDS

University Honors — 2017, 2018, 2019

James B. Angell Scholor — Mar. 2018

EECS Scholar — Mar. 2019