### UNIVERSITY OF TRIESTE

### Department of Engineering and Architecture



Bachelor's degree in Computer Engineering

Restoration and development of a Java-based LEGv8 ISA simulator

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# Summary

In this thesis I will be reporting my work done developing upon a Java-based LEGv8 ISA simulator.

In the Introduction I will provide a brief overview of the LEGv8 ISA together with the reasons for choosing this thesis project in the context of the Digital Architectures course.

In Chapter 1 I will provide a short summary of the current landscape of software simulators available online for the LEGv8 ISA. I will end the chapter with a focus on the simulator chosen for this thesis' project, namely the LEGv8 simulator developed and distributed by Arm Holdings plc. I will give an overview of its working state, functionality and structure prior to my development efforts.

In Chapter 2 I will present the work done to decouple the project from the Eclipse IDE and migrate it to a modern build automation system, namely Mayen.

In the Chapter 3 I will showcase the bugs that have been fixed and I will introduce all of the functionalities that have been added to the simulator and the structural changes by them entailed.

In Chapter 4 I will talk about the shortcomings of the simulator and the work that can be done to further improve it.

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# Introduction

"Simplicity is a great virtue but it requires hard work to achieve it and education to appreciate it. And to make matters worse: complexity sells better."

Edsger W. Dijkstra

### What is an ISA?

A computer is a device which is capable of acquiring data, performing calculations upon it, and making the results available for use at a later date. It is clear from this definition, that when deciding how to design and build a computer one must at least take into consideration the way data is stored and organized (the memory) and the mechanisms through which the computer is able to manipulate said data (the processor). Computers are an abstract concept and do not impose a certain technological choice to their physical realization. Nonetheless, the vast majority of computers nowadays are built through the assembly of digital components and thus natively speak the language of the binary number system. As such, just like when using a mechanical device an operator needs to interact with the physical parts of the system, operating a computer at this level would require the user to manually insert ones and zeros into the right places for it to perform its calculations. It is clear that such an operation would require an intimate knowledge of the physical implementation of the computer, and even minimal changes to its digital circuitry might jeopardize the correctness of any sequences of bits written for an earlier model.

Early on in the history of computers it was understood that an additional layer of abstraction was needed in order to separate the hardware from the software and give more freedom both to the circuit designers and the programmers. This layer of abstraction is called an Instruction Set Architecture, which from now on will be called ISA for short. An ISA provides a logical specification of how a computer manages its memory and what the instruc-

tions that it's capable of performing are. This forms the layer through which all software must interface with in order to interact with the hardware.

### What is the LEGv8 ISA?

The ISA focus of this thesis is the LEGv8 ISA, an ARM-inspired architecture created by David A. Patterson and John L. Hennessy to serve as a teaching tool in their book Computer Organization and Design (ARM Edition). As the title suggests, the book is actually about the ARMv8 ISA, whose first iteration was originally released in 1983 by Acorn Computers and which is now developed by Arm Holdings plc. The authors, however, introduced a few changes and simplifications to the ARMv8 ISA to make it friendlier to students and emphasize certain design concepts. As such, this ISA is used in the sections of the book dedicated to the design of a model processor and its programming, and its these sections upon which the LEGv8 simulator subject of this thesis is based.

### Overview of the LEGv8 ISA

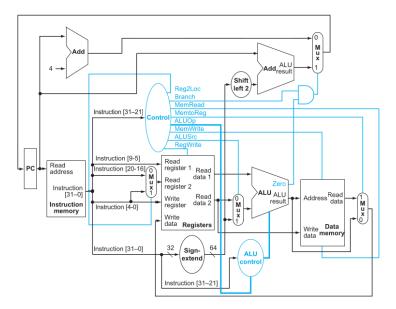


Figure 1: The logical scheme of the LEGv8 architecture

### Architecture type

LEGv8 follows the Von Neumann architecture paradigm and thus contemplates the existence of a single memory containing both the instructions and

the program data. It is a 64-bit architecture and is specifically designed for pipelined execution.

### Registers

LEGv8 defines 32 64-bit X registers for storing integer values and 32 64-bit D registers for storing double precision floating point values. There are also 32 32-bit S registers dedicated to single precision floating point values, albeit being purely logical and simply occupying the lower 32 bits of the D registers. Unlike ARMv8, the presence of 32-bit W integer registers is not contemplated.

### Memory

The memory contains both the program code and the data. It is logically divided into a reserved segment, a text segment containing the program code, a static data segment containing the constants defined at compile time, and a dynamic data and stack segments occupying the same location of memory and respectively growing upwards from the static data segment and downwards from the stack pointer. This section of the memory is the one containing the data defined at execution time.

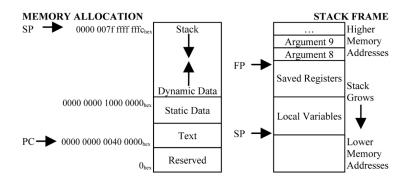


Figure 2: Logical division of the memory

#### Control unit

The control unit is the component responsible for coordinating the pipeline execution flow and configuring the various components to perform the desired operations in the correct order using the correct parameters.

### $\mathbf{ALU}$

The LEGv8 ALU is capable of performing 64-bit integer operations and both single and double precision floating point operations. The operation to

perform at any given moment is configured through an ALUop code provided by the control unit.

#### Pipeline

The LEGv8 pipeline is comprised of 5 stages: fetch, decode, execute, data access, and write back. As the names suggest, the fetch stage is responsible for acquiring instructions from the text segment of the memory, the decode stage decodes the instructions, reads the registers involved in the operation, and configures the control unit accordingly, the execute stage performs the calculation through the ALU, the data access stage is responsible for accessing the memory, and the write back stage finally writes the result into the registers. Of course not all instructions make use of all the pipeline stages and this is taken into consideration when optimizing the execution flow.



Figure 3: The 5 pipeline stages

#### Instructions

LEGv8 can be considered a subset of ARMv8, but with a few caveats. Many higher level instructions have been omitted altogether in order to keep the ISA as minimal as possible, and many of the ones that have been kept have been revisited to make them clearer in their scope. For example, in ARMv8 the ADD instruction can be used with both 32 and 64 bit integer registers, and both with register-based and immediate-based values. This of course allows the ARMv8 programmer to remember a single mnemonic and use it in all sorts of operations, but it obscures some important underlying design differences that might be valuable to computer architecture students. In LEGv8 instead, it has been decided to split the ADD instruction into ADD and ADDI or register and immediate values usage respectively. Similarly, in ARMv8 the FADD instruction is capable of performing additions both in the case of single and double precision registers, whereas in LEGv8 the instruction has been split into FADDS and FADDD for performing the operation only on single precision or double precision registers respectively.

Instruction		Opcode Shamt		11-bit Opcode Range (1)		Instruction			code	Shamt	11-bit ( Rang	ge (1)	
Mnemonic	Format	Width (bits)	Binary	Binary	Start (Hex)		Mnemonic	Format			Binary	Start (Hex) End (He	
В	В	6	000101		0A0	0BF	ADDS	R	- 11	10101011000			
FMULS	R	- 11	00011110001	000010	OF		ADDIS	I	10	1011000100		588	589
FDIVS	R	- 11	00011110001	000110	0F	1	ORRI	I	10	1011001000		590	591
FCMPS	R	11	00011110001	001000	OF		CBZ	CB	- 8	10110100		5A0	5A7
FADDS	R	- 11	00011110001	001010	0F		CBNZ	CB	8	10110101		5A8	5AF
FSUBS	R	11	00011110001	001110	0F	1	STURW	D	- 11	10111000000		50	20
FMULD	R	11	00011110011	000010	0F	3	LDURSW	D	11	10111000100		50	24
FDIVD	R	11	00011110011	000110	0F	3	STURS	R	11	101111100000		51	30
FCMPD	R	11	00011110011	001000	0F	3	LDURS	R	11	101111100010		51	32
FADDD	R	- 11	00011110011	001010	0F	3	STXR	D	11	11001000000		64	10
FSUBD	R	11	00011110011	001110	OF	3	LDXR	D	- 11	11001000010		64	12
STURB	D	11	00111000000		10	0	EOR	R	11	11001010000		6:	50
LDURB	D	- 11	00111000010		10	2	SUB	R	- 11	11001011000		6:	58
B.cond	CB	8	01010100		2A0	2A7	SUBI	I	10	1101000100		688	689
STURH	D	- 11	01111000000		30	0	EORI	I	10	1101001000		690	691
LDURH	D	11	01111000010		30	2	MOVZ	IM	9	110100101		694	697
AND	R	11	10001010000		45	0	LSR	R	11	11010011010		65	A
ADD	R	11	10001011000		45	8	LSL	R	- 11	11010011011		69	B
ADDI	I	10	1001000100		488	489	BR	R	11	11010110000		6H	30
ANDI	I	10	1001001000		490	491	ANDS	R	11	11101010000		7:	50
BL	В	6	100101		4A0	4BF	SUBS	R	11	11101011000		75	58
SDIV	R	11	10011010110	000010	40	)6	SUBIS	I	10	1111000100		788	789
UDIV	R	11	10011010110	000011	40	16	ANDIS	I	10	1111001000		790	791
MUL	R	11	10011011000	011111	40		MOVK	IM	9	111100101		794	797
SMULH	R	11	10011011010		4D	A	STUR	D	11	11111000000		70	20
UMULH	R	11	10011011110		4D		LDUR	D	11	11111000010		70	
ORR	R	11	101010101000		55		STURD	R	11	111111100000		71	
Parties .			10101010000				LDURD	R	11	111111100010		71	

Figure 4: The complete LEGv8 ISA

All the instructions are encoded with the same length of 32 bits in order to fetch and decode them more efficiently. They are also grouped into 5 instruction formats to give a more homogeneous encoding to operations performing similar steps and increase their decoding speed. The *R*-type instructions perform operations solely on registers, the *I*-type instructions make use of immediate values (defined in the code itself), the *D*-type instructions access the memory, the *B*-type and *CB* perform unconditional and conditional branching respectively, and the *IW*-type instructions to perform MOV instructions with wider immediate values.

CORE INSTRUCTION FORMATS											
R	opcode		Rm	shamt	Rn		Rd				
	31	21	20 16	15	10	9	5 4		0		
I	opcode		ALU_in	nmediate		Rn		Rd			
	31	22 21			10	9	5 4		0		
D	opcode		DT_ad	dress	op	Rn		Rt			
	31	21	20	12	11 10	9	5 4		0		
В	opcode			BR_ad	dress						
	31 20	6 25							0		
CB	Opcode		COND	_BR_addre	SS			Rt			
	31 24	4 23					5 4		0		
$\mathbf{IW}$	opcode			MOV_imn	nediat	te		Rd			
	31	21	20				5 4		0		

Figure 5: The 5 formates of LEGv8 instructions with their encoding pattern

### Motivations for choosing LEGv8

The LEGv8 ISA, being presented and defined in one of the major computer architecture undergraduate textbooks, is taught in many university courses around the world, including the Digital Systems Architecture course held by Prof. Carini at UniTS. In spite of its popularity, no real hardware has

### INTRODUCTION

been made to run its instruction set natively, and the simulator landscape is almost equally lacking in viable options. This in turn makes it impossible for educators and students alike to show working examples of LEGv8 code, depriving them of teaching and learning opportunities. For these reasons I have chosen to work on an already existing and partially working LEGv8 simulator provided by Arm Holdings plc. to expand upon its functionalities to include a complete simulation of the ISA.

# Chapter 1

"If 10 years from now, when you are doing something quick and dirty, you suddenly visualize that I am looking over your shoulders and say to yourself: 'Dijkstra would not have liked this', well that would be enough immortality for me."

Edsger W. Dijkstra

### The LEGv8 simulators landscape

The current landscape of publicly available LEGv8 simulators can be divided into two categories: simulators that aim to reproduce the logical design presented in the textbook in chapter?, and the simulators providing a high level simulation of the instruction set as defined in the book. The survey was performed on GitHub using "LEGv8" and "simulator" as keywords and only those in a reasonably working state (as per the author) have been considered.

#### Software simulators

Repository	Language	Integer Support	Pipelined	Registers view	Stack view	Floating Point Support
https://github.com/lcpckp/leg-cpu-sim	Java	Partial	No	Yes	Yes	No
https://github.com/chrwoods/legv8-emul	C/C++	Partial	Yes	Yes	Yes	No
https://github.com/mtalyat/LEGv8Day	C#	Partial	No	Yes	Yes	No
https://github.com/eaxworthy/LegV8Interpreter	Python	Partial	No	Yes	Yes	No
https://github.com/AdinAck/LEGv8-Simulator	Swift	Partial	No	Yes	Yes	No
https://github.com/anvitha305/legv8sim	Python	Partial	No	Yes	Yes	Double precision only
https://github.com/dangbandy/LegV8-Simulator	C++	Partial	No	Yes	Yes	No
https://github.com/schang412/LEGv8-PyEmu	Python	Partial	No	No	No	No
https://github.com/GeorgePerreault/LEGV8_Interpreter	Python	Partial	No	Yes	Yes	No

Table 1.1: The surveyed software simulators

They utilize high level languages such as C++, Python, Swift, TypeScript and Java. Some of them offer a graphical interface, pipelined execution and

none of the implement the LEGv8 ISA in its entirety.

#### Hardware simulators

Repository	Language	Integer Support	Pipelined	Floating Point Support
https://github.com/nxbyte/ARM-LEGv8	Verilog	Partial	Yes	No
https://github.com/phillbush/legv8	Verilog	Partial	Yes	No
https://github.com/ronitrex/ARMLEG	Verilog	Partial	Yes	No
https://github.com/mattco98/LEGv8-Processor	Verilog	Partial	Yes	Partial
https://github.com/amaurilopez90/LEGv8-CPU	Verilog	Partial	Yes	No
https://github.com/miguelangelo78/LEGv8-ISA	Verilog	Partial	Yes	No
https://github.com/brianworts/LEGv8_SingleCycle_Processor	Verilog	Partial	Yes	No
https://github.com/egflo/LEGv8	Verilog	Partial	Yes	No
https://github.com/ad153153/LegV8	Verilog	Partial	Yes	No

Table 1.2: The surveyed hardware simulators

They use mostly Verilog as their hardware description language and implement an incomplete subset of the LEGv8 ISA. Some of them follow closely the design of the textbook while others expand upon it adding more executable instructions. None of them offer a graphical interface nor implement the ISA in its entirety.

It is clear from this brief survey that the LEGv8 simulators space lacks any desirable candidates for code execution and inspection, as the software simulators are incomplete and platform-dependant, and the hardware ones lack interactivity and comprehensive visual output capabilities.

### ARM's LEGv8 simulator

This is the simulator officially provided by ARM Education and is the subject of this thesis' work. It is written in Java 8 and uses Google's GWT framework to transpile the code into native JavaScript to allow the simulator to be executed inside a web browser as a normal web application. It provides a comprehensive user interface displaying an interactive text editor (provided by AceGWT) to input LEGv8 code and to display errors, and a visualization of the state of the X registers. When selecting the single-cycle execution mode, a visualization of the logical scheme of the LEGv8 ISA is presented and for each step of the execution various components change color to indicate the current stage of the pipeline. For the pipelined execution mode, the visualization is slightly modified to include pipeline-specific information such as pipeline registers, the hazard detection unit and the forwarding unit. An additional textual representation of the pipeline is provided to see the stage occupied by each instruction at any given moment.

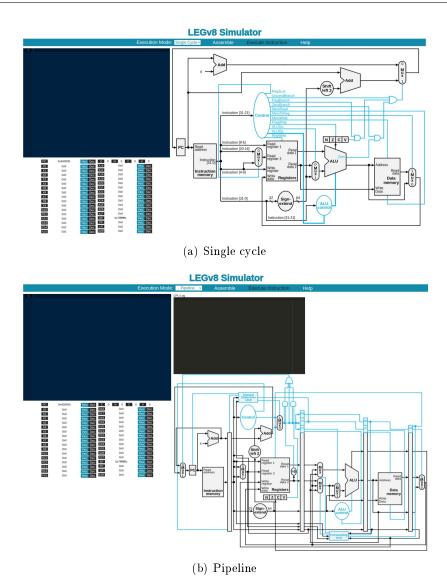


Figure 1.1: The simulator's main page with the two different execution modes

### **Features**

This simulator presents many favorable characteristics:

- Written in Java (platform agnostic, extensible)
- Compiled as a web application (platform agnostic and easily deployable)
- Embedded text editor to input code with and error display

- Clear and rich visualization of the X and flag registers and the datapath of the CPU
- Almost all of the integer arithmetic is already implemented
- All types of integer LOAD and STORE instructions are already implemented, including STXUR and LDXUR
- Officially distributed by ARM Education (biggest support and discoverability)

#### **Problems**

Unfortunately many problems present themselves when trying to run or develop the simulator:

- Absence of any documentation on how to build the project
- Executable version distributed in web page form
- Pipeline execution is incomplete
- The branch and link instruction writes the incorrect address into the LR register, making it impossible to write subroutines as they loop forever
- The integer comparisons do not work properly, making it impossible to perform any kind of loop or branch
- The project is heavily dependent on the Eclipse Java IDE with an old GWT plugin to perform the build process
- The project depends on the outdated and barely supported GWT library to deploy the simulator as a web application. This restricts the developers from using newer Java features or better web frameworks.

I present below a demonstration of the bugs regarding the branch and link instruction and the integer comparisons:

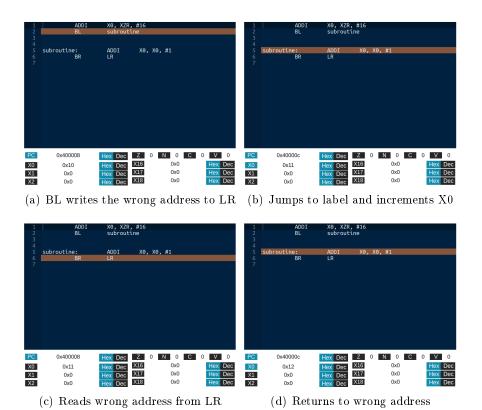


Figure 1.2: Branch returns to the wrong instruction, making it execute the branch in a loop

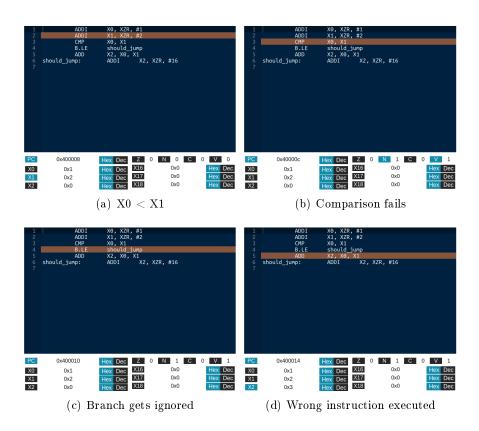


Figure 1.3: Comparisons do not set the correct flags and thus fail

### Motivations

For these reasons then this simulator was chosen as the subject of my thesis:

- Maximize the impact of my work by fixing and improving the most popular simulator available
- Provide the first complete implementation of the LEGv8 instruction set
- My pre-existing knowledge of Java and build automation systems would allow me to quickly get up to speed and extend the codebase efficiently
- Allow the Digital Systems Architecture course at UniTS and other courses in general to have a working LEGv8 simulator for more effective teaching

## Chapter 2

# Sit Amet

"Much of the excitement we get out of our work is that we don't really know what we are doing"

Edsger W. Dijkstra

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### CHAPTER 2. SIT AMET

vel, eleifend faucibus, vehicula eu, lacus.

## Chapter 3

# Lorem Ipsum

"Program testing can be used to show the presence of bugs, but never to show their absence!"

Edsger W. Dijkstra

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### 3.1 Dolor

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### CHAPTER 3. LOREM IPSUM

ultricies ut, mi. Duis nec dui quis leo sagittis commodo.

## Chapter 4

## Dolor

"If debugging is the process of removing software bugs, then programming must be the process of putting them in."

Edsger W. Dijkstra

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## Conclusions

"The purpose of abstracting is not to be vague, but to create a new semantic level in which one can be absolutely precise."

Edsger W. Dijkstra

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# Appendix A

# Sit Amet

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# Appendix B

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# Appendix C

# Lorem

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I thank my family for tolerating my long journey. I thank Beatrice G. for believing in me.