

UNIVERSITY OF TRIESTE

Department of Engineering and Architecture



Bachelor's degree in Computer Engineering

**Restoration and development of a
Java-based LEGv8 ISA simulator**

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Summary

In this thesis I will be reporting my work done developing upon a Java-based LEGv8 ISA simulator.

In the Introduction I will provide a brief overview of the LEGv8 ISA together with the reasons for choosing this thesis project in the context of the Digital Architectures course.

In Chapter 1 I will provide a short summary of the current landscape of software simulators available online for the LEGv8 ISA. I will end the chapter with a focus on the simulator chosen for this thesis' project, namely the LEGv8 simulator developed and distributed by Arm Holdings plc. I will give an overview of its working state, functionality and structure prior to my development efforts.

In Chapter 2 I will present the work done to decouple the project from the Eclipse IDE and migrate it to a modern build automation system, namely Maven.

In the Chapter 3 I will showcase the bugs that have been fixed and I will introduce all of the functionalities that have been added to the simulator and the structural changes by them entailed.

In Chapter 4 I will talk about the shortcomings of the simulator and the work that can be done to further improve it.

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Introduction

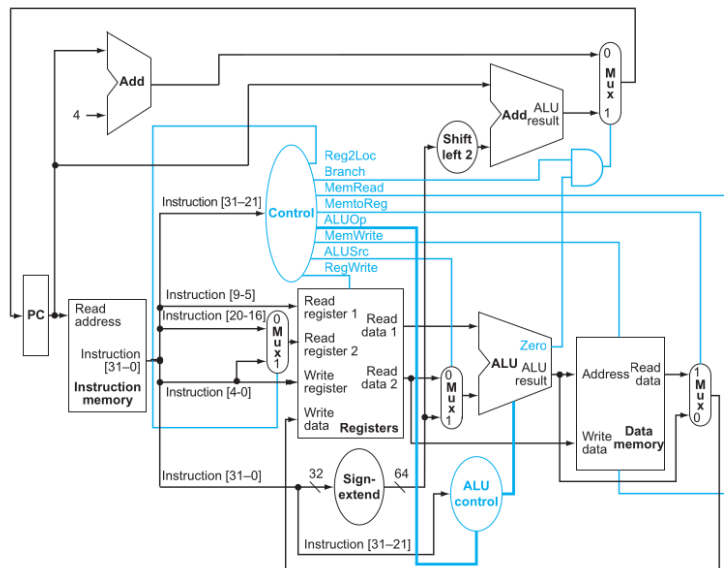
"Simplicity is a great virtue but it requires hard work to achieve it and education to appreciate it. And to make matters worse: complexity sells better."

Edsger W. Dijkstra

What is an ISA?

A computer is a device which is capable of acquiring data, performing calculations upon it, and making the results available for use at a later date. It is clear from this definition, that when deciding how to design and build a computer one must at least take into consideration the way data is stored and organized (the memory) and the mechanisms through which the computer is able to manipulate said data (the processor). Computers are an abstract concept and do not impose a certain technological choice to their physical realization. Nonetheless, the vast majority of computers nowadays are built through the assembly of digital components and thus natively speak the language of the binary number system. As such, just like when using a mechanical device an operator needs to interact with the physical parts of the system, operating a computer at this level would require the user to manually insert ones and zeros into the right places for it to perform its calculations. It is clear that such an operation would require an intimate knowledge of the physical implementation of the computer, and even minimal changes to its digital circuitry might jeopardize the correctness of any sequences of bits written for an earlier model.

Early on in the history of computers it was understood that an additional layer of abstraction was needed in order to separate the hardware from the software and give more freedom both to the circuit designers and the programmers. This layer of abstraction is called an Instruction Set Architecture, which from now on will be called ISA for short. An ISA provides a logical specification of how a computer manages its memory and what the instruc-



the program data. It is a 64-bit architecture and is specifically designed for pipelined execution.

Registers

LEGv8 defines 32 64-bit X registers for storing integer values and 32 64-bit D registers for storing double precision floating point values. There are also 32 32-bit S registers dedicated to single precision floating point values, albeit being purely logical and simply occupying the lower 32 bits of the D registers. Unlike ARMv8, the presence of 32-bit W integer registers is not contemplated.

Memory

The memory contains both the program code and the data. It is logically divided into a *reserved* segment, a *text* segment containing the program code, a *static data* segment containing the constants defined at compile time, and a *dynamic data* and *stack* segments occupying the same location of memory and respectively growing upwards from the *static data* segment and downwards from the stack pointer. This section of the memory is the one containing the data defined at execution time.

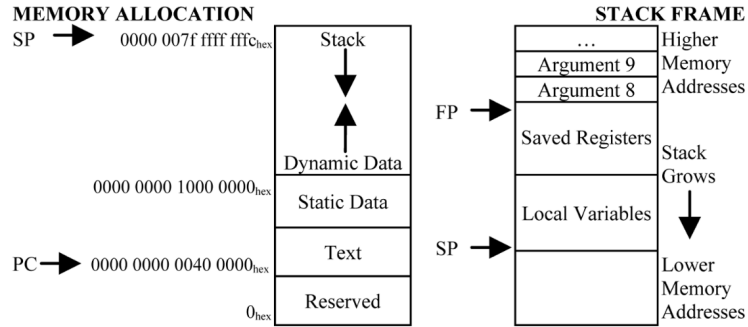


Figure 2: Logical division of the memory

Control unit

The control unit is the component responsible for coordinating the pipeline execution flow and configuring the various components to perform the desired operations in the correct order using the correct parameters.

ALU

The LEGv8 ALU is capable of performing 64-bit integer operations and both single and double precision floating point operations. The operation to

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perform at any given moment is configured through an ALUop code provided by the control unit.

Pipeline

The LEGv8 pipeline is comprised of 5 stages: *fetch*, *decode*, *execute*, *data access*, and *write back*. As the names suggest, the *fetch* stage is responsible for acquiring instructions from the text segment of the memory, the *decode* stage decodes the instructions, reads the registers involved in the operation, and configures the control unit accordingly, the *execute* stage performs the calculation through the ALU, the *data access* stage is responsible for accessing the the memory, and the *write back* stage finally writes the result into the registers. Of course not all instructions make use of all the pipeline stages and this is taken into consideration when optimizing the execution flow.



Figure 3: The 5 pipeline stages

Instructions

LEGv8 can be considered a subset of ARMv8, but with a few caveats. Many higher level instructions have been omitted altogether in order to keep the ISA as minimal as possible, and many of the ones that have been kept have been revisited to make them clearer in their scope. For example, in ARMv8 the *ADD* instruction can be used with both 32 and 64 bit integer registers, and both with register-based and immediate-based values. This of course allows the ARMv8 programmer to remember a single mnemonic and use it in all sorts of operations, but it obscures some important underlying design differences that might be valuable to computer architecture students. In LEGv8 instead, it has been decided to split the *ADD* instruction into *ADD* and *ADDI* or register and immediate values usage respectively. Similarly, in ARMv8 the *FADD* instruction is capable of performing additions both in the case of single and double precision registers, whereas in LEGv8 the instruction has been split into *FADDS* and *FADD* for performing the operation only on single precision or double precision registers respectively.

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Instruction Mnemonic	Format	Width (bits)	Opcode Binary	Shamt Binary	11-bit Opcode Range (1) Start (Hex) End (Hex)	Instruction Mnemonic	Format	Width (bits)	Opcode Binary	Shamt Binary	11-bit Opcode Range (1) Start (Hex) End (Hex)
B	B	6	000101		0A0 0BF	ADDI	R	11	10101011000		588 589
EMULS	R	11	00011110001	000010	0F1	ADDIS	I	10	1011000100		590 591
FDIVS	R	11	00011110001	000110	0F1	ORRI	I	10	1011001000		5A0 5A7
PCMPS	R	11	00011110001	001000	0F1	CBZ	CB	8	1011010100		5C0 5AF
PADDS	R	11	00011110001	001010	0F1	CBNE	CB	8	1011010101		5E0 5E1
FSUBS	R	11	00011110001	001110	0F1	STORW	D	11	101110000000		5E2 5E3
EMULD	R	11	00011110011	000010	0F3	LDORSW	D	11	101110000100		640 641
FDIVD	R	11	00011110011	000110	0F3	STURS	R	11	101111000000		642 643
PCMPD	R	11	00011110011	001000	0F3	LDORS	R	11	101111000100		650 651
PADD	R	11	00011110011	001010	0F3	STXR	D	11	110010000000		652 653
FSUBD	R	11	00011110011	001110	0F3	LDOR	D	11	110010000010		654 655
STORW	D	11	00111000000		1C0	ORR	R	11	110010100000		688 689
LDORW	D	11	00111000010		1C2	SRB	R	11	110010110000		690 691
BLCOND	CB	8	01010100		2A0 2A7	SBRT	I	10	1101000100		692 693
STURW	D	11	01111000000		3C0	EBRT	I	10	1101001000		694 695
LDORW	D	11	01111000010		3C2	MOVZ	IM	9	110100101		696 697
AND	R	11	10001010000		450	LSR	R	11	11010011010		698 699
ADD	R	11	10001011000		458	LSL	R	11	11010011011		700 701
ADDI	I	10	1001000100		488 489	BR	R	11	110101100000		702 703
ANDI	I	10	1001001000		490 491	ANDS	R	11	111010100000		704 705
BL	B	6	100101		4A0 4BF	SRBS	R	11	111010110000		706 707
SDIV	R	11	10011010110	000010	4D6	SRBSL	I	10	1111000100		708 709
UDIV	R	11	10011010110	000011	4D6	ANDIS	I	10	11110001000		710 711
MUL	R	11	10011011000	011111	4D8	MOVK	IM	9	1111000101		712 713
SMULH	R	11	10011011010		4DA	STUR	D	11	111110000000		714 715
SMULB	R	11	10011011011		4DE	LDOR	D	11	111110000010		716 717
ORR	R	11	10101010000		550	STURD	R	11	111111000000		718 719
						LDORD	R	11	111111000010		720 721

Figure 4: The complete LEGv8 ISA

All the instructions are encoded with the same length of 32 bits in order to fetch and decode them more efficiently. They are also grouped into 5 instruction formats to give a more homogeneous encoding to operations performing similar steps and increase their decoding speed. The *R*-type instructions perform operations solely on registers, the *I*-type instructions make use of immediate values (defined in the code itself), the *D*-type instructions access the memory, the *B*-type and *CB* perform unconditional and conditional branching respectively, and the *IW*-type instructions to perform MOV instructions with wider immediate values.

CORE INSTRUCTION FORMATS					
R	opcode	Rm	shamt	Rn	Rd
	31 21 20	16 15	10 9	5 4	0
I	opcode	ALU immediate		Rn	Rd
	31 22 21	10 9		5 4	0
D	opcode	DT address		op	Rn Rt
	31 21 20	12 11 10 9		5 4	0
B	opcode	BR address			
	31 26 25				
CB	Opcode	COND BR address			Rt
	31 24 23	5 4			0
IW	opcode	MOV immediate			Rd
	31 21 20	5 4			0

Figure 5: The 5 formats of LEGv8 instructions with their encoding pattern

Motivations for choosing LEGv8

The LEGv8 ISA, being presented and defined in one of the major computer architecture undergraduate textbooks, is taught in many university courses around the world, including the Digital Systems Architecture course held by Prof. Carini at UniTS. In spite of its popularity, no real hardware has

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been made to run its instruction set natively, and the simulator landscape is almost equally lacking in viable options. This in turn makes it impossible for educators and students alike to show working examples of LEGv8 code, depriving them of teaching and learning opportunities. For these reasons I have chosen to work on an already existing and partially working LEGv8 simulator provided by Arm Holdings plc. to expand upon its functionalities to include a complete simulation of the ISA.

Chapter 1

"If 10 years from now, when you are doing something quick and dirty, you suddenly visualize that I am looking over your shoulders and say to yourself: 'Dijkstra would not have liked this', well that would be enough immortality for me."

Edsger W. Dijkstra

The LEGv8 simulators landscape

The current landscape of publicly available LEGv8 simulators can be divided into two categories: simulators that aim to reproduce the logical design presented in the textbook in chapter ?, and the simulators providing a high level simulation of the instruction set as defined in the book. The survey was performed on GitHub using “LEGv8” and “simulator” as keywords and only those in a reasonably working state (as per the author) have been considered.

Software simulators

Repository	Language	Integer Support	Pipelined	Registers view	Stack view	Floating Point Support
https://github.com/lcpckp/leg-cpu-sim	Java	Partial	No	Yes	Yes	No
https://github.com/chrwoods/legv8-emul	C/C++	Partial	Yes	Yes	Yes	No
https://github.com/mtalyat/LEGv8Day	C#	Partial	No	Yes	Yes	No
https://github.com/earworthy/LegV8Interpreter	Python	Partial	No	Yes	Yes	No
https://github.com/Adinack/LEGv8-Simulator	Swift	Partial	No	Yes	Yes	No
https://github.com/anvitha305/legv8sim	Python	Partial	No	Yes	Yes	Double precision only
https://github.com/dangbandy/LegV8-Simulator	C++	Partial	No	Yes	Yes	No
https://github.com/schang412/LEGv8-PyEmu	Python	Partial	No	No	No	No
https://github.com/GeorgePerrault/LEGv8-Interpreter	Python	Partial	No	Yes	Yes	No

Table 1.1: The surveyed software simulators

They utilize high level languages such as C++, Python, Swift, TypeScript and Java. Some of them offer a graphical interface, pipelined execution and

none of them implement the LEGv8 ISA in its entirety.

Hardware simulators

Repository	Language	Integer Support	Pipelined	Floating Point Support
https://github.com/nrbyte/ARM-LEGv8	Verilog	Partial	Yes	No
https://github.com/philbush/legv8	Verilog	Partial	Yes	No
https://github.com/ronitrex/ARMLEG	Verilog	Partial	Yes	No
https://github.com/mattco98/LEGv8-Processor	Verilog	Partial	Yes	Partial
https://github.com/amauriloquez90/LEGv8-CPU	Verilog	Partial	Yes	No
https://github.com/miguelangelo78/LEGv8-ISA	Verilog	Partial	Yes	No
https://github.com/brianworts/LEGv8_SingleCycle_Processor	Verilog	Partial	Yes	No
https://github.com/egflo/LEGv8	Verilog	Partial	Yes	No
https://github.com/ad153153/LegV8	Verilog	Partial	Yes	No

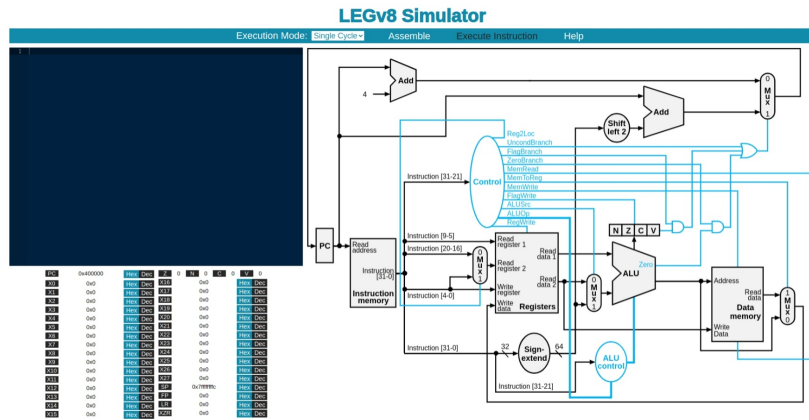
Table 1.2: The surveyed hardware simulators

They use mostly Verilog as their hardware description language and implement an incomplete subset of the LEGv8 ISA. Some of them follow closely the design of the textbook while others expand upon it adding more executable instructions. None of them offer a graphical interface nor implement the ISA in its entirety.

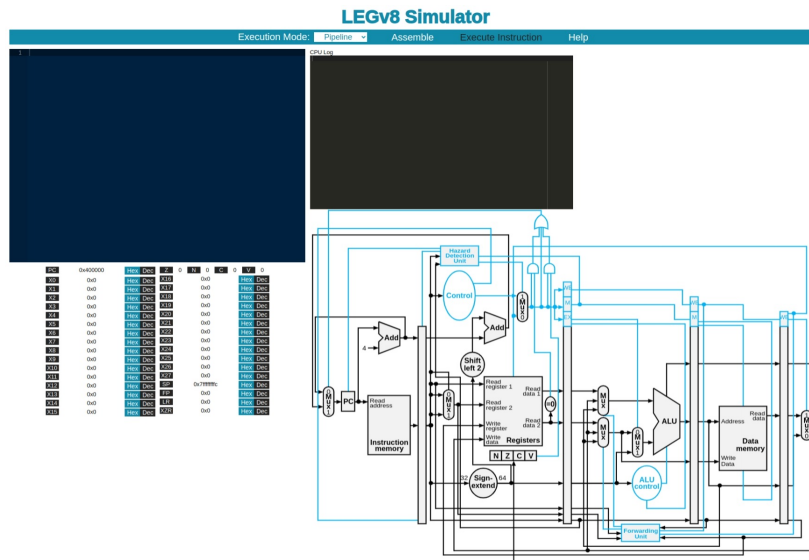
It is clear from this brief survey that the LEGv8 simulators space lacks any desirable candidates for code execution and inspection, as the software simulators are incomplete and platform-dependant, and the hardware ones lack interactivity and comprehensive visual output capabilities.

ARM’s LEGv8 simulator

This is the simulator officially provided by ARM Education and is the subject of this thesis’ work. It is written in Java 8 and uses Google’s GWT framework to transpile the code into native JavaScript to allow the simulator to be executed inside a web browser as a normal web application. It provides a comprehensive user interface displaying an interactive text editor (provided by AceGWT) to input LEGv8 code and to display errors, and a visualization of the state of the X registers. When selecting the single-cycle execution mode, a visualization of the logical scheme of the LEGv8 ISA is presented and for each step of the execution various components change color to indicate the current stage of the pipeline. For the pipelined execution mode, the visualization is slightly modified to include pipeline-specific information such as pipeline registers, the hazard detection unit and the forwarding unit. An additional textual representation of the pipeline is provided to see the stage occupied by each instruction at any given moment.



(a) Single cycle



(b) Pipeline

Figure 1.1: The simulator's main page with the two different execution modes

Features

This simulator presents many favorable characteristics:

- Written in Java (platform agnostic, extensible)
- Compiled as a web application (platform agnostic and easily deployable)
- Embedded text editor to input code with and error display

- Clear and rich visualization of the *X* and flag registers and the data-path of the CPU
- Almost all of the integer arithmetic is already implemented
- All types of integer *LOAD* and *STORE* instructions are already implemented, including *STXUR* and *LDXUR*
- Officially distributed by ARM Education (biggest support and discoverability)

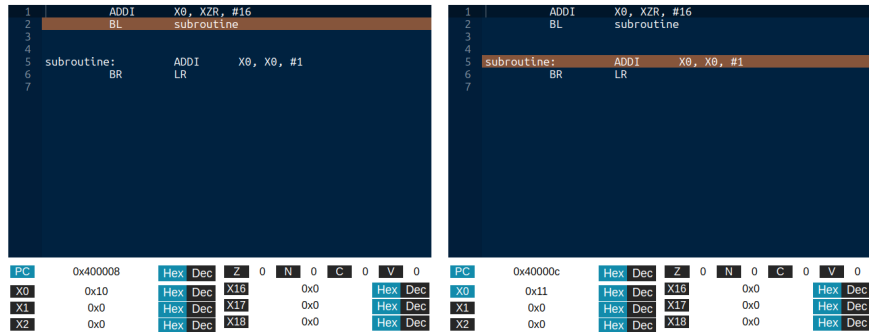
Problems

Unfortunately many problems present themselves when trying to run or develop the simulator:

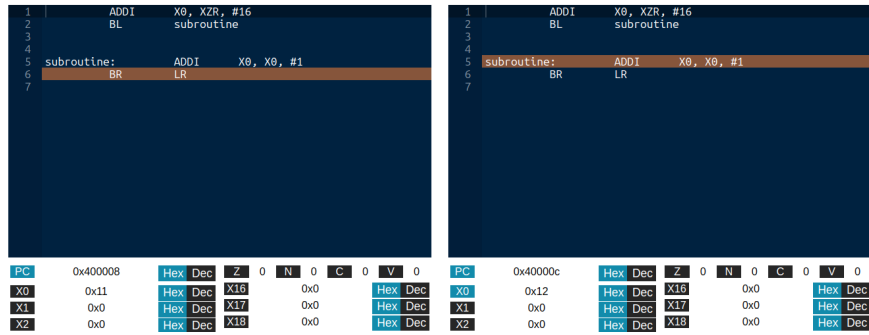
- Absence of any documentation on how to build the project
- Executable version distributed in web page form
- Pipeline execution is incomplete
- The branch and link instruction writes the incorrect address into the LR register, making it impossible to write subroutines as they loop forever
- The integer comparisons do not work properly, making it impossible to perform any kind of loop or branch
- The project is heavily dependent on the Eclipse Java IDE with an old GWT plugin to perform the build process
- The project depends on the outdated and barely supported GWT library to deploy the simulator as a web application. This restricts the developers from using newer Java features or better web frameworks.

I present below a demonstration of the bugs regarding the branch and link instruction and the integer comparisons:

CHAPTER 1.



(a) BL writes the wrong address to LR (b) Jumps to label and increments X0



(c) Reads wrong address from LR (d) Returns to wrong address

Figure 1.2: Branch returns to the wrong instruction, making it execute the branch in a loop

CHAPTER 1.

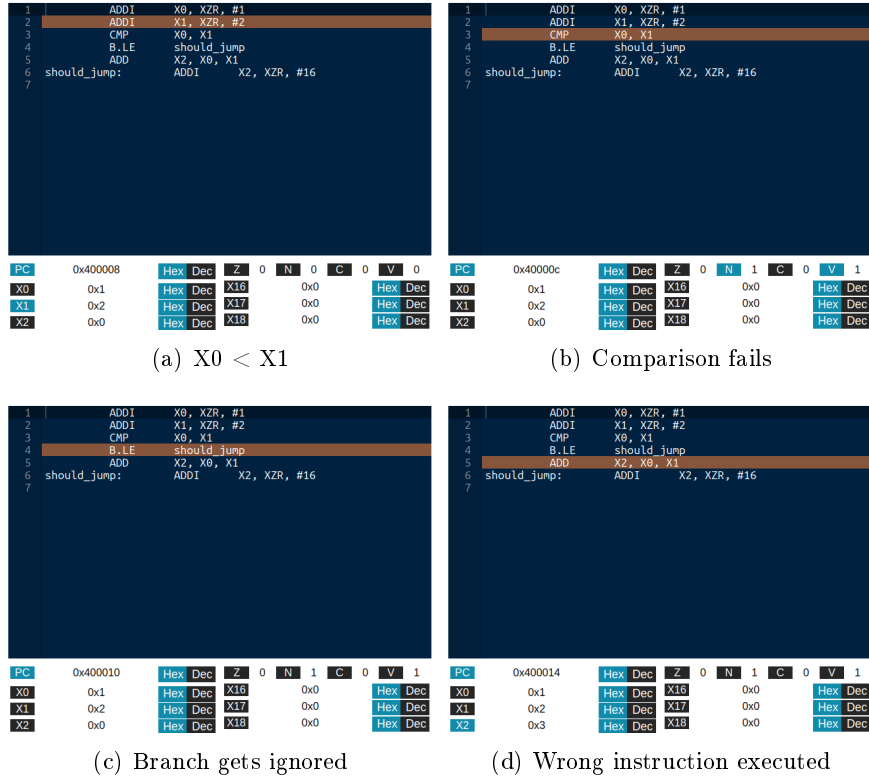


Figure 1.3: Comparisons do not set the correct flags and thus fail

For these reasons then this simulator was chosen as the subject of my thesis:

- Maximize the impact of my work by fixing and improving the most popular simulator available
- Provide the first complete implementation of the LEGv8 instruction set
- My pre-existing knowledge of Java and build automation systems would allow me to quickly get up to speed and extend the codebase efficiently
- Allow the Digital Systems Architecture course at UniTS and other courses in general to have a working LEGv8 simulator for more effective teaching

Chapter 2

Sit Amet

"Much of the excitement we get out of our work is that we don't really know what we are doing"

Edsger W. Dijkstra

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CHAPTER 2. SIT AMET

vel, eleifend faucibus, vehicula eu, lacus.

Chapter 3

Lorem Ipsum

"Program testing can be used to show the presence of bugs, but never to show their absence!"

Edsger W. Dijkstra

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CHAPTER 3. LOREM IPSUM

tricies ut, mi. Duis nec dui quis leo sagittis commodo.

Chapter 4

Dolor

"If debugging is the process of removing software bugs, then programming must be the process of putting them in."

Edsger W. Dijkstra

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4.1 Lorem Ipsum

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Conclusions

"The purpose of abstracting is not to be vague, but to create a new semantic level in which one can be absolutely precise."

Edsger W. Dijkstra

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4.2 Lorem Ipsum

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CONCLUSIONS

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Appendix A

Sit Amet

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A.1 Lorem Ipsum

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Appendix B

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Appendix C

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I thank my family for tolerating my long journey.
I thank Beatrice G. for believing in me.