

# SpaceLab OBDH 2.0

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SpaceLab - UFSC

# Summary

Project Overview

Hardware

Firmware

Documentation

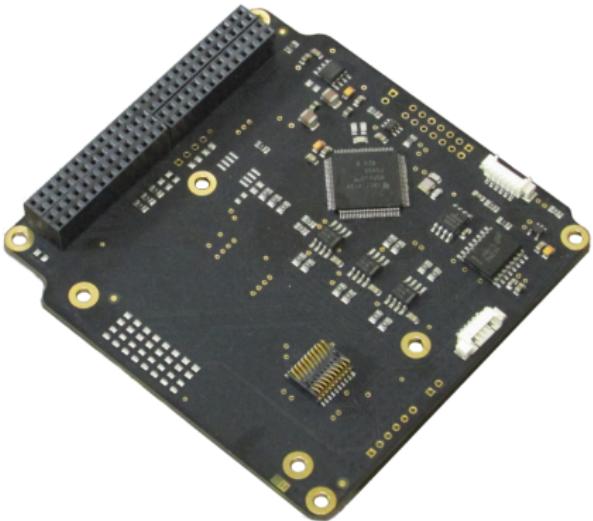
Management

# Project Overview

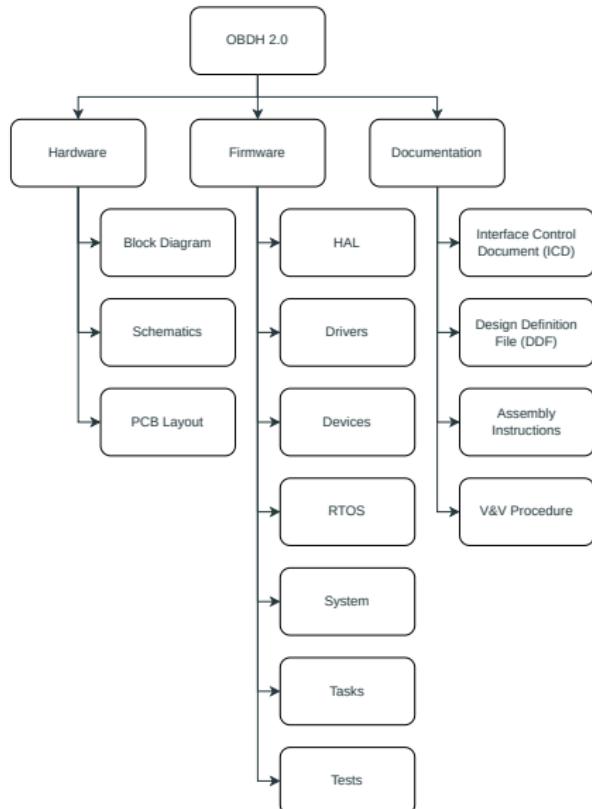
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# Overview

- On-Board Data Handling (OBDH) module for small satellites like CubeSats
- Project name: “*OBDH 2.0*”
- Custom made project
- Fully open source
- Based on FloripaSat-1 heritage



# Product Tree



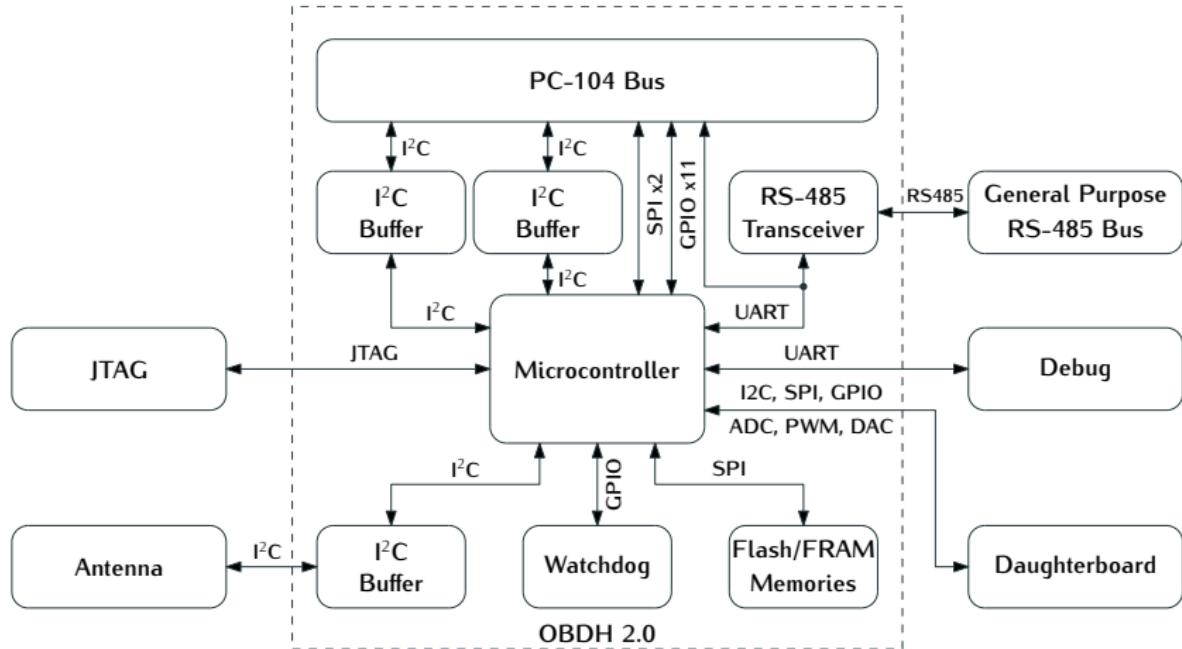
## Hardware

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# Specifications

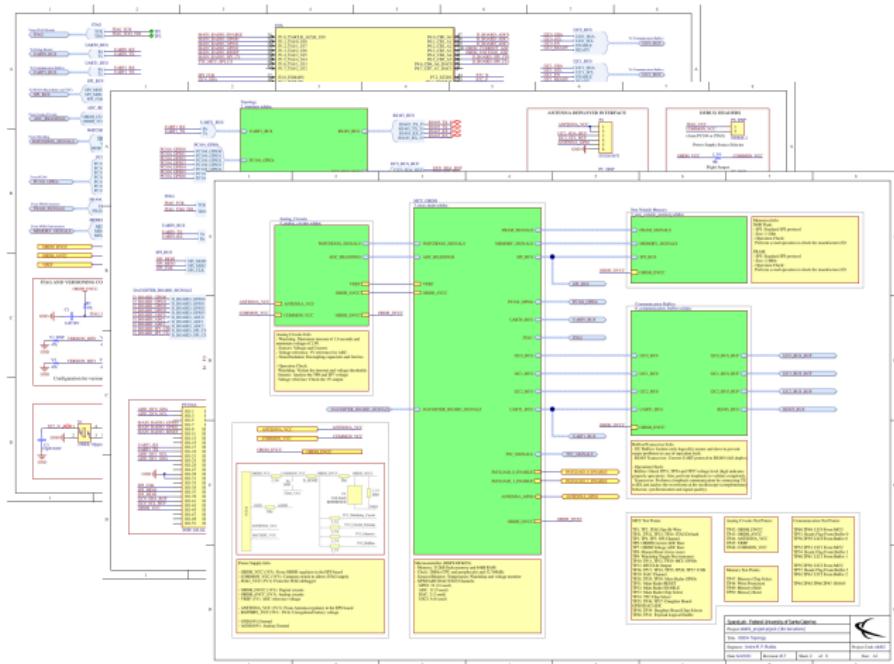
- Microcontroller: MSP430F6659/MSP430F5659
- Clock: 32 MHz
- Memories:
  - RAM: 64 kB (SRAM)
  - Flash: 512 kB (code), 1 Gb NOR (mass storage)
  - FRAM: 2 Mb
- Sensors: Voltage, current and temperature
- Interfaces: UART, I<sup>2</sup>C, SPI, GPIO, PWM, ADC, DAC and RS-485
- Mass: 53 g
- PC-104 compatible

# Electrical Block Diagram



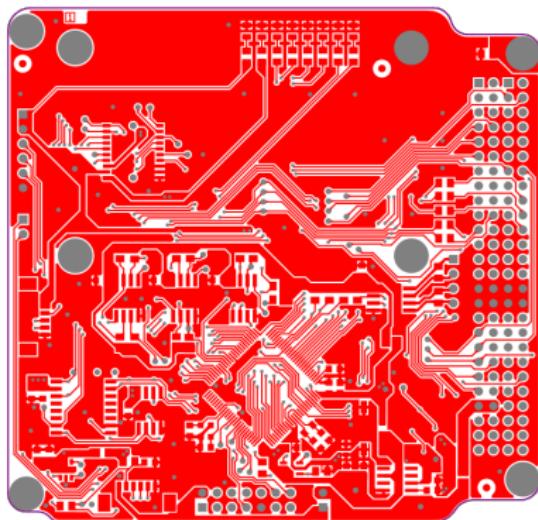
# Schematics

Available at: <https://github.com/spacelab-ufsc/obdh2>

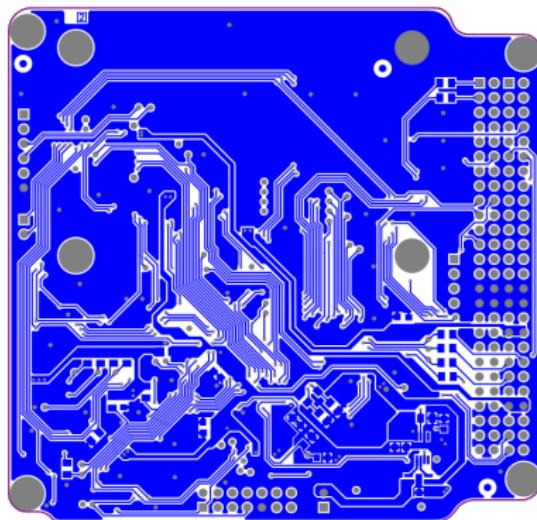


# PCB Layout

Available at: <https://github.com/spacelab-ufsc/obdh2>



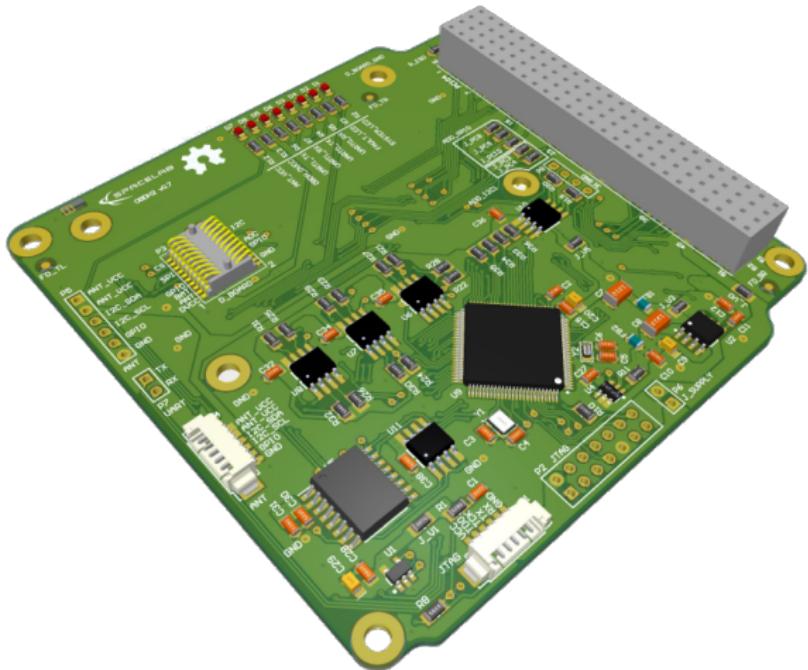
Top side



Bottom side

# 3D Model

Available at: <https://github.com/spacelab-ufsc/obdh2>



# Power Consumption

- Normal operation  $\cong$  **66 mW** (3,3 V @ 20 mA)



# Electrical Interfaces: PC-104

Pin [A-B]	H1A	H1B	H2A	H2B
1-2	-	-	-	-
3-4	-	-	GPIO_4	GPIO_5
5-6	-	-	-	-
7-8	GPIO_0	GPIO_1	-	GPIO_6
9-10	GPIO_2	-	-	-
11-12	GPIO_3	GPIO_7	SPI_0_MOSI	SPI_0_CLK
13-14	-	-	SPI_0_CS_1	SPI_0_MISO
15-16	-	-	-	-
17-18	UART_1_RX	GPIO_8	-	-
19-20	UART_1_TX	GPIO_9	-	-
21-22	-	-	-	-
23-24	-	-	-	-
25-26	-	-	-	-
27-28	-	-	-	-
29-30	GND	GND	GND	GND
31-32	GND	GND	GND	GND
33-34	-	-	-	-
35-36	SPI_0_CLK	-	VCC_3V3_ANT	VCC_3V3_ANT
37-38	SPI_0_MISO	-	-	-
39-40	SPI_0_MOSI	SPI_0_CS_0	-	-
41-42	I2C_0_SDA	-	-	-
43-44	I2C_0_SCL	-	-	-
45-46	VCC_3V3	VCC_3V3	VCC_BAT	VCC_BAT
47-48	-	-	-	-
49-50	-	-	I2C_1_SDA	-
51-52	-	-	I2C_1_SCL	-

# Other Electrical Interfaces

Connector	Interface	Type	Pins
P1	JTAG	PicoBlade	VCC_3V3 TDO_TDI TCK UART_TX UART_RX GND
P2	JTAG	Pin Header	TDO_TDI VCC_3V3 None None None None TCK None GND None None UART_TX None UART_RX

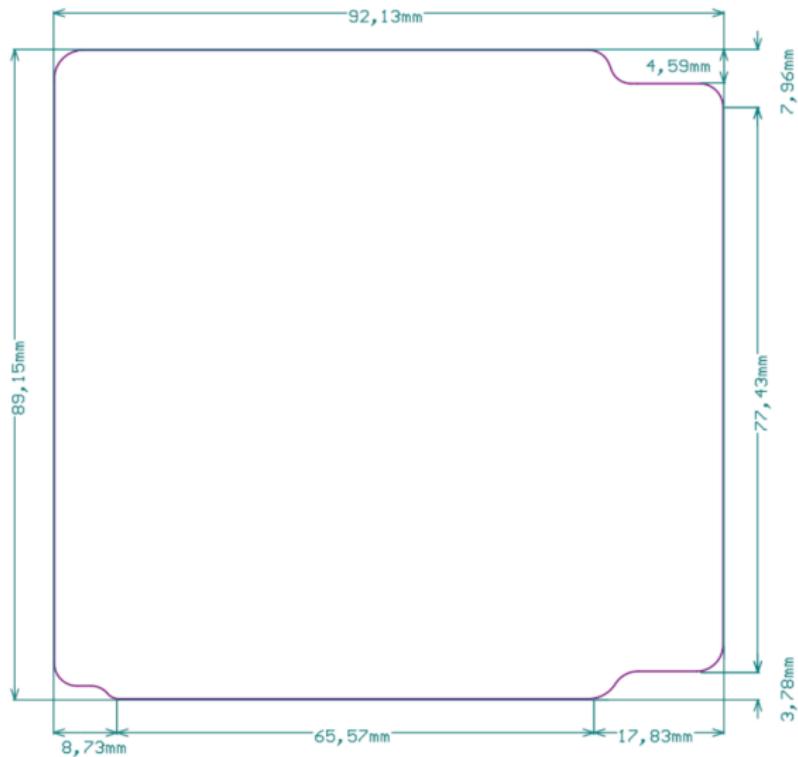
# Other Electrical Interfaces

Connector	Interface	Type	Pins	
			Row A	Row B
P3	Daughterboard	DSI	VCC_3V3	GND
			VCC_3V3_ANT	GND
			VCC_BAT	GND
			GPIO_0	GPIO_1
			GPIO_2	GPIO_3
			SPI_0_CLK	ADC_0
			SPI_0_MISO	ADC_1
			SPI_0_MOSI	ADC_2
			SPI_0_CS_0	I2C_2_SDA
			SPI_0_CS_1	I2C_2_SCL

# Other Electrical Interfaces

Connector	Interface	Type	Pins
P4	I2C	PicoBlade	VCC_3V3_ANT VCC_3V3_ANT I2C_SDA I2C_SCL GPIO GND
P5	I2C	Pin Header	VCC_3V3_ANT VCC_3V3_ANT I2C_SDA I2C_SCL GPIO GND
P6	Power	Pin Header	JTAG_VCC COMMON_VCC
P7	UART	Pin Header	UART_TX UART_RX
P8	RS-485	Pin Header	RS485_RX + RS485_RX - RS485_TX - RS485_TX +

# Dimensions



# External Memories

Characteristic	Flash NOR	FRAM
Manufacturer	Micron	Cypress
Partnumber	MT25QL01GBBB	CY15B102QN
Capacity	128 MB	2 Mb
Erase cycles	$10^5$	$10^{13}$
Data retention	2 years	121 years
Interface	SPI	SPI
Temperature range	-40 to 125 °C	-40 to 125 °C

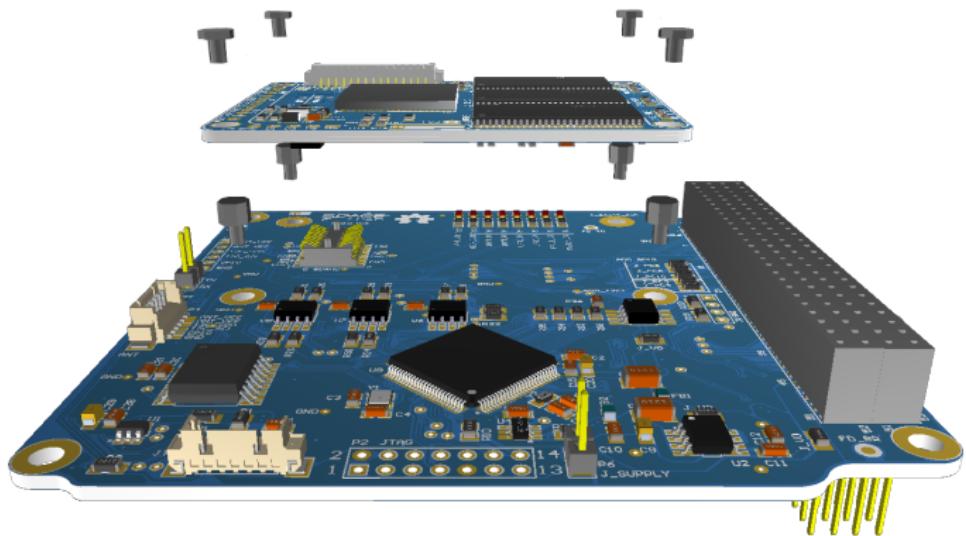
# Sensors

- Current sensor: MAX9934
- Voltage sensor: TLV341A
- Temperature sensor:  $\mu$ C (internal sensor)

## External Watchdog

- IC: Texas Instruments TPS3823
- Voltage monitor with a watchdog timer feature
- Timeout period: 1600 *ms*
- Reset period: 100 *ms*

# Daughterboard



# Flight Model Specs. and Preparation

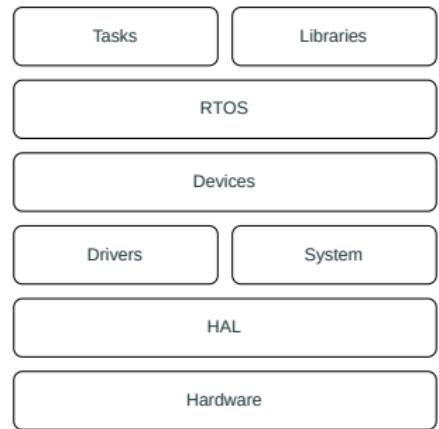
- PCB specs.: IPC 6012 Class 3
- PCB thickness: 1,6 mm
- Material: TG170 FR-4
- Surface finish: ENIG
- Conformal coating application

## Firmware

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# Overview

- Language: C
- OS: FreeRTOS v10.2.1
- Customized for a given mission



# System Tasks

Name	Priority	Initial delay [ms]	Period [ms]	Stack [bytes]
Antenna deployment	Highest	0	Aperiodic	150
Antenna reading	Medium	2000	60000	150
Beacon	High	1000	60000	1000
Data log	Medium	2000	600000	225
EDC reading	Medium	2000	60000	300
EPS reading	Medium	2000	60000	384
Heartbeat	Lowest	2000	500	160
Housekeeping	Medium	2000	10000	160
Read sensors	Medium	2000	60000	140
Startup (boot)	Highest	0	Aperiodic	350
System reset	Medium	0	36000000	128
Telecommand processing	High	10000	5000	500
Time control	Medium	1000	1000	128
TTC reading	Medium	2000	60000	384
Watchdog reset	Lowest	0	100	150

- **Antenna deployment:** This task deploys the antenna module just after the satellite ejection.
- **Peripherals data reading:** Each peripheral has a unique task for data reading.
- **Beacon:** The Beacon task transmits a data package that contains basic telemetry data of the satellite at every 60 seconds.
- **Data log:** This task saves the housekeeping data of the satellite in the flash memory at every 10 minutes.
- **Heartbeat:** The Heartbeat task keeps blinking an status LED at a rate of 1 Hz.
- **Housekeeping:** This task manages the general operation of the OBDH.

## System Tasks

- **Read sensors:** This task reads the internal sensors of the OBDH at every 60 seconds.
- **Startup (boot):** All devices, libraries and data structures are initialized in this task.
- **System reset:** This task resets the microcontroller by software at every 10 hours.
- **Telecommand processing:** This task processes all incoming telecommands.
- **Time control:** This task is responsible for the time management of the system.
- **Watchdog reset:** This task resets the internal and external watchdog timer at every 100 ms.

# System Parameters

ID	Name/Description	Type
0	Time counter in milliseconds	uint32
1	Temperature of the $\mu$ C in Kelvin	uint16
2	Input current in mA	uint16
3	Input voltage in mV	uint16
4	Last reset cause	uint8
5	Reset counter	uint16
6	Last valid telecommand (uplink packet ID)	uint8
7	Temperature of the radio in Kelvin	uint16
8	RSSI of the last valid telecommand	uint16
9	Temperature of the antenna in Kelvin	uint16
10	Antenna status bits	uint16
11	Hardware version	uint8
12	Firmware version (ex.: "v1.2.3" = 0x00010203)	uint32
13	Mode ("Normal" = 0, "Hibernation" = 1)	uint8
14	Timestamp of the last mode change	uint32
15	Mode duration in sec. (valid only in hibernation mode)	uint32
16	Initial hibernation executed	boolean
17	Initial hibernation time counter (minutes)	uint8
18	Antenna deployment executed	boolean
19	Antenna deployment counter	uint8

# Firmware: Development Environment

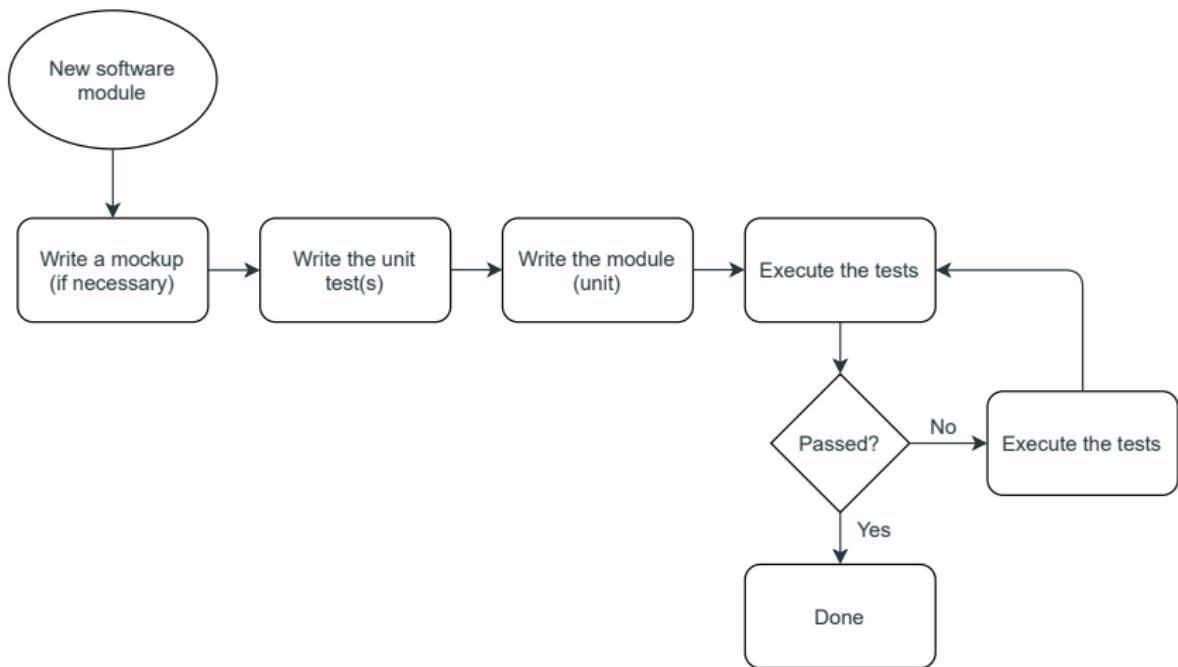
- Hardware: Engineering Model (EM)
- Programmer: Texas Instruments MSP-FET programmer
- IDE/Compiler: Code Composer Studio



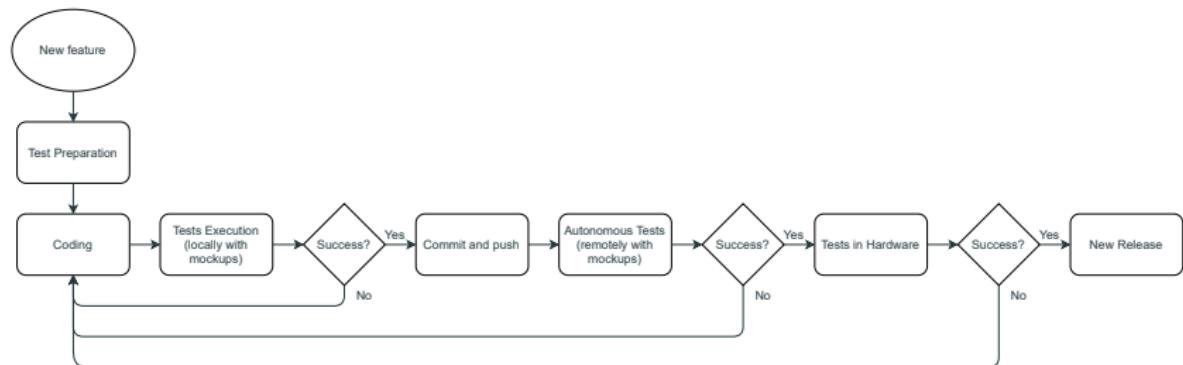
# Verification & Validation

- Unit tests framework: [CMocka](#)
- Static analysis tool: [CppCheck](#)
- Code style standard: [MISRA-C 2012](#)

# Verification & Validation: TDD Flow



# Verification & Validation: Development Flow



## Documentation

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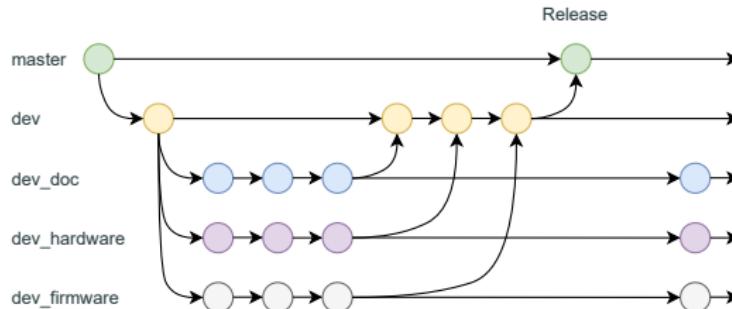
- User manual (PDF)
- This presentation
- Schematics
- Firmware: Doxygen

# Management

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# Project Management

- Activities, tasks and bug report: GitHub issues/project
- Source files and versioning control: Public **Git repository** with three development branches:
  - *dev\_doc*: Documentation
  - *dev\_hardware*: Hardware project
  - *dev\_firmware*: Firmware project



# Thanks!

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