

# SAM D5x/E5x Family Data Sheet

## I/O Multiplexing and Considerations

## 6. I/O Multiplexing and Considerations

### 6.1 Multiplexed Signals

By default each pin is controlled by the PORT as a general purpose I/O, and alternatively it can be assigned a different peripheral functions. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCfGn.PMUXEN, n = 0-31) in the PORT must be written to '1'. The selection of peripheral functions, A to N, is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) of the PORT. The table below describes the peripheral signals multiplexed to the PORT I/O pins.



**Important:** Not all signals are available on all devices. Refer to the Configuration Summary for available peripherals.

Table 6-1. Multiplexed Peripheral Signals

VFQFN 48	TQFP/VQFN/WLCSP 64	TQFP 100	TFBGA 120	TQFP 128	Pad Name	A EIC	B ANARE F	ADC0	ADC1	AC	DAC	PTC	C SERC0 M	D SERC0 M	E TC	F TCC	G TCC, PDEC	H QSPI, CAN1, USB, CORTEX_CM4	I SDHC, CAN0	J I <sup>2</sup> S	K PCC	L GMAC	M GCLK, AC	N CCL
48	64/C6	100	B2	128	PB03	EIC/EXTIN T[3]	-	ADC0/AIN[15]	-	-	-	X21/Y2 1	-	SERC0 M5/PAD[1]	TC8/WO[1]	-	-	-	-	-	-	-	-	-
1	01/B8	1	A1	1	PA00	EIC/EXTIN T[0]	-	-	-	-	-	-	-	SERC0 M1/PAD[0]	TC2/WO[0]	-	-	-	-	-	-	-	-	-
2	02/C8	2	B1	2	PA01	EIC/EXTIN T[1]	-	-	-	-	-	-	-	SERC0 M1/PAD[1]	TC2/WO[1]	-	-	-	-	-	-	-	-	-
		3	C1	3	PC00	EIC/EXTIN T[0]	-	-	ADC1/AIN[10]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		4	C2	4	PC01	EIC/EXTIN T[1]	-	-	ADC1/AIN[11]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		5	D1	7	PC02	EIC/EXTIN T[2]	-	-	ADC1/AIN[4]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		6	E2	8	PC03	EIC/EXTIN T[3]	-	-	ADC1/AIN[5]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3	03/C7	7	E1	9	PA02	EIC/EXTIN T[2]	-	ADC0/AIN[0]	-	-	DAC/VOUT[0]	-	-	-	-	-	-	-	-	-	-	-	-	-
4	04/D6	8	F2	10	PA03	EIC/EXTIN T[3]	ANARE F/VREFA	ADC0/AIN[1]	-	-	-	X0/Y0	-	-	-	-	-	-	-	-	-	-	-	-
	05/D7	9	F1	11	PB04	EIC/EXTIN T[4]	-	-	ADC1/AIN[6]	-	-	X22/Y2 2	-	-	-	-	-	-	-	-	-	-	-	-
	06/D8	10	G1	12	PB05	EIC/EXTIN T[5]	-	-	ADC1/AIN[7]	-	-	X23/Y2 3	-	-	-	-	-	-	-	-	-	-	-	-
		-	G2	13	PD00	EIC/EXTIN T[0]	-	-	ADC1/AIN[14]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		-	H1	16	PD01	EIC/EXTIN T[1]	-	-	ADC1/AIN[15]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	09/E7	13	H2	17	PB06	EIC/EXTIN T[6]	-	-	ADC1/AIN[8]	-	-	X24/Y2 4	-	-	-	-	-	-	-	-	-	-	-	CCL/IN[6]
	10/E6	14	J1	18	PB07	EIC/EXTIN T[7]	-	-	ADC1/AIN[9]	-	-	X25/Y2 5	-	-	-	-	-	-	-	-	-	-	-	CCL/IN[7]

# SAM D5x/E5x Family Data Sheet

## I/O Multiplexing and Considerations

continued																									
VQFN 48	TOFP/VQFN/WLCSP 64	TOFP 100	TFBGA 120	TOFP 128	Pad Name	A EIC	B ANARE F	ADC0	ADC1	AC	DAC	PTC	C SERC0 M	D SERC0 M	E TC	F TCC	G TCC, PDEC	H QSPI, CAN1, USB, CORTEX_CM4	I SDHC, CAN0	J I <sup>2</sup> S	K PCC	L GMAC	M GCLK, AC	N CCL	
7	11/F5	15	J2	19	PB08	EIC/EXTIN T[8]	-	ADC0/AIN[2]	ADC1/AIN[0]	-	-	X1/Y1	-	SERC0 M4/ PAD[0]	TC4/ WO[0]	-	-	-	-	-	-	-	-	-	CCL/ IN[8]
8	12/F8	16	K1	20	PB09	EIC/EXTIN T[9]	-	ADC0/AIN[3]	ADC1/AIN[1]	-	-	X2/Y2	-	SERC0 M4/ PAD[1]	TC4/ WO[1]	-	-	-	-	-	-	-	-	-	CCL/ OUT[2]
9	13/F7	17	K2	21	PA04	EIC/EXTIN T[4]	ANARE F/ VREFB	ADC0/AIN[4]	-	AC/AIN[0]	-	X3/Y3	-	SERC0 M0/ PAD[0]	TC0/ WO[0]	-	-	-	-	-	-	-	-	-	CCL/ IN[0]
10	14/F6	18	L1	22	PA05	EIC/EXTIN T[5]	-	ADC0/AIN[5]	-	AC/AIN[1]	DAC/ VOUT[1]		-	SERC0 M0/ PAD[1]	TC0/ WO[1]	-	-	-	-	-	-	-	-	-	CCL/ IN[1]
11	15/G7	19	L2	23	PA06	EIC/EXTIN T[6]	ANARE F/ VREFC	ADC0/AIN[6]	-	AC/AIN[2]	-	X4/Y4	-	SERC0 M0/ PAD[2]	TC1/ WO[0]	-	-	-	SDHC0/SDCD	-	-	-	-	-	CCL/ IN[2]
12	16/G8	20	M1	24	PA07	EIC/EXTIN T[7]	-	ADC0/AIN[7]	-	AC/AIN[3]	-	X5/Y5	-	SERC0 M0/ PAD[3]	TC1/ WO[1]	-	-	-	SDHC0/SDWP	-	-	-	-	-	CCL/ OUT[0]
		-	N1	27	PC04	EIC/EXTIN T[4]	-	-	-	-	-		SERC0 M6/ PAD[0]	-	-	TCC0/ WO[0]	-	-	-	-	-	-	-	-	
		21	N2	28	PC05	EIC/EXTIN T[5]	-	-	-	-	-		SERC0 M6/ PAD[1]	-	-	-	-	-	-	-	-	-	-	-	
		22	P1	29	PC06	EIC/EXTIN T[6]	-	-	-	-	-		SERC0 M6/ PAD[2]	-	-	-	-	-	SDHC0/SDCD	-	-	-	-	-	
		23	P2	30	PC07	EIC/EXTIN T[9]	-	-	-	-	-		SERC0 M6/ PAD[3]	-	-	-	-	-	SDHC0/SDWP	-	-	-	-	-	
13	17/H8	26	R1	33	PA08	EIC/NMI	-	ADC0/AIN[8]	ADC1/AIN[2]	-	-	X6/Y6	SERC0 M0/ PAD[0]	SERC0 M2/ PAD[1]	TC0/ WO[0]	TCC0/ WO[0]	TCC1/ WO[4]	QSPI/ DATA[0]	SDHC0/SDCMD	I <sup>2</sup> S/ MCK[0]	-	-	-	CCL/ IN[3]	
14	18/G6	27	P3	34	PA09	EIC/EXTIN T[9]	-	ADC0/AIN[9]	ADC1/AIN[3]	-	-	X7/Y7	SERC0 M0/ PAD[1]	SERC0 M2/ PAD[0]	TC0/ WO[1]	TCC0/ WO[1]	TCC1/ WO[5]	QSPI/ DATA[1]	SDHC0/SDDAT[0]	I <sup>2</sup> S/ FS[0]	-	-	-	CCL/ IN[4]	
15	19/H7	28	R2	35	PA10	EIC/EXTIN T[10]	-	ADC0/AIN[10]	-	-	-	X8/Y8	SERC0 M0/ PAD[2]	SERC0 M2/ PAD[2]	TC1/ WO[0]	TCC0/ WO[2]	TCC1/ WO[6]	QSPI/ DATA[2]	SDHC0/SDDAT[1]	I <sup>2</sup> S/ SCK[0]	-	-	GCLK/ IO[4]	CCL/ IN[5]	
16	20/G5	29	P4	36	PA11	EIC/EXTIN T[11]	-	ADC0/AIN[11]	-	-	-	X9/Y9	SERC0 M0/ PAD[3]	SERC0 M2/ PAD[3]	TC1/ WO[1]	TCC0/ WO[3]	TCC1/ WO[7]	QSPI/ DATA[3]	SDHC0/SDDAT[2]	I <sup>2</sup> S/SD O	-	-	GCLK/ IO[5]	CCL/ OUT[1]	
19	23/H6	32	R3	39	PB10	EIC/EXTIN T[10]	-	-	-	-	-		SERC0 M4/ PAD[2]	SERC0 M2/ PAD[2]	TC5/ WO[0]	TCC0/ WO[4]	TCC1/ WO[0]	QSPI/SC CK	SDHC0/SDDAT[3]	I <sup>2</sup> S/SDI	-	-	GCLK/ IO[4]	CCL/ IN[11]	
20	24/G4	33	P5	40	PB11	EIC/EXTIN T[11]	-	-	-	-	-		SERC0 M4/ PAD[3]	SERC0 M2/ PAD[3]	TC5/ WO[1]	TCC0/ WO[5]	TCC1/ WO[1]	QSPI/CS	SDHC0/SDCK	I <sup>2</sup> S/ FS[1]	-	-	GCLK/ IO[5]	CCL/ OUT[1]	
	25/H5	34	R4	41	PB12	EIC/EXTIN T[12]	-	-	-	-	-	X26/Y26	SERC0 M4/ PAD[0]	-	TC4/ WO[0]	TCC3/ WO[0]	TCC0/ WO[0]	CAN1/TX	SDHC0/SDCD	I <sup>2</sup> S/ SCK[1]	-	-	GCLK/ IO[6]	-	
	26/H4	35	P6	42	PB13	EIC/EXTIN T[13]	-	-	-	-	-	X27/Y27	SERC0 M4/ PAD[1]	-	TC4/ WO[1]	TCC3/ WO[1]	TCC0/ WO[1]	CAN1/RX	SDHC0/SDWP	I <sup>2</sup> S/ MCK[1]	-	-	GCLK/ IO[7]	-	
	27/G3	36	R5	43	PB14	EIC/EXTIN T[14]	-	-	-	-	-	X28/Y28	SERC0 M4/ PAD[2]	-	TC5/ WO[0]	TCC4/ WO[0]	TCC0/ WO[2]	CAN1/TX	-	-	PCC/ DATA[8]	GMAC/ GMDC	GCLK/ IO[0]	CCL/ IN[9]	
	28/H3	37	P7	44	PB15	EIC/EXTIN T[15]	-	-	-	-	-	X29/Y29	SERC0 M4/ PAD[3]	-	TC5/ WO[1]	TCC4/ WO[1]	TCC0/ WO[3]	CAN1/RX	-	-	PCC/ DATA[9]	GMAC/ GMDIO	GCLK/ IO[1]	CCL/ IN[10]	
		-	R6	47	PD08	EIC/EXTIN T[3]	-	-	-	-	-		SERC0 M7/ PAD[0]	SERC0 M6/ PAD[1]	-	TCC0/ WO[1]	-	-	-	-	-	-	-	-	
		-	P8	48	PD09	EIC/EXTIN T[4]	-	-	-	-	-		SERC0 M7/ PAD[1]	SERC0 M6/ PAD[0]	-	TCC0/ WO[2]	-	-	-	-	-	-	-	-	
		-	R7	49	PD10	EIC/EXTIN T[5]	-	-	-	-	-		SERC0 M7/ PAD[2]	SERC0 M6/ PAD[2]	-	TCC0/ WO[3]	-	-	-	-	-	-	-	-	
		-	P9	50	PD11	EIC/EXTIN T[6]	-	-	-	-	-		SERC0 M7/ PAD[3]	SERC0 M6/ PAD[3]	-	TCC0/ WO[4]	-	-	-	-	-	-	-	-	
		-	R8	51	PD12	EIC/EXTIN T[7]	-	-	-	-	-		-	-	-	TCC0/ WO[5]	-	-	-	-	-	-	-	-	
		40	P10	52	PC10	EIC/EXTIN T[10]	-	-	-	-	-		SERC0 M6/ PAD[2]	SERC0 M7/ PAD[2]	-	TCC0/ WO[0]	TCC1/ WO[4]	-	-	-	-	-	-	-	

# SAM D5x/E5x Family Data Sheet

## I/O Multiplexing and Considerations

continued																									
VQFN 48	TOFP/VQFN/WLCSP 64	TOFP 100	TFBGA 120	TOFP 128	Pad Name	A EIC	B ANARE F	ADC0	ADC1	AC	DAC	PTC	C SERCO M	D SERCO M	E TC	F TCC	G TCC, PDEC	H QSPI, CAN1, USB, CORTEX_CM4	I SDHC, CAN0	J I <sup>2</sup> S	K PCC	L GMAC	M GCLK, AC	N CCL	
		41	R9	55	PC11	EIC/EXTINT[11]	-	-	-	-	-		SERCO M6/PAD[3]	SERCO M7/PAD[3]	-	TCC0/ WO[1]	TCC1/ WO[5]	-	-	-	-	GMAC/ GMDC	-	-	
		42	R10	56	PC12	EIC/EXTINT[12]	-	-	-	-	-		SERCO M7/PAD[0]	SERCO M6/PAD[1]	-	TCC0/ WO[2]	TCC1/ WO[6]	-	-	-	PCC/ DATA[1 0]	GMAC/ GMDIO	-	-	
		43	P11	57	PC13	EIC/EXTINT[13]	-	-	-	-	-		SERCO M7/PAD[1]	SERCO M6/PAD[0]	-	TCC0/ WO[3]	TCC1/ WO[7]	-	-	-	PCC/ DATA[1 1]	-	-	-	
		44	R11	58	PC14	EIC/EXTINT[14]	-	-	-	-	-		SERCO M7/PAD[2]	SERCO M6/PAD[2]	-	TCC0/ WO[4]	TCC1/ WO[0]	-	-	-	PCC/ DATA[1 2]	GMAC/ GRX[3]	-	-	
		45	P12	59	PC15	EIC/EXTINT[15]	-	-	-	-	-		SERCO M7/PAD[3]	SERCO M6/PAD[3]	-	TCC0/ WO[5]	TCC1/ WO[1]	-	-	-	PCC/ DATA[1 3]	GMAC/ GRX[2]	-	-	
21	29/F2	46	R12	60	PA12	EIC/EXTINT[12]	-	-	-	-	-		SERCO M2/PAD[0]	SERCO M4/PAD[1]	TC2/ WO[0]	TCC0/ WO[6]	TCC1/ WO[2]	-	SDHC0/ SDCD	-	PCC/ DEN1	GMAC/ GRX[1]	AC/ CMP[0]	-	
22	30/G2	47	P13	61	PA13	EIC/EXTINT[13]	-	-	-	-	-		SERCO M2/PAD[1]	SERCO M4/PAD[0]	TC2/ WO[1]	TCC0/ WO[7]	TCC1/ WO[3]	-	SDHC0/ SDWP	-	PCC/ DEN2	GMAC/ GRX[0]	AC/ CMP[1]	-	
23	31/H1	48	R13	62	PA14	EIC/EXTINT[14]	-	-	-	-	-		SERCO M2/PAD[2]	SERCO M4/PAD[2]	TC3/ WO[0]	TCC2/ WO[0]	TCC1/ WO[2]	-	-	-	PCC/CLKK	GMAC/ GTXCK	GCLK/ IO[0]	-	
24	32/H2	49	R14	63	PA15	EIC/EXTINT[15]	-	-	-	-	-		SERCO M2/PAD[3]	SERCO M4/PAD[3]	TC3/ WO[1]	TCC2/ WO[1]	TCC1/ WO[3]	-	-	-	-	GMAC/ GRXER	GCLK/ IO[1]	-	
25	35/G1	52	R15	66	PA16	EIC/EXTINT[0]	-	-	-	-	-	X10/Y1 0	SERCO M1/PAD[0]	SERCO M3/PAD[1]	TC2/ WO[0]	TCC1/ WO[0]	TCC0/ WO[4]	-	-	-	PCC/ DATA[0]	GMAC/ GCRS/ GRXDV (6)	GCLK/ IO[2]	CCL/ IN[0]	
26	36/F1	53	P14	67	PA17	EIC/EXTINT[1]	-	-	-	-	-	X11/Y1 1	SERCO M1/PAD[1]	SERCO M3/PAD[0]	TC2/ WO[1]	TCC1/ WO[1]	TCC0/ WO[5]	-	-	-	PCC/ DATA[1]	GMAC/ GTXEN	GCLK/ IO[3]	CCL/ IN[1]	
27	37/E1	54	P15	68	PA18	EIC/EXTINT[2]	-	-	-	-	-	X12/Y1 2	SERCO M1/PAD[2]	SERCO M3/PAD[2]	TC3/ WO[0]	TCC1/ WO[2]	TCC0/ WO[6]	-	-	-	PCC/ DATA[2]	GMAC/ GTX[0]	AC/ CMP[0]	CCL/ IN[2]	
28	38/E2	55	N14	69	PA19	EIC/EXTINT[3]	-	-	-	-	-	X13/Y1 3	SERCO M1/PAD[3]	SERCO M3/PAD[3]	TC3/ WO[1]	TCC1/ WO[3]	TCC0/ WO[7]	-	-	-	PCC/ DATA[3]	GMAC/ GTX[1]	AC/ CMP[1]	CCL/ OUT[0]	
		56	N15	70	PC16	EIC/EXTINT[0]	-	-	-	-	-		SERCO M6/PAD[0]	SERCO M0/PAD[1]	-	TCC0/ WO[0]	PDEC/ QDI[0]	-	-	-	-	GMAC/ GTX[2]	-	-	
		57	M14	71	PC17	EIC/EXTINT[1]	-	-	-	-	-		SERCO M6/PAD[1]	SERCO M0/PAD[0]	-	TCC0/ WO[1]	PDEC/ QDI[1]	-	-	-	-	GMAC/ GTX[3]	-	-	
		58	M15	72	PC18	EIC/EXTINT[2]	-	-	-	-	-		SERCO M6/PAD[2]	SERCO M0/PAD[2]	-	TCC0/ WO[2]	PDEC/ QDI[2]	-	-	-	-	GMAC/ GRXCK	-	-	
		59	L14	73	PC19	EIC/EXTINT[3]	-	-	-	-	-		SERCO M6/PAD[3]	SERCO M0/PAD[3]	-	TCC0/ WO[3]	-	-	-	-	-	GMAC/ GTXER	-	-	
		60	L15	74	PC20	EIC/EXTINT[4]	-	-	-	-	-		-	-	-	TCC0/ WO[4]	-	-	SDHC1/ SDCD	-	-	GMAC/ GRXDV	-	CCL/ IN[9]	
		61	K14	75	PC21	EIC/EXTINT[5]	-	-	-	-	-		-	-	-	TCC0/ WO[5]	-	-	SDHC1/ SDWP	-	-	GMAC/ GCOL	-	CCL/ IN[10]	
		-	K15	76	PC22	EIC/EXTINT[6]	-	-	-	-	-		SERCO M1/PAD[0]	SERCO M3/PAD[1]	-	TCC0/ WO[6]	-	-	-	-	-	GMAC/ GMDC	-	-	
		-	J14	77	PC23	EIC/EXTINT[7]	-	-	-	-	-		SERCO M1/PAD[1]	SERCO M3/PAD[0]	-	TCC0/ WO[7]	-	-	-	-	-	GMAC/ GMDIO	-	-	
		-	J15	80	PD20	EIC/EXTINT[10]	-	-	-	-	-		SERCO M1/PAD[2]	SERCO M3/PAD[2]	-	TCC1/ WO[0]	-	-	SDHC1/ SDCD	-	-	-	-	-	
		-	H14	81	PD21	EIC/EXTINT[11]	-	-	-	-	-		SERCO M1/PAD[3]	SERCO M3/PAD[3]	-	TCC1/ WO[1]	-	-	SDHC1/ SDWP	-	-	-	-	-	
	39/D4	64	H15	82	PB16	EIC/EXTINT[0]	-	-	-	-	-		SERCO M5/PAD[0]	-	TC6/ WO[0]	TCC3/ WO[0]	TCC0/ WO[4]	-	SDHC1/ SDCD	I <sup>2</sup> S/ SCK[0]	-	-	GCLK/ IO[2]	CCL/ IN[11]	
	40/D1	65	G15	83	PB17	EIC/EXTINT[1]	-	-	-	-	-		SERCO M5/PAD[1]	-	TC6/ WO[1]	TCC3/ WO[1]	TCC0/ WO[5]	-	SDHC1/ SDWP	I <sup>2</sup> S/ MCK[0]	-	-	GCLK/ IO[3]	CCL/ OUT[3]	
		66	G14	84	PB18	EIC/EXTINT[2]	-	-	-	-	-		SERCO M5/PAD[2]	SERCO M7/PAD[2]	-	TCC1/ WO[0]	PDEC/ QDI[0]	-	SDHC1/ SDDAT[0]	-	-	-	GCLK/ IO[4]	-	

# SAM D5x/E5x Family Data Sheet

## I/O Multiplexing and Considerations

continued																								
VQFN 48	TOFP/VQFN/WLCSP 64	TOFP 100	TFBGA 120	TOFP 128	Pad Name	A EIC	B ANARE F	ADC0	ADC1	AC	DAC	PTC	C SERCO M	D SERCO M	E TC	F TCC	G TCC, PDEC	H QSPI, CAN1, USB, CORTE X_CM4	I SDHC, CAN0	J I <sup>2</sup> S	K PCC	L GMAC	M GCLK, AC	N CCL
		67	F15	85	PB19	EIC/EXTIN T[3]	-	-	-	-	-		SERCO M5/ PAD[3]	SERCO M7/ PAD[3]	-	TCC1/ WO[1]	PDEC/ QDI[1]	-	SDHC1/ SDDAT[1]	-	-	-	GCLK/ IO[5]	-
		68	F14	86	PB20	EIC/EXTIN T[4]	-	-	-	-	-		SERCO M3/ PAD[0]	SERCO M7/ PAD[1]	-	TCC1/ WO[2]	PDEC/ QDI[2]	-	SDHC1/ SDDAT[2]	-	-	-	GCLK/ IO[6]	-
		69	E15	87	PB21	EIC/EXTIN T[5]	-	-	-	-	-		SERCO M3/ PAD[1]	SERCO M7/ PAD[0]	-	TCC1/ WO[3]	-	-	SDHC1/ SDDAT[3]	-	-	-	GCLK/ IO[7]	-
29	41/D2	70	E14	88	PA20	EIC/EXTIN T[4]	-	-	-	-	-	X14/Y1 4	SERCO M5/ PAD[2]	SERCO M3/ PAD[2]	TC7/ WO[0]	TCC1/ WO[4]	TCC0/ WO[0]	-	SDHC1/ SDCMD	I <sup>2</sup> S/ FS[0]	PCC/ DATA[4]	GMAC/ GMDC	-	-
30	42/D3	71	D15	89	PA21	EIC/EXTIN T[5]	-	-	-	-	-	X15/Y1 5	SERCO M5/ PAD[3]	SERCO M3/ PAD[3]	TC7/ WO[1]	TCC1/ WO[5]	TCC0/ WO[1]	-	SDHC1/ SDCK	I <sup>2</sup> S/SD O	PCC/ DATA[5]	GMAC/ GMDIO	-	-
31	43/C1	72	D14	92	PA22	EIC/EXTIN T[6]	-	-	-	-	-	X16/Y1 6	SERCO M3/ PAD[0]	SERCO M5/ PAD[1]	TC4/ WO[0]	TCC1/ WO[6]	TCC0/ WO[2]	-	CAN0/T X	I <sup>2</sup> S/SDI X	PCC/ DATA[6]	-	-	CCL/ IN[6]
32	44/C2	73	C14	93	PA23	EIC/EXTIN T[7]	-	-	-	-	-	X17/Y1 7	SERCO M3/ PAD[1]	SERCO M5/ PAD[0]	TC4/ WO[1]	TCC1/ WO[7]	TCC0/ WO[3]	USB/ SOF_1 KHZ	CAN0/R X	I <sup>2</sup> S/ FS[1]	PCC/ DATA[7]	-	-	CCL/ IN[7]
33	45/B1	74	C15	94	PA24	EIC/EXTIN T[8]	-	-	-	-	-		SERCO M3/ PAD[2]	SERCO M5/ PAD[2]	TC5/ WO[0]	TCC2/ WO[2]	PDEC/ QDI[0]	USB/D M	CAN0/T X	-	-	-	-	CCL/ IN[8]
34	46/A1	75	B15	95	PA25	EIC/EXTIN T[9]	-	-	-	-	-		SERCO M3/ PAD[3]	SERCO M5/ PAD[3]	TC5/ WO[1]	-	PDEC/ QDI[1]	USB/DP X	CAN0/R X	-	-	-	-	CCL/ OUT[2]
37	49/A2	78	A15	98	PB22	EIC/EXTIN T[6]	-	-	-	-	-		SERCO M1/ PAD[2]	SERCO M5/ PAD[2]	TC7/ WO[0]	-	PDEC/ QDI[2]	USB/ SOF_1 KHZ	-	-	-	-	GCLK/ IO[0]	CCL/ IN[0]
38	50/A3	79	A14	99	PB23	EIC/EXTIN T[7]	-	-	-	-	-		SERCO M1/ PAD[3]	SERCO M5/ PAD[3]	TC7/ WO[1]	-	PDEC/ QDI[0]	-	-	-	-	-	GCLK/ IO[1]	CCL/ OUT[0]
		80	B14	100	PB24	EIC/EXTIN T[8]	-	-	-	-	-		SERCO M0/ PAD[0]	SERCO M2/ PAD[1]	-	-	PDEC/ QDI[1]	-	-	-	-	-	AC/ CMP[0]	-
		81	B13	101	PB25	EIC/EXTIN T[9]	-	-	-	-	-		SERCO M0/ PAD[1]	SERCO M2/ PAD[0]	-	-	PDEC/ QDI[2]	-	-	-	-	-	AC/ CMP[1]	-
		-	A13	102	PB26	EIC/EXTIN T[12]	-	-	-	-	-		SERCO M2/ PAD[0]	SERCO M4/ PAD[1]	-	TCC1/ WO[2]	-	-	-	-	-	-	-	-
		-	B12	103	PB27	EIC/EXTIN T[13]	-	-	-	-	-		SERCO M2/ PAD[1]	SERCO M4/ PAD[0]	-	TCC1/ WO[3]	-	-	-	-	-	-	-	-
		-	A12	104	PB28	EIC/EXTIN T[14]	-	-	-	-	-		SERCO M2/ PAD[2]	SERCO M4/ PAD[2]	-	TCC1/ WO[4]	-	-	-	I <sup>2</sup> S/ SCK[1]	-	-	-	-
		-	B11	105	PB29	EIC/EXTIN T[15]	-	-	-	-	-		SERCO M2/ PAD[3]	SERCO M4/ PAD[3]	-	TCC1/ WO[5]	-	-	-	I <sup>2</sup> S/ MCK[1]	-	-	-	-
		82	A11	108	PC24	EIC/EXTIN T[8]	-	-	-	-	-		SERCO M0/ PAD[2]	SERCO M2/ PAD[2]	-	-	-	CORTE X_CM4/ TRACE DATA[3]	-	-	-	-	-	-
		83	B10	109	PC25	EIC/EXTIN T[9]	-	-	-	-	-		SERCO M0/ PAD[3]	SERCO M2/ PAD[3]	-	-	-	CORTE X_CM4/ TRACE DATA[2]	-	-	-	-	-	-
		84	A10	110	PC26	EIC/EXTIN T[10]	-	-	-	-	-		-	-	-	-	-	CORTE X_CM4/ TRACE DATA[1]	-	-	-	-	-	-
		85	A9	111	PC27	EIC/EXTIN T[11]	-	-	-	-	-		SERCO M1/ PAD[0]	-	-	-	-	CORTE X_CM4/ TRACE CLK	-	-	-	-	CORTE X_M4/S WO	CCL/ IN[4]
		86	B9	112	PC28	EIC/EXTIN T[12]	-	-	-	-	-		SERCO M1/ PAD[1]	-	-	-	-	CORTE X_CM4/ TRACE DATA[0]	-	-	-	-	-	CCL/ IN[5]
39	51/B3	87	B8	113	PA27	EIC/EXTIN T[11]	-	-	-	-	-	X18/Y1 8	-	-	-	-	-	-	-	-	-	-	GCLK/ IO[1]	-
40	52/B4	88	A8	114	RESET_N	-	-	-	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-
45	57/C5	93	B7	119	PA30	EIC/EXTIN T[14]	-	-	-	-	-	X19/Y1 9	-	SERCO M1/ PAD[2]	TC6/ WO[0]	TCC2/ WO[0]	-	CORTE X_CM4/ SWCLK	-	-	-	-	GCLK/ IO[0]	CCL/ IN[3]

# SAM D5x/E5x Family Data Sheet

## I/O Multiplexing and Considerations

.....continued																								
VQFN 48	TQFP/VQFN/WLCSP 64	TQFP 100	TFBGA 120	TQFP 128	Pad Name	A EIC	B ANARE F	ADC0	ADC1	AC	DAC	PTC	C SERCOM	D SERCOM	E TC	F TCC	G TCC, PDEC	H QSPI, CAN1, USB, CORTEX_CM4	I SDHC, CAN0	J I <sup>2</sup> S	K PCC	L GMAC	M GCLK, AC	N CCL
46	58/D5	94	B6	120	PA31	EIC/EXTINT[15]	-	-	-	-	-	-	-	SERCOM1/PAD[3]	TC6/WO[1]	TCC2/WO[1]	-	CORTEX_CM4/SWDIO-	-	-	-	-	-	CCL/OUT[1]
	59/A6	95	A5	121	PB30	EIC/EXTINT[14]	-	-	-	-	-	-	-	SERCOM5/PAD[1]	TC0/WO[0]	TCC4/WO[0]	TCC0/WO[6]	CORTEX_CM4/SWO	-	-	-	-	-	-
	60/B6	96	B5	122	PB31	EIC/EXTINT[15]	-	-	-	-	-	-	-	SERCOM5/PAD[0]	TC0/WO[1]	TCC4/WO[1]	TCC0/WO[7]	-	-	-	-	-	-	-
		-	A4	123	PC30	EIC/EXTINT[14]	-	-	ADC1/AIN[12]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		-	B4	124	PC31	EIC/EXTINT[15]	-	-	ADC1/AIN[13]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	61/A7	97	A3	125	PB00	EIC/EXTINT[0]	-	ADC0/AIN[12]	-	-	-	X30/Y30	-	SERCOM5/PAD[2]	TC7/WO[0]	-	-	-	-	-	-	-	-	CCL/IN[1]
	62/B7	98	B3	126	PB01	EIC/EXTINT[1]	-	ADC0/AIN[13]	-	-	-	X31/Y31	-	SERCOM5/PAD[3]	TC7/WO[1]	-	-	-	-	-	-	-	-	CCL/IN[2]
47	63/A8	99	A2	127	PB02	EIC/EXTINT[2]	-	ADC0/AIN[14]	-	-	-	X20/Y20	-	SERCOM5/PAD[0]	TC6/WO[0]	TCC2/WO[2]	-	-	-	-	-	-	-	CCL/OUT[0]

### Note:

1. All analog pin functions are on the peripheral function B. The peripheral function B must be selected to disable the digital control of the pin. The AC has analog signals on the peripheral function B and digital signals on the peripheral function M.
2. The pins used by the SERCOM in I<sup>2</sup>C mode are listed in section SERCOM I<sup>2</sup>C Configurations.
3. The following High Sink pins have different properties than the regular pins:  
PA08, PA09, PA12, PA13, PA16, PA17, PA22, PA23, PD08, PD09.
4. Clusters of multiple GPIO pins are sharing the same supply pin.
5. When TRACE is used in single-wire debug mode, PC27 assumes the role of SWO. In other debug modes, PB30 assumes the SWO functionality.
6. GRXDV is available on PA16 for the 64-pin package only.



**Important:** Not all signals are available on all devices. Refer to the Configuration Summary for available peripherals.

### Related Links

[6.2.6 SERCOM I<sup>2</sup>C Configurations](#)

[6.2.9 GPIO Clusters](#)

## 6.2 Other Functions

### 6.2.1 Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing is controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32K Oscillators Controller (OSC32KCTRL).