Epoch SiT58xx & SiT71xx Digital Control Guide

Contents

1 Introduction 1
2 Register Map and Serial Interface 1
2.1 SPI Usage Notes 3
3 Determining Ambient Temperature 3
4 Using the DCOCXO Function 5
4.1 Pull Range, Absolute Pull Range 5
5 DCOCXO-Specific Design Considerations 6
5.1 Pull Range and Absolute Pull Range 6
5.2 Output Frequency 6

1 Introduction

This document details the SiT58xx & SiT71xx product family register map and digital control functionality. Section 2 describes the registers that control heater power readout and digitally controlled OCXOs (DCOCXO) mode operation. DCOCXO mode is a mode of operation where the DCOCXO output can be precisely controlled via digital inputs applied through either the I^2C or SPI interface. It is used commonly to phase lock the DCOCXO output to another reference or to compensate for the DCOCXOs aging. Section 3 describes how to use the SiT58xx/SiT71xx heater power to determine ambient temperature. Section 1 covers the details of DCOCXO mode operation.

2 Register Map and Serial Interface

Table 1 below shows the details of the Epoch register map dealing with heater power and DCOCXO mode. For parts preprogrammed with fixed addresses, the Epoch digital interface address is 0x5x where the last x can be any hex number from 0 to F. For parts that use the A1 A0 pins to set the address the address decode is shown in the last part of Table 1.

Table 1. Epoch Register Detail and I2C Address Decode

Description of Registers					
Register Address	Name	Size (bits)	Format (16 bit registers)	Scaling	Read/ Write
0x00	DCXO_Clip	13	DCXO_Clip[12:0] register bits[12:0]		R
0x0C	DCXO	16	DCXO[38:23]		R/W
0x0D	DCXO	16	DCXO[22:7]		R/W
0x0E	DCXO	7	DCXO[6:0] register bits[15:9]		R/W

0x1E	Power Indicator (PID output)	16	PID[17:2]		R
0x1F	Power Indicator (PID output)	2	PID[1:0] register bits[15:14]		R
0x2A	chip_id	16	chipID[15:0]		R

Preprogrammed Address Decode (I2C)	
Ordering Code	Address (in binary)
0	101 0000
1	101 0001
2	101 0010
3	101 0011
4	101 0100
5	101 0101
6	101 0110
7	101 0111
8	101 1000
9	101 1001
A	101 1010
B	101 1011
C	101 1100
D	101 1101
E	101 1110
F	101 1111

A1 A0 Pin Address Decode (I2C)		
A1	A0	Address (in binary)
0	0	101 0000
0	1	101 0010
1	0	101 1000
1	1	101 1010

2.1 SPI Usage Notes

The SPI bus for the Epoch family uses the below standard pin definitions.

SCLK – Serial clock

MOSI – Master output slave input

MISO – Master input slave output

$\overline{CS}$ – Chip select, active low

The general format of communication to the chip via SPI is as shown below.

Command[7:0]	Address[7:0]	Data[15:0]

The write and read commands are as shown below:

Write: 57h

Read: A5h

Address and data are as shown in Table 1.

3 Determining Ambient Temperature

For the Epoch OCXO, heater power and ambient temperature are linearly related. Since heater power can be read from Epoch, this linear relationship can be used to determine ambient temperature. To read heater power, use the digital interface and read registers 1E and 1F as indicated below.

1. Do a master register read from slave address 0x5x
2. Read registers 0x1E and 0x1F. A block read is best. For this and all other register reads the minimum time between reads is 50ms.
3. The bits are arranged as shown in Table 1. Total of 18 bits. 16 bits in register 0x1E and 2 MSB's of register 0x1F.

To determine the linear relationship between heater power and ambient temp, read (via the digital interface) heater power at 2 known ambient temps. Using these points, the line which describes temperature as a function of heater power can be determined. The equation is shown below in Figure 1, where (T1,P1) and (T2, P2) are the power and temperature pairs .

$$T(P) := \frac{T2 - T1}{P2 - P1} \cdot P + \left(T1 - \frac{T2 - T1}{P2 - P1} \cdot P1 \right)$$

Figure 1: Linear relationship between ambient temperature and heater power

In this equation, T(P) represents ambient temperature and P is the heater power read from Epoch. This equation needs to be determined for each DCOCXO.

4 Using the DCOCXO Function

The DCOXO function is controlled by 39 bits contained in registers 0x0C, 0x0D and 0x0E. The bits are arranged as shown in Table 1. The maximum pull range is controlled by the 13 bits contained in register 0x00 and called DCXO_Clip.

The DCXO binary control number represents the fractional portion of the total possible pull of the output frequency. The total pull available is ±800 ppm. The next sections describe how to determine the DCOCXO control words based upon a desired frequency.

4.1 Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control word over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability and tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$\text{APR} = \text{PR} - F_{\text{stability}} - F_{\text{aging}}$$

where $F_{\text{stability}}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load. In the case of the Epoch DCOCXO $F_{\text{stability}}$ and F_{aging} are insignificant compared to PR, meaning the APR is essentially equal to PR.

Figure 2 shows a typical SiTime DCOCXO Freq vs Frequency Control Word (FCW) characteristic. The Frequency vs FCW characteristic varies with conditions, so that the frequency output at a given FCW can vary by as much as the specified frequency stability of the DCOCXO. For such DCOCXOs, the frequency stability and APR are independent of each other. This allows very wide range of pull options without compromising frequency stability.

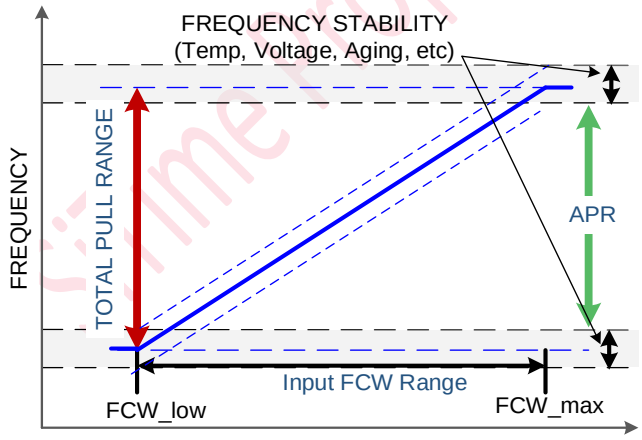

Figure 2: Typical SiTime DCOCXO Frequency vs FCW plot

The FCW_low and FCW_max are the specified limits of the FCW range as shown in Figure 2 above. Applying FCW values beyond the upper and lower limits does not result in significant changes of output frequency. The frequency vs FCW characteristic of the DCOCXO saturates beyond the FCW_low and FCW_max limits.

5 DCOCXO-Specific Design Considerations

5.1 Pull Range and Absolute Pull Range

Pull range and absolute pull range are described in the previous section. Table 2 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

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Table 2. APR Options

Pull Range Ordering Code	Pull Range ppm	APR ppm (±3 ppb option)	APR ppm (±5 ppb option)
V	±3.125	±3.039	±3.035
T	±6.25	±6.164	±6.160
R	±10	±9.914	±9.910
Q	±12.5	±12.414	±12.410
M	±25	±24.914	±24.910
B	±50	±49.914	±49.910
E	±100	±99.914	±99.910
H	±200	±199.914	±199.910
X	±400	±399.914	±399.910

5.2 Output Frequency

The device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up, the output frequency can be controlled via the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The frequency output is specified by the value loaded in the DCXO register. The output frequency, F_{OUT}, is determined by the equation below, where F_{NOM} is the nominal frequency with no pull. DCXO_frac is a signed 39 bit fraction, where the most significant bit represents the sign and the remaining 38 bits represent the fraction, the total range of which is ±1.

$$Fout = (1 + DCXO\_frac \times 800e^{-6})Fnom$$

Table 3 below shows the frequency resolution versus pull range programmed.

Table 3. Frequency Resolution versus Pull Range

Programmed Pull Range	Fractional Frequency Resolution
±3.125 ppm	$5.0x10^{-14}$
±6.25 ppm	$5.0x10^{-14}$
±10 ppm	$5.0x10^{-14}$
±12.5 ppm	$5.0x10^{-14}$
±25 ppm	$5.0x10^{-14}$
±50 ppm	$5.0x10^{-14}$
±100 ppm	$5.0x10^{-14}$
±200 ppm	$5.0x10^{-14}$
±400 ppm	$5.0x10^{-14}$

The ppm frequency offset is specified by the 39 bit DCXO frequency control word in two's complement format as described in the I²C Register Descriptions. The power up default value is 000000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to 0x0E[15:9] (Least Significant Word), 0x0D[22:7] (Next Significant Word) and 0x0C (Most Significant Word). The LSW value should be written first followed by NSW and finally the MSW value; the frequency change is initiated after the MSW value is written.

Figure 3 shows how the two's complement signed value of the frequency control word sets the output frequency within the ±800 ppm full pull range. To set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, convert to two's complement binary, and then write these values to the frequency control registers.

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	011	1111	1111	1111	1111	1111	1111	1111	1111	1111
Decimal	(2^38)-1 = 274,877,906,943									
ppm	+800ppm									

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	000	0000	0000	0000	0000	0000	0000	0000	0000	0000
Decimal	0									
ppm	0ppm									

Bits	38:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Hex	100	0000	0000	0000	0000	0000	0000	0000	0000	0000
Decimal	(2^38) = -274,877,906,944									
ppm	-800ppm									

Figure 3: Frequency Control Word

The following formula generates the control word value:

Control word value = RND((2^{38}-1) × ppm shift from nominal/800ppm), where RND is the rounding function which rounds the number to the nearest whole number.

3 examples follow. Examples 1 and 2 cover the case where DCXO_Clip=0. In this case the full pull range is ±800 ppm. Example 3 shows how the DCXO_Clip factory setting is used to reduce the max pull range.

Example 1:

- Default Output Frequency = 19.2 MHz
- Desired Output Frequency = 19.201728 MHz (+90 ppm)

2^{38}-1 corresponds to +800 ppm, and the fractional value required for +90 ppm can be calculated as follows.

- 90 ppm / 800 ppm × (2^{38}-1) = 30,923,764,531.0875.

Rounding to the nearest whole number yields 30,923,764,531 and converting to two's complement gives a binary value of, 0111 0011 0011 0011 0011 0011 0011 0011 0011 or 733333333 in hex.

In general, the max pull range is calculated using the below relation.

Equation 1: MaxDCOCXOpull = +/-(800ppm*(DCXO_Clip/(2^13))).

The only exception is when DCXO_Clip=0. In this case, the DCOCXO pull range is ±800 ppm.

Example 2:

- Default Output Frequency = 10 MHz
- Desired Output Frequency = 9.9995 MHz (-50 ppm)

Following the formula shown above,

- (-50 ppm / 800 ppm) × (2^{38}) = -17,179,869,184.

Converting this to two's complement binary results in -1*(000 0100 0000 0000 0000 0000 0000 0000 0000 0000) = 111 1100 0000 0000 0000 0000 0000 0000 0000 0000, or 3C00000000 in hex. The negative number is represented as a 2's complement.

Since the DCXO_Clip value is 0 the DCOCXO pull range is ±800 ppm.

Example 3:

In this final example let's look at the case when the max pull range is factory set to 200 ppm. Now the DCXO_Clip value will be set at shown below. Solving Equation 1 from Example 1 and rounding gives:

Equation 2- $$DCXO_{Clip} = RND(2^{13} \cdot \left(\frac{MaxDCXOPull}{800ppm}\right)) = 2048$$

Converting 2048 into binary gives, 0100000000000. This is the value that will be read from register 0x00. The formula to calculate the FCW for a given desired ppm offset remains the same. So the FCW for 90 ppm is still calculated as in Example 1 and is the two's complement value 0111 0011 0011 0011 0011 0011 0011 0011 0011 or 733333333 in hex. Negative values are still calculated as in Example 2. This means the DCXO_Clip value does not change the DCOCXO slope. It only changes the DCOCXO saturation point. This is illustrated in Figure 4 below.

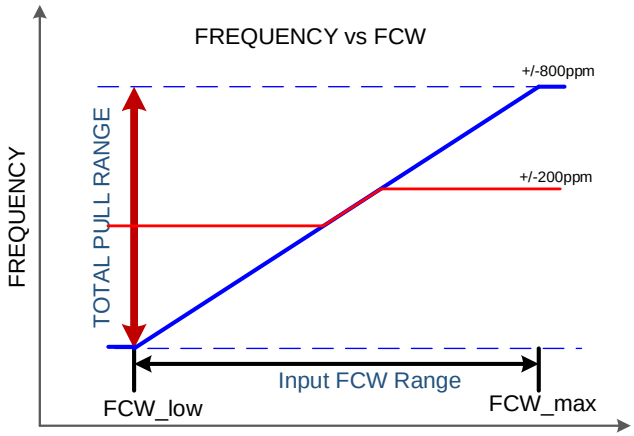

Figure 4: DCXO_Clip Illustration

It is important to note that the maximum digital control update rate is 1000 kHz for the I^2C interface and 5000 kHz for the SPI interface. For faster update rates, contact SiTime.

Table 4: Revision History

Version	Release Date	Change Summary
0.2	8-Mar-2023	Updated DCOCXO description
0.21	2-May-2023	Updated maximum control update rate
0.22	13-Jun-2023	Updated DCXO_Clip Register Address
0.23	16-Jun-2023	Updated sections 3 and 4
0.24	16-Jun-2023	Updated register table
0.25	26-Jun-2023	Updated section 3, register read minimum refresh time, 50ms
0.26	9-Aug-2023	Updated section 5
0.27	16-Aug-2023	Included SiT71xx family
0.28	16-Oct-2023	Updated Section 2 and added SPI details