LG580P (03)

Reference Design

GNSS Module Series

Version: 1.0.0

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Status: Preliminary

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About the Document

Document Information	
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Revision History

Version	Date	Description
-	2024-10-08	Creation of the document
1.0.0	2024-10-11	Preliminary

Contents

1 Reference Design

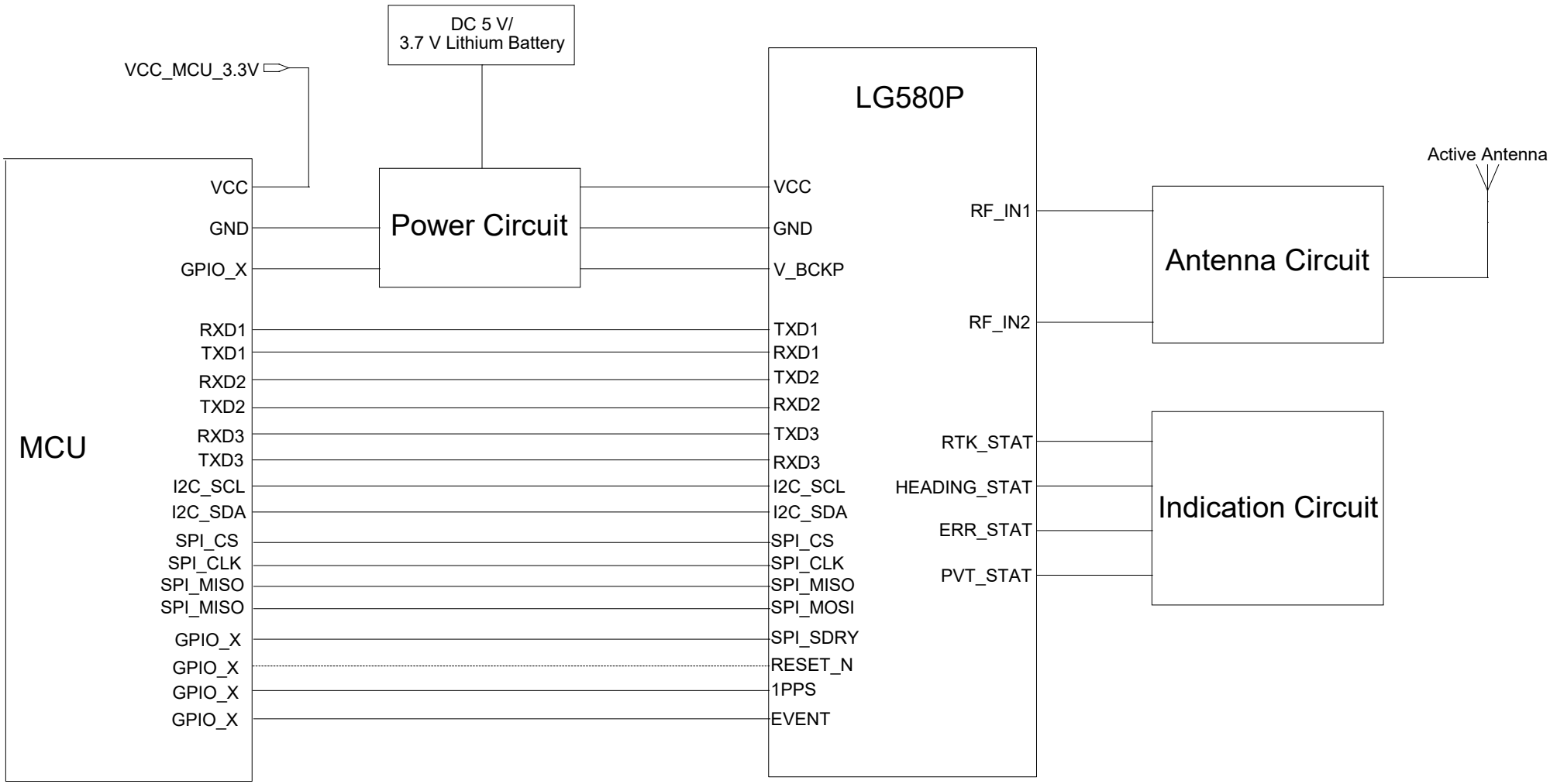
1.1. Introduction

This document provides the reference design of Quectel LG580P (03) GNSS module, including the design of block diagram, MCU circuit and power supply, module interfaces and antenna interface.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



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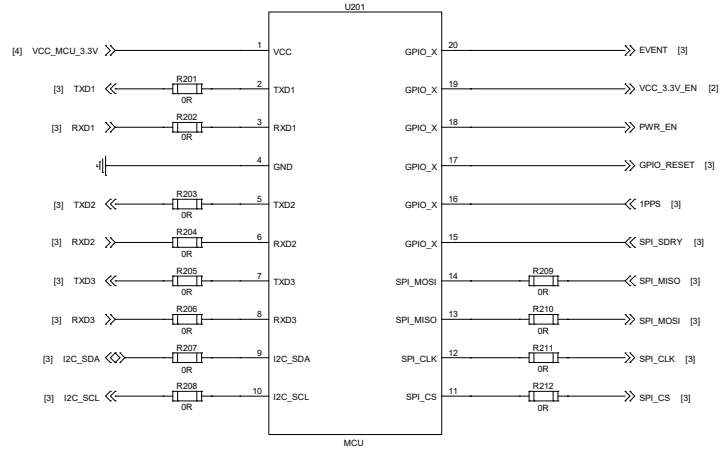
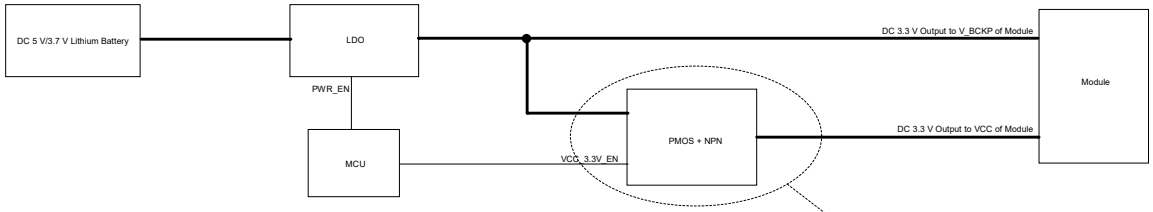
MCU Circuit and Power Supply

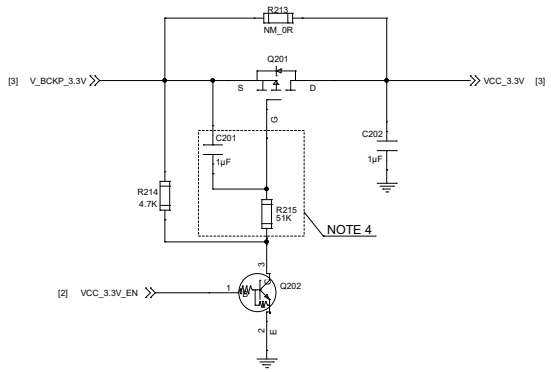
MCU Circuit



Power Supply Circuit



VCC Power Supply Control Circuit



NOTE:
1. Ensure the power supply is controlled by MCU to save power or restart the module when the module enters abnormal state.
2. The VCC should be controlled by the MCU and the V_BCKP should always be powered if hot (warm) start is needed.
3. Select the appropriate lithium battery capacity according to the power consumption of the GNSS module.
4. C201 and R215 form a soft start circuit. The capacitance (C201) and resistance (R215) can be adjusted to set the soft start time according to your requirement.

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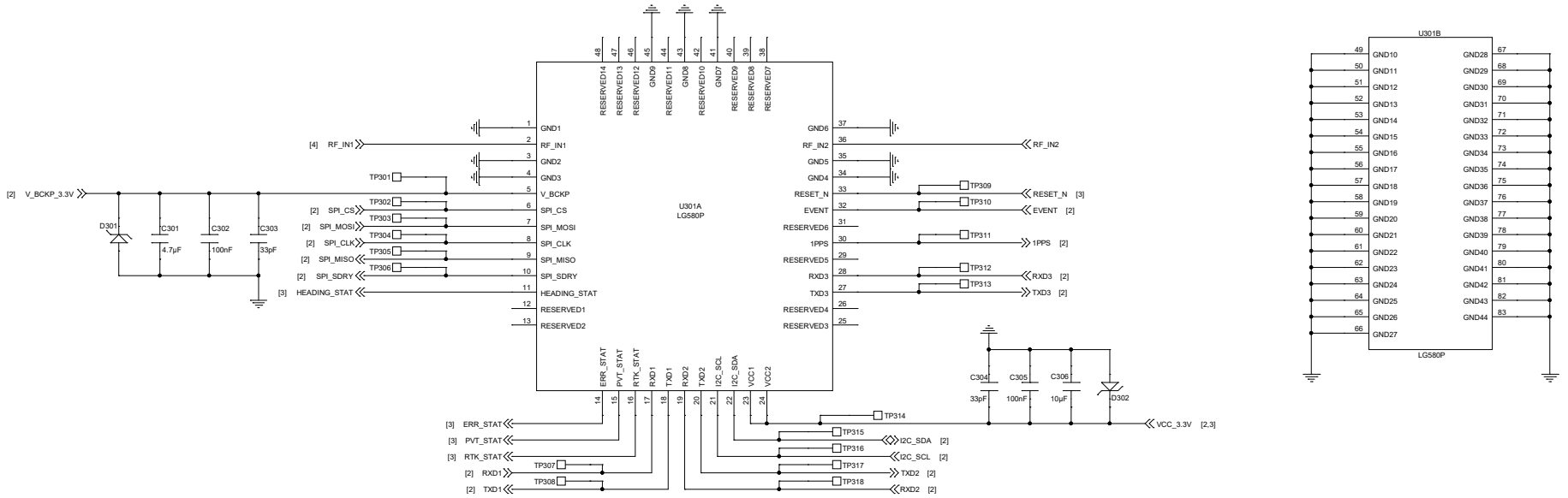
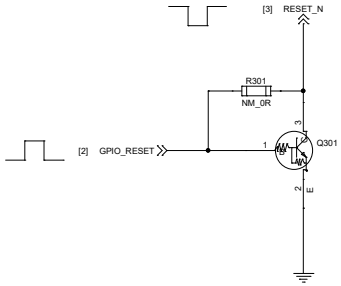
Module Interfaces

Module Interfaces



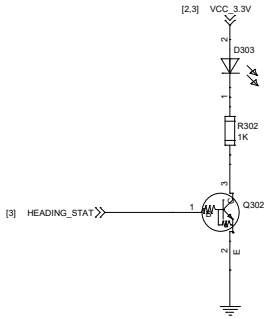
NOTE:
1. The I2C interface has been pulled up internally and does not need to be pulled up externally.
2. The power supply design must meet the sequence requirements in hardware design. See the hardware design document for details.
3. A level-shifting circuit must be used when the I/O voltage of MCU is not matched with that of module.
   Recommended level-shifting chip: SN74AVC4T245. Level-shifting chips with series resistors such as TXB series are not recomended.
4. Reserve test points for debugging the module.

RESET_N Circuit



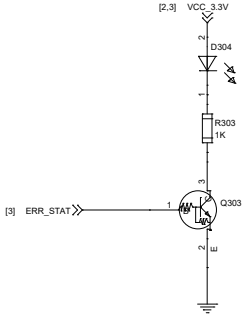
NOTE:
1. The RESET_N pin is internally pulled up to VCC with a 20 kΩ resistor, thus no external pull-up circuit is allowed for this pin. An OC drive circuit is recommended to control the RESET_N pin;
2. The RESET_N must be connected so that it can be used to reset the module if the module enters an abnormal state.

HEADING_STAT Circuit



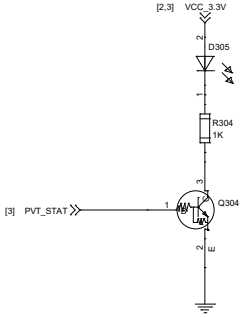
NOTE:
If the HEADING_STAT pin outputs a high level, it indicates that the module enters the HEADING fixed mode.
If the pin outputs a low level, it indicates that the module exits the HEADING fixed mode.

ERR_STAT Circuit



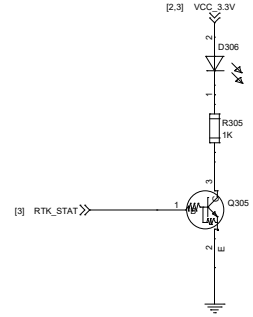
NOTE:
If the ERR_STAT pin outputs a high level, it indicates that the module is successfully initialized;
If the pin outputs a low level, it indicates that the module initialization failed.

PVT_STAT Circuit



NOTE:
If the PVT_STAT outputs a high level, it indicates that the module enters the PVT mode;
If the pin outputs a low level, it indicates that the module exits the PVT mode.

RTK_STAT Circuit



NOTE:
If the RTK_STAT outputs a high level, it indicates that the module enters the RTK fixed mode;
If the pin outputs a low level, it indicates that the module exits the RTK fixed mode;
If the pin outputs blink, it indicates that the module receives correct RTCM message and is not in RTK fixed mode.

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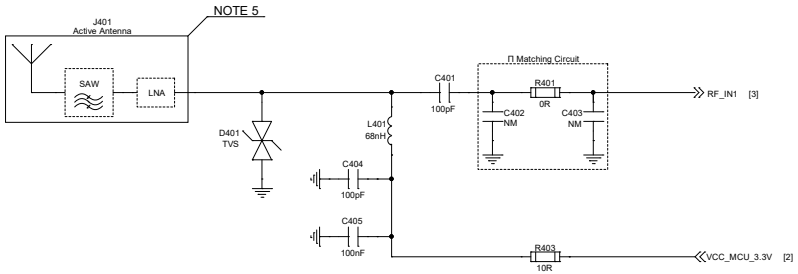
Antenna Interface



NOTE:
1. R401, C402 and C403 form a Π matching circuit for antenna impedance matching. By default, R401 is 0 Ω, C402 and C403 are not mounted.
2. D401 is an electrostatic discharge (ESD) protection device to protect RF components inside the module from the damage caused by ESD through the antenna inrterface.
3. The impedance of the RF trace line on the main PCB should be controlled to 50 Ω and the trace length should be kept as short as possible.
4. L401 is used for preventing the RF signal from leaking into the VDD_RF and preventing noise propagation from the VDD_RF to the antenna.
5. To further mitigate the impact of out-of-band signals on GNSS module performance, you must choose the active antenna whose SAW filter is placed in front of the LNA in the internal framework. DO NOT place the LNA in the front.
6. RF_IN2 pin circuit and antenna selection is consistent with RF_IN1 pin.
7. See the hardware design document for details.
8. The passive antenna is not recommended.

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