

# Simulating Valleytronics Logic at Gate Level

## A C++ Library and Example for Building Fully Electric Valleytronic Processors

T. Jacovich<sup>1</sup>

<sup>1</sup>Department of Physics  
The George Washington University

ECE 6120: Advanced Microarchitecture Final Presentation

# Introduction to Valleytronics

Simulating  
Valleytronics  
Logic at the  
Gate Level

Author

Introduction

What is Valleytronics

Warning: Quantum  
Physics

Reversible  
Logic

Tamper-Evident  
Processing

- Valleytronics is an alternative to CMOS logic that takes advantage a unique property of certain classes of semi-metals.
- It is the subject of active research, with isolated circuits being produced, but large-scale production still a few years off.

# Valleytronics vs. CMOS

Simulating  
Valleytronics  
Logic at the  
Gate Level

Author

Introduction

What is Valleytronics

Warning: Quantum  
Physics

Reversible  
Logic

Tamper-Evident  
Processing

CMOS logic takes advantage of the Pauli Exclusion principle to create diodes and transistors. These allow easy voltage manipulation, but no additional constraints. Valleytronics offers a

- 
- Encryption/Decryption of Off-Chip Memory
- Secure Context Manager

# Reversible Logic

## The Landauer Limit and Beyond

Simulating  
Valleytronics  
Logic at the  
Gate Level

Author

Introduction

What is Valleytronics

Warning: Quantum  
Physics

Reversible  
Logic

Tamper-Evident  
Processing

# Tamper-Evident Processing

Simulating  
Valleytronics  
Logic at the  
Gate Level

Author

Introduction

What is Valleytronics

Warning: Quantum  
Physics

Reversible  
Logic

Tamper-Evident  
Processing

Verifiable computations need a way to identify and prevent operations from being tampered with.