- Setup time t_{setup}: time before clock edge that data must be stable.
- Hold time t_{hold}: time after clock edge that data must be stable.
- Propagation delay t_{pcq}: time after clock edge that output is guaranteed to be stable.
- Contamination delay t_{ccq}: time after clock edge that output might be unstable.

$$T_{clk} \geq t_{pcq} + t_{pd} + t_{setup} \text{ Setup Time Constraint} \tag{1}$$

$$t_{hold} < t_{ccq} + t_{cd} \text{ Hold Time Constraint} \tag{2}$$