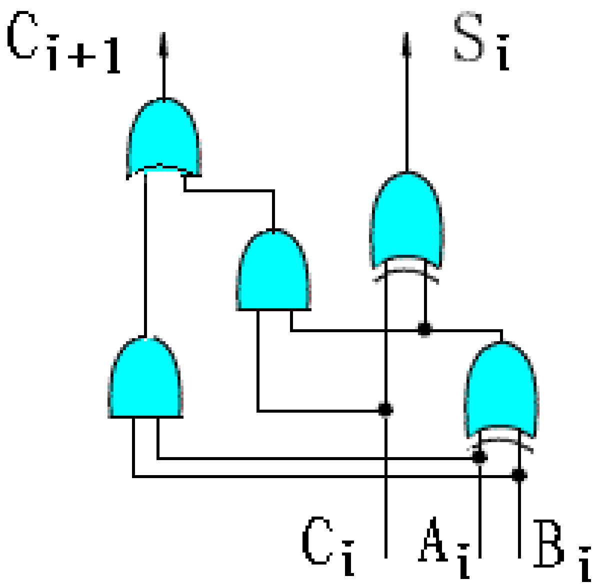
可控加、减法器的原理

1、1位加法器

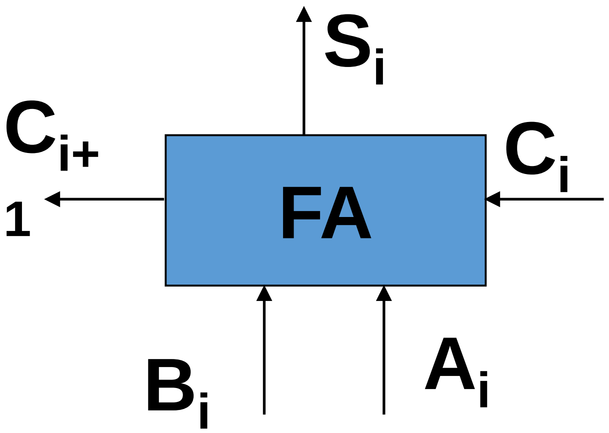
$$S_i = A_i \oplus B_i \oplus C_i$$

$$C_{i+1} = A_iB_i + (A_i \oplus B_i) C_i$$

输入			输出	
A_i	B_i	C_i	S_i	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



一位全加器FA逻辑电路图

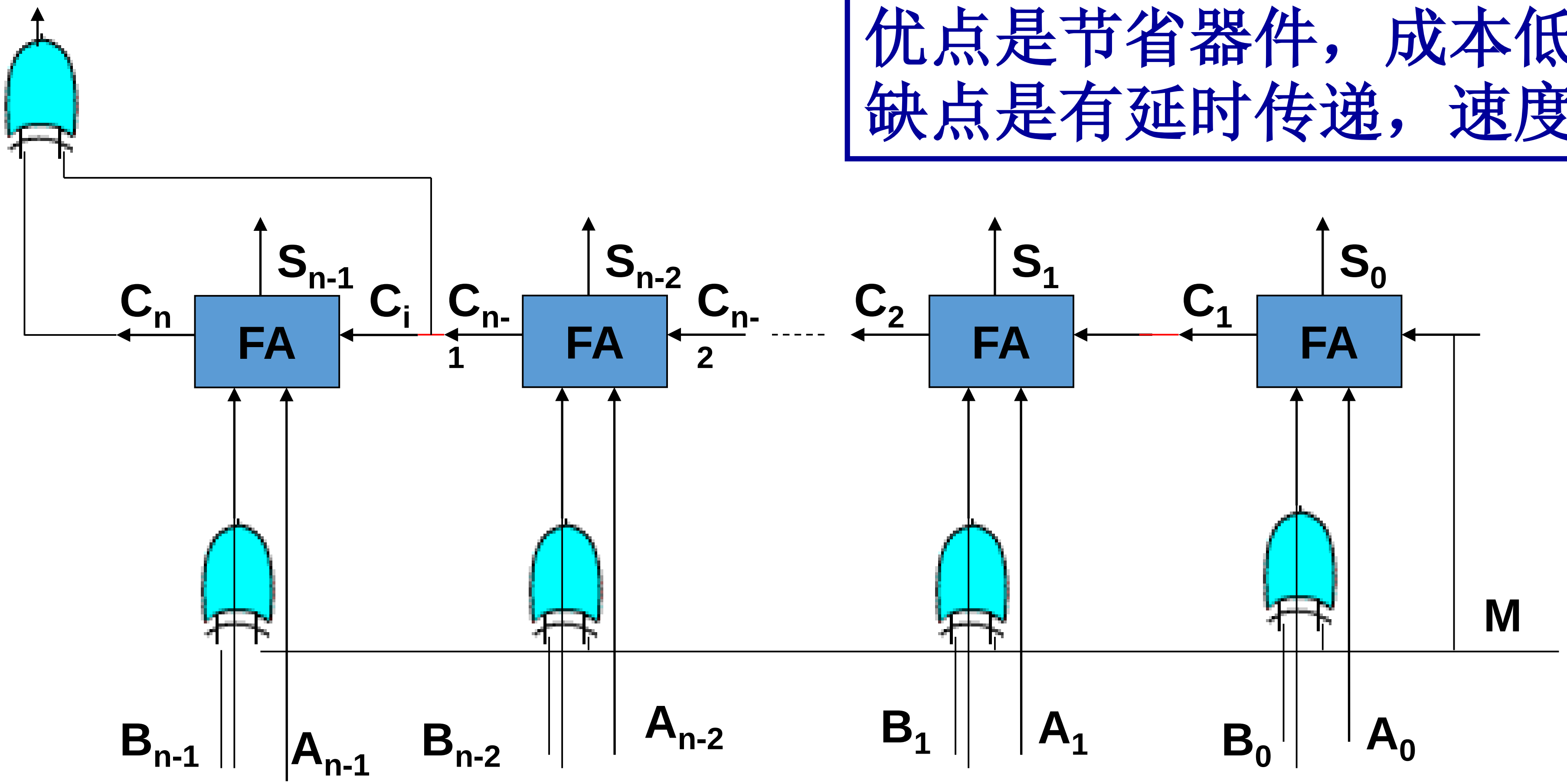


一位全加器FA封装外观

2、n位可控的加法器

- n位加法器可由多个1位加法器级联实现（行波进位加法器）。
- 补码减法器可由加法器实现。控制线M，0表示加，1表示减。

优点是节省器件，成本低，
缺点是有延时传递，速度慢



4位先行进位的原理

设相加的两个n位操作数为:

$$A = A_{n-1}A_{n-2}\cdots A_i\cdots A_0$$

$$B = B_{n-1}B_{n-2}\cdots B_i\cdots B_0$$

进位为：$C_{i+1} = A_iB_i + (A_i \oplus B_i)C_i$

设： $G_i = A_iB_i$ 进位发生输出信号

$P_i = A_i \oplus B_i$ 进位传送输出信号

则： $C_{i+1} = G_i + P_iC_i$

提高运算的速度，关键在于如何加快进位的传递

$$C_{i+1} = G_i + P_i C_i \qquad G_i = A_i B_i$$

$$P_i = A_i \oplus B_i$$

计算出C_0后，C_{i+1}的求解不再依赖于C_i

$$C_1 = G_0 + P_0 C_0$$

$$C_2 = G_1 + P_1 C_1$$

$$= G_1 + P_1 (G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 (G_1 + P_1 (G_0 + P_0 C_0))$$

$$= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$$

$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 (G_2 + P_2 (G_1 + P_1 (G_0 + P_1 (G_0 + P_0 C_0))))$$

$$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$$

并行进位（先行进位、同时进位）的逻辑表达式

$C_1= G_0+P_0C_0$ $\overline{\overline{C_1}} = \overline{\overline{G_0 + P_0C_0}} = \overline{\overline{G_0}\,\overline{P_0} + \overline{G_0}\,\overline{C_0}}$

$C_2= G_1+P_1G_0+P_1P_0C_0$

$C_3= G_2+P_2G_1+P_2P_1G_0+P_2P_1P_0C_0$

$C_4= G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0+P_3P_2P_1P_0C_0 = G'_0+P'_0C_0$