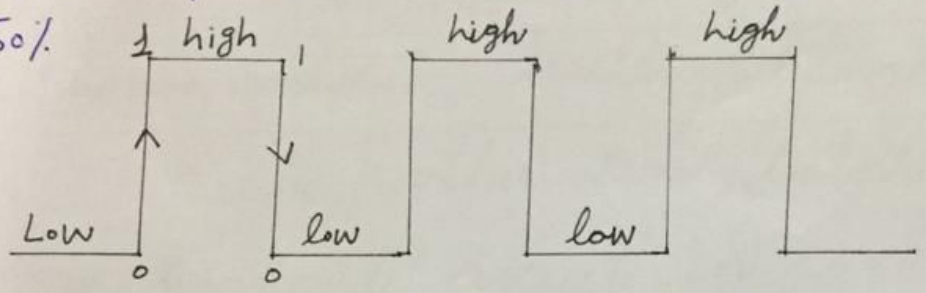
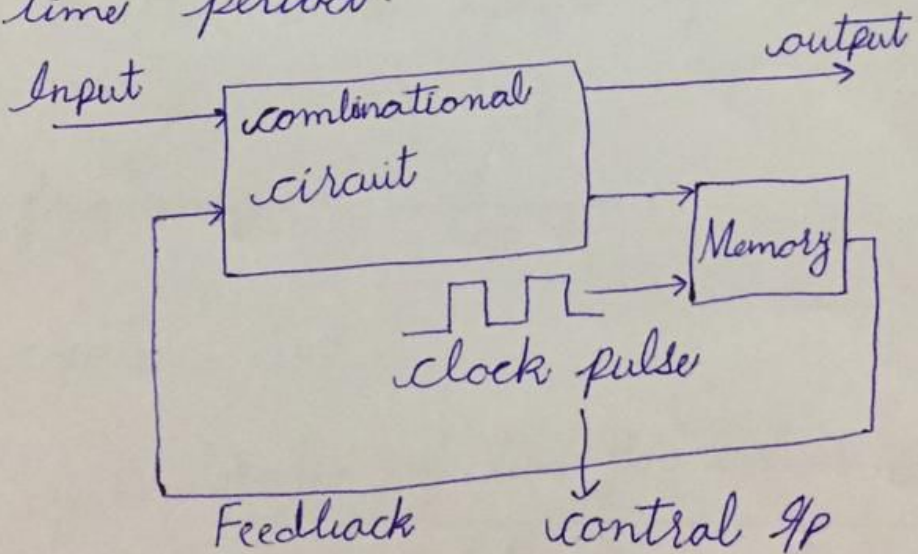
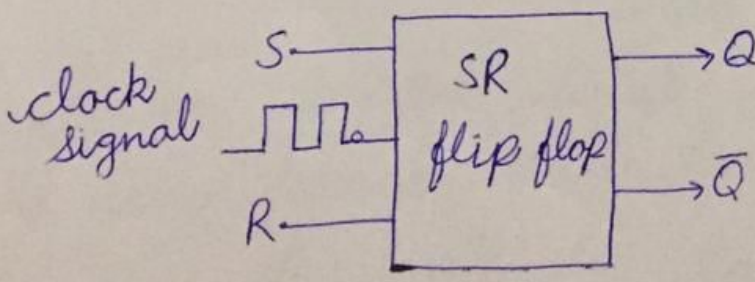
Clock and triggering methods

→ Clock signal is a timing signal.
→ It is used to provide sequence of the clock.
→ Clock is a rectangular signal called clock pulse with duty cycle equal to 50%.



0→1 called leading edge.
1→0 called trailing edge.
time required to complete one cycle is called time period.





→ This is the basic difference between latch and flip flop as latch work without clock signal but flip flop work with clock signal. Flip flop are synchronous circuits means when input changes then clock signal decides either output will change or not.

→ On the other side latch is the asynchronous circuit in which output will change according to the input.

→ So by varying the clock frequency we can control the speed of the circuit.

$$\text{clock frequency} = \frac{1}{T}$$

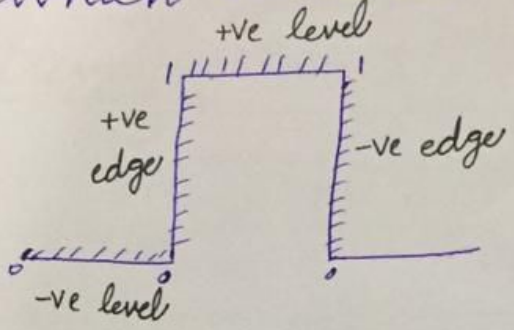
Duty cycle = 50%.

$$\text{Duty cycle} = \frac{\text{ratio of time for which signal high}}{\text{total time}}$$

→ If we suppose total time t then half time signal will be high and for half time it will be low.

Duty cycle = $\frac{t/2}{t} = \frac{1}{2} = 50\%$

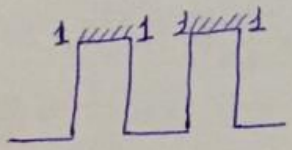
→ Now talk about triggering methods but first of all we see the clock signal which consists of four parts.

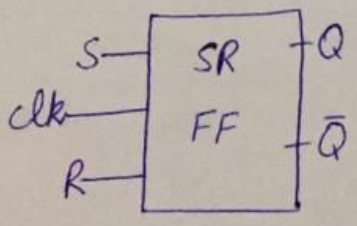


Triggering methods

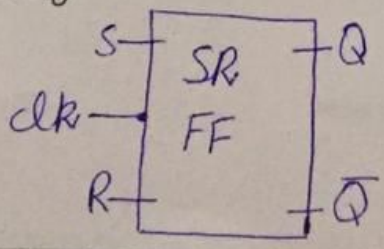
- level triggering
  - +Ve level
  - -Ve level
- edge triggering
  - +Ve edge
  - -Ve edge

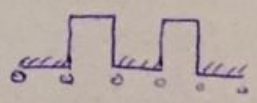
+Ve level triggering



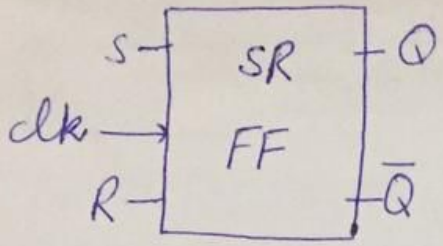


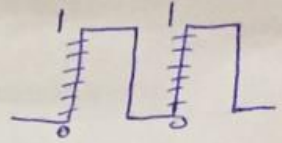
-Ve level triggering



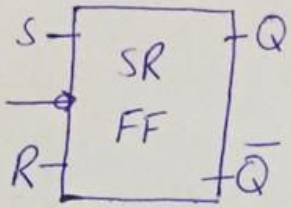


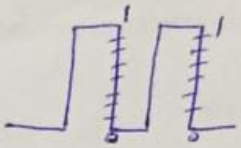
+Ve edge triggering



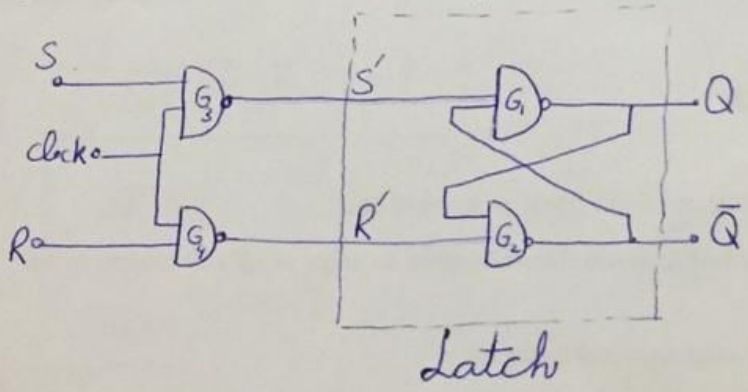


-Ve edge triggering





SR Flip flop



$S' = \overline{\bar{S} \cdot clk}$

$S' = \bar{S} + \overline{clk} \longrightarrow (1)$

$R' = \overline{R \cdot clk}$

$R' = \bar{R} + \overline{clk} \longrightarrow (2)$

case 1

Initially clk is at zero

$S' = \bar{S} + 1 = 1$

$R' = \bar{R} + 1 = 1$

Truth table for SR latch with NAND gates

S'	R'	Q	$\overline{Q}$
0	0	NOT used	
0	1	1	0
1	0	0	1
1	1	Previous state (Memory)	

NAND gate

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Truth table of SR flip flop

clk	S	R	Q	$\overline{Q}$
0	X	X	Previous state (Memory)	
1	0	0	previous state	
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	

case 2

clk = 1

$$\begin{bmatrix} S' = \overline{S} + 0 = \overline{S} \\ R' = \overline{R} + 0 = \overline{R} \end{bmatrix}$$

i) S = 0, R = 0
S' = 1, R' = 1

ii) S = 0, R = 1
S' = 1, R' = 0

iii) S = 1, R = 0
S' = 0, R' = 1

iv) S = 1, R = 1
S' = 0, R' = 0

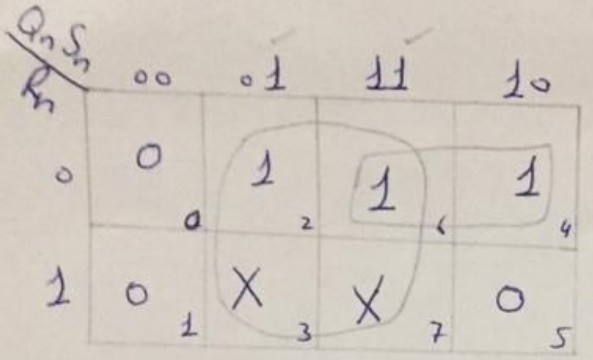
Characterstic equation for SR FF:-

Truth table of SRFF

clk	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0 Reset
1	1	0	1 set
1	1	1	Invalid

charstic table

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X



$$Q_{n+1} = S_n + Q_n \overline{R_n}$$

Excitation table for SR FF

Present state	Next state	I/Ps	
Q_n	Q_{n+1}	S_n	R_n
0	0	0 / 0	0 / 1
0	1	1	0
1	0	0	1
1	1	0 / 1	0 / 0

Timing Analysis of SRFF