

₁ Deep Underground Neutrino Experiment (DUNE)

₂ Technical Proposal

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₄ Volume 3: *The Dual-Phase Far Detector*

₅ May 10, 2018

Contents

1	Contents	i
2	List of Figures	ii
3	List of Tables	iii
4		
5	1 TPC Electronics	2
6	1.1 TPC Electronics System Overview	2
7	1.1.1 Introduction	2
8	1.1.2 Design Considerations	4
9	1.1.3 Scope	6
10	1.2 TPC Electronics System Design	7
11	1.2.1 Cryogenic Analog Front-end Electronics	9
12	1.2.2 Signal Feedthrough Chimneys	12
13	1.2.3 Digital Advanced Mezzanine Card Electronics for Charge Readout	14
14	1.2.4 Electronics for Light Readout	15
15	1.2.5 Network-based μTCA Architecture	19
16	1.2.6 Timing Distribution	21
17	1.3 Production and Quality Assurance	22
18	1.3.1 Cryogenic Analog FE Electronics	22
19	1.3.2 Signal Feedthrough Chimneys	23
20	1.3.3 The Timing System and μTCA	23
21	1.3.4 Charge Readout Electronics	23
22	1.3.5 Light Readout Electronics	24
23	1.4 Interfaces	24
24	1.4.1 Electronics System to charge-readout plane (CRP) and Photon Detection Systems	25
25	1.4.2 Electronics System to DAQ System	26
26	1.4.3 Electronics System to Cryostat and Cryogenics	27
27	1.4.4 Electronics System to Slow Control System	28
28	1.5 Transport and Handling	28
29	1.6 Installation, Integration and Commissioning	28
30	1.6.1 SFT Chimneys	29
31	1.6.2 Digital μTCA Crates	29
1	1.6.3 Integration within the DAQ	29
2	1.6.4 Integration with the Photon Detection System	30
3	1.6.5 Comissioning	30

4	1.7	Risks and Vulnerabilities	30
5	1.8	Organization and Management	31
6	1.8.1	Dual-Phase TPC Electronics Consortium Organization	31
7	1.8.2	Planning Assumptions	32
8	1.8.3	WBS and Responsibilities	32
9	1.8.4	High-level Cost and Schedule	32
10	2	Photon Detection System	34
11	2.1	Photon Calibration System	34
12	2.1.1	System Design and Procurement	34
13	2.1.2	Validation Tests	35
14	2.2	Photon Detector Performance	36
1	2.2.1	Simulations	38
2	2.2.2	Light Data in DP Prototypes	43
3	2.2.3	Simulation of Physics Events	43
4	2.3	Photon Detector Operations	45
5	2.3.1	Trigger Strategy	45
6	2.3.2	Data Quality Monitoring	46
7	2.4	Interfaces	46
1	2.5	Installation, Integration and Commissioning	48
2	2.5.1	Transport and Handling	48
3	2.5.2	Integration and Testing Facility Operations	48
1	2.5.3	Underground Installation and Integration	49
1	2.5.4	Commissioning	49
2	2.6	Quality Control	49
3	2.6.1	Production and Assembly	49
4	2.6.2	Post-Factory Installation	50
5	2.7	Safety	51
6	2.8	Management and Organization	51
7	2.8.1	Consortium Organization	51
8	2.8.2	Planning Assumptions	52
9	2.8.3	WBS and Responsibilities	53
10	2.8.4	High-Level Cost and Schedule	54

¹² List of Figures

13	1.1	Schematic layout of the dual-phase (DP) charge readout (CRO) sub-system	3
14	1.2	Schematic layout of the DP light readout (LRO) sub-system	4
15	1.3	Top corner view of DP module	8
16	1.4	Cryogenic front-end (FE) ASIC properties	9
17	1.5	Image of an analog FE card mounted on the extraction blade	10
18	1.6	Noise measurements in the WA105 DP demonstrator in different conditions	11
19	1.7	Details of the signal feedthrough chimney (SFT chimney) design	12
20	1.8	signal feedthrough (SFT) chimney cold flange	13
21	1.9	Block diagram of advanced mezzanine card (AMC)	15
22	1.10	Block diagram of LRO	16
23	1.11	Photo of prototype LRO card	16
24	1.12	CATIROC ASIC	18
25	1.13	Instrumented Micro Telecommunications Computing Architecture (μ TCA) crate from the WA105 DP demonstrator	20
1	1.14	Picture of White Rabbit (WR) slave node card	21
2	1.15	Architecture of WR network	22
3	1.16	Images of the WA105 DP demonstrator SFT cold feedthrough	25
4	1.17	Details of SFT chimney interface to the cryostat structure	27
5	2.1	Diagram of the photon calibration system to be implemented in ProtoDUNE-DP.	35
6	2.2	A sketch depicting the mechanism of light production in argon.	36
7	2.3	Landau fits of the travel time distributions for a sources close to and far from the photomultiplier tube (PMT).	39
8	2.4	Evolution of the visibility seen by a central PMT	40
9	2.5	Evolution of the visibility and peak time as a function of source-PMT distance (preliminary)	41
10	2.6	Light yield in terms of photoelectron/MeV summed over all PMTs	42
11	2.7	Averaged waveform of the S1 light signal taken with one PMT from the WA105 DP demonstrator	43
12	2.8	Response for simulated supernova neutrino burst (SNB) neutrino interactions (ProtoDUNE- DP geometry)	44
13	2.9	Response for simulated nucleon decays (ProtoDUNE-DP geometry)	45

¹⁸ List of Tables

19	1.1	Parameters for the TPC electronics system design	6
20	1.2	Numbers for DP electronics components to procure	7
21	1.3	Summary of some of the principal parameters of the TPC electronics system.	9
22	1.4	Main characteristics of analog-to-digital converter (ADC) AD9257	14
23	1.5	Main characteristics of ADC AD9249	17
24	1.6	Main characteristics of CATIROC.	19
1	1.7	Bandwidth requirements per μ TCA crate.	20
2	1.8	Interface documents relevant to DP TPC electronics system	25
3	1.9	DP TPC electronics consortium current participants	31
4	1.10	DP TPC electronics consortium key milestones	33
5	1.11	DP TPC electronics consortium schedule	33
6	2.1	Default optical parameters chosen for the light simulation methods	37
7	2.2	DP photon detector (PD) interface documents	47
8	2.3	DP PD consortium institutions	52
9	2.4	Pre-technical design report (TDR) Key Milestones	54
10	2.5	Post-TDR Key Milestones	55

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¹² Todo list

¹³ check this one; small edits	47
¹⁴ need a ref to it?	54

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¹⁶ Chapter 1

¹⁷ TPC Electronics

tpc-elec

¹⁸ 1.1 TPC Electronics System Overview

-elec-ov

¹⁹ 1.1.1 Introduction

²⁰ The aim of the dual-phase (DP) TPC electronics is to collect and digitize the signals from the
²¹ charge-readout planes (CRPs) (see chapter ??) and photon detection systems (PDSs) (see chapter ??), which implements photomultiplier tube (PMT) tubes (PMTs). These two tasks are re-
²² spectively accomplished by the charge readout (CRO) and light readout (LRO) sub-systems. The
²³ design of the system incorporates the components already developed for ProtoDUNE-DP as a re-
²⁴ sult of an R&D activity started in 2006. One of the key objectives of this R&D program has been
¹ the design of an electronics system that is easily scalable and cost-effective in order to meet the
² needs of the large-scale neutrino liquid argon (LAr) detector.

⁴ While a single DP module has a factor of 20 more readout (both charge and light) channels than
⁵ ProtoDUNE-DP, a simple scaling of the number of the components used in the prototype design
⁶ is sufficient to meet these needs without necessitating any additional R&D. A small-scale version
⁷ of the TPC electronics system was used in the WA105 DP demonstrator at CERN, a preliminary
⁸ DP LArTPC prototype with an active volume of $3 \times 1 \times 1 \text{ m}^3$ (CRP area of $3 \times 1 \text{ m}^2$) that took
⁹ data in the summer-fall of 2017. Operation of the WA105 DP demonstrator validated the design
¹⁰ choices and provided checks on various performance markers, e.g., noise.

¹¹ The CRO electronics system, illustrated in the Figure 1.1, is designed to provide continuous, non-
¹² zero-suppressed, and losslessly compressed digital signals by reading the charge collected on the
¹³ CRPs' 3 m long strips that are arranged in two collection views, all with a pitch of 3.125 mm. The
¹⁴ system consists of the front-end (FE) analog electronics operating at cryogenic temperatures and
¹⁵ digital electronics working in the warm environment outside of the cryostat. The cryogenic FE
¹⁶ analog electronics is based on an application-specific integrated circuit (ASIC) chip with a large
¹⁷ dynamic range (up to 1200 fC) to cope with the charge amplification in the CRPs. The analog

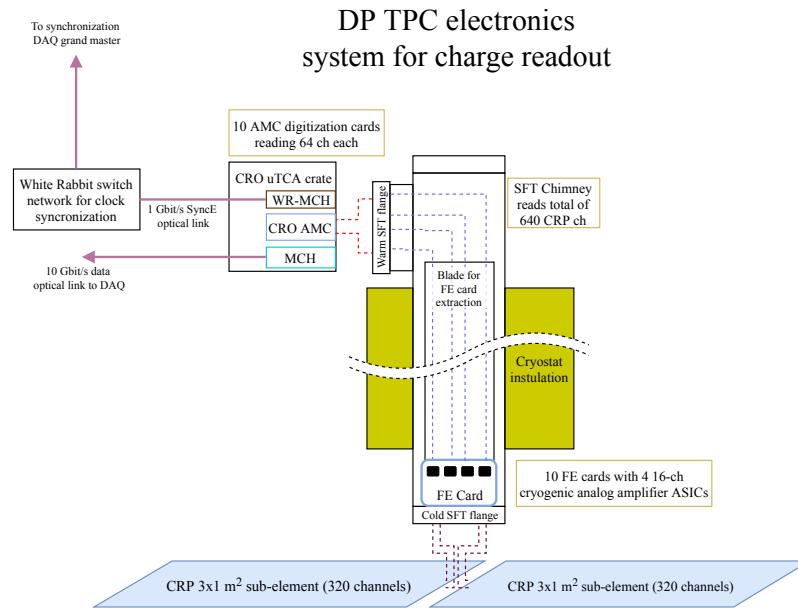


Figure 1.1: Schematic layout of the DP CRO sub-system.

fig:dpel

18 FE cards are housed in dedicated signal feedthrough chimneys (SFT chimneys) and are accessible
 19 from the outside even after the DP module is in operation, thus removing any significant risks
 20 associated with their long-term survivability. The SFT chimneys are approximately 2.3 m long
 21 stainless steel pipes that traverse the entire insulation layer of the cryostat allowing placement of
 22 the FE electronics close to the CRPs to minimize cable capacitance (noise). In addition, their
 23 metallic structure shields the FE cards from any interference from the warm digital electronics
 24 and ambient environment. The analog signals are digitized by Advanced Mezzanine Cards ad-
 25 vanced mezzanine cards (AMCs), which are housed in the commercial Micro Telecommunications
 26 Computing Architecture (μ TCA) crates on top of the cryostat near the SFT chimneys.

27 The CRO data are sampled at the rate of 2.5 MHz with 12 bit resolution. This frequency, tradi-
 28 tionally used in LArTPC experiments, is well matched to the 1 μ s pulse-shaping time of the FE
 29 electronics and the detector response times determined by the electron drift velocity in the LAr.
 30 The corresponding sampling resolution along the drift coordinate is better than 1 mm.

31 The LRO electronics system, illustrated in the Figure 1.1, collects and digitizes the signals from
 32 the PDS, which consists of tetra-phenyl butadiene (TPB)-coated 8 in PMTs (Hamamatsu¹ R5912-
 33 02-mod) located beneath the TPC cathode. The LRO electronics facilitates the detection of the
 34 primary scintillation signals, which provide the absolute time reference for the interaction events.
 35 It also enables recording the light signals generated by photons from the so-called *proportional*
 36 *scintillation component*, the light created by the electrons extracted and amplified in the gaseous
 37 phase. A fraction of this light can reach the PMTs after traversing the entire detector volume.
 1 The LRO electronics, consisting of analog and digital stages, is housed in the μ TCA crates on top
 2 of the cryostat structure (similar to the CRO electronics). The LRO AMC card design shares a
 3 similar architecture with the AMCs for the charge readout. The LRO μ TCA crates are connected
 4 to specific LRO signal feedthrough flanges on top of the cryostat (see chapter 2).

fig:dpel-crosystem-sketch

ch:lddp-pd

¹Hamamatsu™R5912-02-mod

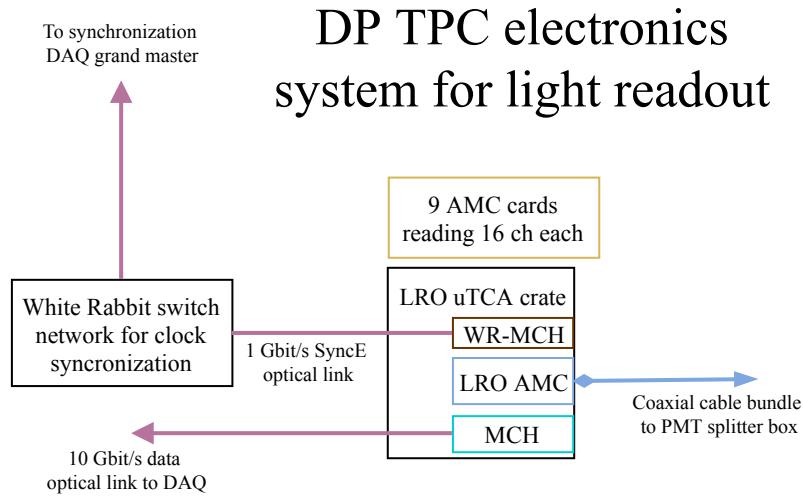


Figure 1.2: Schematic layout of the DP LRO sub-system.

fig:dpe1

- 5 Each μ TCA crate for either charge or light readout is connected to the data acquisition (DAQ)
 6 system via an optical fiber link that supports at least 10 Gbit/s. Every crate also contains a White
 7 Rabbit MicroTCA Carrier Hub (WR-MCH) for the time synchronization of the digital electronics.
 8 This timing slave unit is connected via 1 Gbit/s optical fiber to a master node that serves as
 9 a synchronization reference for all the connected slave nodes on the network. This system for
 10 the time synchronization is based on the commercially available components developed within the
 11 framework of the (White Rabbit (WR)) project with ad-hoc hardware and firmware developments.
 12 The system performs automatic and continuous self-calibrations to account for any propagation
 13 delays and is able to provide sub-ns accuracy for the timing synchronization.

¹⁴ 1.1.2 Design Considerations

- 15 The CRO electronics design covers the analog FE cards containing pre-amplifier ASICs operating
 16 at cryogenic temperatures and digitization cards with the relevant system for their synchronization
 17 working in the warm environment outside of the cryostat. The system reads and digitizes signals
 18 from a total of 153,600 channels (per one DP module) and is capable of continuously streaming
 19 the collected and losslessly compressed data to the DAQ without any zero suppression. The design
₁ of the CRO electronics system was developed to fit the following requirements:

- 2 The CRO electronics shall measure signals of up to 1200 fC without saturation; this has
 3 been optimized following Monte Carlo (MC) studies on the maximal occupancy per channel
 4 in shower events [?]. For a nominal CRP gain of 20, a minimum ionizing particle (MIP)
 5 signal is expected to be around 30 fC – the lowest limit that assumes a particle travelling
 6 horizontally with an azimuthal angle of 0 degrees – giving a maximal operational range of
 7 up to 40 MIPs.
- 8 The electronic noise in the CRO analog electronics is required to be $< 2500 \text{ e}^-$. This condition
 9 can be derived from the requirement on the minimal S/N, which should be greater than 5:1

once the charge attenuation is taken into account. Given the maximum drift distance of 12 m, the largest attenuation factor due to electro-negative impurities assuming the 3 ms (minimally required) electron lifetime and the drift field of 0.5 kV/cm is 0.08. The smallest MIP signal with the CRP effective gain of 20 is therefore 2.5 fC ($15,600 \text{ e}^-$).

- The peaking time of the FE analog amplifiers shall be 1 μs . This requirement is driven by the need for optimal vertex resolution, determined in turn by the single track resolution and the power to separate two or more tracks that are close to one another.
- The sampling frequency shall be 2.5 MHz to match the peaking time of the FE electronics.
- The power dissipated by the FE analog electronics shall be below 50 mW/channel in order to minimize the heat input to the cryostat volume.
- The FE analog electronics shall be replaceable without the risk of contaminating the main LAr volume in order to guarantee the long-term reliability of the system.
- The analog-to-digital converter (ADC) resolution shall be such that the noise is at the level of an ADC given a dynamic range wide enough to match the response of the FE amplifier. This can be achieved with a 12 bit ADC.
- The digital electronics to be placed outside of the cryostat in the warm environment shall be capable of adopting standard industrial components and solutions, to keep the costs lower and to benefit from technological evolution, e.g., higher network speeds.

As described in subsequent sections, the achieved performance of the final system is significantly better with respect to many of the listed requirements.

The magnitude of the noise also has an effect on the quality of the lossless compression of the raw data. A compression factor of about 10 is achieved with the RMS noise level below 1 ADC. To give an idea of the compression efficiency dependency on the noise level a compression factor of 4 is obtained with the noise at around 1.5 ADC.

The primary objective of the LRO system is to detect signals, from a minimum of one photoelectron on one PMT, giving a precise timestamp that can be used in conjunction with the charge signals to determine the absolute event time (T_0). Precise measurements of LRO signal charge allow the continual monitoring of the PMT gain at the single photoelectron level, and the determination of the number of photons in each scintillation event. In addition, an ADC continuously streams data, downsampled to 400 ns as for the CRO signals, which, amongst other items, allows measurements of the scintillation time profile. In addition, the LRO system reads 20 channels from reference SiPM sensors from the photon detector (PD) calibration system.

The cryogenic analog electronics for the CRO is housed in the dedicated SFT chimneys. Its design enables access to the FE card for possible replacement without risk of contaminating the pure LAr in the main cryostat volume. The chimneys possess a cooling system that can control the temperature around the FE cards to roughly 110 K to reach their optimal noise level and that compensates for the heat input from the chimneys into the cryostat volume.

2 The digital electronics for both charge and light readout is located in the warm environment on
 3 the top of the cryostat supporting structure and is therefore easily accessible. This fact removes
 4 any constraints associated with the accessibility and operation in cryogenic environments allowing
 5 for the usage of standard components and industrial solutions in the design. Digital electronics
 6 must be continuously and automatically synchronized to better than 400 ns to ensure the correct
 7 temporal alignment of the ADC samples from all of the readout channels. This is a minimal
 8 requirement dictated by the fact that the sampling rate is 2.5 MHz.

9 Key parameters for the electronics system design are summarized in Table 1.1. tab:dpele-physicsparms

Table 1.1: Parameters for the TPC electronics system design. The numbers are given for one DP module.

Parameter	Value
CRO channels	153,600
CRO continuous sampling rate	2.5 MHz
CRO ADC resolution	12 bit
CRO data compression factor	10
CRO data flow	430 Gbit/s
LRO channels	720
LRO continuous sampling rate	2.5 MHz
LRO ADC resolution	14 bit
LRO data compression factor	1
LRO data flow	24 Gbit/s

10 1.1.3 Scope

11 The scope of the TPC electronics system covers the procurement, production, testing, validation,
 12 installation, and commissioning of all the components necessary to ensure the complete readout
 13 of the charge and light signals from a given DP module. This includes:

- 1 • Cryogenic analog FE cards for charge readout;
- 2 • AMC cards for charge and light readout;
- 3 • The WR-MCH cards for AMC clock synchronization;
- 4 • μ TCA crates;
- 5 • Switches for the WR network;
- 6 • SFT chimneys;
- 7 • Low-voltage power supplies, distribution, and filtering system for the FE cards;

- 8 • Flat cables connecting the FE cards to the warm flange interface of the SFT chimneys;
- 9 • VHDCI cables connecting the warm flange interface of the SFT chimneys to AMCs.

10 The total numbers for components to be procured to instrument one DP module are given in
 11 Table 1.2

Table 1.2: Numbers for DP electronics components to procure for one DP module.

Name	Number
CRO cryogenic ASICs (16 ch)	9600
CRO cryogenic analog FE cards (64 ch)	2400
CRO AMCs	2400
SFT chimneys	240
Flat cables for SFT chimney (68 ch)	2400
Flat cables for SFT chimney (80 ch)	2400
VHDCI cables (32 ch)	4800
LRO AMCs with analog FE	45
μ TCA crates	245
WR-MCH units	245
WR switches (18 ports)	16

12 1.2 TPC Electronics System Design

13 The CRO FE analog electronics is based on cryogenic ASIC chip with a large dynamic range (up to
 14 1200 fC) to accomodate the charge amplification in the CRP. The FE cards read 64 CRP channels
 15 each. They are mounted in dedicated SFT chimneys and are located within a short distance (<1 m)
 16 from each CRP to minimize the noise caused by long cables (large cable capacitance). The cards
 17 remain accessible throughout the DP module operation. Each SFT chimney accommodates 10
 18 FE analog cards, which corresponds to the readout of 640 CRP channels per chimney. There are,
 19 therefore, 240 SFT chimneys to be installed for the charge readout in a given DP module.

20 The differential analog signals from the analog FE cards, carried by the twisted-pair ribbon cables
 21 and routed via an interface flange of the SFT chimneys, are digitized by the AMC cards located
 22 outside of the cryostat. These cards are installed in μ TCA crates placed in the immediate vicinity
 23 of the SFT chimneys (one crate per chimney). In the design for ProtoDUNE-DP, each AMC
 24 digitizes 64 channels, corresponding to reading one FE analog card. Each μ TCA contains 10
 25 AMCs reading a total of 640 channels. However, an implementation with AMCs supporting a
 26 higher channel density is being investigated for cost-reduction purposes.

1 The LRO FE analog and digital electronics is based on a custom-built AMC. The card contains
 2 a CATIROC ASIC, which is used to determine the charge and start times of signals from each
 3 individual PMT to high precision. In addition, a 14 bit 65 MHz ADC digitizes the data for contin-

4 uous streaming of the PMT signals. Each card reads up to 16 channels. A potential upgrade is to
 5 increase the channel density per card to 32 channels. The LRO cards are housed in five dedicated
 6 μ TCA crates located close to the PMT instrumentation feedthroughs.

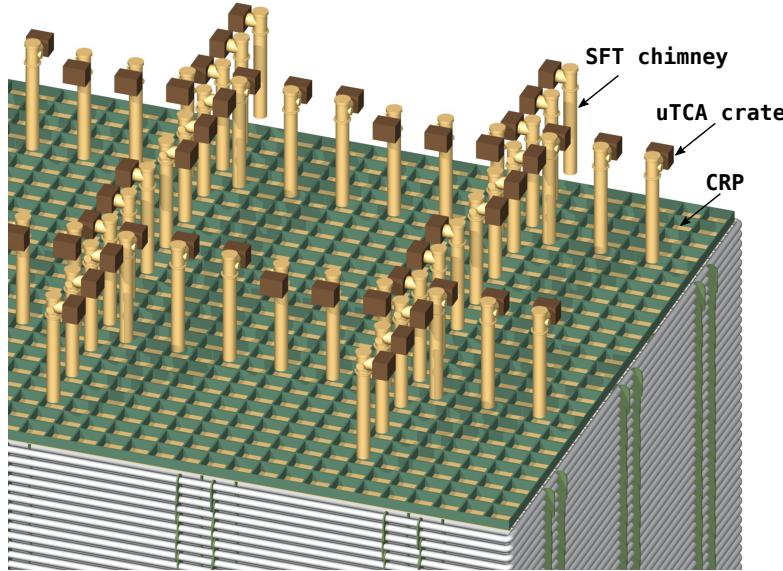


Figure 1.3: Corner view of DP module showing the pattern of the SFT chimneys and μ TCA crates for charge readout above CRPs.

7 Every μ TCA crate contains a network switch, MicroTCA Carrier Hub (MicroTCA Carrier Hub
 8 (MCH)), via which the data are sent to the DAQ and to a (WR-MCH) for time synchronization
 9 and trigger timestamp distribution to the AMCs. Both MCH and WR-MCH require one optical
 10 fiber link each.

11 The MCH switch streams the data from AMCs via a dedicated optical link. Currently ProtoDUNE-
 12 DP uses MCH operating at 10 Gbit/s. However, a move to 40 Gbit/s links for the DP module
 13 implementation is under consideration because of the technology evolution with associated cost
 14 reductions and a possible increase in the channel density of each AMC.

15 The WR-MCH time synchronization unit is based on the WR system, which provides hardware
 16 and protocols for the network-based sub-ns synchronization between a master and different slave
 17 nodes. The connection of the WR-MCH to the WR network is done via 1 Gbit/s synchronous
 18 Ethernet optical link. WR-MCH distributes the timing information for synchronization of the
 19 AMCs via the μ TCA backplane. In addition, this unit can be used to transmit triggers to the
 20 digitization units within the crate. This is achieved by sending it dedicated data packets containing
 21 trigger timestamp information.

22 [fig:dpele-sft-chimney-pattern](#)
 23 Figure 1.3 shows a corner view of the DP module illustrating the pattern of the SFT chimneys
 24 and the attached μ TCA crates above the CRPs. Each crate/SFT chimney collects signals from
 25 3 m long strips of two $1 \times 3 \text{ m}^2$ CRP segments. Each chimney completely penetrates the cryostat
 insulation layers (not shown in the figure).

26 A short summary of some of the number of principal components and channel granularity in the

fig:dpele

Table 1.3: Summary of some of the principal parameters of the TPC electronics system for charge and light readout of a DP module.

Name	Number
CRO SFT chimneys/ μ TCA crates	240
CRO channels per SFT chimney/ μ TCA crate	640
CRO cryogenic analog FE cards per SFT chimney	10
CRO AMCs per μ TCA crate	10
LRO FE cards per μ TCA crate	9
LRO channels per μ TCA crate	144
LRO μ TCA crate	5
WR-MCH per μ TCA crate	1

tab:dpele-numparts
27 design of the DP electronics is provided in Table 1.3.

28 1.2.1 Cryogenic Analog Front-end Electronics

n-cryofe
1 The cryogenic amplifier ASIC is the main component of the FE analog cards. Its design is based
2 on the CMOS 0.35 μ m technology and is an outcome of an R&D activity started in 2006, which
3 resulted in several versions of the cryogenic amplifier for both SP and DP liquid argon time-
4 projection chamber (LArTPC) detectors. Two principal versions of ASIC chips have been produced
5 for DP LArTPC operation. In the first version the amplifiers have a constant gain in the region
6 of 0 to 1200 fC (0 to 40 MIP). In the second, the amplifiers have a higher linear gain for signals
7 up to 400 fC (roughly 10 MIP signals) and a logarithmic response in the 400 to 1200 fC range.
8 This double-slope behavior is obtained by using a MOSCAP capacitor in the feedback loop of the
9 amplifier that changes its capacitance above a certain signal threshold. The aim of this solution is
10 to optimize the resolution for small charge depositions (in a few-MIP region) while preserving the
11 overall large dynamic range of the amplifier.

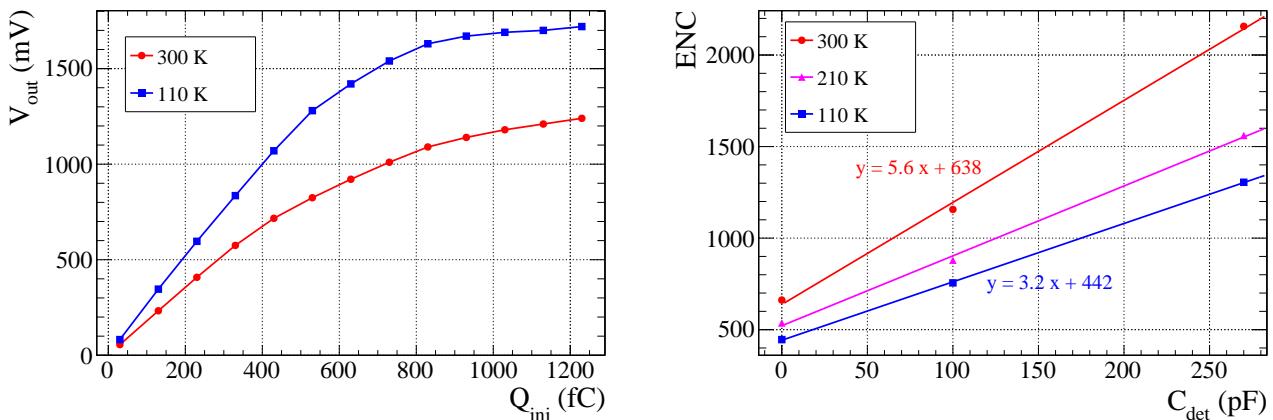


Figure 1.4: Cryogenic FE ASIC properties: amplifier response (left) and noise (right) at different temperatures measured at the output of differential buffer.

12 The ASIC version with the double-slope gain was selected for ProtoDUNE-DP and has been
 13 adopted for the DP TPC electronics design. The left plot in Figure 1.4 illustrates the response
 14 of this amplifier for different values of the injected charge, while that on the right shows the
 15 measured noise in units of Equivalent Noise Charge (ENC) as a function of the detector capacitance
 16 at different temperatures. For the CRP anode (detector) capacitance of 480 pF per 3 m strip,
 17 the expected noise is around $2000 e^-$ at 110 K. Each ASIC contains 16 amplifier channels with
 18 differential line buffers and has a power consumption, which is 11 mW/channel surpassing the
 19 <50 mW/channel requirement.

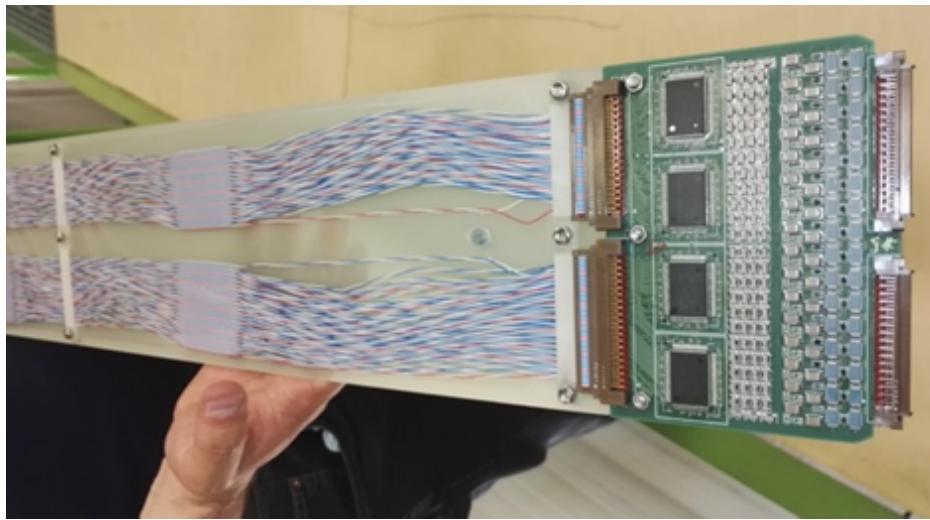


Figure 1.5: Image of an analog cryogenic FE card mounted on the extraction blade, which is a part of the SFT chimney sub-system.

20 Each cryogenic FE card, shown in Figure 1.5, holds four ASIC amplifier chips and a few passive
 1 discrete components. The input stage of each amplifier channel has a $1 G\Omega$ resistor to ground
 2 followed by a $2.2 nF$ decoupling capacitor; both are rated for high voltage (HV) operation. The
 3 resistor grounds the CRP anode strips. A TVS diode² protects each input stage against discharges
 4 coming from the DP module. This component was selected after studying the performance of
 5 different devices for the electrostatic discharge protection by subjecting them systematically to
 6 discharges of a few kV with an energy similar to that of the LEMs in the CRP. The FE cards also
 7 house the blocking capacitors for further filtering of the low-voltage power lines. These are first
 8 filtered at the level of the power supply and transported via shielded cables.

9 Although the FE amplifier ASICs are in a shielded environment provided by the chimneys, which
 10 act as Faraday cages, interference from other equipment (via a noisy ground or ground loops)
 11 could significantly worsen the noise performance from the design target. Figure 1.6 shows results
 12 of noise measurements performed under different conditions in the WA105 DP demonstrator. The
 13 channels reading 3 m (1 m) long strips correspond to negative (positive) channel numbering in the
 14 plots and the 1 ADC count is equivalent to about 900 electrons. The left plot of Figure 1.6 shows
 15 the noise measurements performed at warm temperature with and without slow control cables
 16 (CRP HV, CRP motors, level meters, temperature probes, etc.) connected. The noise is clearly
 17 affected by the grounding of the slow controls: the average value of the noise RMS is around 1.7

²Bourns™ CDSOD323-T08LC TVS diode.

fig:dpele

fig:dpele-fe-card-blade-image

fig:dpele-311-noise

fig:dpele-311-noise

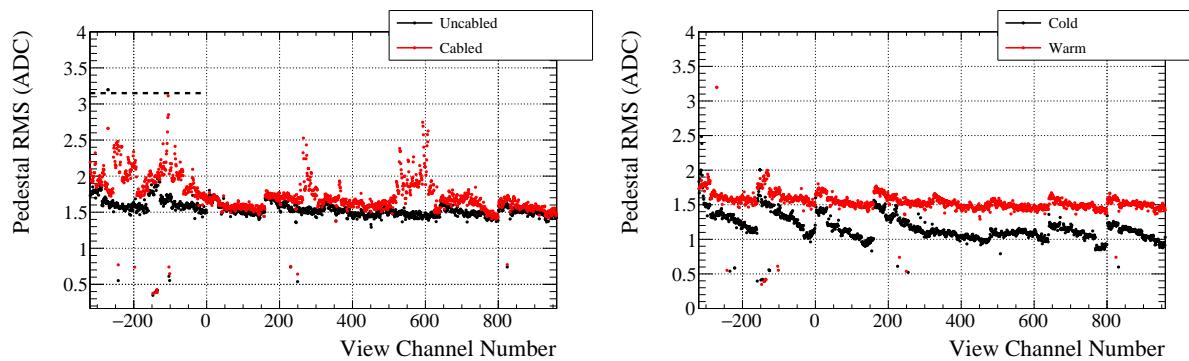


Figure 1.6: Noise of measurements in the WA105 DP demonstrator in different conditions. Left: warm with the slow control cables connected to the cryostat flanges (red points) and disconnected (black points). Right: warm (red points) and cold (black points) with the slow control cables disconnected. The channels with negative (positive) channel number correspond to the strips of 3 m (1 m).

`fig:dpel-fe-asic-prop`

18 ADC with slow control cables connected, and decreases to about 1.5 ADC when they are removed.
 19 The grounding scheme of the WA105 DP demonstrator does not correspond to the one planned
 20 for the DP module, where all electrical equipment is referred uniquely to the cryostat ground and
 21 is completely insulated from the external environment.

22 One interesting feature, particularly visible with the cables disconnected, is the similarity of the
 23 noise measured for the channels connected to the 1m and 3m long strips in the WA105 DP
 24 demonstrator. Given that the longer strips have three times the input capacitance of the shorter
 1 ones, the expected noise (see Figure 1.4) for these should be larger by about a factor of two as
 2 indicated by the dashed line in the plot. In addition, the noise on the short strips is lower than
 3 expected (1.5 ADC) for the 160 pF/m strip input capacitance (1.7 ADC). The reason for this
 4 behavior in the WA105 DP demonstrator is still under investigation. Measurements have already
 5 shown that the capacitance of the CRP anode strips is not purely to ground, but rather it is driven
 6 by the inter-strip couplings, which creates a more complicated electrical network.

7 `fig:dpel-fe-311-noise` Figure 1.6 (right) also shows a comparison of the noise measurements in the WA105 DP demon-
 8 strator taken with the FE electronics at warm (red points) and cold (black points) at around 150 K.
 9 The slow control cables were disconnected in both cases. However, the cold measurements were
 10 performed with the recirculation pump active and the cathode HV connected. The RMS noise
 11 averaged over all channels decreases by about 25% from roughly 1.5 ADC to 1.1 ADC when the
 12 FE analog cards are cold. For comparison, the expected signal for a MIP with the CRP gain of 20
 13 should be around 200 ADC counts.

14 The overall grounding principle of the WA105 DP demonstrator was based on using the cryostat as
 15 the ground reference. The low-voltage power supplies for the FE analog electronics and the μ TCA
 16 crates were powered using insulating transformers to ensure that no other ground could interfere.
 17 In contrast, the design of the slow control system did not include any insulation transformers.
 18 This equipment was grounded to the building electrical network, thereby creating an interference
 19 with the ground of the cryostat. Stricter treatment of the ground connections, as implemented for
 20 ProtoDUNE-DP and planned for the DP module, and a lower SFT chimney operating temperature
 21 of around 110 K (from 150 K) should help to further reduce the noise from the levels observed in

- ²² the WA105 DP demonstrator.

²³ 1.2.2 Signal Feedthrough Chimneys

²⁴ The SFT chimneys are designed to enable access to the FE analog electronics for a potential
²⁵ repair or exchange while the DP module is filled and in operation. In addition, their metallic
²⁶ structure acts as a Faraday cage isolating the FE ASICs from environmental interference. Each
²⁷ SFT chimney hosts 10 analog cryogenic FE cards (reading 640 channels in total). Details of the
²⁸ design are illustrated in Figure 1.7. ^{fig:dpele-sft-chimney-design}

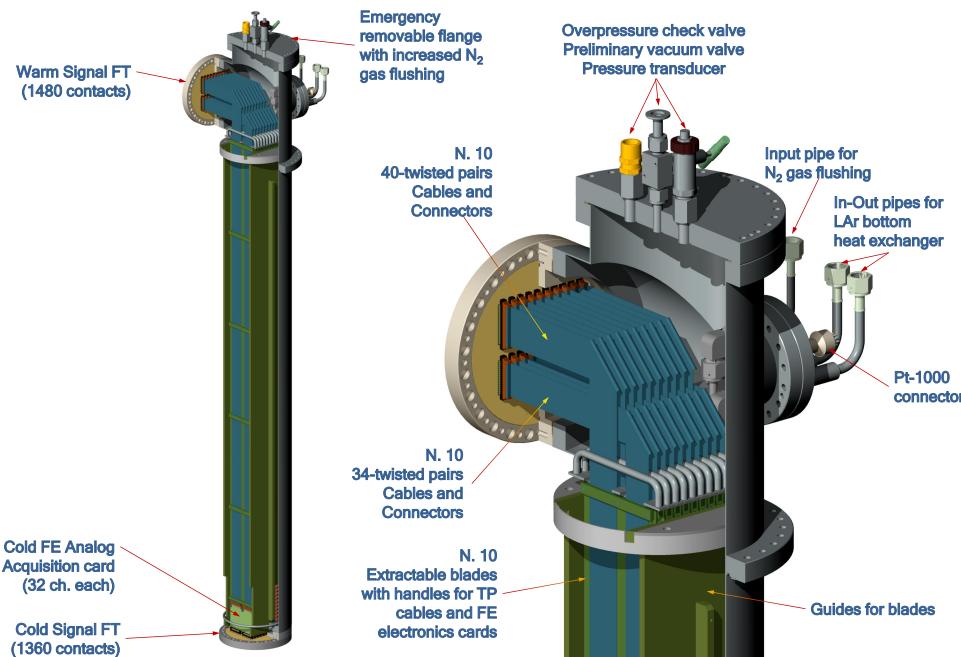


Figure 1.7: Details of the signal feedthrough (SFT) chimney design.

- ¹ The chimneys are closed at the bottom and top with vacuum-tight feedthrough flanges whose
² function is to dispatch the signal and slow control lines. The feedthrough at the bottom, the cold
³ (signal) feedthrough, isolates (Ultra-High Vacuum tightness standard) the inner volume of the DP
⁴ module from the chimney volume and interconnects the signals from the CRP to the analog FE
⁵ cards. The feedthrough at the top, the warm (signal) feedthrough, seals the chimney from the
⁶ outside environment. It also passes the low voltage and control lines to the FE electronics inside
⁷ and brings out the differential analog signal lines from the FE amplifiers.
- ⁸ The SFT chimney volume is filled with nitrogen gas at near-atmospheric pressure. The temperature
⁹ inside the chimney can be adjusted using a heat exchanger copper coil cooled with LAr. It is
¹⁰ located at the bottom close to the cold feedthrough around the FE cards. This cooling system
¹¹ mitigates the heat input to the main DP module volume and provides an optimal (lowest noise)
¹² operating temperature for the FE electronics of around 110 K. A pressure release valve, indicated
¹³ in Figure 1.7, protects the structure from an accidental overpressure in the inner volume. ^{fig:dpele-sft-chimney-design}

¹⁴ The expected heat input from a given SFT chimney is about 20 W. This number includes the heat
¹⁵ through the twisted-pair cables connected to the warm feedthrough, the heat in the SFT outer
¹⁶ metallic tube, as well as the heat dissipation by the FE cards. A total heat input from all 240
¹⁷ SFT chimneys is at the level of 5 kW.

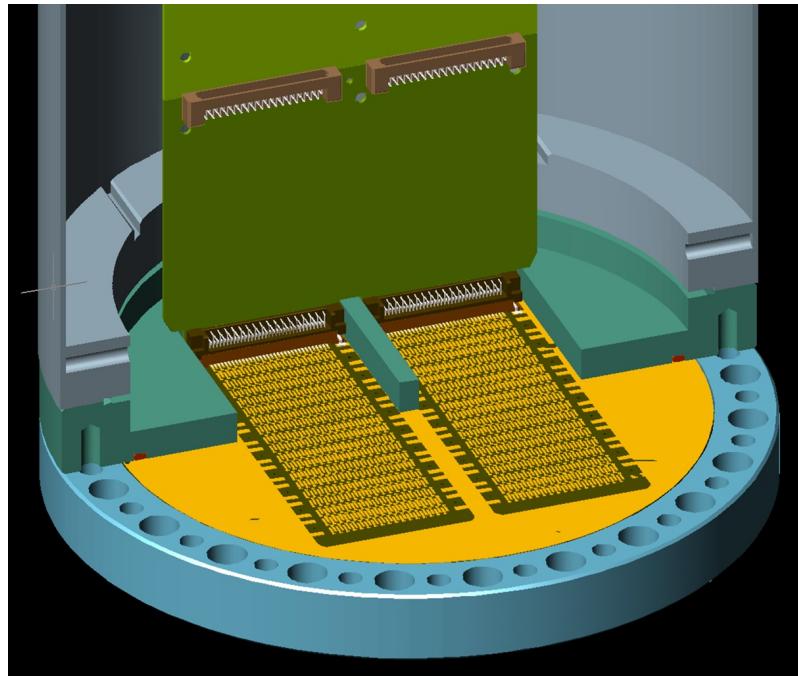


Figure 1.8: SFT chimney cold feedthrough flange with one of the FE cards mounted.

fig:dpel

¹⁸ The analog FE cards are inserted directly onto the PCB of the cold feedthrough of SFT chimney
¹⁹ (see Figure 1.8). The other side of the PCB (facing inside the cryostat) hosts the connectors for
²⁰ the flat cables coming from the CRP anodes. The FE cards are mounted on 2 m long blades made
₁ from FR4 that enable the insertion and extraction of the electronics, and also support the flat
₂ cables carrying signals, low voltages, and slow control to and from the warm flange interface. The
₃ blades slide along the rails installed inside the chimney at opposite sides; these rails guide the FE
₄ cards to their respective connectors on the cold feedthrough.

⁵ Prior to the commissioning of a DP module, the chimneys are evacuated via a dedicated KF16
⁶ port (see Figure 1.7) and then filled with nitrogen gas. This ensures the removal of any moisture
⁷ that would otherwise condense around the FE cards, once the DP module is filled with the LAr,
⁸ damaging the electronics. To access the FE cards once the DP module is cold, the stainless steel
⁹ flange at the top of the SFT chimney (Figure 1.7) must be removed. This procedure requires
¹⁰ continuous flushing of nitrogen gas at slight over-pressure (with respect to atmospheric) in order
¹¹ to prevent the humid air entering. Once a chimney is opened, it is possible to extract the blades
¹² with the FE cards after unplugging the flat cables (two per card) connected on the inner side of
¹³ the warm flange (Figure 1.7).

¹⁴ The procedure to access the FE cards *at cold* was successfully tested during the operation of the
¹⁵ WA105 DP demonstrator detector. The top of the chimney was very close to room temperature,
¹⁶ allowing manipulation of the cable connections on the warm feedthrough flange without cryogenic
¹⁷ gloves. The movement of the blades on the rails and the FE card extraction and insertion did not

18 indicate any mechanical problems due to the shrinking of various elements at lower temperatures.
 19 The signals from the FE cards that underwent this process were also checked and all channels
 20 functioned properly.

21 1.2.3 Digital Advanced Mezzanine Card Electronics for Charge Readout

22 The CRO AMC cards read and digitize the data from the FE amplifiers and transmit them to the
 23 DAQ system. The cards also include a last stage of analog shaping before the ADC input. The
 24 analog FEs produce differential unipolar signals defined with respect to a baseline offset. Prior
 25 to the digitization, this offset is removed and the signals are subtracted in the analog input stage
 1 of the digital electronics. Each card has eight ADC chips (AD9257, Table 1.4), two dual-port
 2 memories (IDT70T3339), and an FPGA (ALTERA Cyclone V) on board. The FPGA provides
 3 a virtual processor (NIOS) that handles the readout and the data transmission. The choices for
 4 all of the components have been optimized with respect to the design requirements and technical
 5 criteria such as costs, chip footprint (small enough to fit on the AMC), power consumption, and
 6 ease of use (available functionality).

Table 1.4: Main characteristics of ADC AD9257.

Item	
Channels	8
Sampling	up to 40 MSPS
Resolution	0.122 mV
Dynamic range	14 bit/ 2.0 V
Differential non-linearity	typical ± 0.6 LSB with min. -1.0 and max. 1.7 LSB
Integral non-linearity	typical ± 1.1 LSB with min. -3.1 and max. 3.1 LSB

7 Figure 1.9 shows block diagram of the AMC functionality. Each AMC generates a continuous
 8 compressed stream of 2.5 MSPS 12 bit data per readout channel. The on-board ADCs operate at a
 9 rate of 25 MHz per channel. The data are down-sampled in the FPGA to 2.5 MHz by performing
 10 ten-sample averaging, which leads to the further digital filtering of the noise. The data, consisting
 11 of only the 12 most significant bits from each digitized 14 bit sample, are then compressed using an
 12 optimized version of the Huffman algorithm and organized in frames for transmission. The frames
 13 contain the absolute timing information of the first data sample for reliability purposes. In the
 14 current design, each AMC has 64 channels and reads one analog FE card.

15 The AMCs are housed in μ TCA crates and send their data via the MCH switch. The timing
 16 synchronization of AMCs is achieved via a WR-MCH module (also housed in the crate) that is
 17 connected to the WR network. In addition, WR-MCH could also be used for triggered readout
 18 of AMCs by sending it dedicated packets containing trigger timestamp information over the WR
 19 network.

1 In ProtoDUNE-DP, AMCs are operated in the triggered mode, reading a 4 ms drift time window

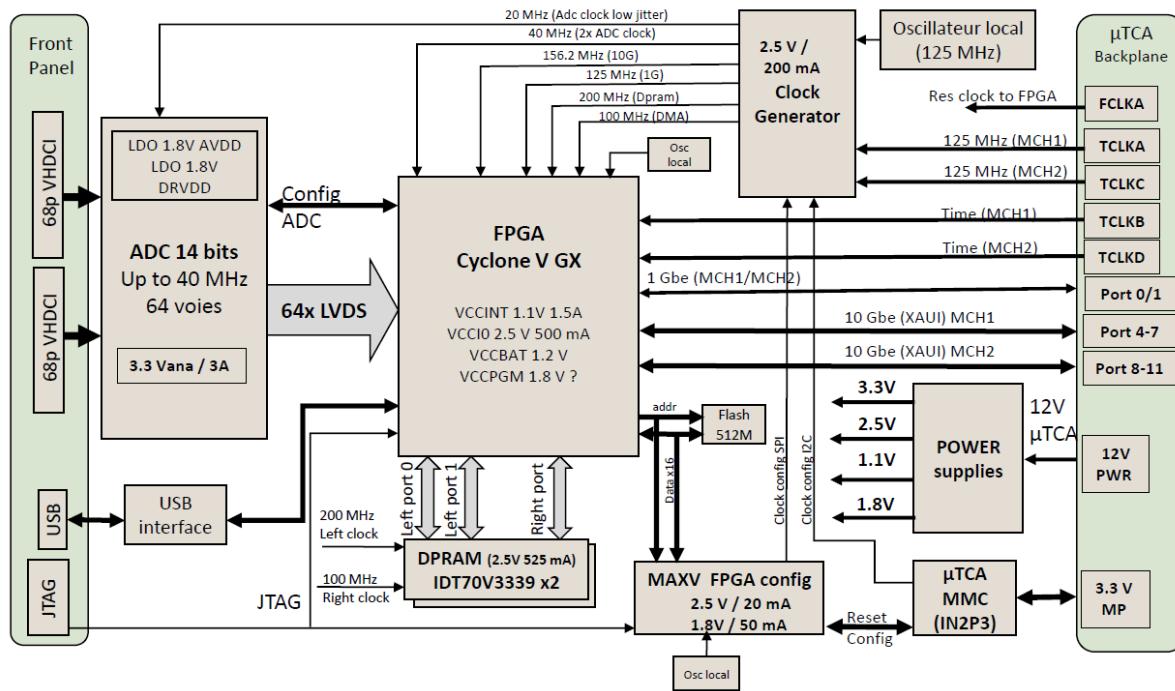


Figure 1.9: Block diagram of AMC.

2 at a trigger rate of 100 Hz, which is not far from continuous readout mode. The analog data
 3 are continuously digitized and buffered. It is possible to acquire a sub-sample of these data by
 4 providing AMC with a timestamp generated by an external trigger. The timestamp defines the
 5 start time for the data sequence to be read, while the length of the sequence is determined by
 6 the size of the drift window. In ProtoDUNE-DP this length corresponds to 10,000 400 ns samples
 7 per full drift window (4 ms). Triggers (beam counters, cosmic-ray counters, PMTs reading the UV
 8 light, and starts of beam spills) are time stamped in a dedicated WR slave node (WR-TSN), an
 9 FMC-DIO mezzanine mounted on WR SPEC carrier card, which runs a custom firmware and is
 10 hosted in a computer. The WR-TSN is connected to the WR grandmaster for synchronization
 11 and for transmission of the trigger information. The timestamp data produced by the WR-TSN
 12 are sent over the WR network as Ethernet packets with a customized protocol.

13 1.2.4 Electronics for Light Readout

14 The LRO card is a 16 channel AMC containing one 16 channel 14 bit 65 MHz ADC (AD9249) and
 15 one CATIROC ASIC [?]. A block diagram of the prototype board used for ProtoDUNE-DP is
 16 shown in Figure 1.10 and a photo in Figure 1.11. In this prototype a mezzanine board containing
 17 the ASIC and ADC sits on a commercial (COTS) mother board (Bittware S4 AMC) with a high
 18 specification FPGA (ALTERA Stratix IV). In the final implementation for the DP module, the
 19 mezzanine is integrated with the layout of the AMC board developed for the charge readout. A
 20 proposed upgrade is a 32 channel card, which would reduce the number of cards required and
 1 increase the channel density to 352 channels per μTCA crate.

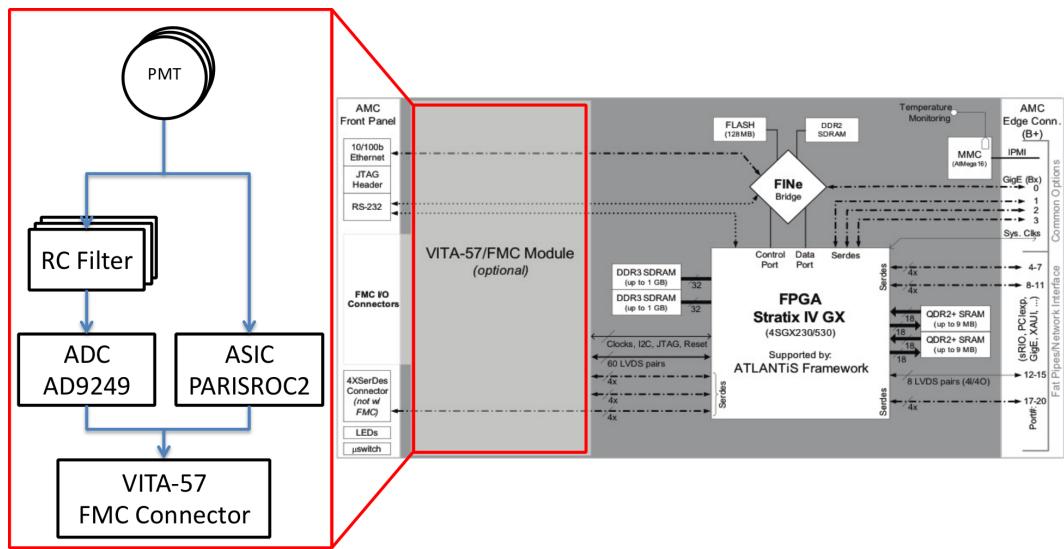


Figure 1.10: Block diagram of LRO prototype.

fig:dpel

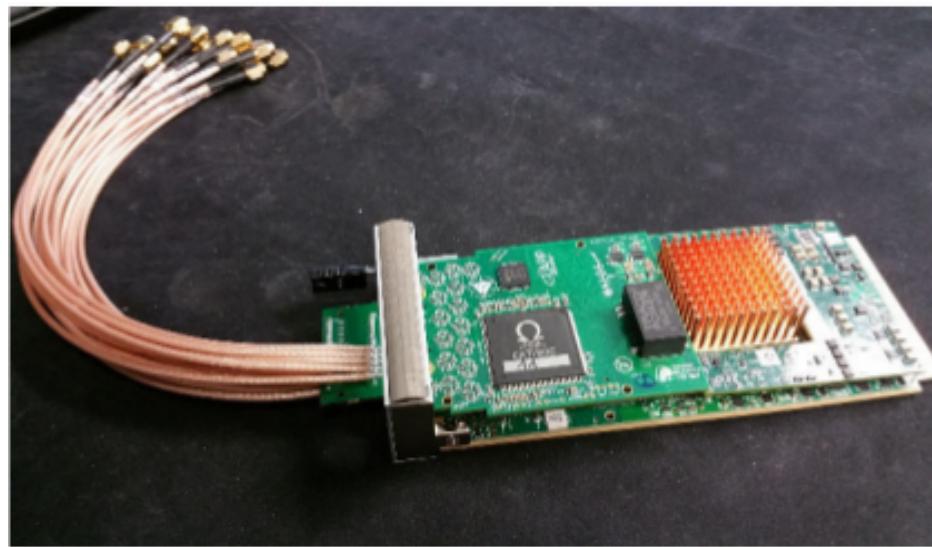


Figure 1.11: A photo of the LRO prototype.

fig:dpel

- ² The analog signals from each PMT channel are split equally into two separate branches (see
³ Figure 1.10) ^{fig:dpele-tro-scheme}. One path (Waveform branch), through an anti-aliasing low-pass filter and the 14
⁴ bit 65 MHz ADC (AD9249), produces continuous digitization of the PMT waveform data, which
⁵ are down-sampled to 2.5 MHz prior to the transmission to DAQ. The other (CATIROC branch)
⁶ is routed directly to the CATIROC ASIC for precise measurements of pulse charge and timing.
⁷ Both paths produce data continuously and independently.

⁸ 1.2.4.1 Waveform branch

- ⁹ The main characteristics of the ADC used for continuous digitization of the PMT signals are shown
¹⁰ in Table 1.5. ^{tab:dpele-adc9249}

Table 1.5: Main characteristics of ADC AD9249.

Item	
Channels	16
Sampling	65 MSPS
Resolution	0.122 mV
Dynamic range	14 bit / 2 V
Differential non-linearity	typical ± 0.6 LSB with min. -0.9 and max. 1.6 LSB
Integral non-linearity	typical ± 0.9 LSB with min. -3 and max. 3 LSB

- ¹ For normal operation, in the continuous mode, the digitized signals are down-sampled by the
² FPGA to a coarse 400 ns sampling to match that of the CRO and limit the quantity of data
³ streamed. The use of a higher specification ADC, with time-sampling of 15.4 ns, allows for greater
⁴ flexibility. For particular calibration runs, waveforms with finer time sampling could be read-
⁵ out, allowing studies of, e.g., the LAr scintillation time profiles. During normal operation, as
⁶ well, online pulse processing is possible within the FPGA using the finer time-sampled waveforms
⁷ (before the down sampling; this would enable continuous measurements of quantities such as the
⁸ rise and fall times of the pulses. Even at the coarse sampling rate of 400 ns, studies of the LAr
⁹ scintillation time profile are possible (given the long fall-time constant of ~ 1500 ns) as is matching
¹⁰ of the electroluminescence signal (also known as proportional scintillation light) to that of the
¹¹ charge signal. Low light-level signals, as from single or a few photoelectrons, will show no time
¹² structure, but will consist of one sample several LSB above the baseline.

¹³ 1.2.4.2 CATIROC branch

- ¹⁴ The CATIROC is a 16 channel ASIC dedicated to measurement of charge and precision timing of
¹⁵ negative-polarity PMT signals ^{plin 2017} [?]. It auto-triggers on single photoelectrons and can sustain a high
¹⁶ dark rate of up to 20 kHz/channel. Charge measurements are possible over the range of 160 fC to

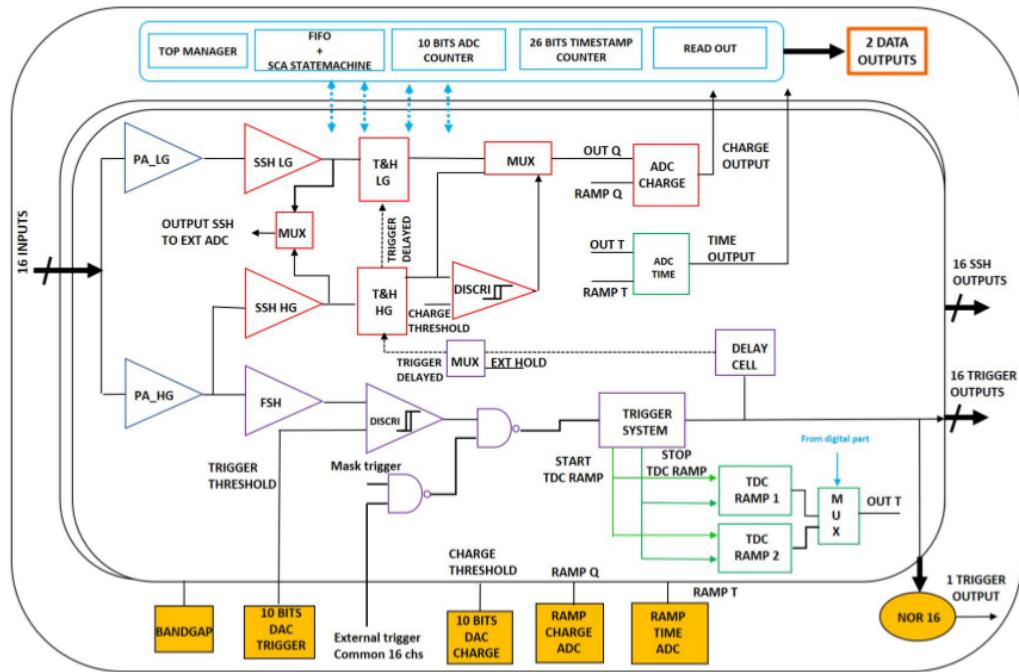


Figure 1.12: Functional diagram of CATIROC ASIC.

fig:dpele

¹⁷ 70 pC (corresponding to approximately to a range of 1 to 400 photoelectrons with a PMT gain of
¹⁸ 1×10^6). Timing measurements per channel can reflect an accuracy of 200 ps.

¹⁹ [fig:dpele-lro-catiroc](#) Figure 1.12 shows the schematic of the CATIROC ASIC. Its main properties are summarized in
²⁰ [tab:dpele-catiroc](#) Table 1.6. The slow channel, from which precision charge and timing measurements are made,
²¹ is formed by two variable-gain (8 bit) amplifiers followed by two variable slow shapers; one high
²² gain for small signals, and one low gain for larger signals, and two track-and-hold stages. The
²³ slow shaper has a tunable shaping time (up to 100 ns) and a variable gain. If the high gain is
²⁴ saturated, corresponding to passing a predetermined threshold common to all 16 channels, the
²⁵ lower gain value is chosen. The chosen charge value is converted by an internal 10-bit Wilkinson
²⁶ ADC operating at 160 MHz. This slow channel operates in a ping-pong mode, with two capacitors
²⁷ to store the slow shaper signals, giving an effective buffer of 2 events. If both capacitors are full,
²⁸ a deadtime of 5 μ s arises.

¹ The fast channel is used to auto-trigger the ASIC and make the fine-timing measurement. It
² comprises a high gain preamplifier, fast shaper (shaping time 5 ns) and discriminator with a 10 bit
³ programmable threshold that is common to all 16 channels. The output of the discriminator is
⁴ used for the two Time to Digital Convertors to get the fine-timing. A coarse timestamp could also
⁵ be obtained from a 26 bit counter running at 40 MHz. Only the data from the triggered channels
⁶ are digitized; their information is transferred to the internal memory, which is read by the external
⁷ FPGA.

Table 1.6: Main characteristics of CATIROC.

Item	
Number of channels	16
Signal polarity	negative
Timing	Timestamp: 26 bit counter at 40 MHz Fine time: resolution <200 ps
Charge Dynamic Range	160 fC to 100 pC
Trigger	auto-trigger Noise = 5 fC Minimum threshold = 25 fC (5σ)
Digital	10-bit Wilkinson ADC at 160 MHz Read-out frame of 50 bits
Outputs	16 trigger outputs NOR16 16 slow shaper outputs Charge measurement over 10 bits Time measurements over 10 bits
Main Internal Programmable Features	Variable preamplifier gain Variable shaping and gain Common trigger threshold Common gain threshold

1.2.5 Network-based μ TCA Architecture

- The digital electronics is based on μ TCA standard which offers industrial solution with a very compact and easily scalable architecture to handle a large number of channels at low cost. The standard (or related standards such as ATCA or xTCA) is widely used in the telecommunication industry and is being adapted by the HEP community. The backplane of the μ TCA crates host high-speed serial links that support a variety of transmission protocols (Ethernet, PCI Express, SRIO, etc.). In addition, dedicated lanes are available for the distribution of the clock signals to all the boards hosted in the crate. The Ethernet-based solution has been adopted for both the data and clock distribution in this design of the DP electronics system for both Charge and Light Read Out.
- Each AMC for either charge or light readout plugged into the μ TCA is connected to the crate MCH board through the backplane serial links. The MCH provides the switch functionality that enables AMCs to communicate with each other or external systems through the MCH uplink interface. In the DP electronics system design, MCH also manages the WR clock distribution.
- In the current design, as used for ProtoDUNE-DP, the MCH operates with a 10 Gbit/s uplink. Given that a μ TCA crate hosts 10 AMCs for charge readout, the required bandwidth to stream the data to DAQ is about 1.8 Gbit/s. This assumes that the data exiting the AMCs are losslessly compressed with the compression factor of 10. The bandwidth required per crate link for streaming the LRO data is 4.7 Gbit/s. The 10 Gbit/s MCH is therefore sufficient to support these data rates. However, the technology is moving towards supporting the 40 Gbit/s rates. In addition, the channel

Table 1.7: Bandwidth requirements per μ TCA crate for continuous data streaming. A compression factor of 10 for the charger readout data is assumed

Parameter	Value
CRO data rate	1.8 Gbit/s
LRO data rate	4.7 Gbit/s
Current MCH bandwidth	10 Gbit/s
Upgradable MCH bandwidth	40 Gbit/s

density per AMC could also be increased for cost optimization. For these reasons an upgrade to a 40 Gbit/s MCH could be foreseen in the future. This would also imply that the optical links connecting the DAQ system to μ TCA MCH should be operable at 40 Gbit/s. A summary of the required and supported bandwidths per μ TCA crate for continuous data streaming is provided in Table 1.7.

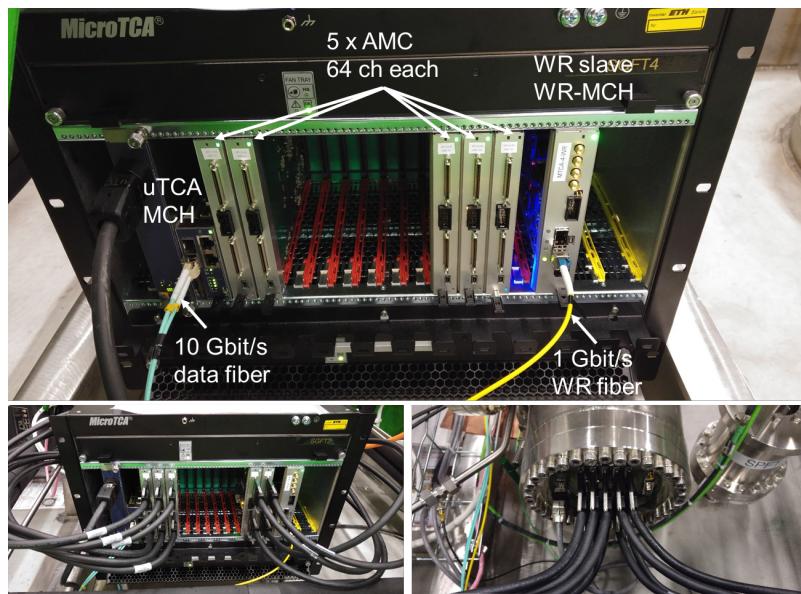


Figure 1.13: Pictures of an instrumented μ TCA crate from the WA105 DP demonstrator. The crate contains five AMC cards, correspondingly to the number of readout channels per the SFT chimney. The images below show the crate after the cables are connected to the warm flange of the SFT chimney.

As an illustration, Figure 1.13 shows pictures of one of the instrumented μ TCA crates used for the charge readout of the WA105 DP demonstrator at CERN. In this detector each SFT chimney reads 320 channels thus requiring only five AMCs per the μ TCA crate. The two optical fiber links, one (10 Gbit/s) for data and the other (1 Gbit/s) for clock/trigger timing distribution, are visible in the images.

22 1.2.6 Timing Distribution

-elec-wr

23 The time synchronization system selected for the DP module utilizes a WR network, which com-
 24 bines the synchronous 1 Gbit/s Ethernet (SyncE) technology with the exchange of PTPV2 packets,
 25 to synchronize clocks of distant nodes to a common time. A high stability GPS disciplined oscillator
 26 (GPSDO) with accuracy similar to that of an atomic clock provides a clock reference signal to
 1 be distributed over the physical layer interface of the WR Ethernet network. The network topol-
 2 ogy is built using specially designed switches that have the standard IEEE802.1x Ethernet Bridge
 3 functionality with an addition of WR-specific extensions to preserve the clock accuracy. Time and
 4 frequency information are distributed to the nodes on the WR network via optical fibers. The WR
 5 protocol automatically performs dynamic self-calibrations to account for any propagation delays
 6 and keeps all connected nodes continuously synchronized to sub-ns precision.

7 The sub-ns precision on the clock synchronization is not strictly needed for aligning samples in the
 8 different AMC digitization units, since the timing granularity on the data is 400 ns. However, the
 9 WR timing system offers readily available industrial components and the necessary protocols for
 10 synchronization with automatic calibration of delay propagation. R&D on this timing distribution
 11 solution started in 2006; the final design for integrating this system, foreseen for the DP module,
 12 into the ProtoDUNE-DP and the WA105 DP demonstrator readout was completed in 2016.

13 In the implementation specific to ProtoDUNE-DP, a GPS-disciplined clock unit (Meinberg LAN-
 14 TIME M600) feeds 10 MHz and 1 PPS reference signals to a commercial WR switch (Seven Sol-
 15 lutions WRS V3.4). The switch acts as Grand Master of the WR network. It is connected via
 16 1 Gbit/s optical links to the dedicated WR timestamping node (WR-TSN) and the WR end-node
 17 slave cards present within each μ TCA crate (WR-MCH) keeping these synchronized to its refer-
 18 ence time. The WR grandmaster also communicates through a standard Ethernet port with the
 19 LANTIME unit for its date and time synchronization via NTP. The WR-TSN module receives
 20 analog TTL-level trigger signals, generates their timestamps, and transmits them over the WR
 21 network to the connected WR-MCH units. This timestamp information is then used by AMCs to
 22 find the data frame corresponding to the trigger.



Figure 1.14: Picture of the WR slave node card (WR-MCH) present in each μ TCA crate for time synchronization. The WR-LEN mezzanine card is visible in the bottom right corner.

fig:dpele-wrmch-image

23 The WR-MCH card (Figure 1.14) enables clock/timing/trigger distribution to AMCs. It com-

24 municates with them via dedicated lines in the backplane of the μ TCA crate using a customized
 25 data-frame protocol. The module contains a commercial WR slave node card, the WR Lite Embed-
 26 ded Node (Seven Solutions OEM WR-LEN), as mezzanine card. WR-LEN runs on a customized
 27 firmware which also enables it to decode the trigger timestamp data packet received over the WR
 28 network.

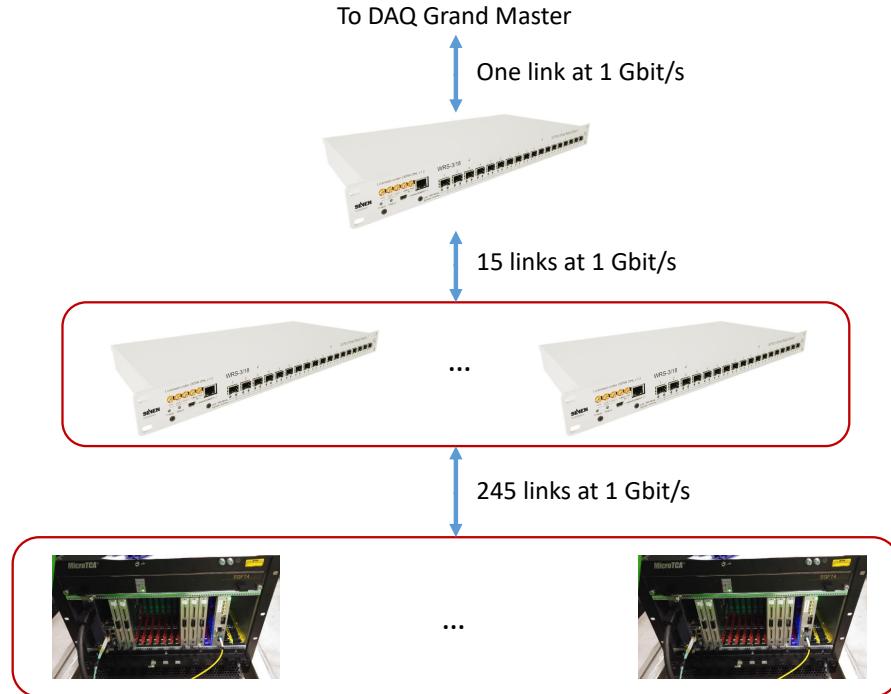


Figure 1.15: Architecture of WR network for time synchronization of digital readout electronics.

fig:dpele-wrnet-layout

29 The architecture of the WR network layout for one DP module is illustrated Figure 1.15. It is built
 30 in a hierarchical structure from 16 WR switches with 18 ports each, chained with 1 Gbit/s optical
 1 fibers. The switch at the top of the hierarchy interconnects the synchronization WR grandmaster
 2 from the DAQ system with the 15 switches in the middle layer. These are in turn connected to
 3 the WR-MCH slave nodes in each μ TCA crate (245 in total for charge and light readout).

4 1.3 Production and Quality Assurance

5 1.3.1 Cryogenic Analog FE Electronics

6 The production of the cryogenic ASICs and analog FE cards is envisioned to be split between several
 7 sites located in France and Japan at the moment. The delivered cards are then split between five
 8 institutions in France (IPNL), Japan (KEK, NITKC, IU), and USA (SMU), where they are tested
 9 for various performance parameters such as noise levels, dead channels, hot channels, gain and its

¹⁰ uniformity across channels, etc., at both room and operating cold temperature. An appropriate
¹¹ and common database will be developed and populated with test results.

¹² 1.3.2 Signal Feedthrough Chimneys

¹³ A number of items require manufacture in order to produce the SFT chimneys. These include

- ¹ • the PCB flanges for the warm and cold feedthrough flange interfaces,
- ² • the stainless steel pipe structure,
- ³ • the flanges containing the interfaces to the gas and liquid lines and slow control,
- ⁴ • the blades and railing, and
- ⁵ • the heat exchanger system.

⁶ The flat cables that connect the FE cards to the warm flange are commercially available products
⁷ and are part of the SFT chimney procurement process.

⁸ The manufactured components are delivered to designated institutions participating in the DP
⁹ electronics consortium where teams verify the signal continuity for both cold and warm flanges,
¹⁰ then assemble them into SFT chimneys and test for leaks. They also check the blade insertion,
¹¹ test the flat cables, then, once verified, pack the assembled SFT chimneys and ship them to SURF.

¹² 1.3.3 The Timing System and μ TCA

¹³ The timing system components, the 16 WR switches and the 245 μ TCA crates containing the
¹⁴ power modules, carrier hubs (MCH), and fan units, are commercially available. The manufacturer
¹⁵ takes the responsibility for the necessary quality control and quality assurance of these components,
¹⁶ requiring no further testing on the part of the DP electronics consortium. Once the components
¹⁷ are delivered to the designated institutions, they can be sent to SURF for the installation.

¹⁸ The commercial VHDCI signal cables (connecting the AMCs to the SFT chimneys) are procured
¹⁹ and tested with the SFT chimney warm flanges.

²⁰ 1.3.4 Charge Readout Electronics

²¹ The production of the AMC cards for the charge readout as well as the WR-MCH slave cards
²² for synchronization is currently shared between four institutions (IPNL, KEK, NITKC, IU). The

²³ cards ordered and delivered to each respective institution are subjected to quality assurance tests
²⁴ agreed upon by all participants.

²⁵ 1.3.5 Light Readout Electronics

²⁶ The production of the LRO AMC cards occurs in the same manner as the cards for ProtoDUNE-
²⁷ DP since the number of cards to be produced and the channels to test are both small. The cards'
²⁸ electronic components, meeting required specifications, are purchased commercially. The project
²⁹ will be managed by a qualified engineer manages this project, working with a specialist in quality
³⁰ assurance (QA).

³¹ The produced cards are delivered to designated consortium institutions. Upon delivery, teams
³² conduct basic quality tests, including visual inspection and electrical testing, to ensure conformity
³³ of production.

³⁴ Another series of tests is performed on the cards to ensure their correct functionality and to
³⁵ evaluate their performance. Measurements include: linearity measurements (DNL and INL) of
³⁶ each ADC channel, and linearity of response of the ASIC. The level of cross-talk on the ASIC is
³⁷ also quantified.

³⁸ A dedicated single-channel setup, with PMT (Hamamatsu R5912-02-mod), and identical cabling
¹ and splitter, can be used to characterize the expected noise level of each channel, and response to
² single photoelectrons up to saturation.

³ Multiple cards are operated in a μ TCA crate with the DAQ.

⁴ After shipment to SURF and installation on-site, a small series of tests is performed with a pulse
⁵ generator to verify the good working condition of the cards. Noise-level measurements are included
⁶ in the integration effort.

⁷ 1.4 Interfaces

⁸ The DP electronics system interfaces to several other systems, starting with the CRP and the PD
⁹ systems. The digitized data must in turn flow to the DAQ via the optical links in each μ TCA
¹⁰ crate. The SFT chimneys integrate into the cryostat structure and connect to the cryogenics and
¹¹ gas systems. The slow-control system takes on management of the low-voltage power supplies for
¹² the FE analog electronics and μ TCA crates, and monitors various sensors in the SFT chimneys.
¹³ Table 1.8 provides the references to the relevant interface documents for each interface, stored in
¹⁴ the DUNE document database (DocDB).

Table 1.8: Interface documents relevant to DP electronics system.

Interface document	DUNE DocDB No.
DP TPC electronics to DP CRP	6751
DP TPC electronics to DP PD	6772
DP TPC electronics to Joint DAQ	6778
DP TPC electronics to Joint CISC	6784
Facility Interfaces to DP TPC electronics	6982
Installation interfaces to DP TPC electronics	7009
Integration facility to DP TPC electronics	7036
Calibration to DP TPC electronics	7063
DUNE physics to DP TPC electronics	7090
Software and computing to DP TPC electronics	7117

1.4.1 Electronics System to CRP and Photon Detection Systems

The cold feedthrough flange of the SFT chimneys forms the interface between the CRP and the CRO electronics system. On the side facing the cryostat the flange PCB has 20 68 pin connectors (KEL 8930E-068-178MS-F) for plugging the flat cables from the CRP. These are 68 channel twisted-pair flat cables, each carrying signals from 32 anode strips and are within the scope of the CRP system. Each analog FE card reads 64 anode strips, i.e., signals from two KEL connectors. The order in which the cables are connected to the cold flange determines the mapping of the electronic channels to the physical location of the strips on the CRP and is coordinated carefully with the CRP consortium. Figure 1.16 shows two images of the cold feedthrough from the WA105 DP demonstrator.

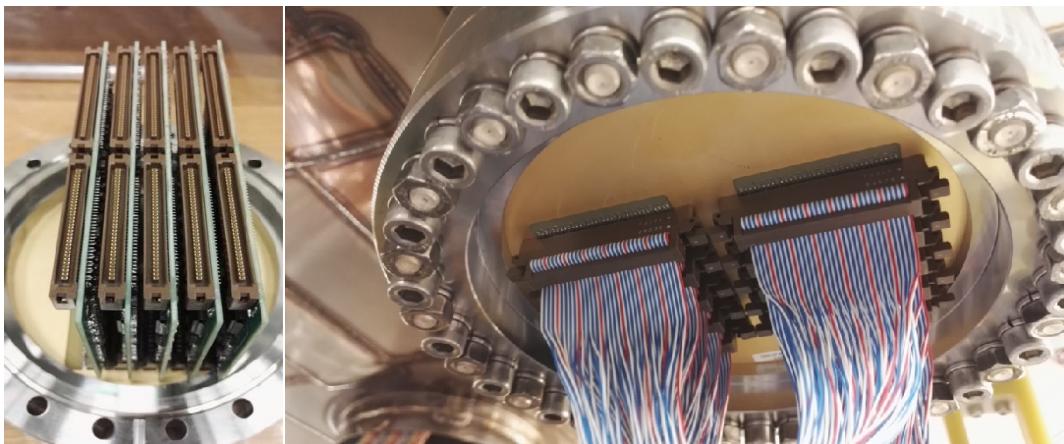


Figure 1.16: Images of the WA105 DP demonstrator SFT cold feedthrough with the FE cards inserted (right) and signal cables from CRP connected (left). The WA105 DP demonstrator SFT chimneys read only 320 channels thus requiring 5 FE cards.

fig:dpele-sft-cold-flange

The LRO electronics system is connected to the specific LRO signal feedthrough flanges on top of the cryostat via coaxial cables, which are within the scope of the PDSs system. The LRO electronics is designed for negative polarity PMT signals, with the amplitude of single photoelectrons on the

8 input of the card between 1 and 10 mV. Typically assuming a PMT gain of 1×10^6 (no accounting
 9 for attenuation of the signals), the Catiroc ASIC can measure a range of 1 to 400 photoelectrons
 10 (160 fC to 70 pC), the ADC samples from 1 mV to 1 V corresponding to 1 to 1000 photoelectrons,
 11 including the time response of the scintillator the range can increase to \sim 6000. Increasing the gain
 12 of the PMT to 1×10^7 , lowers the upper values by a factor of 10. The internal noise level of the
 13 CATIROC is below 0.1 mV. The objective for the noise level of the ADC is for each channel to
 14 have the RMS noise level greater than 0.5 LSB, aiming for 1 LSB 0.1 mV.

15 1.4.2 Electronics System to DAQ System

16 The hardware interface between the DP CRO and LRO electronics sub-systems and DAQ has two
 17 components. The first interface is the 10 Gbit/s optical fibers for data transfer between the μ TCA
 18 crates and the network interface of the DAQ system. The second one is a 1 Gbit/s optical fiber
 19 that connects the DAQ WR grandmaster switch to the DP electronics timing system.

20 In the current design a given DP module would have 245 10 Gbit/s optical links for streaming the
 21 digitized data to the DAQ from the CRO (240 links) and LRO (5 links) electronics housed in μ TCA
 22 crates on top of the cryostat structure. In the current specifications, the fibers are multimode OM3
 23 fibers [?] with LC-LC connectors suitable for the transmission over distances of up to 300 m. They
 24 are provided by the DAQ consortium. On the side of the μ TCA crate, the fibers are connected
 25 to an optical transceiver in the MCH (two SFP+ (XAUI) links) [?]. On the DAQ, they go to
 26 the Level 1 (LV1) machines of the trigger farm, or switches, depending on the network topology
 27 adopted in the DAQ system design.

28 The 1 Gbit/s link going from the WR grandmaster to the DP electronics time distribution net-
 29 work serves to provide the synchronization to the reference clock common for the entire FD and
 30 derived from a GPSDO (GPS-Disciplined Oscillator) clock unit installed on the surface. The clock
 31 information is distributed to the WR-MCH slave module in each μ TCA crate via a set of WR
 32 switches. These switches and the interconnecting 1 Gbit/s fibers form the timing sub-system of
 1 the DP electronics system and are included in the design of the latter. The WR synchronization
 2 protocol includes the automatic and continuous calibration of the propagation delays between the
 3 master and the connected slaves. This allows maintaining the overall synchronization between
 4 different nodes at sub-ns level. The WR grandmaster will be located either:

- 5 • On the surface (above-ground) near the GPSDO. In this case, a single fiber connects it to
 6 the DP timing system underground. The system automatically accounts for the incurred
 7 latency due to the extensive fiber length.
- 8 • Underground in the central utility cavern (CUC). In this case, calibration of the propaga-
 9 tion delays between GPSDO and the WR grandmaster is performed manually and a timing
 10 correction is applied to the data afterward.

11 The TPC electronics design assumes that the data are streamed continuously via the 10 Gbit/s
 12 links to the DAQ, where they are buffered until a trigger decision is made. The triggers are to
 13 be issued by processing the buffered data in some suitable sliding time window on the trigger

¹⁴ farm machines. The window may be as long as 10 s for Supernova-triggered events. The triggers
¹⁵ determine whether the data contained in the buffers are to be written on disk.

¹⁶ The software interface between the DAQ and the electronics system includes the tools for handling
¹⁷ the data transmission and buffering, i.e., data formatting in user datagram protocol (UDP) packets,
¹⁸ compression and decompression, and exchange of the control packets.

¹⁹ 1.4.3 Electronics System to Cryostat and Cryogenics

²⁰ The interface point between the cryostat and the DP electronics system is at the cryostat penetrations where the SFT chimneys are installed. Each penetration accommodates the chimney (of
²¹ external diameter 254 mm). Each chimney has a CF-273 flange welded to its outer structure (see
²² ~~fig:dpel-e-sit-chimney-crosspipe~~
²³ Figure 1.17). After the chimney is inserted, this flange is in contact with the corresponding flange
²⁴ on the crossing (or penetration) pipe embedded in the cryostat structure to which it is eventually
²⁵ fastened. In order to avoid any leaks at this interface a CF-273 copper gasket is used to ensure
²⁶ the vacuum tightness.

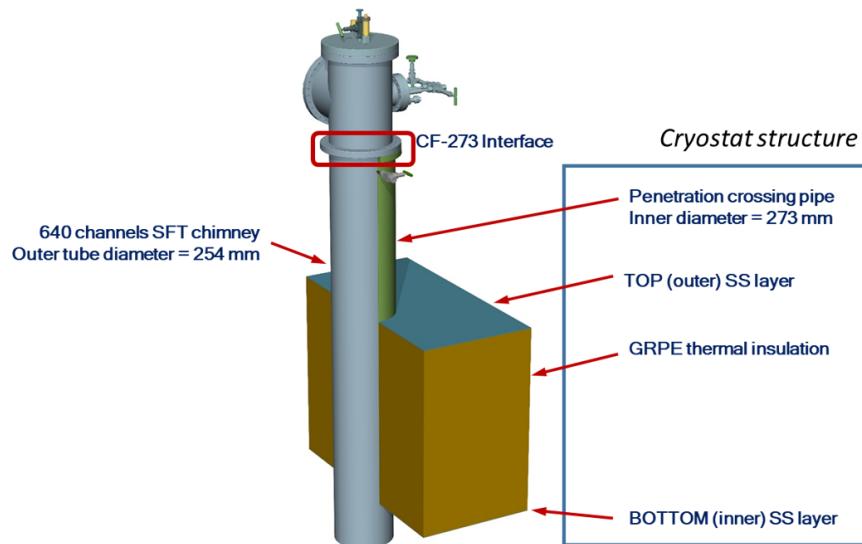


Figure 1.17: Details of SFT chimney interface to the cryostat structure.

²⁷ Each chimney contains a heat exchanger copper coil cooled with LAr. There are two (inlet and
²⁸ outlet) stainless steel pipe connections with 10 mm (12 mm) inner (outer) diameter that need to be
²⁹ branched to the respective system for the LAr delivery and recirculation. In addition, a connection
¹ for nitrogen gas line with the same pipe dimensions as those for the LAr cooling, is used for filling
² the chimney after it is closed following the installation of the FE electronics. The nitrogen line is
³ also required for flushing the chimney in the case of an access to the FE cards after the DP module
⁴ is cooled for the operation.

- 5 The μ TCA crates for charge readout are installed within a short <0.5 m distance from the SFT
 6 chimneys on top of the cryostat roof. The five μ TCA crates for the light readout are also placed
 7 on the roof of the cryostat at optimal locations defined by the routing of the PMT signal cables.
 8 The required volume to accommodate the crates is roughly $60 \times 50 \times 40$ cm 3 .

9 1.4.4 Electronics System to Slow Control System

10 The integration with the slow control of the low-voltage power supply system for the FE cards and
 11 μ TCA crates is required to enable the remote management and monitoring (current consumption
 12 by ASICs, set voltage, etc.). In addition, the SFT chimneys contain several sensors that need to
 13 be monitored. These include a pressure transducer that measures the pressure inside the chimney
 14 and at least two temperature probes (PT1000) that monitor the gas temperature inside near the
 15 cold flange at the bottom and close to the warm flange at the top. The readout of the μ TCA crate
 16 information and the sensors in the SFT chimneys is part of the Slow Control system.

17 1.5 Transport and Handling

18 The SFT chimneys are 2350 mm long and weigh 180 kg. The cold and warm flanges are mounted on
 19 them at the assembly site, and the chimneys undergo leak-testing prior to shipping in wooden crates
 20 (approximate dimensions $2.5 \times 0.5 \times 0.5$ m 3). Once at SURF the crates are moved underground
 21 and placed on the roof of the cryostat by the underground installation team (UIT). The DP
 22 electronics consortium is then responsible for unpacking the crates and installing the SFT chimneys.
 23 The chimneys are delivered with the cold and warm flanges already mounted and leak tested.
 24 The boxes containing the electronic cards and μ TCA crates are also handled by DP electronics
 25 consortium personnel. These are expected to be lightweight and easy to carry. A box containing
 26 100 AMC cards has a maximal dimensions of 60 cm and weights less than 10 kg.

27 1.6 Installation, Integration and Commissioning

28 The installation of the TPC electronics systems proceeds in several stages. In order to cable
 29 the CRPs to the SFT chimneys, the chimneys are installed first, prior to the start of the CRP
 30 installation inside the cryostat. Next the FE cards are mounted on the blades and inserted. The
 1 installation of the digital electronics and μ TCA crates is postponed until all of the heavy work
 2 finishes on top of the cryostat in order to prevent damage to the fragile components (e.g., optical
 3 fibers) due to movement of material and traffic. Once the μ TCA crates are installed and all the
 4 digital cards are inserted, the AMCs are cabled to the warm flanges of the SFTs for the charge
 5 readout and are connected to the PMT signal cables for the light readout. Finally, to complete
 6 the installation and integrate the system with the DAQ, the 10 Gbit/s and 1 Gbit/s optical links

- 7 to the DAQ and WR timing network are connected. At this stage the full system is ready for
 8 commissioning.

9 1.6.1 SFT Chimneys

10 The installation of the SFT chimneys requires a compact gantry crane with movable supports
 11 along the length of the cryostat. The crane itself moves along the transverse direction. The
 12 crates containing the SFT chimneys are placed along the edges of the cryostat roof. An unpacked
 13 chimney is hoisted and transported to the appropriate penetration crossing pipe for installation.
 14 Once in place, the chimney is fastened to the flange on the crossing pipe. Enough overhead room
 15 to accommodate a chimney's 2.4 m length is required to allow free movement of the chimney
 16 with the crane along the direction transverse to the beam axis.

17 In parallel with the SFT chimney installation, the FE cards are unpacked on top of the cryostat
 18 and mounted on the blades prior to their insertion in the chimneys. With SFT chimneys secured in
 19 the cryostat structure, the blades with mounted FE cards are inserted prior to sealing the chimney.
 20 At this stage, the LAr and gas nitrogen delivery pipes are already installed and it is possible to
 1 make the connections with them. The pressure probes and temperature sensors are also connected
 2 to the slow control system.

3 1.6.2 Digital μ TCA Crates

- 4 The installation of the μ TCA crates with the digital electronics takes place in the final stage of the
 5 DP module installation to avoid damaging the fragile equipment. The crates are placed in their
 6 designated positions on the cryostat and connected to the power distribution network. The AMC
 7 cards and WR-MCH modules are inserted in their slots. The VHDCI cables are then attached
 8 connecting the CRO AMCs to the warm flange interface of the SFT chimneys. The fibers from
 9 the timing system are connected to WR-MCH.

10 1.6.3 Integration within the DAQ

11 The integration of the DP TPC electronics with the DAQ system requires connecting the 10 Gbit/s
 12 fiber links to each of 245 μ TCA crates. The connection of the timing system to the synchronization
 13 WR grandmaster is done via a single 1 Gbit/s fiber link.
 14 The necessary software for the DAQ to read and decode the data packets sent by each μ TCA crate
 1 would also be provided by the electronics consortium.

2 1.6.4 Integration with the Photon Detection System

3 The cables carrying the PMT signals from the splitter boxes are connected to the LRO analog
4 electronics in each μ TCA crate. The position of the crates is optimized with respect to the layout
5 of PMT cables. In addition, the calibration system of the PDS is connected to specified inputs on
6 the cards.

7 1.6.5 Comissioning

8 The SFT chimneys are commissioned as a first step. This consists of evacuating and then filling
9 them with nitrogen gas at slight overpressure with respect to It is necessary to check the leak rate
10 when the chimney is under vacuum and to monitor the nitrogen pressure once it is filled in order
11 to verify that no damage occurred to the flange interfaces during installation.

12 The electronics system is commissioned after completing the installation of the μ TCA crates with
13 the AMCs, and the timing system. (The functionality of the full DAQ system is not strictly
14 required at this stage.) The data from each crate is read with a portable computer connected to
15 the crate MCH 10 Gbit/s or 1 Gbit/s interface. The non-functioning channels are identified by
16 pulsing the CRP strips and the data quality is examined to ensure the correct functioning of the
17 digital electronics and the temporal alignment of the data segments.

18 1.7 Risks and Vulnerabilities

19 The design of the DP electronics system takes into account several risk factors:

- 20 • Obsolescence of electronic components over the period of experiment:** allocation
**21 of enough spares (preferably complete cards instead of components) should be sufficient to
22 address this issue.**
- 23 • Modification to FE electronics due to evolution in design of PDs:** Strict and timely
1 follow-up of the FE requirements from the DP PDS is required.
- 2 • Damage to electronics due HV discharges or other causes:** The FE cards should
**3 include suitable protection components. The TVS diodes used in the current design have
**4 been sufficient to protect the electronics in the WA105 DP demonstrator. In addition, the
5 cards are accessible and could be replaced if damaged.****
- 6 • Overpressure in the SFT chimneys:** The SFT chimneys are equipped with safety valves
**7 that vent the excess gas in case of the sudden pressure rise. The overpressure threshold shall
8 be set low enough such that no significant damage could happen to the flanges.**

- Leak of nitrogen inside the DP module via cold flange:** The chimney volume is filled with argon gas instead of nitrogen.
- Mechanical problems with FE card extraction due to insufficient overhead clearance:** This is addressed by imposing a requirement for LBNF to ensure enough overhead clearance to extract the blades from the SFT chimneys.
- Data flow increase due to inefficient compression caused by higher noise:** Currently there is a factor of 5 margin in the available bandwidth with 10 Gbit/s MCH.
- Damage to μ TCA crates due to presence of water on the roof of the cryostat:** This is addressed by imposing a requirement for LBNF to ensure that the top cryostat surface remains dry.
- Problems with the ventilation system of the μ TCA crates due to bad air quality:** Normal conditions similar to any industrial environment (e.g., at CERN or Fermilab) is expected to be sufficient for proper crate functioning. It is important to avoid liberation of large quantities of dust in the detector caverns at SURF.

1.8 Organization and Management

1.8.1 Dual-Phase TPC Electronics Consortium Organization

The DP TPC electronics consortium consists of seven participating institutions from France (3), Japan (3), and the USA (1). The consortium leader is Dario Autiero (IPNL, France) and the technical leader is Takuya Hasegawa (KEK, Japan). The composition of the consortium along with the information for each institutional representative is provided in Table 1.9.

Table 1.9: DP TPC electronics consortium current participants.

Institution	Investigator	Contact
France: APC	Thomas Patzak	thomas.patzak@cern.ch
France: IPNL	Dario Autiero	autiero@cern.ch
France: LAPP	Dominique Duchesneau	duchesneau@lapp.in2p3.fr
Japan: Iwate University	Shinya Narita	narita@iwate-u.ac.jp
Japan: KEK	Takuya Hasegawa	takuya.hasegawa@kek
Japan: NITKC	Seiji Kasai	kasai@kure-nct.ac.jp
USA: Southern Methodist University	Thomas Coan	coan@smu.edu

9 1.8.2 Planning Assumptions

10 The design of the DP TPC electronics system largely on the elements that have already been
11 developed and tested in the WA105 DP demonstrator. Commissioning of the ProtoDUNE-DP
12 towards the end of 2018 should provide some additional information, but is not expected to affect
13 the design of principal components. Some additional improvements related to the increase in the
14 channel density supported by AMCs is possible for the purpose of further cost reduction.

15 1.8.3 WBS and Responsibilities

16 The description of the work breakdown structure (WBS) including the assignments of the respon-
17 sible institutions is documented in DUNE-doc-5594.

18 1.8.4 High-level Cost and Schedule

19 The key milestones are listed in Table 1.10. Table 1.11 shows an extract from the international
20 project schedule pertaining to the technical activities of this consortium. The detailed cost model
21 has been developed based on the scaling of the costs for the electronics system of ProtoDUNE-DP.
22 It is provided in an addendum.

tab:dpele-milestone-schedule

Table 1.10: DP TPC electronics consortium key milestones.

Date	Milestone
September 2018	Number of LRO channels finalized
November 2018	Final routing for LRO AMCs for production
March 2019	Costing model for technical design report (TDR) finalized
March 2019	Firmware for CRO AMCs finalized
March 2019	Commissioning of ProtoDUNE-DP finished
January 2023	Start of component production and procurement
July 2023	μ TCA infrastructure components produced
July 2023	Components of WR system delivered and validated
January 2024	SFT chimneys produced and tested
January 2024	Cryogenic FE analog electronics produced and tested
January 2024	AMCs for CRO and LRO produced and tested
August 2024	Cryostat of the second detector module is ready
November 2024	SFT chimneys installed
December 2024	Cryogenic FE electronics installed
December 2024	μ TCA crates and WR network installed
January 2025	Installation of AMCs completed
January 2025	Commissioning of the DP TPC electronics system
August 2025	Closure of the cryostat temporary construction opening (TCO)

Table 1.11: DP TPC electronics consortium schedule.

Technical activity	Days	Start date	End date
Preparation of costing for Technical Proposal	20	02/26/18	03/23/18
Initial Development of Installation Schedule	20	02/26/18	03/23/18
Further Development of Installation Schedule	145	09/03/18	03/22/19
Installation and Commissioning of ProtoDUNE-DP	320	01/01/18	03/22/19
Finalization of the number of channels for LRO	20	09/03/18	09/28/18
Implementation of routing for digital cards of LRO	40	10/01/18	11/23/18
Preparation of final costing for TDR	85	11/26/18	03/22/19
Firmware development for charge readout cards	145	09/03/18	03/22/19

²³ Chapter 2

²⁴ Photon Detection System

²⁵ 2.1 Photon Calibration System

²⁶ 2.1.1 System Design and Procurement

²⁷ A photon calibration system is required to be integrated into the DP module to calibrate the
²⁸ photomultiplier tubes (PMTs) installed in the LAr volume. The goal is to determine the PMT
²⁹ gain and maintain the PMT performance stability. A design similar to the one used in ProtoDUNE-
₁ DP will be used although some R&D measurements are planned to make it more effective, reduce
₂ the cost and mitigate issues related to the scaling.

³ In ProtoDUNE-DP, an optical fiber is installed at each PMT in order to provide a configurable
⁴ amount of light (see Figure ^{Fig:dppd_3_2} ??). The calibration light is provided by a blue LED of 460 nm using
⁵ a Kapuschinski circuit as LED driver; this is much less expensive than using a laser. One LED
⁶ is connected to one fiber that goes to one female optical feedthrough from Allectra ¹ In total,
⁷ six LEDs are placed in a hexagonal geometry. The direct light goes to the fiber, and the stray
⁸ light to a silicon photomultiplier (SiPM) used as a single reference sensor in the center. Fibers of
⁹ length 22.5 m (from Thorlabs ϕ 800 μm , FT800UMT, ² and stainless-steel jacket) are used inside
¹⁰ the cryostat. Each of these fibers is attached to a 1 to 7-fiber bundle (from Thorlabs ϕ 200 μm ,
¹¹ FT200UMT ³ stainless-steel jacket common end, and black jacket at split ends), so that one fiber
¹² is finally installed at each PMT. A diagram of the ProtoDUNE-DP photon calibration system is
¹³ shown in Figure ^{Fig:dppd_5_1} 2.1.

¹⁴ Assuming the ProtoDUNE-DP design for the DUNE FD with 720 PMTs, 120 bundles, 120 fibers,
¹⁵ 120 light sources, 120 flange feedthroughs, and 20 reference sensors will be needed. The length
¹⁶ of the fibers and bundles has to be calculated considering the exact position of the feedthrough

¹Allectra™, <http://www.lectra.com/index.php/en/>.

²Thorlabs™, <https://www.thorlabs.com/thorproduct.cfm?partnumber=FT800UMT>.

³Thorlabs™, <https://www.thorlabs.com/thorproduct.cfm?partnumber=FT200UMT>.

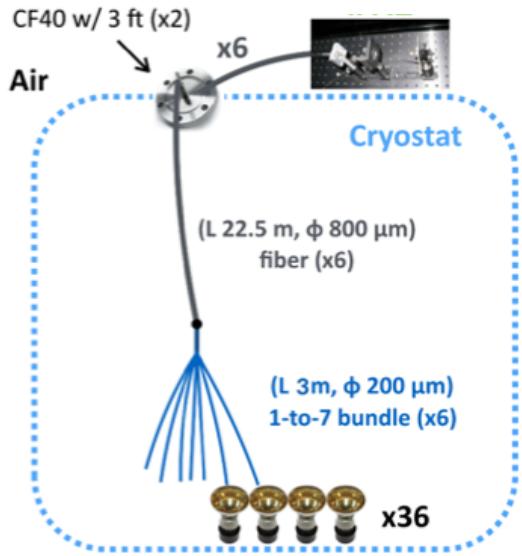


Figure 2.1: Diagram of the photon calibration system to be implemented in ProtoDUNE-DP

fig:dpp

¹⁷ flanges. The number of flanges required to host 120 SMA feedthroughs will depend on their size.
¹⁸ However, alternatives to this design will be pursued with R&D measurements in order to reduce
¹⁹ the amount of fibers, study other options for the reference sensor, and increase the input light if
²⁰ necessary. In order to reduce the number of fibers, light diffusers can be used, so that one fiber
²¹ can illuminate at least 4 PMTs. For instance, a diffuser could be placed at the ground grid.

²² 2.1.2 Validation Tests

²³ In order to validate the design, the most important result will come from the ProtoDUNE-DP
²⁴ performance. In any case, since the fibers to be used in DUNE FD will be longer, dedicated
²⁵ calculations and measurements to confirm that sufficient light reaches the PMTs will be performed.
²⁶ Also, alternative designs, will be validated in different laboratories. The possibility of using a
₁ diffuser can be tested in a vessel. The light source will also be validated by studying the different
₂ options in the lab. All these measurements will be performed at room temperature and in liquid
₃ nitrogen to test the behavior at cryogenic temperatures.

⁴ Once the design is fixed, basic characterization measurements will be performed on the fibers
⁵ upon receiving them from the manufacturer. Those measurements will consist of providing light
⁶ with a known source and measuring the output with a power meter. Measurements at cryogenic
⁷ temperatures may not be needed at this point.

⁸ Finally, during the photon calibration system installation, each fiber and source will be re-tested to
⁹ check that the expected light is arriving to each PMT using a photodiode. A dedicated procedure
¹⁰ will be designed with this purpose, similar to the one used in ProtoDUNE-DP.

11 2.2 Photon Detector Performance

12 To define the photon detection system (PDS) performance, a good understanding of the light
 13 generation is needed. For this, optical simulations and a good knowledge of the light properties are
 14 required. The DUNE experiment expects to record not only accelerator neutrino interactions, but
 15 also rare non-beam events such as supernova neutrino bursts (SNBs) or nucleon decays. In those
 16 cases, an internal trigger is required: an optimized light collection system is hence mandatory. This
 17 section describes the tools developed in the consortium for the light simulation in large detector
 18 volumes for these purposes.

19 The main feature of a LArTPC detector is to collect electrons produced by the energy loss of
 20 charged tracks when crossing the volume. This signal provides a high resolution 3D image of the
 21 event. The reconstructed topology and the amount of charge collected gives the characterization of
 22 the tracks (identification and energy). Together with the charge, scintillation light is also produced
 23 in LAr. There are many advantages to collect and exploit the scintillation signal. As only a fraction
 24 of the initial energy deposition is converted into electrons, the rest being emitted as photons, light
 25 collection can improve the calorimetry of the detector. The light signal can provide the t_0 of
 26 the event, which is a necessary observable for a proper reconstruction. The study of the slow
 27 component can give insights into the purity of the LAr.

28 When energy deposition occurs, either the knocked argon atom gets excited or an electron is ejected.
 29 For the latter case, the electron has a probability to be recaptured by an argon ion,
 30 which depends on the drift field and on the amount of energy deposited. In this case, an excited
 31 argon state is also produced. In order to decay to ground state, the excited argon combines with
 32 another argon atom, to form an excited eximer. A photon at 127 nm is then emitted to allow the
 33 eximer to return to ground state. As the eximer can be formed in a singlet or triplet state, two
 34 time constants will be observed: the singlet at 6 ns and the triplet at 1.3 μ s. These principles are
 35 sketched in Figure 2.2. fig:dppd 60

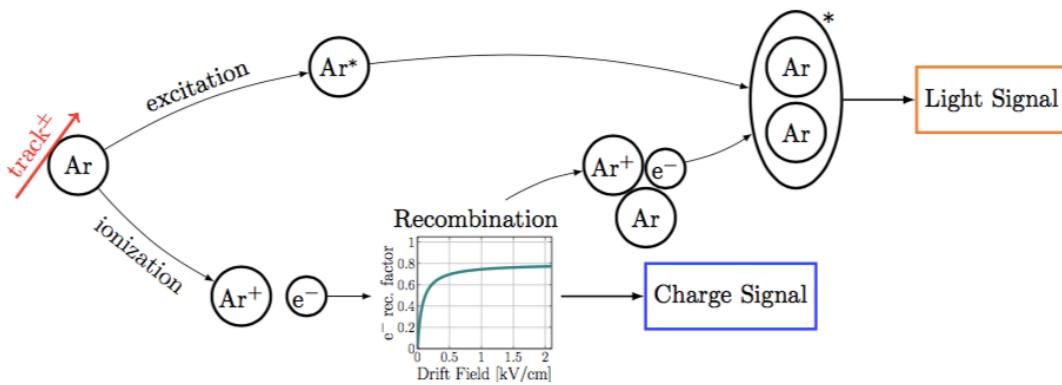


Figure 2.2: A sketch depicting the mechanism of light production in argon.

36 In the DP technology two light signals produced, one (S1) when a charged particle crosses the
 37 LAr volume and the second (S2) once the particle is above the liquid surface in the argon gas. As
 1 electrons drifting in the gas enter high field regions (such as the extraction field or the amplification
 2 field in the LEMs), their velocities increase and Townsend avalanches occur. This current of

3 electrons produces electroluminescence light with the same wavelength and similar time structure
 4 as for the S1 signal. The S2 light is expected to be an irreducible background for the light studies
 5 in ProtoDUNE-DP, since the detector is on the surface. Indeed, the S2 signal can last as long as
 6 the total drift time of the electrons: 0.625 ms per meter of drift at a drift field of 500 V/cm.

7 *tab:ddp_t_6_0* Table 2.1 summarizes the default optical parameters chosen for the light simulation methods
 8 described in Section 2.2.1. The LAr optical properties are the subject of significant discussions
 9 in the community, in particular regarding the LAr absorption length and the Rayleigh scattering
 10 length. The former affects the collected light yield whereas the latter mostly affects its uniformity
 11 and timing resolution. The absorption and reflection of the VUV photons on stainless steel (i.e., the
 12 drift cage, cathode, extraction grid and ground grid) and on copper (the LEM surfaces) are poorly
 13 known, largely because those reflection coefficients depend strongly on the polishing procedure.

14 The measurement of the quantum efficiency of the PMTs at VUV wavelengths requires a specific
 15 setup operating in vacuum since VUV photons are absorbed in air. The PMT quantum efficiencies
 16 in the WA105 DP demonstrator PMTs were measured before and after the tetra-phenyl butadiene
 17 (TPB) coating using a LED that could emit light in the 200 to 800 nm range.

18 Finally, the electroluminescence gain G , defined as the number of S2 photons produced per ex-
 19 tracted drifting electron, is also subject to discussion. Experimental measurements of G have been
 20 performed in a setup quite similar to the amplification design of the DP technology, although the
 21 measurements were made above the LEM [?]. In our case, the S2 photons are the ones leaving the
 22 LEM from below, where the number can be significantly lower. *Monteiro:2012zz*

Table 2.1: Default optical parameters chosen for the light simulation methods. Below the thick line are presented some quantities used in our studies although they are not linked to the optical properties of the LAr.

	VUVs photons $\lambda = 127 \text{ nm}$	Shifted photons $\lambda = 435 \text{ nm}$
Absorption length		∞
Rayleigh scattering length	55 cm	350 cm
Absorption coefficients	100%	50%
LAr refractive index	1.38	1.25
PMT quantum efficiency		0.2
Electroluminescence gain	300	

23 To understand the performance of the PDS, it is important to take into account the following
 24 indicators:

- 25 • Overall detected light yield, in photoelectrons per MeV of deposited energy in LAr;
 26 • Uniformity of the light yield across the entire LArTPC active volume;
 27 • Event time resolution extracted from the detected photon signal.

28 In turn, these indicators directly affect the strategy and performance of the DP module trigger

²⁹ system (Section 2.3), and determine whether the photon detector (PD) technical design is sufficient
³⁰ to meet the DUNE physics goals. These higher-level studies will be available on the technical design
¹ report (TDR) timescale.

² Our current understanding of these performance indicators is largely based on ProtoDUNE-DP
³ simulations and the current status of the simulation work is discussed in detail in Section 2.2.1.
⁴ Work is focused on ProtoDUNE-DP in a first phase, and will expand to the DP module. For a
⁵ realistic ProtoDUNE-DP geometry, an average light yield of 2.5 photoelectron/MeV is expected
⁶ across the entire active volume. This promising yield assumes 36 8 in PMTs located below the
⁷ ProtoDUNE-DP cathode plane, averaging to one PMT per m². On the other hand, spatial non-
⁸ uniformities in the PD response are found to be important and need to be modeled in detail.
⁹ Variations as large as one order of magnitude both parallel to the drift direction (due to geometrical
¹⁰ effects and absorption of light by LAr) as well as perpendicular to it (due to light absorption on
¹¹ detector boundaries) are obtained. The event time resolution due solely to light production and
¹² light propagation times, i.e., neglecting electronics and data acquisition (DAQ) effects for now, is
¹³ expected to be of order $\mathcal{O}(100 \text{ ns})$ and hence largely sufficient for our purposes. These initial low-
¹⁴ level performance estimates will be refined with more realistic simulations and with ProtoDUNE-
¹⁵ DP data (Section 2.2.2) in the future. They will also be extended to the full DP module geometry
¹⁶ on the TDR timescale.

¹⁷ 2.2.1 Simulations

¹⁸ At zero drift field, when the electron recombination is maximum, roughly 40,000 γ/MeV are pro-
¹⁹ duced. At the nominal drift field of 500 V/cm, then 24,000 γ/MeV are generated. For reference,
²⁰ the energy deposited by a minimum ionizing particle (MIP) track is 2.12 MeV/cm. Given the size
²¹ of the ProtoDUNE-DP ($6 \times 6 \times 6 \text{ m}^3$) and the fact that it is located on surface, roughly 100 muons
²² are expected to cross the fiducial volume during the 4 ms time window of the DAQ. With a full
²³ GEometry ANd Tracking, version 4 (Geant4) ^{Geant4} [?] simulation, it takes more than three hours to
²⁴ propagate all the photons emitted by a single MIP track crossing the ProtoDUNE-DP detector. A
²⁵ full optical simulation is hence computationally prohibitive. Three simulation approaches are being
¹ explored to provide the light simulation needed for the design optimization of the DP module.

² 2.2.1.1 Generation of light maps

³ In this method, the photons are propagated in a full dedicated Geant4 simulation only once. The
⁴ main light characteristics needed for light studies (photon detection probability, called *visibility*
⁵ hereafter, and time profile) are stored in a map in a ROOT ^{root} [?] file format which can then be read
⁶ by any other simulation program. This work was done first using LightSim, a dedicated software
⁷ developed at LAPP, France. These maps have been adapted to be readable by LArSoft, where
¹ light maps are known as *photon libraries*. Work to generate them directly in LArSoft is in progress,
² in particular for S2 light, which has not yet been simulated for DP technology.

³ In the dedicated Geant4 code, special care has been taken to precisely describe all subdetector

components that might affect the light propagation: LEM plates, extraction grid, field cage (FC) rings, the cathode and its supporting structure, and the ground grid above the PMTs. The LAr fiducial volume is then divided into voxels of 25 cm^3 and 10^8 photons are isotropically generated at the center of each voxel. The number of photons reaching each PMT, and their arrival times are stored. The light map can then be built from these results. For each voxel and for each PMT, the visibility is computed as: $w = N\gamma^{\text{collected}}/N\gamma^{\text{generated}}$. In order to be able to reproduce the time profile, each distribution is fit to a Landau function. From the fits, three parameters are extracted: the minimum time for photons to arrive to the PMT, t_0 ; the peak of the distribution, t_{peak} from the Landau most probable value (MPV); and the distribution spread, the σ of the Landau function. These three parameters are stored in the light maps for each PD. The same procedure is done for the gaseous phase, although the voxel size is smaller in height (only 5 mm). In Figure 2.3, two fitted time distributions are presented. As is visible, the shapes of the time distributions depend strongly on the source-to-PMT distance. For close sources, the distributions are very sharp and the Landau description may not be the optimal function to use. On the other hand, for longer distances, the distribution is broader and the Landau fit reproduces the simulations quite well. For practical purposes, the Landau parametrization was used for all cases.

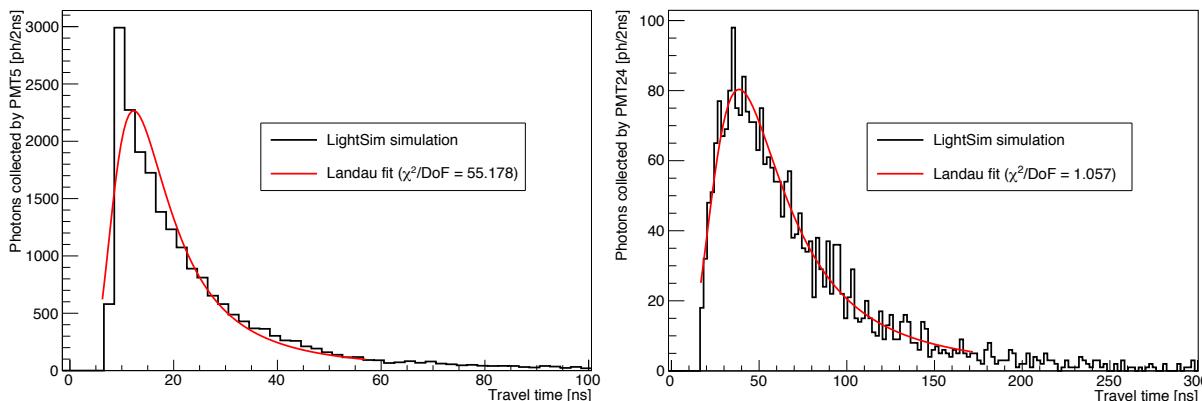


Figure 2.3: Landau fits (red line) of the travel time distributions (black histogram) for a source close to (left) and far from (right) the PMT.

As the map has been computed with discrete entries, an interpolation of the four light parameters (w , t_0 , t_{peak} , σ) between the actual source position and the closest voxel centers is performed. An example of the distribution of the visibility and its 3D interpolation is presented in Figure 2.4. The loss of photons due to the cathode and ground grid are visible. For the ProtoDUNE-DP cathode and supporting structure design, and using the default optical parameters presented in Table 2.1, it has been shown that up to $\sim 70\%$ of the photons generated in the active volume are absorbed by those structures before reaching the PMT array.

Table 2.1 presents the light propagation parameters used during the generation of the light maps. After generation, it is possible to study the loss of photons due to absorption using an approximation of the probability that the medium absorbs the photon as: $p_{\text{abs}} = \exp(-\frac{D_{\text{travel}}}{\lambda_{\text{abs}}})$. For the study of other light propagation parameters (Rayleigh scattering and absorption on the stainless-steel and copper) new maps have to be generated.

It takes roughly three days of computing to generate the light maps for ProtoDUNE-DP, even though only an eighth of the voxels need to be simulated, since the detector and the PMT po-

sitioning are symmetric. Generating maps for larger volumes such as the DP module, where the maximum source-to-PMT distance is around 60 m, could be too time-consuming. Moreover, the light simulation for the DP module is foreseen to drive the optimization of the positioning of the PMTs and will guide the studies of possible implementation of light reflectors. As most of the light propagation parameters in LAr are still subject to large uncertainties, these studies will have to consider various absorption and diffusion values. Therefore, it is crucial to find a faster way to simulate the light reliably, even at the cost of losing some precision.

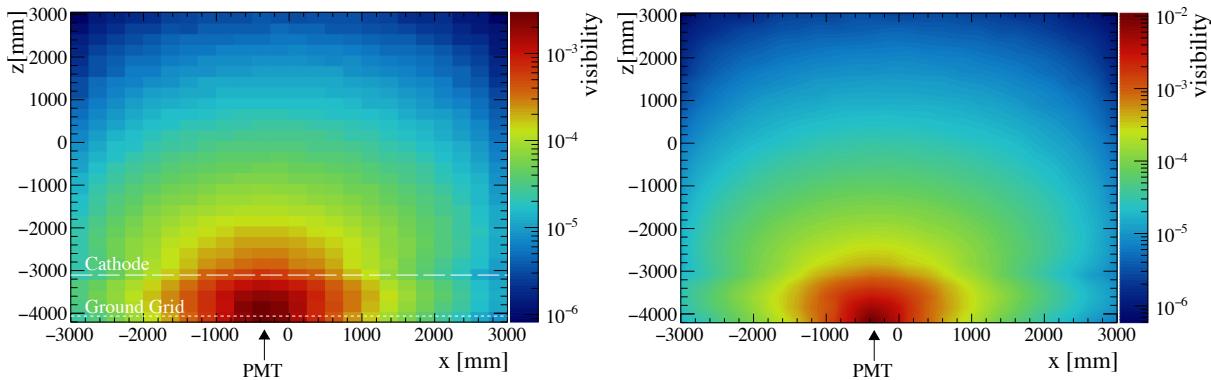


Figure 2.4: Evolution of the visibility seen by a central PMT (see arrow) in ProtoDUNE-DP as a function of different source positions in x and z (y is set at 0 mm). The position of the cathode and the ground grid are highlighted. Results are limited by the number of photons generated (10^7 photons per voxel), and voxels with less than 50 photons arriving to the PMT are not taken into account. Left: discrete values from the maps, right: after 3D interpolation.

fig:dppd

2.2.1.2 Parametrization from the Light Maps

Without considering the border effects where the photons are mostly absorbed, the visibility and the time profile depend only on the source-to-PMT distance.

This approach has been followed for the SBND^[?] light simulation and is under consideration for the DP module as well. In Figure 2.5 the evolution of the visibility and the peak time as a function of the source-to-PMT distance are shown. On the left, the borders are taken into account, and the visibility structure is quite complicated due to the complexity of the light simulation in a closed space. However, on the right, the same evolutions are presented only for voxels at least 1 m from the active volume boundaries, and a clear correlation between distance and visibility is observed. As for the time distribution (here for the peak time, but the same goes for t_0 and σ parameters), one can notice two different regimes when looking at all voxels, with a transition at a propagation distance of around 2 m. When considering only the central voxels, the evolution of the peak time is fully correlated with the propagation distance. The parametrization of the light propagation parameters as a function of the propagation distance is a promising option for very large volumes such as the DP module, at least for light sources far from the fiducial volume boundaries.

This preliminary study is quite encouraging for the light simulation in the DP module, at least for light sources far from the fiducial volume boundaries. Since it is complicated to disentangle the effects due to the propagation and absorption parameters from the light maps, a careful dedicated

20 study should be performed to get parametrization of the visibility and time distribution parameters
 21 as a function of the photon traveling distance.

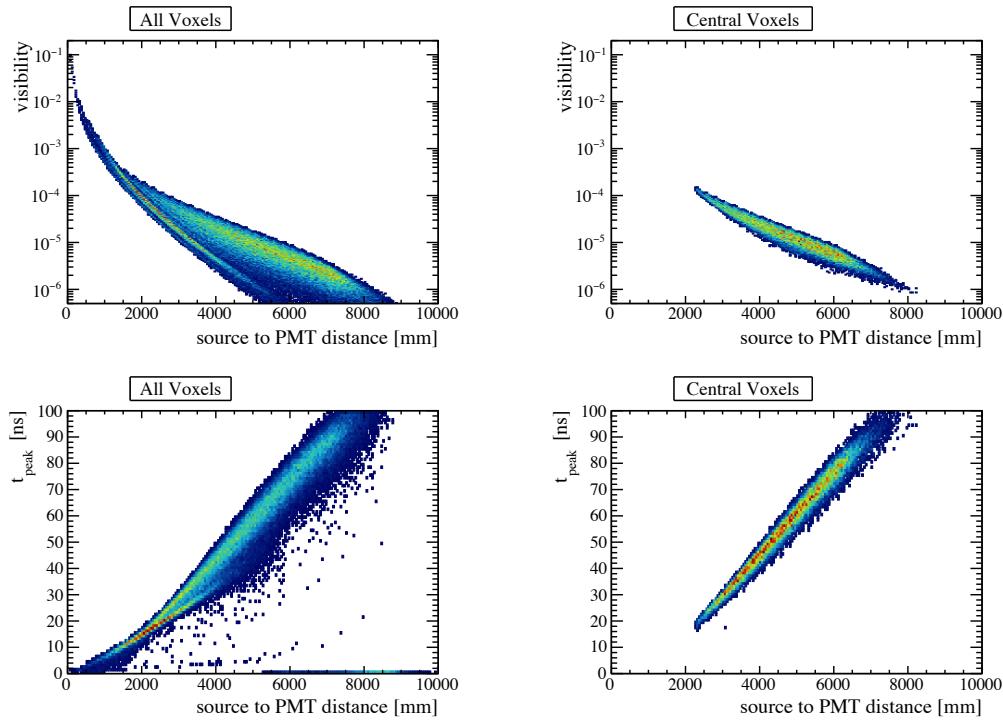


Figure 2.5: Evolution of the visibility (top) and peak time (bottom) as a function of the source-PMT distance as simulated in the ProtoDUNE-DP geometry (Preliminary study). On the left, all voxels are considered, on the right only the voxels at least 1 m away from the fiducial border are considered.

fig:dpp

22 2.2.1.3 Analytical approach

23 The propagation of light in a uniform material such as LAr can be described by the Fokker-Planck
 24 diffusion equation:

$$\frac{\partial}{\partial t} p(x, y, z, t) = D \left[\frac{\partial^2}{\partial x^2} p(x, y, z, t) + \frac{\partial^2}{\partial y^2} p(x, y, z, t) + \frac{\partial^2}{\partial z^2} p(x, y, z, t) \right]$$

25 where D is the diffusion coefficient. In an unbound medium, the Fokker-Planck equation is solved
 26 by the Green function:

$$G(\mathbf{r}, t; \mathbf{r}_0, t_0) = \frac{1}{[4\pi Dc(t - t_0)^{3/2}]} \exp \left(-\frac{|\mathbf{r} - \mathbf{r}_0|^2}{4Dc(t - t_0)} \right)$$

$$D = \frac{1}{3(\mu_A + (1 - g)\mu_S)}$$

where μ_A and μ_S are the absorption and scattering coefficients, respectively (both in units of m^{-1}), g is the average scattering cosine ($g = 0.025$). In LAr with the default optical properties in Table 2.1, $D = 18.8\text{ cm}$. In a bound medium, with full absorption of the photons by the FC and LEMs, a few additional techniques have to be used to obtain a solution. With this method, it takes only a few ms to generate the photon density at a given PD from a specific point source. From preliminary studies, relatively good agreement between analytical approach and full simulation has been found. In particular, the arrival time distributions of photons on the PMTs are well reproduced. The only drawback is that one cannot easily implement or study a complicated geometry including regions that are semi-transparent to light. Hence, the visibilities generated by the two methods are not in agreement. in the overall light yield, but have a very similar trend in terms of spatial dependences. Studies to improve the analytical method results are in progress since this approach could be extremely powerful for physics studies in the SP module.

2.2.1.4 Simulation of light yield

The light collected per PMT can be simulated together with the charge for crossing tracks in a standard simulation code where a detailed description of the detector is not needed. At each step of the track propagation, the energy deposited is computed by Geant4. This energy is converted into number of electrons and photons produced. As for the light simulation, the number of photons reaching each PMT and their time of arrival is now obtained from the light maps. As an example, the light yield from a uniform generation of 10 MeV electrons in the active volume is shown in Figure 2.6. The number of photoelectrons/MeV shown is summed over all PMTs and averaged over the y axis (z being the drift direction). One can notice the large spread in terms of light yield.

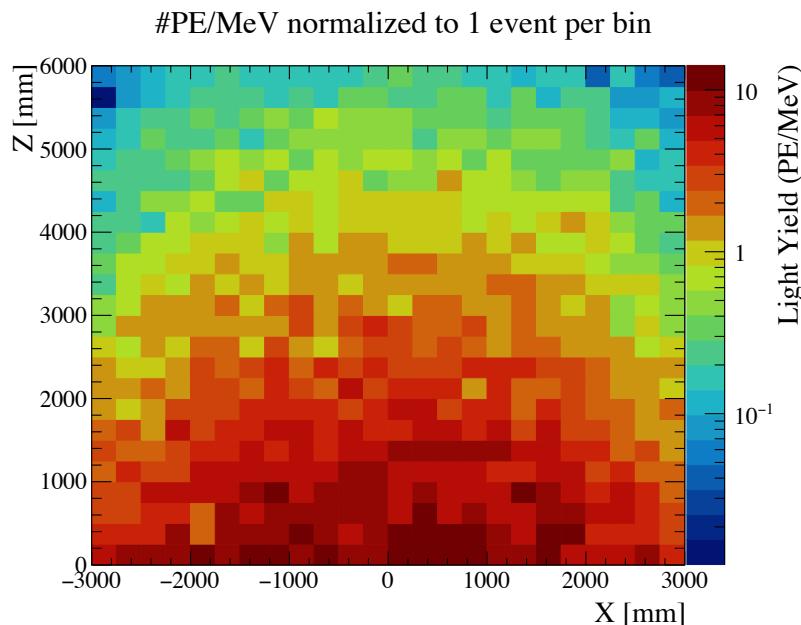


Figure 2.6: Light yield in terms of photoelectron/MeV summed over all PMTs and averaged along the y -axis. The mean of all voxels gives a light yield of 2.5 photoelectron/MeV, although the distribution is not uniform, in particular along the z (drift) axis.

For larger volumes such as the DP module, the light maps might be too big and the time spent

21 accessing the four parameters might strongly reduce the speed of the simulation. Either the
 1 parametrization method or the analytical approach are foreseen to replace the current light map
 2 usage, the exact strategy is yet to be defined.

3 2.2.2 Light Data in DP Prototypes

4 The WA105 DP demonstrator was operated from June to November 2017 with cosmic data. About
 5 million light events were taken with various configurations. The study of the S1 light as a function
 6 of the drift field was performed. An example of an averaged waveform fitted to a fast and a slow
 7 scintillation components is shown in Figure 2.7. The amount of S2 light can be monitored as a
 8 function of the extraction and LEM amplification fields.
fig:dppd_6

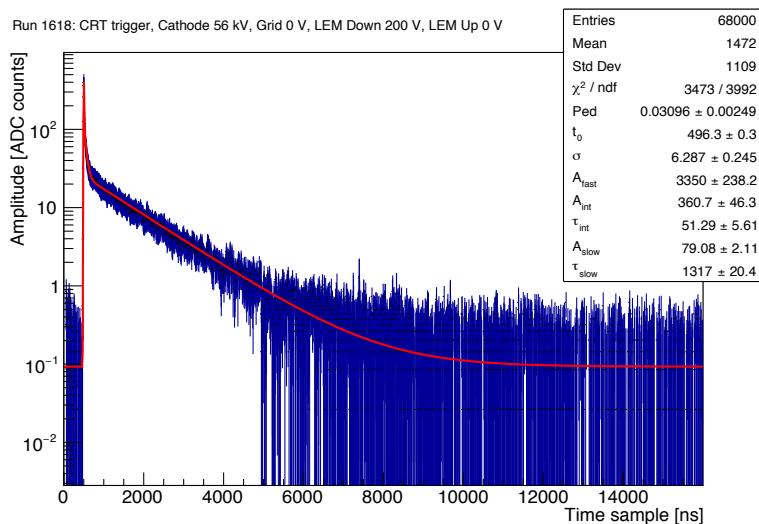


Figure 2.7: Averaged waveform of the S1 light signal taken with one PMT from the WA105 DP demonstrator, fitted with a function (red line) that is the sum of a Gaussian, parametrized by t_0 and σ , and two exponential functions, with decay time constants τ_{fast} and τ_{slow} , and normalization factors A_{fast} and A_{slow}

9 Light maps have also been generated with the demonstrator geometry, and data-Monte Carlo (MC)
 10 comparisons are ongoing. The preliminary results look promising, although the statistics in each
 11 setting and the relatively small size of the detector still constitute a challenge to extract the entire
 12 optical properties of the LAr.

13 2.2.3 Simulation of Physics Events

14 A preliminary study to understand whether the DP PD technical design meets the experiment's
 15 physics requirements has been performed. In this study, event topologies of interest for DUNE
 16 physics have been simulated using LArSoft fast optical simulation tools.

The simulation framework used represents the current state of the art. It includes realistic models for the primary scintillation production yields in LAr, for Rayleigh scattering in LAr, for detector optical properties (such as FC reflectivity and cathode transparency), for the density of PMTs underneath the cathode, and for the quantum efficiency of the TPB-coated PMTs (taken to be 20%). On the other hand, these simulations do not yet include the full DP module geometry, but are rather performed in a ProtoDUNE-DP geometry with the same average PMT density as the one proposed here for the DP module (one PMT per m²). Relevant aspects such as secondary scintillation light emission in gaseous argon (a nuisance for event t_0 determination), light absorption in LAr, electronics effects, reconstruction effects, and background contributions coming from ³⁹Ar decays are not accounted for either in this study. While more realistic simulation results including the above effects will be produced on the DUNE TDR timescale, this preliminary study already provides a sense of the capabilities of the planned PD design.

fig:dpd 6 3 1
Figure 2.8 shows the expected light yield for SNB neutrino CC interactions. As a representative ν_e flux from a SNB, we assume a Fermi-Dirac distribution with $T=3.5$ MeV temperature and no neutrino oscillation effects, yielding an average neutrino energy of about 11 MeV. Low-energy ν_e CC interactions throughout the entire LArTPC active volume are generated with the LArSoft-based Marley package. For the assumed SNB neutrino flux and for a single interacting neutrino (hence, after convoluting flux and cross-section effects), Marley expects about 19 MeV of energy deposited in the LAr active volume, primarily from the final state electron and from nuclear de-excitation gamma rays. The left panel of Figure 2.8 shows a broad light yield distribution, averaging at about 50 detected photoelectrons per interaction and after summing all PMTs. This is as expected from fig:dpd 6 3 1 the light yield distributions per deposited energy shown in Figure 2.6. The right panel shows the fraction of SNB ν_e CC interactions within the LArTPC active volume above a given photoelectron detection threshold, as a function of the photoelectron threshold. From the figure, we conclude that about a 70% fraction of SNB ν_e CC interactions would be seen by the PD, if the detector threshold was set at 10 photoelectrons on the sum of the PMT charges.

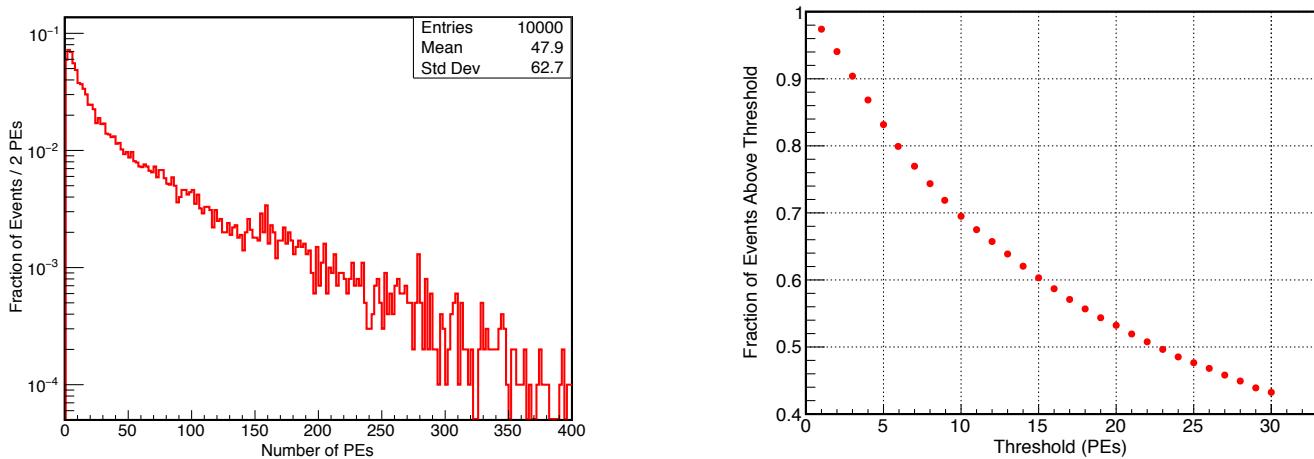


Figure 2.8: Photon detector response for simulated SNB neutrino interactions in the ProtoDUNE-DP geometry. Left panel: distribution of detected photoelectrons per neutrino interaction, for SNB ν_e CC interactions throughout the active volume. Right panel: fraction of SNB ν_e CC interactions above photoelectron threshold, as a function of the photoelectron threshold.

fig:dpd 6 3 2
Figure 2.9 shows the corresponding plots for a representative nucleon decay final state in DUNE, namely $p \rightarrow \bar{\nu}K^+$. Nucleon decay events are generated using Generates Events for Neutrino

11 Interaction Experiments (GENIE), accounting for both initial and final state nuclear effects in
 12 argon nuclei. Particles exiting the nucleus are then propagated in LAr using all relevant, Geant4-
 13 based, physics processes. The deposited energy per nucleon decay, of order 300 MeV, is much higher
 14 than the one per SNB neutrino interaction. As a result, the expected light yield for $p \rightarrow \bar{\nu}K^+$
 15 events throughout the active volume, shown in the left panel of Figure 2.9, averages to about
 16 800 photoelectrons in this case. The right panel of Figure 2.9 shows that about a 98% fraction
 17 of $p^+ \rightarrow K^+\bar{\nu}$ decays in the TPC active volume are expected to be seen by the PD, for a PD
 18 threshold of 10 photoelectrons on the PMT charge sum.

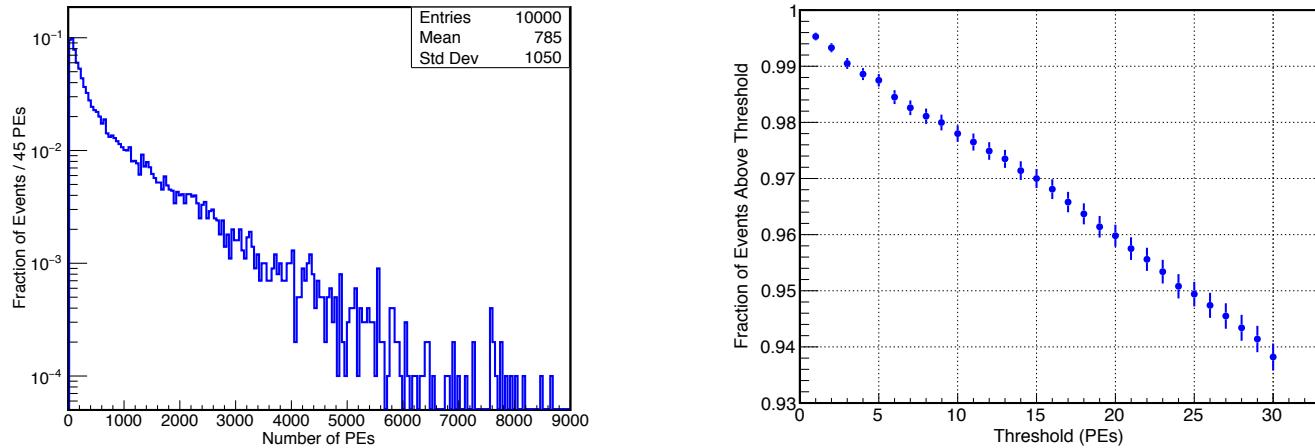


Figure 2.9: Photon detector response for simulated nucleon decays in the ProtoDUNE-DP geometry. Left panel: distribution of detected photoelectrons per nucleon decay, for $p \rightarrow \bar{\nu}K^+$ decays throughout the active volume. Right panel: fraction of $p^+ \rightarrow K^+\bar{\nu}$ decays above photoelectron threshold, as a function of the photoelectron threshold.

fig:ddp

19 2.3 Photon Detector Operations

20 2.3.1 Trigger Strategy

21 As explained in Section ??, the PDS will operate in different acquisition modes. These modes
 22 include the external trigger, which is the case of the beam events; the trigger for non-beam events
 23 such as SNBs; and the calibration mode.

- 1 In the LArTPC there are different uses of the light signal: cosmic ray and track timing for the
 2 reconstruction; non-beam events trigger such as SNB, atmospheric neutrinos, and proton decay;
 3 and calorimetry, as the light and charge signal are anti-correlated. These physics studies imply
 4 different requirements in terms of dynamics of the electronics and data sampling, from a few
 5 photoelectron to a much higher level.
- 6 For the non-beam event trigger strategies, the requirements can be very different. In the event
 7 of a nearby (10 kpc) SNB, it is expected that a few thousands of neutrinos will homogeneously
 8 interact in the detector module for a period as long as ~ 100 s. Hence, the SNB trigger strategy

9 is mostly driven by the energy threshold set for ν detection and its efficiency: 30 MeV is sufficient
 10 for a galactic SN, 5 MeV is needed for a burst in Andromeda. A high-efficiency trigger for proton
 11 decay events has to be designed considering the worst case scenario, e.g., the event happening at
 12 the top of the detector module, 12 m away from the closest PMT. In order to minimize the amount
 13 of spurious triggers, one can think of signal thresholds for a cluster of close-by PMTs.

14 All these important studies will be further investigated once a reliable light simulation of the DP
 15 module is available. For the DP technology, the main light trigger concerns are the amount of
 16 light collectable for a photon traveling distance of 12 m and the S1-S2 separation. The data that is
 17 collected in the ProtoDUNE-DP will provide crucial inputs for the optimization of the DP module
 18 light-collection system and for the design of an efficient trigger strategy for rare non-beam events.

19 The PDS trigger design is flexible so as to fulfill the different physics requirements explained before.
 20 The light readout front-end (FE) board will be in charge of the PDS trigger generation. The trigger
 21 will be decided based on the coincidence of several PMT signals over a threshold during a time
 22 window. The number of PMTs that contribute to the trigger, the signal threshold and the length of
 23 the coincidence time window will be programmable on-line to be able to adapt to different physics
 24 cases.

25 **2.3.2 Data Quality Monitoring**

26 The PMTs installed at the bottom of the tank will be operated for 10 to 20 years with no possibility
 27 to access them. Monitoring tools to ensure data quality of the PDS will have to be developed to
 28 catch any malfunctioning detector before data analysis. For instance, the amount of dark noise
 29 and the stability of the PMT response will have to be monitored over time. For the gain evolution,
 30 either studies of standard candles, e.g., from Michel electrons or average collected light produced
 31 by cosmic tracks, or with the dedicated calibration system are considered.

32 Monitoring tasks were performed during the six months of operation of the WA105 DP demon-
 1 strator with no dedicated light calibration system. This and the forthcoming operation of the
 2 ProtoDUNE-DP, will again provide crucial input towards the PDS monitoring system in the DP
 3 module.

4 **2.4 Interfaces**

5 The PDS will have several interfaces with other subsystems and the global DUNE systems. The
 6 interface documents related to DP module PDS are given in Table 2.2. Only part of the basic
 7 interfaces are summarized below.

- 8 • DP module electronics: The PDS shares the same FE electronics standard as the charge
 9 readout, which is μ TCA based [?]. Specifications of both PDS and FE electronics will be
 10 determined by the simulations and ProtoDUNE-DP data.

Table 2.2: DP PD interface documents

DP PD Interface Document	DUNE docdb number
DP module electronics	6772
DP module high voltage (HV)	6799
DAQ	6802
cryogenic instrumentation and slow controls (CISC)	6781
DUNE Physics	7087
Software and Computing	7114
Calibration	7060
integration and test facility (ITF)	7033
Detector and Facilities (LBNF) Infrastructure	6979
Installation	7006

- 11 • HV: This interface includes the consideration of the distance between the cathode and the
 12 PMT planes, power dissipation from the PMTs and the combined impact on the simulations.
- 13 • DAQ: The hardware interface is mainly through optical fibers. DP module PDS provides
 14 trigger and data in continuous streaming; the interface also includes the DAQ software.
- 15 • CISC: The main interface points are the layout of the cryogenic instrumentation (e.g., purity
 16 monitors and light emitting system for the cameras) and the PMT support structures and
 17 cabling; and the slow control and the PDS power supplies and calibration system.
- 18 • DUNE physics: DP PD has interfaces with the overall physics requirements on energy and
 19 time together with classification of events, decay modes and neutrino flavors.
- 20 • Software and Computing: This interface is on the development of simulation, reconstruction
 21 and analysis tools.
- 22 • Calibration: The PDS is participating in the Global Calibration Task Force and will provide
 23 handles to allow global monitoring of the PMT performance.
- 24 • ITF: The operations at the ITF are described in Section 2.5.2. The interface items can be
 25 summarized as shipping and receiving of the PDS components and basic testing and repairing
 26 at the facility. The interface also includes recycling and returning the packaging materials.
- 27 • Detector and Facilities (LBNF) Infrastructure: The PDS PMT mounting structures stand
 28 on the cryostat membrane; cold cables are routed in cable trays to the ceiling feedthrough
 29 flanges and racks and to cable trays on top of the cryostat. Other interfaces with the facility
 30 include access to conventional facilities and participation in the detector safety systems.

31 check this one; small edits

- 32 • Installation: This interface includes the transportation of the PDS components to and be-
 33 tween underground areas, clean room activities and storage, and installation coordination

2 with the other teams.

3 **2.5 Installation, Integration and Commissioning**

4 **2.5.1 Transport and Handling**

- 5 The 720 PMTs of the PDS are shipped from various locations following base and cable assembly
6 for the TPB coating at the ITF. They are shipped in boxes of 24, for a total of 30 deliveries. The
7 PMTs are individually wrapped with special wrapping materials.
- 8 The PMTs are placed in modular shock-absorbing assemblies inside the boxes. The boxes have
9 integrated pallets for easy handling and short distance transportation, and a limited amount of safe
10 inclination for the assemblies is allowed. The PMTs will reach the ITF by means of air and ground
11 transportation. Each box has a dedicated bar-code which is visible on each side. This bar-code is
12 also associated with the shipping documents.

13 **2.5.2 Integration and Testing Facility Operations**

- 14 The ITF receives the PMT boxes and also manages a shipping and delivery database. The received
15 status of the boxes is available to the DP PD consortium as the boxes arrive at the ITF. The PDS
16 characteristics database managed by the DP PD consortium is updated accordingly to reflect the
17 received status of the contents of the boxes. Each PMT assembly gets an identifying bar code that
18 is directly connected to the PDS characteristics database. This database stores the PMT serial
19 number, the base board serial number, special information about TPB coating and assembly if any,
20 and performance and calibration characteristics. This database forms the basis of the operations
21 database, providing the initial calibration values. It also stores information about the ITF tests
22 and underground installation and commissioning tests.
- 23 The TPB coating is performed at the ITF in the coating stations, after which the PMTs are placed
24 back in their boxes and dedicated testing electronics are connected to the PMT cables soldered
25 to the PMT bases. The test electronics enables connecting several PMTs at a time. The tests
26 include basic functionality checks of both the PMTs and the base boards to assess the performance
27 after transportation. No detailed performance characteristics are measured at the ITF. The tests
28 are performed in a dedicated room with light and climate control. Once the performance of the
29 PMTs in a box is validated, the boxes are closed with the original covers. Before closing, additional
30 quality checks on the shock absorbing assemblies are made.
- 31 The preparation of the PMT boxes for underground transportation includes installing holding and
32 lifting fixtures to the top and sides that allow crane operation. The boxes are delivered to the
33 surface station by ground transportation with appropriate updates to the shipping database.

34 **2.5.3 Underground Installation and Integration**

35 Once the PMT boxes are underground, the same top and side covers are opened as at the ITF. The
36 PMTs are carried to the underground storage area in sub-units of the modular shock-absorbing
1 assemblies. The underground storage area for the PDS is expected to be sufficiently large to store
2 at least 30 PMTs, enabling continuous installation operations.

3 The removal of the individual PMT wrappings is done in the clean room. PMTs together with
4 their base boards undergo visual inspection by the PDS installation supervisor. Once signed-off,
5 the installation can proceed with multiple PMTs at a time by multiple teams. Cabling is carried
6 out in parallel and relevant database updates are made in situ. The installation time management
7 is done in coordination with the cathode and FC installation groups.

8 The bundles of cables are routed through the cable trays along the cryostat walls from the PDS
9 flanges. Following the mechanical mounting of the PMTs to the cryostat floor, the PMT cables
10 are connected to the cables coming from the flanges. In parallel, the calibration fibers are installed
11 and routed through cable trays.

12 **2.5.4 Commissioning**

13 The commissioning of the PDS is performed in partitions. The size of a single partition will mainly
14 be determined by the DAQ and the HV systems. The DAQ and HV partitions are commissioned,
15 including the relevant control systems, prior to the connection of the PMTs to these systems.
16 Once the physical sector corresponding to a partition is installed, the PMTs are powered up, and
17 basic functionality and performance checks are performed. These include pedestal data taking,
18 i.e., recording event data with external periodic triggering, and tests with the calibration system
19 where the data taking is triggered in synchronization with a light source, as described in Section
20 2.1.

21 As a result of the commissioning tests, the basic performance characteristics of the PMTs, e.g.,
22 the dark count rate and gain, are measured in their final places. Installation-related issues are
23 identified and eliminated at this stage. A commissioned sector becomes a part of the overall
24 detector and can join the global calibration data taking and commissioning.

25 **2.6 Quality Control**

26 **2.6.1 Production and Assembly**

27 The quality control (QC) performed at the different institutions labs includes reception of PMTs
28 from the manufacturer and execution of the QC tests to accept or return the PMTs according to
29 the acceptance and rejection criteria.

- The PMT support structure design is validated by immersing its mounted PMT in cryogenic temperatures and at an over-pressure equivalent to a depth of 12 m in LAr.
- Design validation tests are carried out to confirm that the PMT base design fulfills the specifications at room and cryogenic temperatures. A cable with SHV connector is soldered to each PMT base to facilitate the different base and PMT tests and the final PMT connection during the installation. The PMT bases are labeled (on the cable) in order to keep track of them. After production of the PMT base boards they are individually tested before mounting to the PMT to verify that components are correctly mounted. Later they are cleaned and tested at maximum voltage in an argon gas environment to confirm that there are no sparks on these (worst case conditions). After mounting the bases on the PMTs they are tested again in argon gas at maximum voltage to confirm that there are no sparks due to bad soldering.
- All the light readout units (PMT + base + support) are tested and characterized in liquid nitrogen in order to check their performance at cryogenic temperature and to obtain a database with the most important parameters from each PMT (gain versus voltage, dark counts, etc.). The PMT base number attached to each PMT is also included in the database.
- The wrapping materials and techniques are studied with one fully assembled light readout unit. The handling, transportation and installation scenarios are carefully studied and the transportation box design is validated. The transport box and PMT wrapping must ensure complete darkness.
- The light output of the LEDs and the fibers' light transmission from the photon calibration system are measured with a power meter.

2.6.2 Post-Factory Installation

- Upon receipt at ITF, the PMTs go through verification measurements in order to identify any items damaged during transport. Gain versus voltage and dark current values are compared with those obtained before transportation.
- The TPB coating is also performed at the ITF. The first few samples undergo microscopic examination and surface uniformity tests, and the coating procedure is validated. The production PMTs are randomly sampled for basic coating QC.
- After transport from the ITF to SURF the PMTs are tested again before installation to confirm that no damage occurred during the last stage of transportation. During the installation, the PMTs database is updated with the position in the detector module of each PMT (identified by its serial number and base number). After installation, the full connection from the FE to the PMTs is checked. The FE channel and splitter number connected to each PMT are also included in the PMT database. Once it is possible to fully darken the detector module, voltage can be applied to the PMTs to test the signal with a scope or, if available, with the FE electronics.

¹⁶ 2.7 Safety

¹⁷ Safety is the highest priority at all stages of DP PD operations. Since DUNE is an international
¹⁸ project, the international safety regulations will be followed closely during the course of preparation
¹⁹ of safety documents.

²⁰ The main risks at the production and testing sites are electrocution, exposure to excessive heat,
²¹ chemicals and cryogenics, and heavy lifting. Detailed procedures will be developed by the relevant
²² institutes and approved by the DP PD consortium. Contents of the electrical safety rules will
²³ range from utilizing regular power equipment to handling PMTs for testing. The chemical and
²⁴ heat exposure hazards only concern the sites where the TPB coating is performed. The heavy-
²⁵ lifting risks concern mainly the PMT delivery boxes.

²⁶ The ITF DP PD safety regulations will be developed the same way. Main hazards at this site
²⁷ are electrocution and heavy lifting. Also, due to the quantity and frequency of shipments from all
²⁸ other subsystems, tripping and operating in a limited space will also be considered.

²⁹ The underground operation and installation safety rules will follow the general facility rules on
¹ e.g., working in confined spaces, oxygen deficiency hazard and emergency procedures. The DP PD-
² specific safety rules are particularly related to lifting the boxes and their contents for installation
³ and working at heights for cabling.

⁴ 2.8 Management and Organization

⁵ The DP PD consortium was formed in 2017 and it is composed of eleven institutes from France,
⁶ Peru, Spain, UK and USA. The charge of the DP PD consortium is to plan and execute the
⁷ construction, installation and commissioning of the DP module PDS.

¹²⁹⁵ 2.8.1 Consortium Organization

¹²⁹⁶ The DP PD consortium Leader (CL) is Inés Gil-Botella from CIEMAT (Spain) and the Technical
¹²⁹⁷ Lead (TL) is Dominique Duchesneau from LAPP (France). They are members of the DUNE
¹²⁹⁸ Technical Board and they represent the consortium to the overall DUNE collaboration. The CL
¹²⁹⁹ is responsible for the subsystem deliverables and for the effective management of the consortium.
¹³⁰⁰ The TL acts as the overall project manager and is the interface to the International Project Office
¹³⁰¹ (IPO); he is responsible for monitoring and reporting on progress with respect to the agreed
¹³⁰² schedule and for issues related to interface documentation.

¹³⁰³ The institutions participating in the consortium are responsible for the design or construction of
¹³⁰⁴ a particular subsystem. It is hoped that the national groups within the consortia will be able to
¹³⁰⁵ approach relevant funding agencies with a specific construction-phase proposal, such that a likely

¹³⁰⁶ funding line can be established in or before 2019. The DP PD consortium is open to any new
¹³⁰⁷ institution willing to join the current effort.

¹³⁰⁸ The current institutions participating in the DP PD consortium are summarized in Table 2.3. tab:dppd_t_12_1

Table 2.3: DP PD consortium institutions

Country	Institution	Contact
France	LAPP	Dominique Duchesneau
Peru	PUCP	Alberto Gago
Spain	IFAE	Thorsten Lux
Spain	CIEMAT	Inés Gil-Botella
Spain	IFIC	Michel Sorel
United Kingdom	University College London	Anna Holin
USA	Argonne National Lab	Zelimir Djurcic
USA	Duke University	Kate Scholberg
USA	University of Iowa	Jane Nachtman
USA	South Dakota School of Mines and Technology	Juergen Reichenbacher
USA	University of Texas at Austin	Karol Lang

¹³⁰⁹ The DP PD consortium is divided into four working groups: photosensors and electronics, cali-
¹³¹⁰ bration system, mechanics and integration, and simulation and physics. The corresponding WG
¹³¹¹ conveners are:

- ¹³¹² • WG1: Photosensors and Electronics - A. Verdugo (CIEMAT)
- ¹³¹³ • WG2: Calibration System - C. Cuesta (CIEMAT)
- ¹³¹⁴ • WG3: Mechanics and Integration - B. Bilki (Iowa)
- ¹³¹⁵ • WG4: Sim. & Phys. - K. Scholberg (Duke), M. Sorel (IFIC), L. Zambelli (LAPP)

¹³¹⁶ 2.8.2 Planning Assumptions

¹³¹⁷ The optimization and final design of the DP PD system will be driven by:

- ¹³¹⁸ 1. ProtoDUNE-DP data (expected by beginning of 2019)
- ¹³¹⁹ 2. Simulation studies (in progress)

¹³²⁰ ProtoDUNE-DP operation and data analysis are fundamental steps to understanding whether the
¹³²¹ current PDS design considered as baseline, based on cryogenic PMTs with TPB coating, is able to
¹³²² provide t_0 for non-beam events, background rejection and triggering on non-beam events. These
¹³²³ data will be used to tune the MC simulations and extrapolate the performance of the system to

1324 the DP module.

1325 Simulations are needed to determine and optimize the DP PD system to meet the physics require-
1326 ments in terms of:

- 1327 • Light collection efficiency,
- 1328 • Number of channels,
- 1329 • Photosensor requirements,
- 1330 • Dynamic range of readout electronics and timing resolution,
- 1331 • Trigger strategy on non-beam events.

1332 The DUNE physics requirements in terms of expected performance of the PDS should be provided
1333 by the DUNE Physics WG. Alternative design aspects of the proposed PDS considered as base-
1334 line for the DP module (see CDR document arXiv:1601.02984) will be developed based on the
1335 compatibility of ProtoDUNE-DP data and MC light simulation results with the DUNE physics
1336 requirements.

1337 2.8.3 WBS and Responsibilities

-pd-12.3

1338 The DP PD consortium has developed a detailed breakdown of deliverables and responsibilities
1339 included in the overall DUNE collaboration work breakdown structure (WBS), DUNE-doc-5594,
1340 coordinated by the IPO. The main deliverables are based on the ProtoDUNE-DP PDS and are
1341 divided into seven topics:

1342 WBS Element - *Institutions*

1343

- 1344 1. Management DP PDS (includes milestones and review dates) - *LAPP, CIEMAT*
- 1345 2. Physics and Simulations - *Duke, LAPP, IFIC, SDSMT, CIEMAT, PUCP, UCL, Texas-*
1346 *Austin*
- 1347 3. Design, Engineering, R&D and validation tests - *Iowa, CIEMAT, IFIC, UCL, Texas-Austin,*
1348 *IFAE, SDSMT*
- 1349 4. Production Setup (includes tooling) - *UCL*
- 1350 5. Production (includes component production, assembly, testing, and QC) - *Iowa, CIEMAT,*
1351 *IFAE, IFIC, UCL, Texas-Austin, Duke, SDSMT, LAPP*
- 1352 6. Integration (contributions to activities at global integration facility) - *SDSMT*

- ¹³⁵³ 7. Installation (contributions to activities at SURF) - *CIEMAT, IFIC, SDSMT, Iowa*

¹³⁵⁴ 2.8.4 High-Level Cost and Schedule

- ¹³⁵⁵ The cost of the baseline DP PDS will be defined in a separate document.

¹³⁵⁶ need a ref to it?

¹³⁵⁷ The DP PDS consortium's main activities during the next 16 months are focused on developing the TDR. The main high-level milestones are detailed in Table 2.4 for this period. The plan for ^{tab:dppd t 12_5} the activities in the post-TDR period is summarized in Table 2.5. ^{tab:dppd t 12_6}

Table 2.4: Pre-TDR Key Milestones

Milestone	End date
Simulations and physics: Implementation of DP optical simulation in LArSoft for ProtoDUNE-DP	08/2018
Simulations and physics: Optimization of the DP module performance to fulfill the physics requirements and definition of a trigger strategy	05/2019
Photosensors: Components selection and final design	03/2019
PMT calibration system design and selection of components	03/2019
Cabling definition and design of flange	03/2019
Design review in light of ProtoDUNE-DP calibration data	03/2019
QC plan	06/2018
Identification of Interfaces	06/2018
Integration, installation and commissioning plans	12/2018
DP module TDR	06/2019

Table 2.5: Post-TDR Key Milestones

Milestone	Start date	End date
PMT preparation and installation (can be done in batches)		
PMT procurement procedure and production	01/2021	12/2022
PMT base design and manufacturing	01/2022	12/2022
PMT support structure production and assembly	08/2022	01/2023
PMT characterization - 10 PMTs/week (two facilities)	02/2023	12/2023
TPB coating (two facilities similar to that for CERN ICARUS)	01/2024	12/2024
Splitter production and tests	05/2024	12/2024
Installation at SURF		
PMT cable and fiber routing in cryostat from flange to bottom (depends on FC and flange installation)	9/2024	9/2024
PMT testing, installation in cryostat and cabling (72 PMTs/month)	10/2024	07/2025
PMT support installation on the membrane (in parallel by sector with PMT installation)	10/2024	07/2025
Splitter installation (in parallel with PMT installation to test cabling and connections)	10/2024	07/2025
Light calibration system		
Fibers, light source tests and procurement	06/2023	05/2024
Fiber calibration system installation (in parallel with PMT installation with validation test)	9/2024	07/2025

1360 Chapter 3

1361 Data Acquisition System

fddp-daq

1362 3.1 Overview

d-daq-ov

DP/SP shared. Georgia Karagiorgi and Dave Newbold. 2 Pages - largely generic but some highlighting of SP-specifics. Focus on describing to HEP but non-data acquisition (DAQ) expert. Include how design is resilient in the face of potential uncertainties such as excess noise or the need to reduce drift HV (just two examples, maybe there are more).

1363

1364 3.1.1 Introduction

aq-intro

1365 The DUNE far detector (FD) DAQ system must enable the readout, triggering, processing and
1366 distribution to permanent storage of data from all detector modules which includes both their
1367 electrical time projection chamber (TPC) and optical photon detection system (PDS) signals. The
1368 final output data must retain, with very high efficiency and low bias, a record of all activity in the
1369 detector which pertains to the recognized physics goals of the DUNE experiment. The practical
1370 constraints of managing this output requires that the DAQ achieve these goals while reducing the
1371 input data volume by almost four orders of magnitude.

1372 The current generation of LArTPC DAQ, such as used in ProtoDUNE and MicroBooNE, produce
1373 data spanning a fixed window of time which is chosen based on the acceptance of an external
1374 trigger. The DUNE DAQ faces several major challenges beyond those of the current generation.
1375 Foremost, it must accept data from about two orders of magnitude more channels and from that
1376 data it must form its own triggers. This self-triggering functionality requires immediate processing
1377 of the full-stream data from a large portion of all TPC channels with a throughput of approximately
1378 one terabyte per second per detector module. From this data stream, triggers must be raised based
1379 on two very different patterns of activity. The first is activity is localized in a small region of one
1380 detector module, such as due to beam neutrino interactions or the passage of relatively rare cosmic-
1381 ray muons. This activity tends to correspond to a relatively large deposition of energy, around

1382 100 MeV or more. The second pattern that must lead to a trigger is lower energy activity dispersed
1383 in both time and spatial extent of the detector module, such as due to supernova neutrino burst
1384 (SNB).

1385 The DAQ must also contend with a higher order of complexity compared to the current generation.
1386 The FD is not monolithic but ultimately will consist of four detector modules each of 10 kt fiducial
1387 mass. Each module will implement somewhat different technologies and the inevitable asymmetries
1388 in the details of how data are read out from each must be absorbed by the unified DAQ at its front
1389 end. Further, each detector module is not monolithic but has at least one layer of divisions, here
1390 generically named detector units. For example, the SP module has anode plane assemblies (APAs)
1391 each providing data from a number of warm interface boards (WIBs) and the DP module has charge
1392 readout (CRO) and light readout (LRO) units associated with specific electronics crates. In each
1393 detector module, there are on the order of 100 detector units (150 for single-phase (SP) and 245 for
1394 dual-phase (DP)) and each unit has a channel count that is of the same order as that of an entire
1395 LArTPC detector of the current generation. The DUNE DAQ, composed of a cohesive collection
1396 DAQ instances called DAQ partitions, must run on a subset of all possible detector units for each
1397 given detector module. Each instance effectively runs independently from all others, however some
1398 instances indirectly communicate through the exchange of high-level trigger information. This
1399 allows, for example, each detector module to take data in isolation. It also allows for all detector
1400 modules to contribute to forming and accepting global SNB triggers, and to simultaneously run
1401 small portions – consisting of a few detector units – separately in order to debug problems, run
1402 calibrations or perform other activities while not interfering with nominal data taking in order to
1403 maintain high uptime.

1404 Substantial computing hardware is required to provide the processing capability needed to identify
1405 such activity while keeping up with the rate of data. The nature of various technical, financial
1406 and physical constraints leads to the need to house much of the computing hardware required for
1407 this processing to reside underground, near the detector modules. In such an environment, power,
1408 cooling, space, and access is far more costly than typical data centers.

1409 Past LArTPC and long-baseline (LBL) neutrino detectors have successfully demonstrated external
1410 triggering using information related to their beam. The DUNE FD DAQ will accept external
1411 information on recent times of Main Injector beam spills from Fermilab. This will assure triggering
1412 with high efficiency to capture activity pertaining to interactions from the produced neutrinos.

1413 However, even if the DUNE experiment were interested only in neutrinos from beam spills, an
1414 external beam trigger alone would not be sufficient. Absent any other information, such a trigger
1415 must inevitably call for the readout of all possible data from the FD over at least one LArTPC
1416 drift time. This would lead to an annual data volume approaching an exabyte (10^{18} bytes), the
1417 vast majority of which would consist of just noise. This entire data volume would have to be saved
1418 to permanent storage and then processed offline in order to get to the signals.

1419 DUNE’s physics goals of course extend beyond beam-related interactions, including cosmic-ray
1420 muons, which provide an important source of detector calibration, and atmospheric neutrino inter-
1421 actions, which give a secondary source from which to measure neutrino properties. Taken together,
1422 recording their activity will dominate the data rate. The DAQ must also record data with sen-
1423 sitivity to rare interactions (both known and hypothetical) such as nucleon decay, other baryon

number violating processes (such as neutron-antineutron oscillation), and interactions from the products of SNBs as well as possibly being able to observe isolated low-energy interactions from solar neutrinos and diffuse supernova neutrinos.

Some of these events, while rare in themselves, produce patterns of activity that can be mimicked by other higher-rate backgrounds, particularly in the case of SNBs. While the exact processes involved in SNBs are not fully understood, it is expected that a prolonged period of activity of many tens of seconds will occur over which their neutrino interactions may be observed. Individually, these interactions will be of low energy (relative to that of beam neutrino interactions, for example), and will be spread over time and over the bulk of the detector modules. Because of their signature and their importance, special attention is required to first ascertain that a SNBs may be occurring and to save as much data as possible over its duration.

Thus the DAQ must greatly reduce the full-stream of its input data while using the data itself to do so. It must do this efficiently both in terms of recording essentially all activity important to the physics goals of DUNE and in terms of a rate of data output that is manageable. To perform these primary duties the DAQ provides run control, configuration management, monitoring of both its processes and the general health of the data, and a user interface for these activities.

3.1.2 Design Considerations

The different detector modules vary in terms of their readout technology and schemes, timing systems, channel counts and data throughput and format. These aspects determine the nature of the digital data input to the DAQ. The design of the DAQ strives to contain the unique layers that adapt to the variation in the detector modules toward its front end in order to allow as many of its back end components to remain as identical across the detector modules as possible. In particular, the DAQ must present a unified interface to the ultimate consumer of its data, DUNE offline computing. It must also accept and process the data from a variety of other sources including the accelerator, various calibration systems (including laser, cold electronics (CE), photon detectors (PDs), and potentially others) as well as trigger sources external to DUNE. The modular nature of the DUNE FD implies that the DAQ instances running on each module must also exchange trigger information. In particular, exchanging module-local SNB trigger information will allow higher efficiency for this important physics. The DAQ must be optimized for the above while also retaining the flexibility to scale to handle risks such as excess noise, changes in high voltage (HV), cut network connectivity and other issues that could arise.

Currently, two major variations for the DUNE DAQ are under consideration. The eventual goal is to reduce this to a single high-level design which will service both SP and DP detector modules and be reasonably expected to support the third and forth modules to come. The first design, designated in this proposal as *nominal*, is illustrated in a high-level way in terms of its data and trigger flow in Figure ??^{Fig:daq-overview}. The second design, designated as alternative, is similarly illustrated in Figure ??^{Fig:daq-overview-alt}. The two variants differ largely at their FEs in terms of the order in which they buffer the data received from the detector module electronics and use it to form trigger primitives. They also differ in how they treat triggering and data flow due to a potential SNB. As their FEs are also sensitive to differences between the detector module electronics, this further variation for each

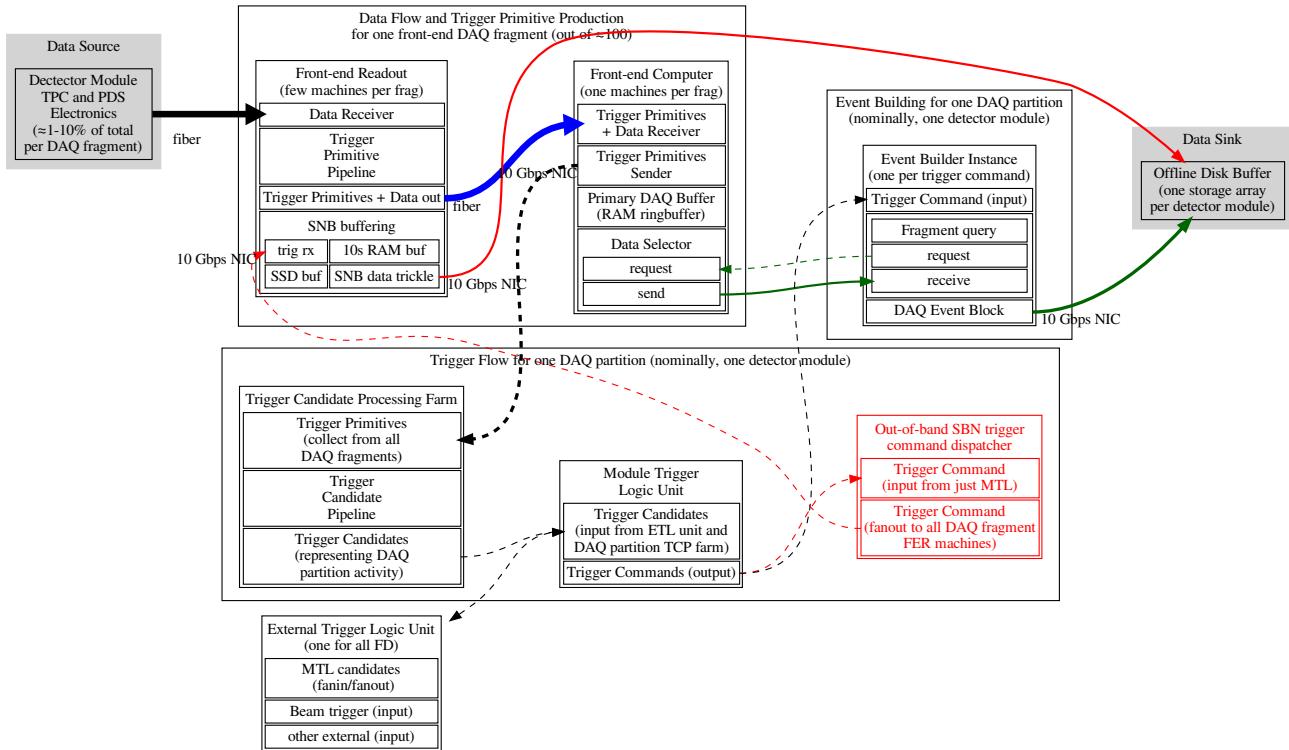


Figure 3.1: The high-level, *nominal* design for the DUNE FD DAQ in terms of data (solid) and trigger (dashed) flows between one DAQ front-end fragment FE and the trigger processing and event building back end for one DAQ partition. Line thickness indicates relative bandwidth requirements. Blue indicates where the full data flow for the DAQ front-end fragment is concentrated to one endpoint. Green indicates final output of normally triggered (non-SNB) data. Red indicates special handling of potential SNB. Each detector module has specialized implementation of some of these high level components, particularly toward the upstream FE as described in the text. The grayed boxes are not in the DAQ scope.

fig:daq-

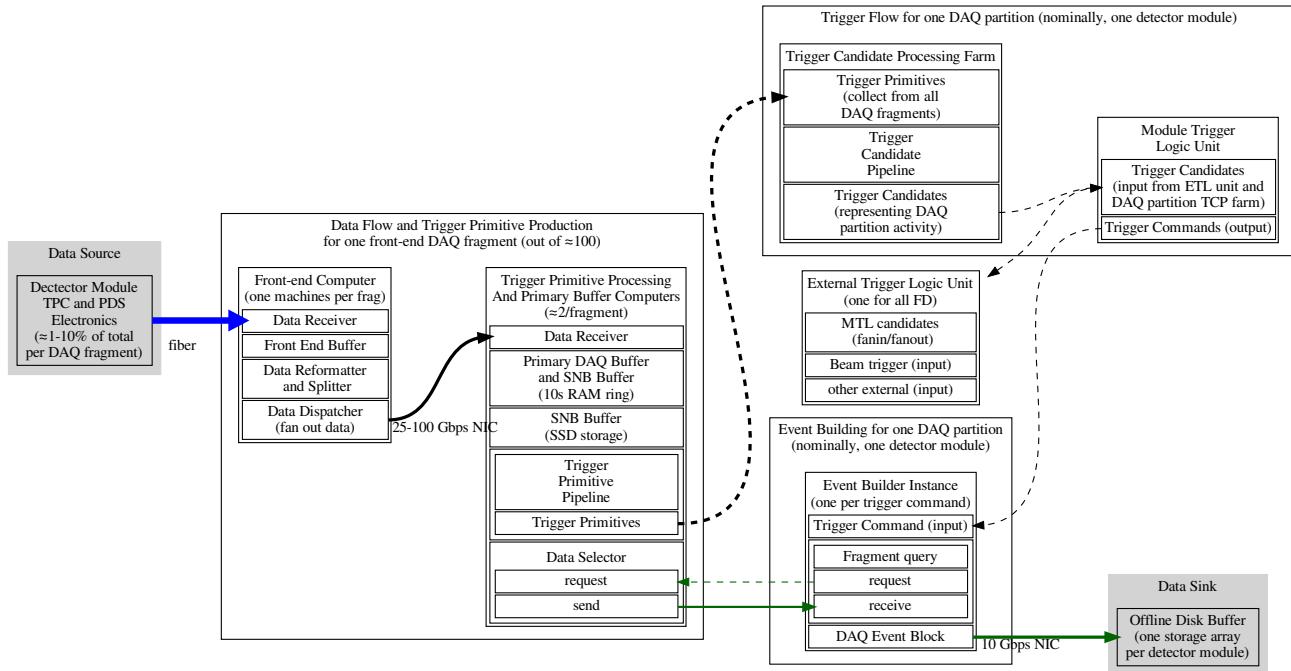


Figure 3.2: The high-level, alternative design for the DUNE FDFD DAQ in terms of data (solid) and trigger (dashed) flows between one DAQ front-end fragment FE and the trigger processing and event building back end for one DAQ partition. Line thickness indicates relative bandwidth requirements. Blue indicates where the full data flow for the DAQ front-end fragment is concentrated to one endpoint. Green indicates final output. Note, except for a longer readout, SNB is handled symmetric to normal data. Each detector module has specialized implementation of some of these high level components, particularly toward the upstream front-end as described in the text. The grayed boxes are not in the DAQ scope.

fig:daq-

1464 general design is described below in Sections [??](#) and [??](#) for the detector module specific to this
1465 volume.

1466 At this general high level, the two designs are outlined. For both, the diagrams are centered
1467 on one DAQ front-end fragment FE, which is a portion of the entire DAQ partition servicing a
1468 detector module that has one front-end computer (FEC) accepting about 10 to 20 Gbit/s of data
1469 (uncompressed rate) from some integral number of detector units. Each of the participating DAQ
1470 front-end fragments provide the actions:

- 1471 • Accept TPC and PDS data from the detector units associated with the DAQ front-end
1472 fragment.
- 1473 • Produce and emit a stream of per-channel trigger primitives.
- 1474 • Buffer the full data stream long enough for the trigger decision to complete (at least 10 s as
1475 driven by SNB requirements).
- 1476 • Accept data selection requests and return corresponding data fragments.

1477 All participating DAQ front-end fragments in the particular DAQ partition (i.e., the DAQ instance)
1478 servicing a portion of one detector module communicate with one trigger processing and event
1479 building system. The trigger processing system must:

- 1480 • Receive the stream of per-channel trigger primitives from all DAQ front-end fragments.
- 1481 • Correlate the primitives in time and spatially (across channels), and otherwise use them to
1482 form higher-level trigger candidates.
- 1483 • Exchange trigger candidates with the external trigger logic (ETL).
- 1484 • From them form trigger commands, each of which describes a portion of the data in time
1485 and a channel to be read out, such that no two trigger commands overlap.
- 1486 • Dispatch these commands as required (in general to the event builder (EB)).

1487 The event building system is responsible to perform the following actions:

- 1488 • Accept a trigger command and allocate one EB instance to dispatch it.
- 1489 • Interpret and execute the command by making data selection requests to referenced DAQ
1490 front-end fragments.
- 1491 • Accept the returned data fragment from each DAQ front-end fragment and combine them
1492 into a DAQ event block.
- 1493 • Write the result to the secondary DAQ buffer, which is the boundary shared with DUNE
1494 offline computing.

The nominal and the alternative DAQ designs differ largely in where the trigger primitive and SNB buffering exist. The *nominal* design places these functions in machines comprising a DAQ front-end readout (FER) which is upstream to the FEC. This then requires the SNB data and trigger handling to be different than that for normal (non-SNB) data. When a SNB trigger command is raised it is forwarded to the Out-of-band trigger command dispatcher (OOB dispatcher) which sends it down to the FERs. After the SNB data is dumped to solid-state disks (SSDs) it is “trickled” out via a path separate from the normal data to the secondary DAQ buffer. On the other hand, the alternative design places these functions downstream of the FEC in trigger processing and data buffering nodes. The RAM of those nodes is used to provide the primary DAQ buffer for normal triggering as well as the deeper buffers needed for SNB. The alternative design handles the SNB data somewhat symmetrically with normal data. When an EB makes a request for SNB data, it differs only in its duration, spanning tens of seconds of instead just a few milliseconds. The FE buffering nodes, instead of directly attempting to return the full SBN data immediately, streams it to local SSD storage. From that storage, the data is sent to the EB as a low priority (i.e., also trickled out). Since the module trigger logic (MTL) ensures no overlapping commands, the buffer nodes may service subsequent requests from post-dump data that is in the RAM buffer. Since each trigger command is handled by an individual EB instance, the trickle proceeds asynchronously with respect to any subsequent trigger command handled by another EB instances.

Further description of these designs is given in Section [??](#).
[sec:fd-daq-design](#)

The most critical requirements for the DUNE FD DAQ are summarized in Table [??](#).
[tab:daqrequirements](#)

Table 3.1: Important requirements on the DAQ system design

Requirement	Description
Scalability	The DUNE FD DAQ shall be capable of receiving and buffering the full raw data from all four detector modules
Zero deadtime	The DUNE FD DAQ shall operate without deadtime under <i>normal</i> operating conditions
Triggering	The DUNE FD DAQ shall provide full-detector triggering functionality as well as self-triggering functionality; the data selection shall maintain high efficiency to physics events while operating within a total bandwidth of 30 PB/year for all operating detector modules
Synchronization	The DUNE FD DAQ will provide synchronization of different detector modules to within 1 μ s, and of different subsystems within a module to within 10 ns

The input bandwidth and processing needs of the DAQ are expected to be dominated by the rate of data produced by the TPC system of each detector module. These rates vary between the modules and their estimations are summarized in Table [??](#).
[tab:daq-input-bandwidth](#)

The ultimate limit on the output data rate of the DUNE FD DAQ is expected to be provided by the available bandwidth to the tape, disk and processing capacity of Fermilab. An ample guideline has been established that places this limit at about 30 PB/year or 8 Gbit/s. Extrapolating to four detector module this requires the DAQ to perform a data reduction factor of almost four orders of

Table 3.2: The parameters governing the pre-trigger data rate from units of each detector module TPC CEs and the aggregate throughput into the FECs of the DAQ DAQ front-end fragments. Compression is an estimate and will be reduced if excess noise is introduced.

parameter	single-phase	dual-phase
TPC unit	APA	CRO crate
unit multiplicity	150	240
channels per unit	2560 (800 collection)	640 (all collection)
analog-to-digital converter (ADC) sampling	2 MHz	2.5 MHz
ADC resolution	12 bit	12 bit
aggregate from CE with compression	1440 GB/s 288 GB/s ($5\times$)	576 GB/s 58 GB/s ($10\times$)

magnitude. This is achieved through a simple self-triggered readout strategy.

An overestimate of the annual, triggered but uncompressed data volume for one 10 kt detector module is summarized in Table ???. It assumes a very generous and simple trigger scheme whereby the data from the entire detector module is saved for a period longer than two drift times around the trigger time. This essentially removes any selection bias at the cost of recording a substantial amount of data that will simply contain noise. Detailed trigger efficiency studies still remain to be performed. Initial understanding indicates that trigger efficiency should be near 100 % for localized energy depositions of at least 10 MeV. Sub-MeV signals can be ascertained from noise in existing LArTPCs so the effective trigger threshold may be even lower with high efficiency. Of course, data rates rise quickly when the threshold drops into the range of an MeV. Additional simulation and use of early data will be used to better optimize this threshold.

The data volume estimates also assume that any excess noise beyond what is expected due to intrinsic electronics noise will not lead to an increase in trigger rates. If, for example, excess noise occurs such that it frequently mimics more than about 10 MeV of localized ionization then this would lead to an increase in various types of triggers and subsequently more data. However, at the same time, these estimates do not take into account that some amount of lossless compression of the TPC data will be achieved. In the absence of excess noise it is expected that a compression factor of at least $5\times$ can be achieved with the SP data and up to $10\times$ may be achieved with the DP data. Of course, the compression factor achieved will ultimately depend on the level of excess noise experienced in each detector module cryostat. Studies using data from the DUNE 35 ton prototype and early MicroBooNE running have shown that a compression factor of at least $4\times$ can be expected even in the case of rather high levels of excess noise.

One category that will be particularly sensitive to excess noise will be the trigger primitives. As discussed more in Section ???, their primary intended use is as transient objects produced and consumed locally and directly by the DAQ in the trigger decision process. However, as their production is expected to be dominated by ^{39}Ar decays (absent excess noise) they may carry information that proves very useful for calibration purposes. Future studies with simulation and with early data will determine the most feasible methods to exploit this data. These may include committing all or a portion to permanent storage or potentially developing processes that can summarize their data while still retaining information salient to calibration.

Table 3.3: Anticipated annual, uncompressed data rates for a single SP module. The rates for normal (non-SNB triggers) assume a readout window of 5.4 ms. For planning purposes these rates are assumed to apply to the DP module as well, which has a longer readout time but fewer channels. In reality, lossless compression will be applied which is expected to provide as much as a $5\times$ reduction in data volume for the SP module and as much as $10\times$ for the DP module.

Event Type	Data Volume PB/year	Assumptions
Beam interactions	0.03	800 beam and 800 dirt muons; 10 MeV threshold in coincidence with beam time; include cosmics
Cosmics and atmospheric	10	10 MeV threshold, anti-coincident with beam time
Radiologicals	≤ 1	fake rate of ≤ 100 per year [?]
Front-end calibration	0.2	Four calibration runs per year, 100 measurements per point
Radioactive source calibration	0.1	source rate ≤ 10 Hz; single fragment readout; lossless readout
Laser calibration	0.2	1×10^6 total laser pulses, lossy readout
Supernova candidates	0.5	30 seconds full readout, average once per month
Random triggers	0.06	45 per day
Trigger primitives	≤ 6	all three wire planes; 12 bits per primitive word; 4 primitive quantities; ^{39}Ar -dominated

data-rates

Finally, it is important to note that early data will be used to evaluate other selection criteria. It is expected that efficient and bias-free selections can be developed and validated that save a subset of the entire detector module for any given trigger type. For example, a cosmic-muon trigger command will indicate which APAs contributed to its formation (i.e., which ones had local ionization activity). This command can then direct reading out these APAs, possibly also including their neighbors, while discarding the data from all other APAs. This may reduce the estimated 10 PB/year for cosmics and atmospherics by an order of magnitude. A similar advanced scheme can be applied the DP module by retaining data for the given readout window from only the subset of CRO crates (and again, potentially their nearest neighbors) that contributed to the formation of the given trigger.

3.1.3 Scope

The nominal scope of the DAQ system is illustrated in Figure [? fig:daq-overview](#) by the boxes that are not grayed out. It includes the continued procurement of materials for, and the fabrication, testing, delivery and installation of the following systems:

- FE readout (nominal design) or trigger farm (alternative design) hardware and firmware or software development for trigger primitive generation.
- FE computing for hosting of DAQ data receiver (DDR), DAQ primary buffer (primary buffer) and data selector.
- Back-end computing for hosting MTL, EB and the OOB dispatcher processes.
- External trigger logic and its host computing.
- Algorithms to generate trigger commands that perform data selection.
- Timing distribution system.
- DAQ data handling software including that for receiving and building events.
- The online monitoring (OM) of DAQ performance and data content.
- Run control software, configuration database, and user interface
- Rack infrastructure in the central utility cavern (CUC) for readout electronics, FE computing, timing distribution, and data selection.
- Rack infrastructure on surface at SURF for back-end computing.

3.2 DAQ Design

1580

q-design

1581

16 Pages. This section is mostly DP/SP shared but with some subsections broken out. This file is far-detector-dual-phase/chapter-fddp-daq/design.tex

1582

overview

The design for the DAQ has been driven by finding a cost-effective solution that satisfies the requirements. Several design choices have nevertheless been made and two major variations remain to be studied. From a hardware perspective, the DAQ design follows a standard HEP experiment design, with customized hardware at the upstream, feeding and funnelling (merging) and moving the data into computers. Once the data and triggering information are in computers, a considerable degree of flexibility is available; the processing proceeds with a pipelined sequence of software operations, involving both parallel processing on multi-core computers and switched networks. The flexibility allows the procurement of computers and networking to be done late in the delivery cycle of the DUNE detector modules, to benefit from increased capability of commercial devices and falling prices.

Since DUNE will operate over a number of decades, the DAQ has been designed with upgradability in mind. With the fall in cost of serial links, a guiding principle is to include enough output bandwidth to allow all the data to be passed downstream of the custom hardware. This allows the possibility for a future very-fast farm of computing elements to accommodate new ideas in how to collect the DUNE data. The high output bandwidth also gives a risk mitigation path in case the noise levels in a part of the detector are higher than specified and higher than tolerable by the baseline trigger decision mechanism; it will allow additional data processing infrastructure to be added (at additional cost).

Digital data will be collected from the TPC and PD readout electronics of the SP and DP detector modules. These categories of data sources are viewed as essentially four types of subdetectors within the DAQ and will follow the same overall data collection scheme as shown for the nominal design in Figure ?? and for the alternative design in Figure ???. The readout is arranged to allow for a trigger decision to be made in a hierarchical manner. Initial inputs are formed at the channel level, then combined at the detector unit level and likewise these are combined at the detector module level. In addition, the trigger decision process combines this level of information that may come from the other detector modules as well as information sources external to the DAQ. This hierarchical structure in forming and consuming triggers will allow safeguards to be developed so that any problems in one cavern or in one detector unit of one detector module need not overwhelm the entire DAQ. It will also allow a SNB to be recorded in all operational parts of the detector while others may be down for calibration or maintenance.

Generally speaking, the DAQ consists of data and trigger flow. The trigger flow involved in self-triggering originates from processing a portion of the data flow. The trigger flow is then consumed back by the DAQ in order to govern what portion of the data flow is finally written out

1616 to permanent storage. The nominal and alternative designs differ in where in the data flow the
1617 trigger flow originates.

1618 In both designs, a single DAQ front-end fragment associates an integral number of detector units
1619 with one front-end computer (FEC). This fragment forms one conceptual unit of the FE DAQ. The
1620 processing on a FEC is kept minimal such that each has a throughput limited by I/O bandwidth.
1621 The recently released PCIe v4 doubles the bandwidth from the prior version and thus we assume
1622 ≈ 20 GB/s throughput (out of a theoretical 32 GB/s max) can be achieved based on tests using
1623 PCIe v3. In principle then, this allows one FEC to accept the data from: two (if uncompressed)
1624 or ten (if 5 \times compressed) of the 150 SP APAs, ten of the 240 DP CRO crates given their nominal
1625 10 \times compression or the uncompressed data from all five DP LRO crates.

1626 In the nominal design, the data enters the DAQ via the fragment's DAQ front-end readout (FER)
1627 component. In the SP the FER consists of eight reconfigurable computing elements (RCEs) and
1628 in the DP it consists of a number of Bump On Wire (BOW) computers, (see Section ?? in each
1629 respective detector module volume). The FER is responsible for accepting that data and from
1630 it producing channel level trigger primitives. It is also responsible for forwarding compressed
1631 data and the primitives to the DAQ data receiver (DDR) in the corresponding FEC. The FER is
1632 also responsible for supplying transient memory (RAM) and non-volatile buffer in the form of SSD
1633 sufficient for SNB triggering and readout. The DDR accepts the full data stream and transfers it to
1634 the DAQ primary buffer of its DAQ front-end fragment. There it is held awaiting a query from the
1635 event builder (EB). When the EB receives a trigger command it uses the included information to
1636 query all appropriate data selectors and from their returned data fragments an DAQ event block is
1637 built and written to file on the secondary DAQ buffer. From there the data becomes responsibility
1638 of the offline group to transfer to Fermilab for permanent storage and further processing.

1639 In the alternative design, the data is accepted directly by the DAQ data receiver (DDR) in a FEC
1640 from the detector electronics for the particular detector module. The data then flows into the
1641 primary buffer and the portion required for forming trigger primitives is dispatched to the trigger
1642 computers of the fragment for the production of trigger primitives. Current SSD technology may
1643 allow SSD to be directly mounted to the FEC to provide for the SNB dump buffer. Another solution
1644 which puts less pressure on write throughput is to distribute the SSD for the SNB dumps to the
1645 trigger computers. In order to supply enough CPU for trigger primitive pipelines it is expected that
1646 at least two hosts per FEC will be needed. While their CPUs are busy finding trigger primitives,
1647 their I/O bandwidth will be relatively unused and thus they provide synergistic, cost effective
1648 hosting for the SSDs.

1649 Regardless of where the trigger primitives are produced in either the nominal or alternative design
1650 they are further processed at the DAQ front-end fragment level to produce trigger candidates. At
1651 this level, they represent possible activity localized in time and channel to a portion of the overall
1652 detector module. The trigger candidates emitted by all DAQ front-end fragments are sent to the
1653 module trigger logic (MTL) associated with the DAQ partition. There, they are time ordered
1654 and otherwise processed to form trigger commands. At this level they represent activity localized
1655 across the detector module and over some period of time.

1656 The DAQ partition (or DAQ instance) just introduced is the cohesive collection of DAQ parts.
1657 One DAQ partition operates essentially independently from any other, and there is typically one

1658 per detector module. In some cases multiple DAQ partitions may operate simultaneously in a
 1659 detector module, such as when some fraction of detector units are undergoing isolated testing or
 1660 calibration.

1661 Each trigger command is consumed by a single EB instance in order to query back to the DAQ
 1662 front-end fragments of its DAQ partition as described above. In addition, the MTL of one module
 1663 is exchanging messages in the form of trigger candidates with the others. For example, one module
 1664 may raise a local SNB trigger candidate and forward it to all other modules. Each module is also
 1665 emitting candidates to sinks and accepting them from sources of external trigger information.

1666 The exact implementation of some of these high-level functions, particularly those near the FE,
 1667 depends on the particular detector module. The required specialization and in general, more
 1668 implementation-level details are described in the following sections. Subsequent description pro-
 1669 ceeds toward the DAQ back end including processes handling dataflow, trigger, event building and
 1670 data selection.

1671 3.2.2 Front-end Readout and Buffering

daq-fero
 1672 Giles Barr & Giovanna Miotto & Brett Viren, this is DP-specific. This file is
far-detector-dual-phase/chapter-fddp-daq/design-fero.tex

1673 Figurere [fig:daq-readout-buffering-baseline](#)
 1674 illustrates DP-specific implementation of the nominal, generic DAQ front-end DAQ
 1675 front-end fragment design shown in Figure [??](#). The CRO crates deliver data on user datagram
 1676 protocol (UDP) to BOW computers which implement the FER duties. The CRO data is delivered
 1677 to the DAQ BOW computers with lossless compression applied and so before the trigger primitives
 can be produced the data must be decompressed.

1678 In order to save on cost, power, space, cooling, etc., a number of CRO crate data streams can
 1679 be aggregated into one FEC. The CRO data stream is sent using UDP which is not expected
 1680 to provide reliable transport of high-throughput data if a network switch intervenes. Thus each
 1681 CRO requires a corresponding 10 Gbit/s network interface controller (NIC) in the receiving BOW
 1682 computer. With the expected 10× lossless compression factor the nominal output from each CRO
 1683 crate will be 2 Gbps. If noise levels are higher than expected the throughput will increase, however
 1684 even very noisy data should be compressible enough to fit into the 10 Gbps bandwidth. Noise will
 1685 be better understood from ProtoDUNE-DP data, and studies are needed to optimize the number
 1686 of CRO crates per BOW computer.

1687 After processing, the input data is sent out, along with the corresponding primitives to a Front-End
 1688 Link eXchange (FELIX) board in a FEC. Similar to the argument above about noise, bandwidth
 1689 and BOW computer multiplicity, the number of BOW data streams that can be aggregated into
 1690 each FELIX board requires additional study. The current generation of FELIX boards have been
 1691 tested with a throughput to system RAM of 10 GB/s. The next generation is expected to at least
 1692 double that. With the caveat that these tests did not receive data on UDP, a nominal 20 GB/s
 1693 throughput is assumed possible for the next-generation PCIe v4 boards. Given this assumption

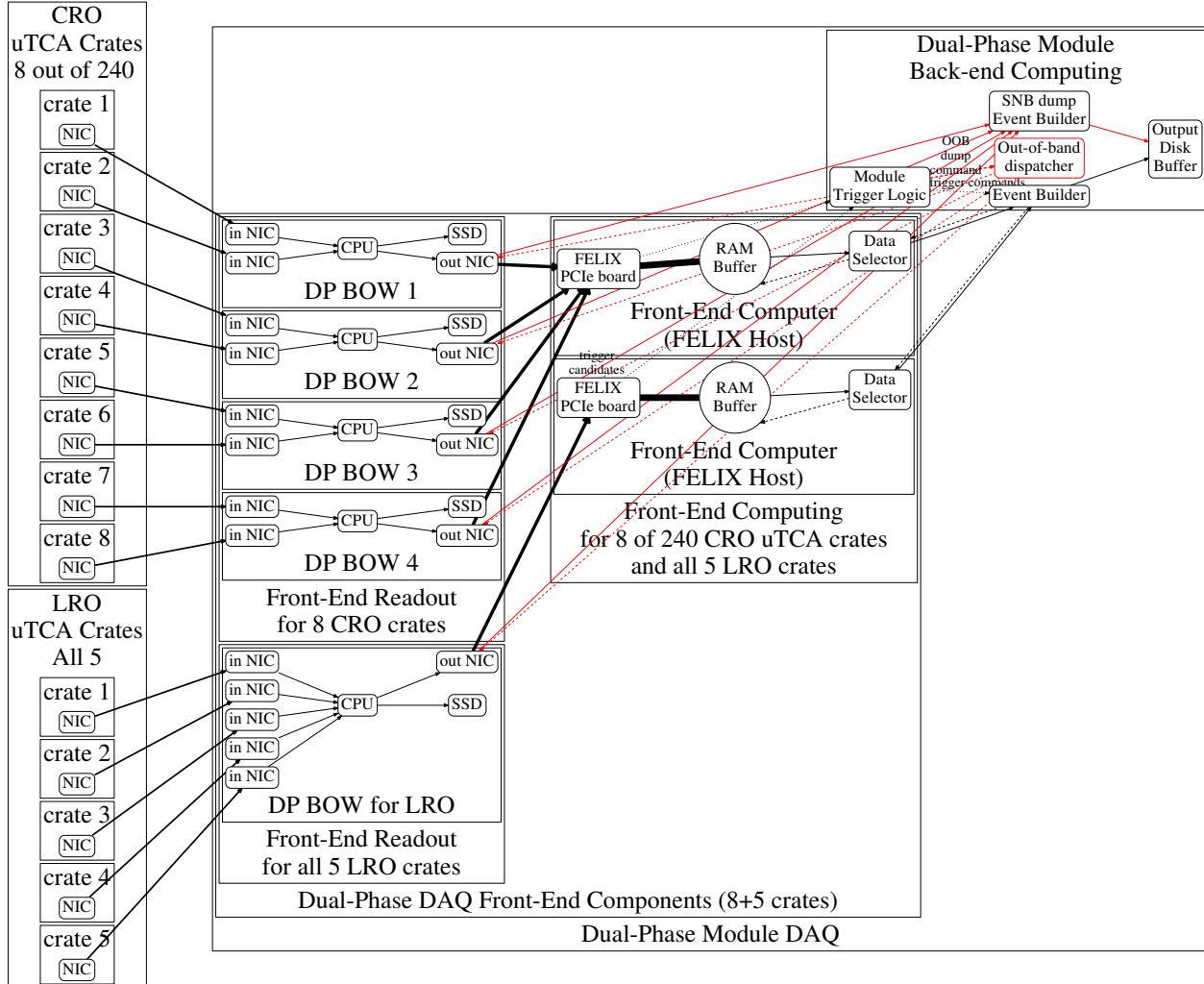


Figure 3.3: Illustration of data (solid arrows) and trigger (dashed) flow for two DP FE DAQ fragments. One servicing eight of 240 CRO crates and the other servicing all five LRO crates. Black arrows indicate nominal flow and red indicate special flow for handling of potential SNB.

fig:daq-

1694 and that the expected noise levels are achieved, then based solely on bandwidth, as many as 80
 1695 CRO data streams might be aggregated into a single next-generation FELIX board. Figure ??
 1696 indicates the aggregation of eight CRO streams, which represents the multiplicity required to deal
 1697 with very high noise. Future studies are needed to determine which of these two extremes to favor
 1698 for optimization of the design, but the basic design itself is fairly elastic between them.

1699 The LRO crates are nominally not involved in self-triggering although the data from all five LRO
 1700 crates are assumed to flow through a LRO BOW. The data are then sent to a single FELIX board.
 1701 Given the expected data rates, that FELIX board must ingest about 25 GB/s.

1702 The second duty of the FER in the nominal design is to provide non-volatile storage for receiving
 1703 full-stream data dumps when an SNB dump trigger command is issued. With today's technology,
 1704 individual SSDs can write at about 2.5 GB/s. Up to four SSDs have been placed on a 1-lane PCIe
 1705 v3 board and have achieved about three times this speed. This would allow an individual BOW
 1706 computer to aggregate 10 to 30 CRO data streams before the SSDs become a bottleneck. The five
 1707 LRO data streams, each producing 5 Gbps, could together be streamed to a two modern SSDs.
 1708 The BOW computers must also have sufficient RAM to hold pre-SNB-trigger data of about 10
 1709 seconds.

1710 The alternative design (not diagrammed), which corresponds to Figure ??, deletes the layer containing BOW
 1711 computers and directly connects the UDP streams from the CRO and LRO crates to the FELIX boards in the FECs. The CRO (compressed) data is buffered on the FELIX host
 1712 computer RAM and distributed to the trigger farm for decompression and trigger primitive and
 1713 trigger candidate processing. The remaining part of the trigger decision is as in the nominal design
 1714 except that the SNB dump data stream is handled symmetrically with the normal triggered data.

1716 3.2.3 Front-end Trigger Primitive Generation

1717 In the nominal design, the BOW computers decompress the CRO data stream and execute algorithms
 1718 to search for per-channel localized activity above some threshold based on a recent measure
 1719 of the noise. These trigger primitives are then sent out along with the original, compressed CRO
 1720 data to the FEC associated with the BOW.

1721 Initial studies have shown some promise that this type of trigger primitives pipeline can be implemented
 1722 on commodity CPUs and keep up with the data. The studies made use of SP signal and
 1723 noise simulation but given the relatively higher signal-to-noise ratio expected in the DP module
 1724 data, coupled with fewer total channels, these studies should be applicable and even better performance
 1725 may be expected. With that said, more realistic studies using DP-specific simulations
 1726 and with ProtoDUNE-DP data are needed.

1727 Most of the same technical triggering issues apply in the nominal and the alternative design
 1728 (generically diagrammed in Figure ??), as both call for deploying trigger primitive pipelines on
 1729 commodity CPUs. The main difference is that the BOWs hosts become trigger farm hosts. They
 1730 move from being upstream and inline of the data flow before the FEC to being downstream and
 1731 receiving the data after it has been buffered. Their trigger candidates no longer have to be inserted

1732 into the stream and stripped out by the FEC and instead are sent directly to the MTL. Additional
 1733 study is required to understand the multiplicity of trigger processing computers and how that
 1734 might scale as one considers different multiplicities of CRO Micro Telecommunications Computing
 1735 Architecture (μ TCA) crates with respect to each FEC.

1736 In both designs, the LRO data is currently not considered for triggering as the CRO triggering is
 1737 expected to be more efficient. However, using light information for triggering has not yet been ruled
 1738 out. Future studies may indicate additional benefit to including LRO information in triggering
 1739 and both the nominal and alternative design can elastically accommodate this increased scope
 1740 although possibly at the cost of either more BOW or trigger processor computers. As described
 1741 elsewhere, the LRO data flow is handled by separate DAQ front-end fragments from those that
 1742 service the CROs. Thus, if any trigger primitives and trigger candidates are to be formed from
 1743 LRO data they would come from these separate fragments and be combined in the MTL as peers
 1744 of the CRO and external candidates.

1745 3.2.4 Dataflow, Trigger and Event Builder

-daq-hlt
 1746 Giles Barr & Josh Klein & Giovanna Miotto & Kurt Biery & Brett Viren. This is a DP/SP
 shared section. It's file is `far-detector-generic/chapter-generic-daq/design-flow.tex`

1747 In the general data and trigger flow diagrams for the nominal (Figure ??) and alternative (Figure
 1748 ??) designs, the dataflow, trigger and event builder functions take as input data from the
 1749 detector module electronics and culminate in files deposited to secondary DAQ buffer for transfer
 1750 to permanent storage by offline computing processes. The continuous, uncompressed data rate
 1751 of the input from one detector module is on order of 1 TB/s. The final output data rate, for all
 1752 detector modules operating at any given time is approximately limited to 1 GB/s.
fig:daq-overview
~~tip:daq-overview-alt~~

1753 To accept this high data-inflow rate and to apply the substantial processing needed to achieve the
 1754 required reduction factor, which is on the order of 1000, the DAQ follows a distributed design.
 1755 The units of distribution for the front end of the DAQ must match up with natural units of the
 1756 detector module providing the data. This unit is called the DAQ front-end fragment and each
 1757 accepts input at a rate of about 10 to 20 GB/s. The exact choice maps to some integral number
 1758 of physical detector module units (e.g., SP APAs or DP CROs and LROs).

1759 As described in the previous sections, the nominal and alternative designs differ essentially in the
 1760 order and manner in which the SNB buffering occurs and the trigger primitives are formed. The
 1761 overall data flow, higher level triggering and building of *event* data blocks for final writing are
 1762 conceptually very similar. This processing begins with the data being received by the FELIX
 1763 PCIe board hosted in the FEC. The FELIX board performs a DMA transfer of the data into
 1764 the primary buffer for the DAQ front-end fragment which resides in the FEC host system RAM.
 1765 This buffer is sized to hold ten seconds of data assuming the maximum uncompressed input rate
 1766 associated with the fragment. While data is being written to the buffer, a delayed portion is also
 1767 being read in order to dispatch it for various purposes. Any and all requests to further dispatch
 1768 a subset of this data from the primary buffer must arrive within this buffer time. In the nominal

1769 design, the only dispatching will be from a request made by an EB (described more below) on
 1770 its receipt of a trigger command. In the alternative design, a suitable fraction of the data is also
 1771 dispatched via high bandwidth (at least 25 to 50 Gbit/s simplex, less if data is compressed at this
 1772 stage) network connections to a trigger farm so that trigger primitives may be formed. Whether
 1773 the primitives are formed in this manner or extracted from the stream sent by the FER (as in the
 1774 nominal design) these trigger primitives from one DAQ front-end fragment are collectively sent for
 1775 further processing in order to be combined across channels and so to produce trigger candidates.
 1776 These are finally combined for one detector module in the MTL. It is in the MTL where trigger
 1777 candidates from additional sources are also considered as described more in section [??](#).

1778 In both the nominal and alternative design the dispatch of data initiated by normal (non-SNB)
 1779 trigger commands is identical. This dispatch, commonly termed *event building* involves collection
 1780 of data spanning an identical and continuous period of time from multiple primary buffers across
 1781 the DAQ. As introduced above, each trigger command is consumed by an EB process. It will use
 1782 fragment address information in the trigger command to query the data selector process repre-
 1783 senting each referenced DAQ front-end fragment and accept the returned a data fragment. In the
 1784 exceptional case that the delay of this request is so large that the primary buffer no longer contains
 1785 the data, then an error return will be supplied and recorded by the EB in place of the lost data.
 1786 Such failures lead to indicators displayed by the detector operation monitoring system. The EB
 1787 finally assembles all responses into a DAQ event block and write it to file on the secondary DAQ
 1788 buffer where it becomes responsibility of DUNE offline computing.

1789 The data selector and EB services are implemented using the general-purpose Fermilab data ac-
 1790 quisition framework *artDAQ* for distributed data combination and processing. It is designed to
 1791 exploit the parallelism that is possible with modern multi-core and networked computers, and has
 1792 been used in ProtoDUNE and other experiments. The *artDAQ* framework is the principal archi-
 1793 tecture that will be used for the DUNE DAQ back-end computing. The authors of *artDAQ* have
 1794 accommodated DUNE-specific requests for feature additions. Also a number of libraries have been
 1795 developed based on existing parts of *artDAQ* used to handle incoming data from data sources. It
 1796 is likely that future DUNE extensions will be made by one of these two routes.

1797 Unlike the dispatch of data initiated by a normal trigger commands, a command formed to indicate
 1798 the possibility of a SNB is handled differently between the nominal and alternative designs. Such
 1799 a command is interpreted to save all data from all channels for a rather extended time of 30 s
 1800 starting from 10 s before the time associated with the trigger command. As no data selection is
 1801 being performed, the bandwidth needed requires special buffering to nonvolatile storage in the
 1802 form of SSD. Today's technology supplies individual SSD in the M.2 expansion card form factor,
 1803 which supports individual write speeds up to 2.5 GB/s. The two designs differ as to the location
 1804 of and data source for these buffers.

1805 In the nominal design, these SSDs reside in the FER as described in Section [??](#). In that location,
 1806 due to larger granularity of computing units, the data rate into any one SSD is within the quoted
 1807 write bandwidth. However, and as shown in Figure [??](#), the data and trigger flow for SNB in the
 1808 nominal case, takes a special path. Instead of an EB consuming the trigger command as described
 1809 above, it is sent to the Out-of-band trigger command dispatcher (OOB dispatcher) which dispatches
 1810 it to each FER unit hosting an SSD. This component is used in order to immediately free up the
 1811 MTL to continue to process normal triggers. When the command is received, each host must

1812 begin to stream data from its local RAM supplying at least 10 s of buffer to the SSD and continue
1813 until the full 30 s has elapsed. While it is performing this dump it must continue to form trigger
1814 primitives and pass them and the full data stream to the connected FEC.

1815 In the alternative design the same primary buffer provides the 10 s of pre-trigger SNB buffering.
1816 Like in the nominal case, it must rely on fast, local SSD storage to sink the dump. Current SSD
1817 technology allows four M.2 SSD devices to be hosted on a PCIe board. Initial benchmarks of
1818 this technology show such a combination can achieve 7.5 GB/s write bandwidth, which is short of
1819 linear scaling. To support the maximum of 20 GB/s, three such boards would be required. The
1820 alternative design presents a synergy between the need to dump high-rate data and the need to
1821 provide CPU to form the trigger primitives. With current commodity computing hardware it is
1822 expected that each FEC will need to be augmented with about two computers in the trigger farm.
1823 These trigger processors will need to accept the entire DP and three-eighths of the SP data stream
1824 from their DAQ front-end fragment. If they instead accepted the entire stream, they can also
1825 provide RAM buffering and split up the data rate which must be sunk to SSD buffers.

1826 In both designs, the data dumped to SSD may contain precious information about a potential SNB.
1827 It must be extracted from the buffer, processed and either discarded or saved to permanent storage.
1828 The requirements on these processes are not easy to determine. The average period between actual
1829 SNB to which DUNE is sensitive is measured in decades. However, to maintain high efficiency
1830 for capturing such important physics, the thresholds will be placed as low as feasible, limited only
1831 by the ability to acquire, validate and (if validated) write out the data to permanent storage.
1832 Notwithstanding, the (largely false positive) SNB trigger rate is expected to be minuscule relative
1833 to normal triggers. Understanding the exact rate requires more study, including using early data,
1834 but for planning purposes it is simply assumed that one whole-detector data dump will occur per
1835 month on average. Using the SP module as an example, and choosing the nominal time span for
1836 the dump to be 30 s, about 45 PB of uncompressed data would result. In the nominal SP DAQ
1837 design, this dump would be spread over 600 SSD units leading to 75 GB per SSD per dump. Thus,
1838 typical SSDs offer storage to allow any given dump to be held for at least one half year before it
1839 must be purged to assure storage is available for subsequent dumps. If every dump were to be sent
1840 to permanent storage, it would represent a sustained 0.14 Gbit/s (per detector module), which is a
1841 small perturbation on the bandwidth supplied throughout the DAQ network. Saved to permanent
1842 storage this rate integrates to 0.5 PB/year which while substantial, is a minor fraction of the total
1843 data budget. The size of each dump is still larger than is convenient to place into a single file, so
1844 the SNB event-building will likely differ from that for normal triggers in that the entire dump is
1845 not held in a single DAQ event block. Finally, it is important to qualify that these rates assume
1846 uncompressed data. At the cost of additional processing elements, lossless compression can be
1847 expected to reduce this data rate by 5 to 10 × or alternatively allow lower thresholds leading to
1848 the same factor of more dumps. Additional study is required to optimize the costs against the
1849 expected increase in sensitivity.

3.2.5 Data Selection Algorithms

1850 -daq-sel
 1851 Josh Klein & Brett Viren. This is a shared DP/SP section. Its file is
 1852 `far-detector-generic/chapter-generic-daq/design-sel.tex`

1853 Data selection follows a hierarchical design. It begins with forming detector unit-level trigger
 1854 candidates inside the DAQ front-end fragment FE computing using channel-level trigger primitives.
 1855 These are then used to form detector module trigger commands in the MTL. When executed,
 1856 they lead to readout of a small subset of the total data. In addition, trigger candidates are
 1857 provided to the MTL from external sources such as the ETL in order to indicate external events
 1858 such as beam spills, or SNB candidates detected by the other detector modules. In addition to
 1859 supplying triggers to SuperNova Early Warning System (SNEWS), triggers from SNEWS or other
 1860 cosmological detector sources such as LIGO and VIRGO can be accepted in order to possibly
 1861 record low-energy or dispersed activity that would not pass the self-triggering. The latency of
 1862 arrival for these sources must be less than the nominal 10 s buffers used to capture low-level early
 1863 SNB activity. A high-level trigger (HLT) may also be active within the MTL. The hierarchical
 1864 approach is both natural from a design standpoint, and it allows for vertical slice testing and
 1865 running multiple DAQ partitions simultaneously during commissioning of the system or when
 debugging of individual detector units is required.

1866 As discussed in Sections ?? and ??, trigger primitives will be generated in either in FERs (in the
 1867 nominal design) or in trigger processing computers (in the alternative design). In both designs, and
 1868 for both SP and DP detector modules, only data from TPC collection channels (three-eighths of SP
 1869 and all of DP channels) will feed the self-triggering, as their waveforms directly supply a measure
 1870 of ionization activity without computationally costly signal processing. The trigger primitives
 1871 contain summary information for each channel, such as the time of any threshold-crossing pulse,
 1872 its integral charge, and time over threshold. A channel with an associated trigger primitive is said
 1873 to be *hit* for the time spanned by the primitive. Trigger primitives from one detector unit are
 1874 then further processed to produce a trigger candidate. The candidate represents a cluster of *hits*
 1875 across time and channel, localized to the detector unit. The candidates from all DAQ front-end
 1876 fragments are passed to the MTL.

1877 The MTL arbitrates between various trigger types, determines trigger priority and ultimately the
 1878 time range and detector coverage for a trigger command, which it emits back to the FECs. The
 1879 MTL assures that no trigger commands are issued that overlap in time or in detector channel
 1880 space. It also may employ a HLT to reduce or aggregate triggers into fewer trigger commands so
 1881 as to optimize the subsequent readout. For example, aggregating many small readouts into fewer
 1882 but larger ones may allow for more efficient processing. This can be particularly important during
 1883 periods of high rate activity such as due to various backgrounds or instrumental effects.

1884 When activity leads to the formation of a trigger command this command is sent down to the
 1885 FECs instructing which slice of time of its buffered data should be saved. The trigger command
 1886 information is saved along with this data. At the start of DUNE data taking, it is anticipated
 1887 that for any given single-interaction trigger (a cosmic-ray track, for example) waveforms from all
 1888 channels in the detector module will be recorded over a one readout window (nominally, 5.4 ms for

1889 SP and 16.4 ms for DP, chosen to be two drift times plus an extra 20 %).

1890 Such an approach is clearly very generous in terms of the amount of data saved, but it ensures that
1891 associated low-energy physics (such as captures of neutrons produced by neutrino interactions or
1892 cosmic rays) are recorded without any need to fine-tune detector unit-level triggering, and does
1893 not depend on the noise environment across detector units. In addition, the wide readout window
1894 ensures that the data of all associated activity is recorded. As generous as it is, it is estimated that
1895 this readout window will not produce an unmanageable volume of data. As shown in Table ??,
1896 the uncompressed selected data from the SP module will fill about half of the nominal annual
1897 data budget. The longer DP drift and its fewer channels will give approximately the same data
1898 rate. However, once a modest amount of lossless compression is applied, the nominal data budget
1899 can be met. Early running will allow experience to be gained and more advanced data selection
1900 algorithms to be validated allowing the DAQ to discard the many data fragments in each trigger
1901 consistent with just electronics noise. This has the potential for a reduction of at least another
1902 factor of ten.

1903 Other trigger streams – calibrations, random triggers, and prescales of various trigger thresholds
1904 – are also generated at the detector module level, and filtering and compression can be applied
1905 based upon the trigger stream. For example, a large fraction of random triggers may have zero-
1906 suppression (ZS) applied to their waveforms, reducing the data volume substantially, as the dom-
1907 inant data source for these will be ^{39}Ar events. Additional signal-processing can also be done
1908 on particular trigger streams if needed and if the processing is available, such as fast analyses of
1909 calibration data.

1910 At the detector module level, a decision can also be made on whether a series of interactions is
1911 consistent with an SNB. If the number of detector unit-level, low-energy trigger candidates exceeds
1912 a threshold for the number of such events in a given time, a trigger command is sent from the
1913 MTL back to the FERs, which store up to 10 s of full waveform data. That data is then streamed
1914 to non-volatile storage to allow for subsequent analysis by the SNB working group, perhaps as an
1915 automated process. If not rejected, it is sent out of the DAQ to permanent offline storage.

1916 In addition, the MTL passes trigger candidates up to a detector-wide ETL, which among other
1917 functions, can decide whether, integrated across all modules, enough detector units have detected
1918 interactions to qualify as an SNB, even if within a particular module the threshold is not exceeded.
1919 Trigger candidates from the ETL are passed to the MTL for dispatch to the FECs (or FERs in the
1920 case of SNB dump commands in the nominal design). That is, to the MTL, an external trigger
1921 candidate looks like just one more *external* trigger input.

1922 Detector unit level trigger candidates are generated within the context of one DAQ front-end
1923 fragment, specifically in each FEC. The trigger decision is based on the number of nearby channels
1924 hit in a given fragment within a time window (roughly 100 μs), the total charge collected in
1925 these adjacent channels, and possibly the union of time-over-threshold for the trigger primitives
1926 in the collection plane. Studies show that even for low-energy events (roughly 10 MeV to 20 MeV)
1927 the reduction in radiological backgrounds is extremely high with such criteria. The highest-rate
1928 background, ^{39}Ar , which has an overall rate of 10 MBq within a 10 kt volume of argon, has an
1929 endpoint of 500 keV and requires significant pileup in both space and time to get near a 10 MeV
1930 threshold. One important background source is ^{42}Ar , which has a 3.5 MeV endpoint and an overall

tab:daq-data-r

1931 rate of 1 kBq. ^{222}Rn decays via a 5.5 MeV kinetic energy α and is also an important source of
1932 background. The radon decays to ^{218}Po , which within a few minutes leads to a 6 MeV kinetic
1933 energy α , and ultimately to a ^{214}Bi daughter (many minutes later), which has a β decay with its
1934 endpoint near 3.5 MeV kinetic energy. The α ranges are short, resulting in charge being collected
1935 on one or two anode wires at most, but the charge deposit can be large, and therefore the charge
1936 threshold must be well above the α deposits plus any pileup from ^{39}Ar and noise.

1937 At the level of one detector unit, two kinds of local trigger candidates can be generated. One
1938 is a high-energy trigger that indicates local ionization activity corresponding to more than than
1939 10 MeV. The per-channel thresholds on total charge and time-over-threshold will be optimized to
1940 achieve at least 50 % efficiency at this energy threshold, with efficiency increasing to 100 % via a
1941 turn-on curve that ensures at least 90 % efficiency at 20 MeV. The second type of trigger candidate
1942 generated is for low-energy events between 5 MeV and 10 MeV. In isolation, these candidates do not
1943 lead to formation of a trigger command. Rather, at the detector module level they are combined,
1944 time ordered and their aggregate rate compared against a threshold based on fluctuations due to
1945 noise and backgrounds in order to form an SNB trigger command.

1946 The MTL takes as input trigger candidates (both low-energy and high-energy) from the partici-
1947 pating DAQ front-end fragments, as well as external trigger candidate sources, such as the ETL,
1948 which includes global, detector-wide triggers, external trigger sources such as SNEWS, and in-
1949 formation about the time of a Fermilab beam spill. The MTL also generates trigger commands
1950 for internal consumption, such as random triggers and calibration triggers (for example, telling a
1951 laser system to fire at a prescribed time). The MTL can also generate trigger commands from a
1952 prescaled fraction of trigger types that otherwise do not generate such commands on their own. For
1953 example, a prescaled fraction of single, low-energy trigger commands could be allowed to generate
1954 a trigger command, even though those candidates normally only result in a trigger command when
1955 aggregated (i.e., as they would be for an SNB).

1956 The MTL is also responsible for checking candidate triggers against the current run control (RC)
1957 trigger mask: in some runs, for example, we may decide that only random triggers are accepted,
1958 or that certain trigger candidates streams should not be considered because their DAQ front-end
1959 fragments have been producing unreasonably large rates in the recent past (such as may be due to
1960 noise spikes, flaky hardware or buggy software). In addition, the MTL counts low-energy trigger
1961 candidates, and based upon their number and distribution over a long time interval (e.g., 10 s),
1962 decides to generate an SNB trigger command. The trigger logic will be optimized to record the
1963 data due to at least 90 % of all Milky Way supernovae, and studies of simple low-energy trigger
1964 criteria show that a much higher efficiency can likely be achieved.

1965 The HLT can also be applied at this level, particularly if there are unexpectedly higher rates from
1966 instrumental or low-energy backgrounds that require some level of reconstruction or pattern recog-
1967 nition. An HLT might also allow for efficiently triggering on lower-energy single interactions, or
1968 allow for better sensitivity for supernovae originating outside the Milky Way galaxy, by employing
1969 a weighting scheme to individual trigger candidates – higher-energy trigger candidates receiving
1970 higher weights. Thus, for example, two trigger candidates consistent with 10 MeV interactions in
1971 10 s might be enough to create a SNB candidate trigger, while a hundred 5 MeV trigger candidates
1972 in 10 s might not. Lastly, the HLT can allow for dynamic thresholding; for example, if a trigger
1973 appears to be due to a cosmic-ray muon, the threshold for single interactions can be lowered (and

possibly prescaled) for a short time after that to identify spallation products. In addition, the HLT could allow for a dynamic threshold after a SNB, to extend sensitivity beyond the 10 s SNB readout window, while not increasing the data volume associated with SNB candidates linearly.

All low-energy trigger candidates are also passed upwards to the ETL so that they may be integrated across all 10 kt detector modules in order to determine that a SNB may be occurring. This approach increases the sensitivity to trigger on SNBs by a factor of four (for 40 kt), thus extending the burst sensitivity to a distance twice as far as for a single 10 kt detector module.

The MTL is also responsible for including in the trigger command a global timestamp built from its input trigger candidates, and information on what type of trigger was created. Information on trigger candidates is also kept, whether or not they contribute to the formation of a trigger command. As described above, the readout window for nominal trigger commands (those other than for SNB candidates) is somewhat more than two times the maximum drift time. Further, a nominal readout spans all channels in a detector module. The MTL is also responsible for sending the trigger commands that tell the FERs to stream all data from the past 10 s and for a total of 30 s in hopes to catch SNBs. This command may be produced based on trigger candidates from inside the MTL itself or it may be produced based on an external SNB trigger candidate passed to the MTL by the ETL.

3.2.6 Timing and Synchronization

David Cussans & Kostas Manolopoulos. This is a DP-specific section. The file is
`far-detector-dual-phase/chapter-fddp-daq/design-timing.tex`

The timing distribution is integrated into the TPC electronics design and is described in section 1.4.2 and 1.2.6 using a White Rabbit (WR) network over synchronous 1 Gbit/s Ethernet (SyncE), using Precision Time Protocol-version 2 (PTPv2) packets.

The synchronization between the FD and the beam pulses from the LBNF beamline is done by a single overall system for SP and DP and is described in the following section.

3.2.6.1 Beam timing

The neutrino beam is produced at the Fermilab accelerator complex in spills of 10 μ s duration. A spill location system (SLS) at the far detector site will locate the time periods in the data when beam could be present, based on network packets received from Fermilab containing predictions of the GPS-time of spills soon to occur or absolute time stamps of spills recently occurring. Experience from MINOS and NO ν A shows that this can provide beam triggering with high reliability with some small fraction of late or dropped packets. To improve further the system outlined here contains an extra layer of redundancy in the prediction process. Several stages prediction based on recent spill behavior will be applied aiming for an accuracy of better than 10% of a readout

2007 time (sub-ms) in time for the data to be selected from the DAQ buffers. Ultimately, an offline
 2008 database will match the actual time of the spill with the data, thus removing any reliance on real-
 2009 time network transfer for this crucial stage of the oscillation measurements. The network transfer
 2010 of spill-timing information is simply to ensure a correctly located and sufficiently wide window
 2011 of data is considered as beam data. This system is not required, and is not designed to provide
 2012 signals accurate enough to measure neutrino time-of-flight.

2013 The precision to which the spill time can be predicted at Fermilab improves as the acceleration
 2014 process of the protons producing the spill in question advances. The spills currently occur at
 2015 intervals of 1.3 s; the system will be designed to work with any interval, and to be adaptable in
 2016 case the sequence described here changes. For redundancy, three packets will be sent to the far
 2017 detector for each spill. The first is approximately 1.6 s before the spill-time, which is at the point
 2018 where a 15 Hz booster cycle is selected; from this point on, there will be a fixed number of booster
 2019 cycles until the neutrinos and the time is subject to a few ms of jitter. The second is about 0.7 s
 2020 before the spill, at the point where the main injector acceleration is no longer coupled to the
 2021 booster timing; this is governed by a crystal oscillator and so has a few μ s of jitter. The third will
 2022 be at the so called ‘\$74’ signal generated before the beam line kicker magnet fires to direct the
 2023 protons at the LBNF target; this doesn’t improve the timing at the far detector much, but serves
 2024 as a cross check for missing packets. This system is enhanced compared to that of MINOS-NO ν A,
 2025 which only use the third of the above timing signals. The reason for the larger uncertainty in the
 2026 time interval from 1.6 s to 0.7 s is that the booster cycle time is synchronised to the electricity
 2027 supply company’s 60 Hz which has a variation of about 1%.

2028 Arrival-time monitoring information from a year of MINOS data-taking was analysed, and it was
 2029 found that 97% of packets arrived within 100 ms of being sent and 99.88% within 300 ms.

2030 The SLS will therefore have estimators of the GPS-times of future spills, and recent spills with
 2031 associated data contained in the primary buffers. These estimators will improve in precision as
 2032 more packets arrive. The DAQ will use data in a wider window than usual, if, at the time the
 2033 trigger decision has to be made, the precision is less accurate due to missing or late packets. From
 2034 the MINOS monitoring analysis, this will be very rare.

2035 3.2.7 Computing and Network Infrastructure

aq-infra

2036 Kurt Biery & Babak Abi. This is a DP/SP shared section. It’s file is
far-detector-generic/chapter-generic-daq/design-compnet.tex

2037 The computing and network infrastructure that will be used in each of the four detector modules
 2038 is similar, if not identical. It supports the buffering, data selection, event building, and data flow
 2039 functionality described above, and it includes computing elements that consist of servers that:

- 2040 • buffer the data until a trigger decision is received;
- 2041 • host the software processes that build the data fragments from the relevant parts of the

2042 detector into complete events;

2043 whole detector or module?

2044 • host the processes that make the trigger decision;

2045 • host the data logging processes and the disk buffer where the data is written;

2046 • host the real-time data quality monitoring processing;

2047 • host the control and monitoring processes.

2048 The network infrastructure that connects these computers has the following components:

2049 • subnets for transferring triggered data from the buffer nodes to the event builder nodes.
2050 These need to connect underground and above-ground computers.

2051 • a control and monitoring subnet that connects all computers in the DAQ system and all
2052 FE electronics that support Ethernet communication. This sub-network must connect to
2053 underground and above-ground computers.

2054 • a subnet for transferring complete events from the event builder servers to the storage servers.
2055 This subnet is completely above-ground.

2056 3.2.8 Run Control and Monitoring

-daq-tcm
2057 Giovanna Miotto & Jingbo Wang. THis is a DP/SP shared section. The file is
far-detector-generic/chapter-generic-daq/design-ctrmon.tex

2058 The online software constitutes the backbone of the DUNE DAQ system and provides control,
2059 configuration and monitoring of the data taking in a uniform way. It can be subdivided logically
2060 into four subsystems: the run control, the management of the DAQ and detector module electronics
2061 configuration, the monitoring, and the non-physics data archival. Each of these subsystems has a
2062 distinct function, but their implementation will share underlying technologies and tools.

2063 In contrast to experiments in which data taking sessions, i.e., runs, are naturally subdivided
2064 into time slots by external conditions (e.g., a collider fill, a beam extraction period), the DUNE
2065 experiment aims to take data continuously. Therefore, a classic run control with a coherent state
2066 machine and a predefined and concurrently configured number of active detector and DAQ elements
2067 does not seem adequate.

2068 The DUNE online software is thus structured according to the architecture principle of loose
2069 coupling: each component has as little knowledge as possible of other components. While the
2070 granularity of the back-end DAQ components may match the individual software processes, for

2071 the front-end DAQ a minimum granularity must be defined, balancing fault tolerance and recovery
 2072 capability against the requirement of data consistency. The smallest independent component is
 2073 called a DAQ front-end fragment, which is made up of the detector units associated with a single
 2074 front-end computer. In the nominal design, this corresponds to two SP APAs and about ten DP
 2075 CRO crates.

2076 The concept of *run* represents a period of time in which the same FE elements are active or the
 2077 same data selection criteria are in effect (possibly with maximum lengths for offline processing
 2078 reasons). More than just orchestrating data taking, the run control provides the mechanisms
 2079 allowing DAQ applications to publish their availability, subscribe to information, and exchange
 2080 messages. In addition, the online software provides a configuration service for DAQ elements to
 2081 store their settings and a conditions archive, keeping track of varying detector electronics settings
 2082 and status.

2083 Another important aspect of the online software is the monitoring service. Monitoring can be
 2084 subdivided into two main domains: the monitoring of the data taking operations (rates, number of
 2085 data fragments in flight, error flags, application logs, network bandwidth, computing and network
 2086 infrastructure) and the monitoring of the physics data. Both are essential to the success of the
 2087 experiment and must be designed and integrated into the DAQ system from the start. In partic-
 2088 ular, for such a large and distributed system, the information sharing and archival system is very
 2089 important, as are scalable and easily accessible data visualization tools, which will evolve during
 2090 the lifetime of the experiment. The online software provides the glue that holds the DAQ applica-
 2091 tions together and enables data taking. Its architecture guides the approach to DAQ application
 2092 design and also shapes the view that the operators will have of the experiment.

2093 3.3 Interfaces

2094 5 Pages. This is a shared SP/DP section. If there are assymetries simply describe both detec-
 2095 tor modules.

2096 Include an image of each interface in appropriate section. Can maybe refer to Figure ?? but it
 2097 currently lacks some of the interfaces.

2096 3.3.1 TPC Electronics

2097 Details about the interfaces between the DAQ and the DP charge readout TPC electronics are
 2098 documented in [?].

2099 Add references to bib.

2100 In the case of the DP detector module, signals from the charge readout electrodes are amplified

2101 and then digitized by advanced mezzanine card (AMC) boards residing in 240 μ TCA crates. Each
 2102 crate produces 2.5 MHz samples from 640 channels on a 10 Gbit/s optical fiber. Data is loss-
 2103 lessly compressed and sent via UDP producing a stream with an expected average throughput of
 2104 2 Gbit/s. The DAQ consortium will be responsible for acquiring the fibers while the DP-Electronic
 2105 consortium will be responsible for their installation on the cryostat roof down to their connection
 2106 to the μ TCA crates.

2107 Need some statement about the white rabbit fiber?

2108 3.3.2 PD Electronics

2109 Details about the interfaces between the DAQ the DP light readout [?] are documented.
 2110

2111 Add references to bib.

2112 For the DP LRO, the signals are digitized in 14 bits at 65 MHz and then downsampled to 2.5 MHz.
 2113 The data is then handled largely symmetrically with the CRO data except that only five μ TCA
 2114 crates are required and their average, uncompressed output is expected to fill 5 Gbit/s on 10 Gbit/s
 fiber optical connections. The installation of these fibers are as described above for the CROs fibers.

2115 3.3.3 Offline Computing

2116 The interface between the DAQ and offline computing is described in DUNE DocDB-7123 [?].
 2117 The DAQ team is responsible for reducing the data volume to the level that is agreed upon by all
 2118 interested parties, and the raw data files are transferred from SURF to Fermilab using a dedicated
 2119 network connection. A disk buffer is provided by the DAQ on or near the SURF site to hold the
 2120 data from several days of data taking so that the operation of the experiment is not affected if there
 2121 happens to be a network disruption between SURF and Fermilab.

2122 During stable running, the data volume produced by the DAQ systems of all four detector modules
 2123 will be no larger than 30 PB/year. This maximum data rate is expected to be independent of the
 2124 number of detector modules that are operational. During the construction of the second, third,
 2125 and fourth detector modules, the extra rate per detector module will be used to gather data to
 2126 aid in the refinement of the data selection algorithms. During commissioning, the data rate is
 2127 expected to be higher than nominal running and it is anticipated that a data volume on the order
 2128 of one year will be necessary to commission a detector module.

2129 The disk buffer at SURF is planned to be 300 TB in size. The data link from SURF to Fermilab
 2130 will support 100 Gbit/s (30 PB/year corresponds to about 8 Gbit/s). The offline computing team
 2131 is responsible for developing the software to manage the transfer of files from SURF to Fermilab.
 2132 The DAQ team is responsible for producing a reference implementation of the software that is used
 2133 to access and decode the raw electronics data. The offline group is also responsible for providing

2134 the framework for real-time data quality monitoring (DQM). This monitoring is distinct from the
 2135 online monitoring (OM). Developing the payload jobs that run various algorithms to summarize
 2136 the data is the joint responsibility of the DAQ, offline, reconstruction and other groups. The
 2137 DQM system includes a visualization system that can be accessed from the Internet and shows
 2138 specifically where operation shifts are performed.

2139 **3.3.4 Slow Control**

intfc-sc
 2140 The cryogenic instrumentation and slow controls (CISC) systems monitor detector hardware and
 2141 conditions not directly involved in taking the data described above. That data is stored both
 2142 locally (in CISC database servers in the CUC) and offline (the databases will be replicated back
 2143 to Fermilab) in a relational database indexed by timestamp. This allows bi-directional communi-
 2144 cations between the DAQ and CISC by reading or inserting data into the database as needed for
 2145 non time-critical information.

2146 For prompt, time sensitive status information such as *run is in progress* or *camera is on*, a low-
 2147 latency software status register is available on the local network to both systems.

2148 There is no hardware interface. However, several racks of CISC servers are in the counting room
 2149 of the CUC, and rack monitors in DAQ racks are read out into the CISC data stream.

2150 Note that life and hardware safety-critical items will be hardware interlocked according to Fermilab
 2151 standards, and fall outside the scope of this interface.

2152 **3.3.5 External Systems**

ntfc-ext
 2153 Need to receive information on beam spills (Giles) , SNEWS (Alec).

2154 The DAQ is required to save data based on external triggers, e.g., when a pulse of beam neutrinos
 2155 arrives at the FD; or upon notice of an interesting astrophysical event by SNEWS [?] or LIGO.
 2156 This could involve going back to save data that has already been buffered (see Section ??), or
 2157 changing the trigger or zero suppression criteria for data taken during the interesting time period.

2158 **3.3.5.1 Beam Trigger**

2159 The method for predicting and receiving the time of the beam spill is described in Section ?? Once
 2160 that time is known to the DAQ, a high-level trigger can be issued to ensure that the necessary full
 2161 data can be saved from the buffer and saved as an event.

[sec:fd-daq-design-beam-spills]

2162 3.3.5.2 Astrophysical Triggers

2163 SuperNova Early Warning System (SNEWS) is a coincidence network of neutrino experiments that
 2164 are individually sensitive to an SNB observed from a core-collapse supernova somewhere in our
 2165 galaxy. While DUNE must be sensitive to such a burst ~~on its own~~^{sec:id-daqsel}, and is expected to be able to
 2166 contribute to the coincidence network (Section ??) via a TCP/IP socket, the capability to save
 2167 data based on other observations provides an additional opportunity to ensure capture of this rare
 2168 and valuable data. A SNEWS alert is formed when two or more neutrino experiments report a
 2169 potential SNB signal within 10 s. A script running on the SNEWS server at BNL, provided by a
 2170 given experiment that wishes to receive an alert, sends out a message with the earliest time in the
 2171 coincidence. The latency from the neutrino burst is set by the response time of the second fastest
 2172 detector to report to SNEWS. This could be as short as seconds, but could be tens of seconds.
 2173 At latencies larger than 10 s, full data might not be available, but selected data is expected to be
 2174 manageable.

2175 Other astrophysical triggers are available to which DUNE alone is unlikely to have sensitivity,
 2176 except in rare cases, or if the triggers are taken as an ensemble. Among these are gravitational
 2177 wave triggers (the details are being worked out during the current LIGO shutdown), and high-
 2178 energy photon transients, most notably gamma ray bursts. In fact, the use of network sockets on
 2179 the timescale of seconds enabled cooperation between LIGO, VIRGO, the Gamma Ray Coordinates
 2180 Network (GCN)¹, and a number of automated telescopes to make the discovery that *short/hard*
 2181 gamma ray bursts are caused by colliding neutron stars [?].

2182 3.4 Production and Assembly

2183 3.4.1 DAQ Components

2184 The FD DAQ system comprises the classes of components listed below. In each case, we outline
 2185 the production, procurement, quality assurance (QA), and quality control (QC) strategies.

2186 3.4.1.1 Custom Electronic Modules

2187 Custom electronic modules, specified and designed by the DAQ consortium, are used for two
 2188 functional components in the DAQ FE. The first is to interface the detector module electronics
 2189 to the DAQ FEC systems, which are likely to be based on the FELIX PCIe board. The other is
 2190 for real-time data processing (particularly for the SP module), which will likely be based on the
 2191 Cluster On Board (COB) ATCA blade. PROTODUNE-SP currently implements both designs,
 2192 and new designs optimized according to DUNE requirements will be developed. It is possible
 2193 that we will make use of commercially-designed hardware in one or other of these roles. DAQ
 2194 consortium institutes have significant experience in the design and production of high-performance

¹Described in detail at https://gcn.gsfc.nasa.gov/gcn_describe.html

2195 digital electronics for previous experiments. Our strategy is therefore to carry out design in-house,
2196 manufacturing and QA steps in industry, and testing and QC procedures at a number of specialized
2197 centers within the DUNE collaboration. Where technically and economically feasible, modules will
2198 be split into subassemblies (e.g., carrier board plus processing daughtercards), allowing production
2199 tasks to be spread over more consortium institutes.

2200 DUNE electronic hardware will be of relatively high performance by commercial standards, and will
2201 contain high-value subassemblies such as large field programmable gate arrays (FPGAs). Achieving
2202 a high yield will require significant effort in design verification, prototyping and pre-production
2203 tests, as well as in tendering and vendor selection. The production schedule is largely driven by
2204 these stages and the need for thorough testing and integration with firmware and software before
2205 installation, rather than by the time for series hardware manufacture. This is somewhat different
2206 from the majority of other DUNE FD components.

2207 **3.4.1.2 Commercial Computing**

2208 The majority of procured items will be standard commercial computing equipment, in the form
2209 of compute and storage servers. Here, the emphasis is on correct definition of the detailed specifici-
2210 cation, and the tracking of technology development, in order to obtain the best value during the
2211 tendering process. Computing hardware will be procured in several batches, as the need for DAQ
2212 throughput increases during the construction period.

2213 **3.4.1.3 Networking and data links**

2214 The data movement system is a combination of custom optical links (for data transmission from the
2215 cryostats to the CUC) and commercial networking equipment. The latter items will be procured
2216 in the same way as other computing components. The favored approach to procurement of custom
2217 optics is purchase of pre-manufactured assemblies ready for installation, rather than on-site fiber
2218 preparation and termination. Since transmission distances and latencies in the underground area
2219 are not critical, the fiber run lengths do not need to be of more than a few variants. It is assumed
2220 that fibers will not be easily accessible for servicing or replacement during the lifetime of the
2221 experiment, meaning that procurement and installation of spare *dark* fibers (including, if necessary,
2222 riser fibers up the SURF hoist shafts) is necessary.

2223 **3.4.1.4 Infrastructure**

2224 All DAQ components will be designed for installation in 48.3 cm (standard 19 in) rack infrastruc-
2225 ture, either in the CUC or above ground. Standard commercial server racks with local air-water
2226 heat exchangers are likely to be used. These items will be specified and procured within the
2227 consortium, but will be pre-installed (along with the necessary electrical, cooling and safety in-
2228 frastructure) under the control of technical coordination (TC) before DAQ beneficial occupancy.

2229 3.4.1.5 Software and firmware

2230 The majority of the DAQ construction effort will be invested in the production of custom software
2231 and firmware. Based on previous experiments, these projects are likely to use tens to hundreds of
2232 staff-years of effort, and will be significant projects even by commercial standards, mainly due to
2233 the specialized skills required for real-time software and firmware. A major project management
2234 effort is required to guide the specification, design, implementation and testing of the necessary
2235 components, especially as developers will be distributed around the world. Use of common com-
2236 ponents and frameworks across all areas of the DAQ is mandatory. Effective DAQ software and
2237 firmware development has been a demonstrated weakness of several previous experiments, and sub-
2238 stantial work is required in the next two years to put in place the necessary project management
2239 regime.

2240 3.4.2 Quality Assurance and Quality Control

2241 High availability is a basic requirement for the DAQ, and this rests upon three key principles:

- 2242 • A rigorous QA and QC regime for components (including software and firmware);
2243 • Redundancy in system design, to avoid single points of failure;
2244 • Ease of component replacement or upgrade with minimal downtime.

2245 The lifetime of most electronic assemblies or commercial computing components will not match the
2246 20 year lifespan of the DUNE experiment. It is to be expected that essentially all components will
2247 therefore be replaced during this time. Careful system design will allow this to take place without
2248 changes to interfaces. However, it is intended that the system run for at least the first three
2249 to four years without substantial replacements, and QA and QC, as well as spares production,
2250 will be steered by this goal. Of particular importance is adequate burn-in of all components
2251 before installation underground, and careful record-keeping of both module and subcomponent
2252 provenance, in order to identify systematic lifetime issues during running.

2253 3.4.3 Integration testing

2254 Since the DAQ will use subcomponents produced by many different teams, integration testing is a
2255 key tool in ensuring compatibility and conformance to specification. This is particularly important
2256 in the prototyping phase before the design of final hardware. Once pre-production hardware is
2257 in hand, an extended integration phase will be necessary in order to perform final debugging
2258 and performance tuning of firmware and software. In order to facilitate ongoing optimization in
2259 parallel with operations, and compatibility testing of new hardware or software, we envisage the
2260 construction of one or more permanent integration test stands at DAQ institutions. These will be
2261 in locations convenient to the majority of consortium members, i.e., at major labs in Europe and

2262 the USA. A temporary DAQ integration and testing facility near SURF will also be required as
2263 part of the installation procedure.

2264 **3.5 Installation, Integration and Commissioning**

2265 **3.5.1 Installation**

2266 The majority of DAQ components will be installed in a dedicated and partitioned area of the CUC
2267 as shown in Figure ??, starting as soon as the consortium has beneficial occupancy of this space.
2268 Conventional facilities (CF) is responsible for running fiber from the SP module's WIBs to the
2269 DAQ, and from the DAQ to the surface. This is currently projected to take place eighteen months
2270 before APAs are installed in the SP module, allowing time for final component acceptance testing
2271 in the underground environment, and to prepare the DAQ for detector testing and commissioning.
2272 Some DAQ components (event builder, storage cluster and WAN routers, plus any post-event-
2273 builder processing) will be installed above ground.

2274 A total of 500 kVA of power and cooling will be available to run the computers in the counting room.
2275 Twelve 48.3 cm (standard 19 in) server racks (of up to 58U height) per module have initially been
2276 allocated for each detector module, with two more each for facilities and CISC. An optimized layout,
2277 including the necessary space for hardware installation and maintenance, plus on-site spares, will be
2278 developed once the DAQ design is finalized. The racks will be water cooled with local air-to-water
2279 heat exchangers. To allow expanded headroom for initial testing, development, and commissioning
2280 throughput, the full complement of rack infrastructure and network equipment for four detector
2281 modules will be installed from the start.

2282 The counting room is similar to a server room at a university or national lab in terms of the need for
2283 cleanliness, ventilation, fire protection, drop flooring, and access control. Networking infrastructure
2284 and fiber breakout will take up some of the rack space, but very little of the power budget. Power
2285 to individual machines and crates must to be controlled remotely via power distribution units,
2286 since it is desirable to minimize DAQ workers' presence underground if there is work that can be
2287 done from the surface or remotely. Some uninterruptible power supply (UPS) capacity is needed
2288 to allow for an orderly shutdown of computers, but only networking equipment requires longer-
2289 duration backup power, this is to enable remote recovery from short-term power failures.

2290 **3.5.2 Integration with Detector Electronics**

2291 Basic technical integration with detector electronics will take place before installation, during a
2292 number of integration exercises in the preceding years. We anticipate that the consortium will
2293 supply and support small-scale instances of the DAQ system for testing of readout hardware at
2294 the production sites, based on prototype or pre-production hardware. Full-scale DAQ testing
2295 will have been completed with artificial data sources during internal integration. The work to be

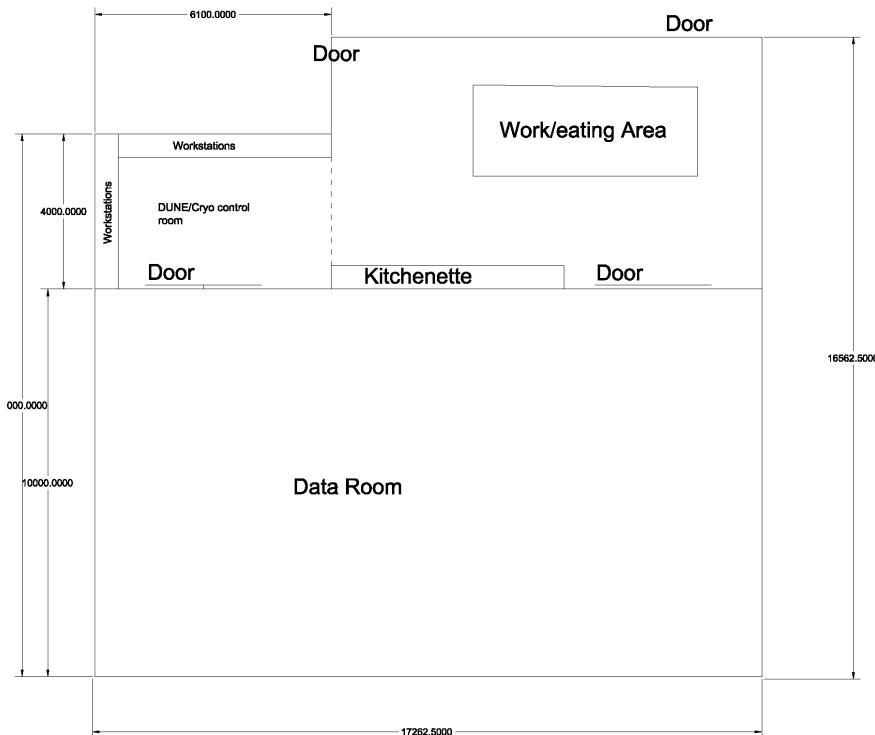


Figure 3.4: Floor plan for the DAQ and control room space in the CUC. The DAQ Room has space for at least 52 racks of servers and routers. Fiber from the WIBs in the detector caverns enter in the upper right of this room, terminate in a breakout panel, and are distributed to the RCEs in these racks, then to FELIX servers (also in this room) as outlined in Figure ??.

[fig:daq-readout-buffering-baseline](#)

done during installation is therefore essentially channel-by-channel verification of the final system as it is installed, on a schedule allowing for any rectifying work to be carried out on the detector immediately (i.e., the DAQ must gather and present data in effectively real time). This implies the presence of a minimal but sufficient functional DAQ system before detector installation commences, along with the timing and fast control system, and the capability to permanently record data for offline analysis. However, it does not require triggering, substantial event building or data transfer capacity. The DAQ installation schedule is essentially driven by this requirement.

In addition, the data pipeline from event builder, via the storage buffer and WAN, to the offline computing facilities, must be developed and tested. We anticipate this work largely happening at Fermilab in parallel with detector installation, and the full-scale instances of these components being installed at SURF in preparation for start of data-taking.

3.5.3 Commissioning

System commissioning for the DAQ comprises the following steps:

- Integration with detector subsystems of successive detector modules;
- Final integration and functional testing of all DAQ components;
- Establishment of the necessary tools and procedures to achieve high-efficiency operation;
- Selection, optimization and testing of trigger criteria;
- Ongoing and continuous self-test of the system to identify actual or imminent failures, and to assess performance.

Each of these steps will have been carried out at the integration test stands before being used on the final system. The final steps are to some extent continuous activities over the experiment lifetime, but which require knowledge of realistic detector working conditions before final validation of the system can take place. We anticipate that these steps will be carried out during the cryostat filling period, and form the major focus of the DAQ consortium effort during this time.

3.6 Safety

Two overall safety plans will be followed by the FD DAQ. General work underground will comply with all safety procedures in place for working in the detector caverns and CUC underground at SURF. DAQ-specific procedures for working with racks full of electronics or computers, as defined at Fermilab, will be followed, especially with respect to electrical safety and the fire suppression system chosen for the counting room. For example, a glass wall between the server room space and the other areas in Figure ?? will be necessary to prevent workers in the server room from being

2327 unseen if they are in distress, and an adequate hearing protection regime must be put in place.

2328 There are no other special safety items for the DAQ system not already covered by the more
2329 general safety plans referenced above. The long-term emphasis is on remote operations capability
2330 from around the world, limiting the need for physical presence at SURF, and with underground
2331 access required only for urgent interventions or hardware replacement.

2332 **3.7 Organization and Management**

-daq-org

2333 At the time of writing, the DAQ consortium comprises 30 institutions, including universities and
2334 national labs, from five countries. Since its conception, the DAQ consortium has met on roughly
2335 a weekly basis, and has so far held two international workshops dedicated to advancing the FD
2336 DAQ design. The current DAQ consortium leader is Dave Newbold, U. Bristol, UK.

2337 Several key technical and architectural decisions have been made in the last months, that have
2338 formed an agreed basis for the DAQ design and implementation presented in this document.

2339 **3.7.1 DAQ Consortium Organization**

nsortium

2340 The DUNE DAQ consortium is currently organized in the form of five active Working Groups
2341 (WG) and WG Leaders:

- 2342 • Architecture, WG Leaders: Giles Barr (U. Oxford) and Giovanna Lehman-Miotto (CERN);
- 2343 • Hardware, WG Leaders: David Cussans (U. Bristol) and Matthew Graham (SLAC);
- 2344 • Data selection, WG Leader: Josh Klein (U. Penn.);
- 2345 • Back-end, WG Leader: Kurt Biery (Fermilab);
- 2346 • Integration and Infrastructure, WG Leader: Alec Habig (U. Minnesota Duluth).

2347 During the ongoing early stages of the design, the architecture and hardware WGs have been
2348 holding additional meetings focused on aspects of the design related to architecture solutions and
2349 costing. In parallel, the DAQ Simulation Task Force effort, which was in place at the time of
2350 the consortium inception, has been adopted under the data selection WG, and simulation studies
2351 have continued to inform design considerations. This working structure is expected to remain in
2352 place through at least the completion of the Technical Proposal. During the construction phase
2353 of the project we anticipate a new organization, built around major subsystem construction and
2354 commissioning responsibilities, and drawing also upon expertise build up during the ProtoDUNE
2355 projects.

3.7.2 Planning Assumptions

The DAQ planning is based the assumption of a SP module first, followed by a DP module. The schedule is sensitive to this assumption, as the DAQ requirements for the two module types are quite different. Five partially overlapping phases of activity are planned (see Figure ??):^{fig:daq_schedule}

- A further period of R&D activity, beginning at the time of writing, and culminating in a documented system design in the technical design report (TDR) around July 2019;
- Production and testing of a full prototype DAQ slice of realistic design, culminating in an Engineering Design Review;
- Preparation and fit out of the CUC counting room with a minimal DAQ slice, in support of the first module installation;
- Production and delivery of final hardware, computing, software and firmware for the first module;
- Production and delivery of final hardware, computing, software and firmware for the second module.

This schedule assumes beneficial occupancy of the CUC ounting room by end of the first quarter of 2022, and the availability of facilities to support an extended large-scale integration test in 2020 (e.g., CERN or Fermilab). We assume the availability of resources for installation and commissioning of final DAQ hardware (e.g., surface control room and server room facilities) from around the first quarter of 2023, and the integration and test facility (ITF) from the second quarter of 2022. The majority of capital resources for DAQ construction will be required from the second quarter of 2022, with a first portion of funds for the minimal DAQ slice from the first quarter of 2021.

3.7.3 High-level Cost and Schedule

The high-level DAQ schedule, which is based upon the current DUNE FD top-level schedule, is shown in Figure ??.^{fig:daq-schedule}

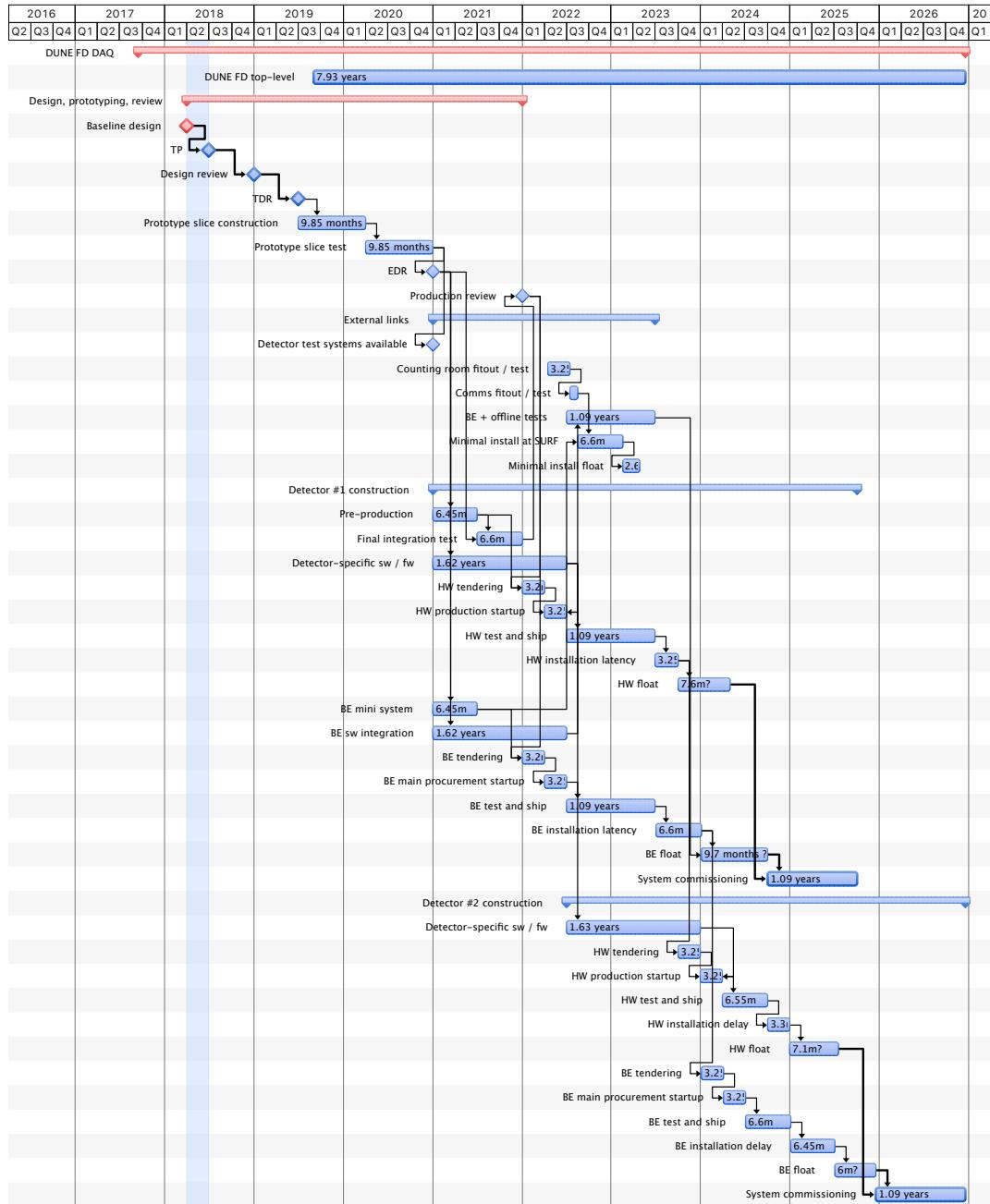


Figure 3.5: DAQ high-level schedule

fig:daq-

