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BiSS® C-mode (unidirectional) for RESOLUTE™ encoders

For a full description of *BiSS* C-mode (unidirectional), please refer to Renishaw datasheet L-9709-9001.

More information on *BiSS* protocols is available on the *BiSS* website: **www.biss-interface.com**

About RESOLUTE encoders

Renishaw RESOLUTE *BiSS* encoders use the C-mode (unidirectional) *BiSS* serial protocol.

- Rotary encoders are single-turn (with 2^n counts per revolution and no revolution counting).
- Linear encoders are available with a range of different resolutions (and maximum measuring lengths) as specified on the product data sheet.

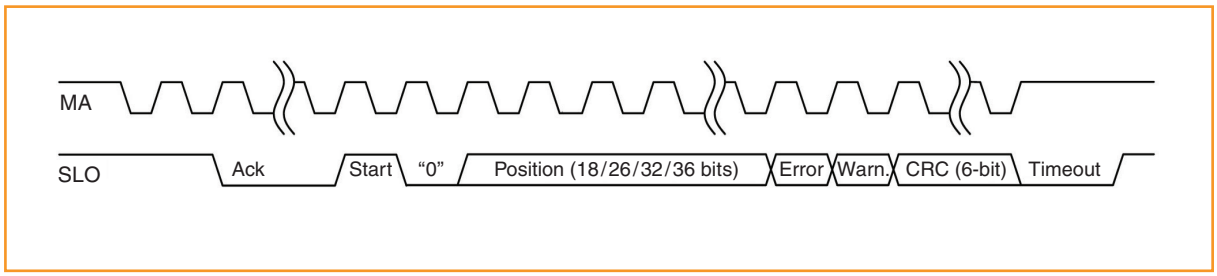
Description of the *BiSS* interface

BiSS C-mode (unidirectional) is a fast synchronous serial interface for acquiring position data from an encoder. It is a master-slave interface. The master controls the timing of position acquisition and the data transmission speed, and the encoder is the slave. The interface consists of two unidirectional differential pairs of lines:

- "MA" transmits position acquisition requests and timing information (clock) from master to encoder
- "SLO" transfers position data from encoder to master, synchronised to MA.

The diagram below shows the data transmitted.

Data format



The master-slave signal communication format is RS485/RS422 differential line-driven.

A typical request cycle proceeds as follows:

1. When idle, the master holds MA high. The encoder indicates it is ready by holding SLO high.
2. The master requests position acquisition by starting to transmit clock pulses on MA.
3. The encoder responds by setting SLO low on the second rising edge on MA.
4. After the "Ack" period is complete, the encoder transmits data to the master synchronised with the clock as shown in the diagrams above.
5. When all data has been transferred, the master stops the clock and sets MA high.
6. If the encoder is not yet ready for the next request cycle, it sets SLO low (the Timeout period).
7. When the encoder is ready for the next request cycle, it indicates this to the master by setting SLO high.

Data sheet
BiSS® C-mode (unidirectional) for RESOLUTE encoders

Description of data

- **Ack**
  This is the period during which the readhead calculates the absolute position.
  See the timing information table below.

- **Start and "0" (1 bit each)**
  The encoder transmits the start bit to signal to the master that it is starting to transmit data.
  The start bit is always high and the "0" bit is always low.

- **Position (18, 26, 32 or 36 bits)**
  The absolute position data is in binary format and sent MSB first. For rotary encoders, there are exactly 2^n counts per revolution, after which the count "wraps around" to zero.
  [Lower resolutions may be achieved by ignoring the least significant bit(s) of the position data.]

- **Error (1 bit)**
  The error bit is active low: "1" indicates that the transmitted position information has been verified by the readhead's internal safety checking algorithm and is correct; "0" indicates that the internal check has failed and the position information should not be trusted. The error bit is also set to "0" if the temperature exceeds the maximum specified for the product.

  Note that the operating temperature limits of RESOLUTE systems are specified in the product datasheets.

- **Warning (1 bit)**
  The warning bit is active low: "0" indicates that the encoder scale (and/or reading window) should be cleaned.
  Note that the warning bit is not an indication of the trustworthiness of the position data. Only the error bit should be used for this purpose.

- **CRC for position data (6 bit)**
  The CRC polynomial for position, error and warning data is: $x^6 + x^1 + x^0$. It is transmitted MSB first and inverted.
  The start bit and "0" bit are omitted from the CRC calculation.

- **Timeout**
  RESOLUTE encoders are capable of acquiring a new position reading every 40 µs (a maximum request cycle rate of 25 kHz). Therefore 40 µs must elapse between the start of one request cycle and the start of the next. However, it is possible for data transmission to be complete before 40 µs have elapsed. In this case, the encoder signals this to the master by holding the SLO line low until 40 µs have elapsed. This is the timeout period.

Resetting the encoder

The master may reset the encoder at any time during a request cycle by stopping the clock and setting MA high.
MA must be held high for the remaining duration of the full request cycle, including timeout period if applicable.
Note that SLO may be high or low during resetting (typically depending on the state of the last bit transmitted).

Line delay compensation

Signals travelling between master and encoder experience a time delay due to the cable length and signal propagation delays within the master and encoder. The time delay has no effect at low clock speeds (where the time delay is much shorter than the clock period). However, for high clock speeds, it is necessary for the master to implement line delay compensation.
The master determines the round-trip time delay by measuring the time between transmitting the second rising edge on MA and receiving the falling edge of “Ack” on SLO.

MA clock speed	Maximum cable length	
	Without line delay compensation	With line delay compensation
250 kHz	95 m	100
1 MHz	20 m	100
2 MHz	8 m	100
5 MHz	0.5 m	100
10 MHz	NA	50

Notes:

1. All figures relate to installations using Resolute readheads with original Renishaw cable up to 10 m in length, with the remainder cable length consisting of Renishaw 14-core extension cable (A-9531-0238).
2. Care should be taken to ensure supply voltage is maintained within 5 V ±10% at the readhead connector. For extension cable lengths greater than 50 m, it is recommended that the spare 8 x 26 awg cores are also used for power supply and the Resolute readhead cable should be limited to 5 m to minimise voltage drop.
3. This table makes no allowance for propagation delays within the master.

Timing information

	Min	Typical	Max	Units	Notes
Ack time			20	µs	Note that Ack period always ends on a rising edge of MA.Therefore at low MA clock frequencies, the Ack time may exceed 20 µs
MA clock frequency	0.25		10	MHz	Within any one request cycle, the MA clock frequency must be constant. The duty cycle should be 1:1
Request cycle rate			25	kHz	Note that 25 kHz is not achievable for all MA clock frequencies (because data transmission takes too long).
Sampling moment	3.975	4.000	4.025	µs	Timed from the first rising edge on MA
RESOLUTE internal line delay			42.5	ns	This is the internal propagation delay (MA-SLO) within RESOLUTE encoders.
Line delay due to cable length		10		ns/m	This is the round-trip delay experienced by signals travelling through RESOLUTE cable (i.e. from master to encoder and back to master again).

Renishaw plc
New Mills, Wotton-under-Edge,
Gloucestershire GL12 8JR
United Kingdom

T +44 (0)1453 524524
F +44 (0)1453 524901
E uk@renishaw.com

www.renishaw.com

RENISHAW
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For worldwide contact details, please visit our main website at www.renishaw.com/contact

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