VLSI DESIGN
CSE460
SECTION : 08L
Assignment 1 [Lab]
Deadline: 07/03/2022 11:59 pm

Rules:

1. You need to submit the code, the compilation report and the simulation report with a brief description for each of the problems.
2. Prepare your assignment in a doc file. For each of the problems, paste the code in the doc file (Not screenshot, copy-paste the code), add screenshots (full screen) of the compilation and simulation report and give a brief description of how your timing diagrams manifest expected outputs.The explanation can either be typed or scanned. Next, export the doc as pdf and rename it as **Section_StudentID_Assignment3.pdf.**
3. Finally, submit the pdf within the deadline.

Problem 1 :
Design a 4 bit adder/subtractor circuit in Verilog. The circuit should have a control pin e.g. **add_sub.** If **add_sub** is high, the circuit will behave as an adder and if **add-sub** is low, the circuit will behave as a subtractor.

Problem 2:
Design a 4 to 2 priority encoder (0>1>3>2) using Verilog HDL and verify using timing diagram.

Note:

1. Show and discuss the case when multiple input bits are high.

Submission Link
https://forms.gle/81JiUPV2bZKxve227