



CSE460
VLSI Design Lab
(Sec 08)

Assignment-2

Submitted By:

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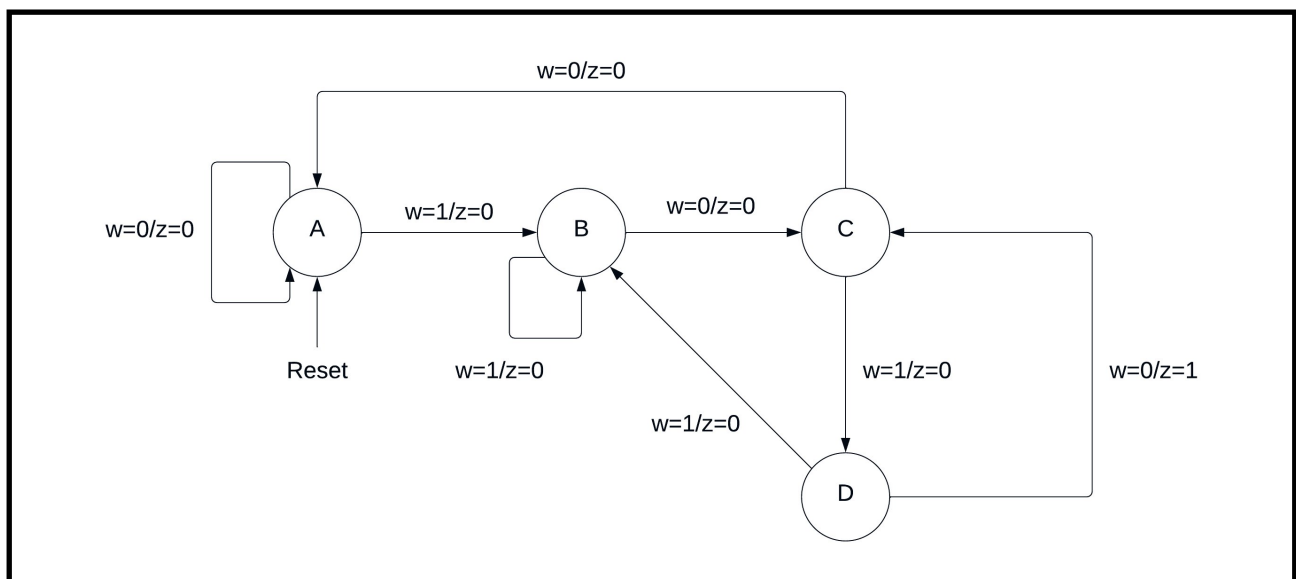
Submission Date: 30th March, 2022

Problem 1:

An FSM has an input w and an output z . The machine has to generate $z = 1$ when the following patterns in w are detected: 1010; otherwise, $z = 0$. The machine should reset when ($\text{Reset} = 0$).

A. We need to use a Mealy-Type FSM since the output is happening in the same clock cycle as when the pattern is detected instead of being a clock cycle later.

B. State Diagram:



C. State-Assigned Table:

Present State	Next State		z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
00	00	01	0	0
01	10	01	0	0
10	00	11	0	0
11	10	01	1	0

where, $A = 00$, $B = 01$, $C = 10$ and $D = 11$.

D. module problem1_18301033 (clk, rst, w, z);

```
input clk, rst, w;
output reg z;
reg [1:0] present, next;
parameter [1:0] A=0, B=1, C=2, D=3;
```

```

always @(present, w)
  case (present)

    A: if (w) begin
          next = B;
          z = 0;
        end
      else begin
          next = A;
          z = 0;
        end

    B: if (w) begin
          next = B;
          z = 0;
        end
      else begin
          next = C;
          z = 0;
        end

    C: if (w) begin
          next = D;
          z = 0;
        end
      else begin
          next = A;
          z = 0;
        end

    D: if (w) begin
          next = B;
          z = 0;
        end
      else begin
          next = C;
          z = 1;
        end
      endcase

always @(posedge clk, negedge rst)
  if (rst == 0)
    present <= A;
  else
    present <= next;

endmodule

```

E. Compilation Report:

Quartus II - C:/Users/rafa/OneDrive/Documents/CSE460 Labs/Assignments/Assignment 2/Problem 1/problem1_18301033 - problem1_18301033 - [Compilation Report - FI]

File Edit View Project Assignments Processing Tools Window Help

problem1_18301033

Project Navigator

Entity	Logic Cells	LC Registers	Memory Bits
FLEX10KE: AUTO			
problem1_18301... 5 (5)	4		0

Tasks

Row: Compilation

Task	Time
Compile Design	00:00:06
Analysis & Synthesis	00:00:01
Fitter (Place & Route)	00:00:01
Assembler (Generate programming files)	00:00:02
Classic Timing Analysis	00:00:01
EDA Netlist Writer	00:00:01
Program Device (Open Programmer)	

Compilation Report - Flow Summary

Flow Status: Successful - Mon Mar 28 21:08:20 2022

Quartus II Version: 8.1 Build 163 10/28/2008 SJ Web Edition

Revision Name: problem1_18301033

Top-level Entity Name: problem1_18301033

Family: FLEX10KE

Met timing requirements: Yes

Total logic elements: 5 / 1,728 (< 1 %)

Total pins: 4 / 102 (4 %)

Total memory bits: 0 / 24,576 (0 %)

Total PLLs: 0

Device: EPF10K30ETC144-1

Timing Models: Final

Messages

Type: Message

Info: Simulation partitioned into 1 sub-simulations

Info: Simulation coverage is 88.24 %

Info: Number of transitions in simulation is 176

Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (43) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16

For Help, press F1

Simulation Report:

Quartus II - C:/Users/rafa/OneDrive/Documents/CSE460 Labs/Assignments/Assignment 2/Problem 1/problem1_18301033 - problem1_18301033 - [Simulation Report - Sim]

File Edit View Project Assignments Processing Tools Window Help

problem1_18301033

Project Navigator

Entity	Logic Cells	LC Registers	Memory Bits
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problem1_18301... 5 (5)	4		0

Tasks

Row: Compilation

Task	Time
Compile Design	00:00:06
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Classic Timing Analysis	00:00:01
EDA Netlist Writer	00:00:01
Program Device (Open Programmer)	

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 12.725 ns

Pointer: 190.3 ns

Interval: 177.58 ns

Start: End:

Name	Value at 12.73 ns
clk	A 1
rst	A 1
w	A 1
z	A 0

Messages

Type: Message

Info: Simulation partitioned into 1 sub-simulations

Info: Simulation coverage is 88.24 %

Info: Number of transitions in simulation is 176

Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (43) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16

For Help, press F1

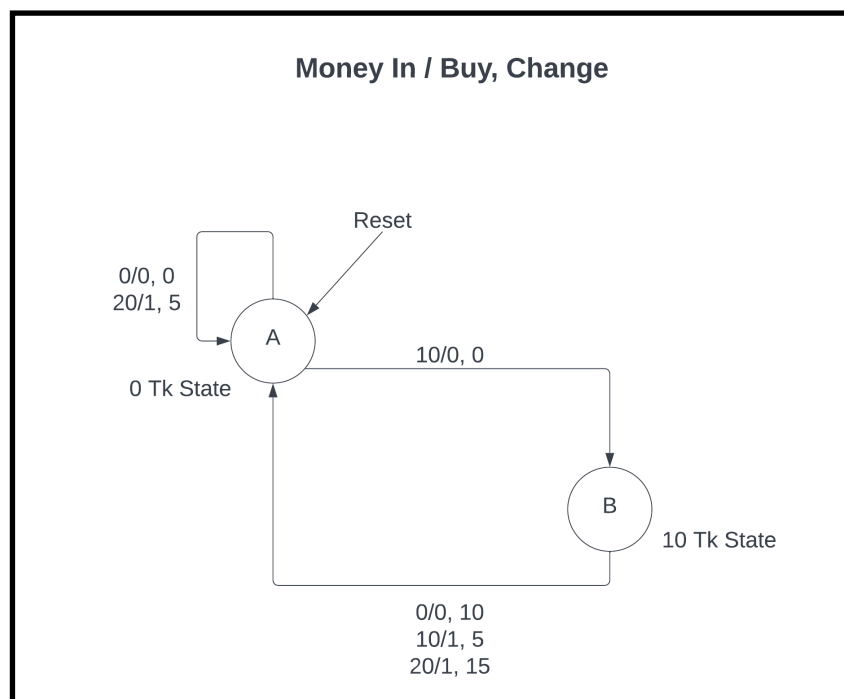
Explanation:

As can be seen in the simulation report, between 100 - 300 ns, there was a 1010 pattern, making the output equal to 1 during 250 - 300 ns (the same clock cycle the pattern was detected). Then again, between 200 - 400 ns, there was another overlapping 1010 pattern detected, making the output equal to 1 during 350 - 400 ns (the same clock cycle the pattern was detected). In all other times, the output was equal to 0.

Problem 2:

You have to design a vending machine for a 15 Tk product. User's money, returned money by the machine, and product bought condition is represented as mny (2-bit input), chg (output), and buy (1-bit output). The vending machine can only accept inputs: no money (mny = 00), Tk 10 (mny = 01), and Tk 20 (mny = 10). If no money is inserted into the machine, it will immediately return the user's money back. Once an acceptable input is more than or equal to 20 Tk, the machine immediately generates an output (buy=1), goes back to the initial state, and gives back the change (if required).

A. State Diagram:



B. It will produce 4 types of changes: 0Tk, 5Tk, 10Tk and 15Tk.

clock	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12
mny	0	10	0	0	10	10	0	0	20	0	10	20
buy	0	0	0	0	0	1	0	0	1	0	0	1
chg	0	0	10	0	0	5	0	0	5	0	0	15

Hence, the chg output should be of 2bits to represent 4 changes.

C. State-Assigned Table:

Present State	Next State			buy			chg		
	mny			mny			mny		
	00	01	10	00	01	10	00	01	10
0	0	1	0	0	0	1	00	00	01
1	0	0	0	0	1	1	10	01	11

where A = 0 and B = 1 for states, and 0Tk = 00, 5Tk = 01, 10Tk = 10 and 15Tk = 11 for change given.

D. module problem2_18301033 (clk, rst, mny, buy, chg);

```

input clk, rst;
input [1:0] mny;
output reg buy;
output reg [1:0] chg;
reg present, next;
parameter A=0, B=1;
parameter [1:0] R0=0, R5=1, R10=2, R15=3;

```

```

always @(present, mny)
    case(present)
        A: if (mny == 2'b00)
            begin
                next = A;
                buy = 0;
                chg = R0;
            end

        else if (mny == 2'b01)

```

```

        begin
            next = B;
            buy = 0;
            chg = R0;
        end

        else if (mny == 2'b10)
        begin
            next = A;
            buy = 1;
            chg = R5;
        end

B: if (mny == 2'b00)
    begin
        next = A;
        buy = 0;
        chg = R10;
    end

    else if (mny == 2'b01)
    begin
        next = A;
        buy = 1;
        chg = R5;
    end

    else if (mny == 2'b10)
    begin
        next = A;
        buy = 1;
        chg = R15;
    end

endcase

always @(posedge clk, negedge rst)
    if (rst == 0)
        present <= A;

    else
        present <= next;

endmodule

```

E. Compilation Report:

The screenshot shows the Quartus II interface with the 'Compilation Report - Flow Summary' window open. The 'Flow Summary' tab is selected, displaying the following information:

- Flow Status: Successful - Wed Mar 30 22:23:45 2022
- Quartus II Version: 8.1 Build 163 10/28/2008 SJ Web Edition
- Revision Name: problem2_18301033
- Top-level Entity Name: problem2_18301033
- Family: FLEX10KE
- Met timing requirements: Yes
- Total logic elements: 9 / 1,728 (< 1 %)
- Total pins: 7 / 102 (7 %)
- Total memory bts: 0 / 24,576 (0 %)
- Total PLLs: 0
- Device: EPF10K30ETC144-1
- Timing Models: Final

The 'Tasks' window on the left shows the compilation process flow:

- Compile Design: 00:00:06
- Analysis & Synthesis: 00:00:01
- Fitter (Place & Route): 00:00:02
- Assembler (Generate programming files): 00:00:01
- Classic Timing Analysis: 00:00:01
- EDA Netlist Writer: 00:00:01
- Program Device (Open Programmer):

The 'Messages' window at the bottom shows the following information:

- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 95.83 %
- Info: Number of transitions in simulation is 176
- Info: Quartus II Simulator was successful. 0 errors, 0 warnings

Simulation Report:

The screenshot shows the Quartus II interface with the 'Simulation Report - Simulation Waveforms' window open. The 'Simulation Waveforms' tab is selected, displaying the following information:

- Simulation mode: Functional

The 'Master Time Bar' shows the following values:

- 12.725 ns
- Pointer: 66.48 ns
- Interval: 53.76 ns
- Start: 0 ps
- End: 560.0 ns

The 'Waveform' window displays the following signals:

- clk: A 1
- rst: A 1
- mny: U 0
- buy: A 0
- chg: A [0]

The 'Messages' window at the bottom shows the following information:

- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 95.83 %
- Info: Number of transitions in simulation is 176
- Info: Quartus II Simulator was successful. 0 errors, 0 warnings

Explanation:

As can be seen from the simulation report, whenever there is a 0Tk input only ($mny = 00$), $buy = 0$ and the change is 0Tk as well ($chg = 00$) [0-50ns]. When there is a single 10Tk input ($mny = 01$), $buy = 0$ and the change is 0Tk also ($chg = 00$) [50-100ns]. However, when this input is followed by:

- A 0Tk input ($mny = 00$), $buy = 0$ and the change is 10Tk ($chg = 10$) since $10Tk < 15Tk$ [100-150ns].
- A 10Tk input ($mny = 01$), $buy = 1$ and the change is 5Tk ($chg = 01$) since $20Tk > 15Tk$ [250-300ns].
- A 20Tk input ($mny = 10$), $buy = 1$ and the change is 15Tk ($chg = 11$) since $30Tk > 15Tk$ [550-600ns].

When there is a single 20Tk input ($mny = 10$), $buy = 1$ and change is 5Tk ($chg = 01$) since $20Tk > 15Tk$ [400-450ns]. Hence, the simulation follows the expected outputs of the problem statement.