BL0942 datasheet

BL0942 Calibration-free Metering IC

Datasheet

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Catalog

1 Product Description

1.1 Function Introduction

BL0942 is a calibration-free energy metering IC with built-in clock, suitable for single-phase multi-function electricity meters, smart sockets, smart home appliances and other applications with better cost performance.

BL0942 incorporates two sigma delta ADC with a high accuracy energy measurement core. It can measure electric parameters such as current and voltage RMS, active power, active energy, fast current RMS (for over-current protection).

BL0942 provides access to on-chip registers via UART/SPI interfaces. the output Pin(CF1) provide pulse that is proportional to active energy.　Zero-crossing voltage (ZX_V), zero-crossing current (ZX_I) and overcurrent are accessible via the external pin.

BL0942 has a patent active power no-load detection to prevent meter-creep. which can be combined with reasonable external hardware design to ensure that the noise energy isn't calculated in the energy pulse when there is no load

1.2 Features

● Two independent Sigma-Delta ADC, one current and one voltage.
● Range of Current (10mA ~ 30A) @ 1mOhm current sense resistor
● Range of Active energy（1w~6600w）@1mohm@220V
● Measure current and voltage RMS, fast current RMS, active power, active energy
● Gain error is less than 1%, calibration-free when peripheral components meet certain conditions
● Programmable over-current detection
● ZX_V/ZX_I output
● Provide sampled waveform data for load type analysis
● SPI (≤900kHz)/ UART (4800~38400bps), UART supports multi-chip communication(available only with BL0942-TSSOP14L package)
● On-chip power supply monitoring, IC resets when VDD is lower than 2.7V(typical)
● On-chip reference 1.218v(typical)
● On-chip oscillator as clock source
● Single 3.3V supply, low power consumption 10mW (typical)
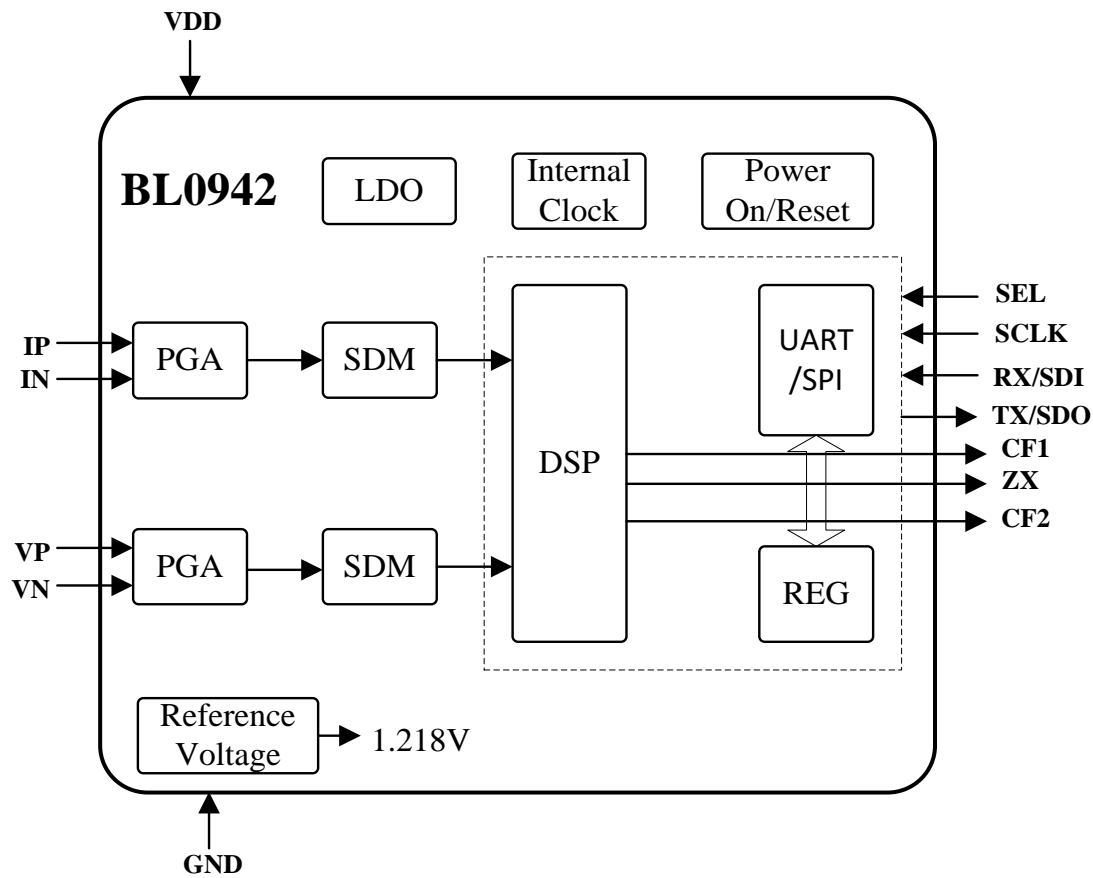● SOP8/SSOP10L/TSSOP14L package

1.3 System Block Diagram

Figure 1

1.4 Pin Configuration and Function Description
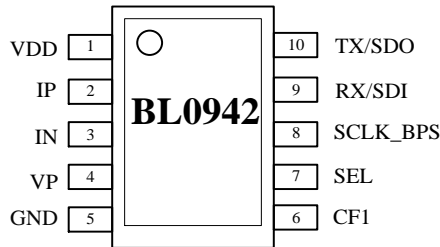
Figure 2

Pin Description (SSOP10L)

Pin No	Mnemonic	Description
1	VDD	Power supply (3.3V)
2,3	IP, IN	Analog input for Current Channel, this differential voltage input has a maximum input range of ± 42mVpp (30mV RMS)
4	VP	Analog input for Voltage Channel, this voltage input has a maximum input range of ± 100mVpp (70mV RMS)
5	GND	Ground reference
6	CF1	Logic output. See the OT_FunX register configuration section
7	SEL	UART/SPI interface selection (0: UART 1: SPI), pull-down resistance inside, connected to GND is 0 level (UART), connected directly to VDD is high level (SPI)
8	SCLK_BPS	Serial Clock input for SPI. If using UART, this pin is used to config baud rate of UART, =0 or NC, Baudrate=4800bps; =1, Baudrate=9600bps.
9	RX/SDI	Receive Line for UART interface/Data input for SPI interface, need external pull-up resistor for UART interface.
10	TX/SDO	Transmit Line for UART interface/Data output for SPI interface, need external pull-up resistor for UART interface.

Figure 3

Pin Description (TSSOP14L)

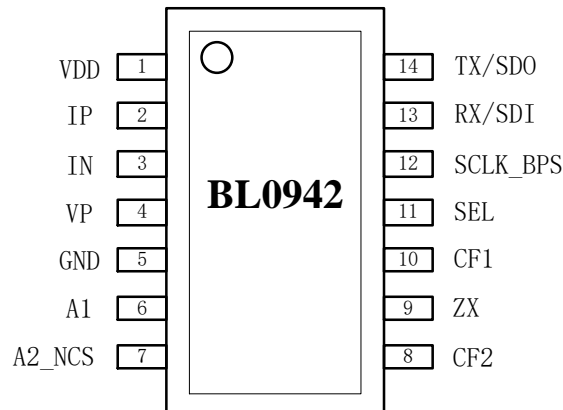| Pin No	Mnemonic	Description
1	VDD	Power supply (3.3V)
2,3	IP,IN	Analog input for Current Channel, this differential voltage input has a maximum input range of $\pm$ 42mVpp (30mV RMS)
4	VP	Analog input for Voltage Channel, this voltage input has a maximum input range of $\pm$ 100mVpp (70mV RMS)
5	GND	Ground reference
6	A1	Chip Address set for UART interface
7	A2_NCS	Chip select for SPI interface. Chip Address set for UART interface
8	CF2	Logic output. See the OT_FunX register configuration section
9	ZX	Zero crossing Voltage logic output. See the OT_FunX register configuration section
10	CF1	Logic output. See the OT_FunX register configuration section
11	SEL	UART/SPI mode selection (0: UART 1: SPI), pull-down resistance inside, connected to GND is 0 level (UART), connected directly to VDD is high level (SPI)
12	SCLK_BPS	Serial Clock input for SPI. If using UART, this pin is used to config baud rate of UART, =0 or NC, Baudrate=4800bps; =1, Baudrate=9600bps.
13	RX/SDI	Receive Line for UART interface/Data input for SPI interface, need external pull-up resistor for UART interface.
14	TX/SDO	Transmit Line for UART interface/Data output for SPI interface, need external pull-up resistor for UART interface.
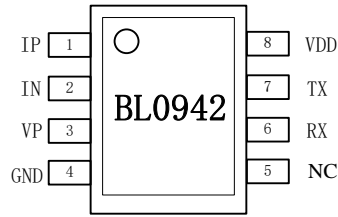
Figure 4

Pin Description（SOP8）

Pin No	Mnemonic	Description
8	VDD	Power supply (3.3V)
1,2	IP, IN	Analog input for Current Channel, this differential voltage input has a maximum input range of $\pm$ 42mVpp (30mV RMS)
3	VP	Analog input for Voltage Channel, this voltage input has a maximum input range of $\pm$ 100mVpp (70mV RMS)
4	GND	Ground reference
5	NC	Reserved
6	RX	Receive Line for UART interface, need external pull-up resistor for UART interface.
7	TX	Transmit Line for UART interface, need external pull-up resistor for UART interface.

BL0942   calibration-free metering IC

1.5 Register List

Address	Register Name	Significant bit	Default	Register Description
Electrical parameter register(read only)				
0x01	I_WAVE	20	0x00000	Current waveform data, signed
0x02	V_WAVE	20	0x00000	Voltage waveform data, signed
0x03	I_RMS	24	0x000000	Current RMS, unsigned
0x04	V_RMS	24	0x000000	Voltage RMS, unsigned
0x05	I_FAST_RMS	24	0x000000	Fast Current RMS, unsigned
0x06	WATT	24	0x000000	Active power, signed
0x07	CF_CNT	24	0x000000	Active energy pulse counter, unsigned
0x08	FREQ	16	0x4E20	Line voltage frequency
0x09	STATUS	10	0x000	System Status
User operated register (read / write)				
0x12	I_RMSOS	8	0x00	Current RMS Offset
0x14	WA_CREEP	8	0x0B	Active power No-load threshold
0x15	I_FAST_RMS_TH	16	0xFFFF	Fast Current RMS threshold
0x16	I_FAST_RMS_CYC	3	0x1	Cycles for Fast Current RMS measurement
0x17	FREQ_CYC	2	0x3	Cycles for Line voltage frequency measurement
0x18	OT_ FUNX	6	0x24	Logic output configuration
0x19	MODE	10	0x87	User mode selection
0x1A	GAIN_CR	2	0x2	Current channel gain
0x1C	SOFT_RESET	24	0x000000	Software reset, BL0942 resets if 0x5a5a5a is written to this register
0x1D	USR_WRPROT	8	0x00	User write protection. Only 0x55 is written to this register, the user operation register can be written

Note: the data frame of communication protocol is 24bit, and the upper invalid bit need be supplemented with 0.

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1.6 Special Register Description

User mode selection register

0x19	MODE			
Bits	Bit Name	Default	Description	
[1:0]	reserved	b11	reserved	
[2]	CF_EN	b1	Active energy and pulse output Enable	0: Disable
				1: Enable
[3]	RMS_UPDATE_SEL	b0	Selection of refresh time for RMS	0：400ms
				1：800ms
[4]	FAST_RMS_SEL	b0	FAST_RMS waveform from； 0：full wave；1；AC wave	
[5]	AC_FREQ_SEL	b0	Selection of AC frequency	0：50Hz
				1：60Hz
[6]	CF_CNT_CLR_SEL	b0	Clear after read of CF_CNT register Enable	0: Disable
				1: Enable
[7]	CF_CNT_ADD_SEL	b1	Mode selection of active energy pulse accumulation	0: Algebraic accumulation mode
				1: Absolute accumulation mode
[9:8]	UART_RATE_SEL	b00	Baud rate selection	00 01 : The baud rate is decided by the external pin SCLK_BPS SCLK_BPS=0, 4800bps SCLK_BPS=1, 9600bps
				10 : 19200bps
				11 : 38400bps
[23:10]	reserved	b0	reserved	

Logic Output configuration register

0x18	OT_ FUNX		
Bits	Bit Name	Default	Description
[1:0]	CF1_FUNX_SEL	b00	CF1 output selection bit: b00: Active energy pulse Output (CF) b01: Logic output of over-current event(O_C) b10: Logic output of zero crossing voltage (ZX_V) b11: Logic output of zero crossing current (ZX_I)
[3:2]	CF2_FUNX_SEL	b01	CF2 output selection bit: b00: Active energy pulse Output (CF) b01: Logic output of over-current event(O_C) b10: Logic output of zero crossing voltage (ZX_V) b11: Logic output of zero crossing current (ZX_I)
[5:4]	ZX_FUNX_SEL	b10	ZX output selection bit: b00: Active energy pulse Output (CF) b01: Logic output of over-current event(O_C) b10: Logic output of zero crossing voltage (ZX_V) b11: Logic output of zero crossing current (ZX_I)
[23:6]	reserved	b0	reserved

System Status register

0x09	STATUS		
Bits	Bit Name	Default	Description
[0]	CF_REVP_F	b0	This bit indicates the direction of the last energy Pulse CF 0: positive energy pulse; 1: negative energy pulse
[1]	CREEP_F	b0	This bit indicates whether the BL0942 is in active power no-load status 0: not active power no-load state; 1: active power no-load state
[7:2]	reserved	b0	reserved
[8]	I_ZX_LTH_F	b0	This bit indicates the current signal is below zero crossing current detection threshold
[9]	V_ZX_LTH_F	b0	This bit indicates the current signal is below zero crossing current detection threshold
[23:10]	reserved	b0	reserved

The Gain config of Current channel

0x1A	GAIN_CR	The Gain config of Current channel	
No.	name	default value	description
[1:0]	GAIN_CR	B10	00：Gain=1； 01：Gain=4； 10：Gain=16(default)；11：Gain=24；
[23:10]	reserved	b0	reserved

1.7 Performance

1.7.1 Electronic Characteristic Parameter

(VDD = 3.3V, GND = 0V, 25 °C, Energy accuracy error measure via CF output)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Power Supply	VDD		3.0		3.6	V
Power Consumption	Iop	VDD=3.3V		3		mA
Active Energy Measurement Error		Dynamic range 4000:1		0.1		%
Active Power Measurement Error (large signal)		30A~100mA@1mOhm sampling resistor		0.2		%
Active Power Measurement Error (small signal)		100mA~50mA@1mOhm sampling resistor		0.4		%
Active Power Measurement Error (tiny signal)		50mA~10mA@1mOhm sampling resistor		0.6		%
RMS Measurement Error (large signal)		35A~100mA@1mOhm sampling resistor		0.2		%
RMS Measurement Error (small signal)		100mA~50mA@1mOhm sampling resistor		2		%
RMS Measurement Error (tiny signal)		50mA~10mA@1mOhm sampling resistor		6		%
Refresh time of I_FAST_RMS	50Hz	Set by I_FAST_RMS_CYC register	10		160	mS
	60Hz		8.3		133	mS
Zero-crossing logic output delay		ZX_V/ZX_I		570		uS
Phase Error between Channels	PF08err	Phase lead 37° （PF=0.8C）			0.5	%
	PF05err	Phase lag 60° （PF=0.5L）			0.5	%
AC Power Supply Rejection (output frequency variation)	ACPSRR	IP/N=100mV		0.1		%

DC Power Supply Rejection (output frequency variation)	DCPSRR	VP/N=100mV		0.1		%
Analog input (current)		differential input (peak)			42	mV
Analog input (voltage)		differential input (peak)			100	mV
Analog input impedance		IP, IN,VP		370		kΩ
SEL pull-down resistor		SEL PIN		56.9		kΩ
Analog input bandwidth		（-3dB）		3.5		kHz
On-chip reference	Vref			1.218		V
Logic input high-level	V_{INH}	VDD=3.3V±5%	2.6			V
Logic input low-level	V_{INL}	VDD=3.3V±5%			0.8	V
Logic output high-level	V_{OH}	VDD=3.3V±5% IOH=5mA	VDD-0.5			V
Logic output low-level	V_{OL}	VDD=3.3V±5% IOL=5mA			0.5	V

1.7.2   Absolute Maximum Rations

（T = 25 ℃）

Paramter	Symbol	Value	Unit
Supply Voltage VDD	VDD	-0.3 ~ +4	V
Analog Input Voltage (to GND)	IP, IN, VP	-4 ~ +4	V
Digital Input Voltage (to GND)	A1, A2_NCS, SEL, SCLK_BPS, RX/SDI	-0.3 ~ VDD+0.3	V
Digital Output Voltage (to GND)	CF1,CF2,ZX,TX/SDO	-0.3 ~ VDD+0.3	V
Operating Temperature Range	Topr	-40 ~ +85	℃
Storage Temperature Range	Tstr	-55 ~ +150	℃

2 Theory of Operation

BL0942 includes two-channel PGA, two-channel sigma delta ADC, internal clock, POR, LDO and digital signal processing module (DSP).

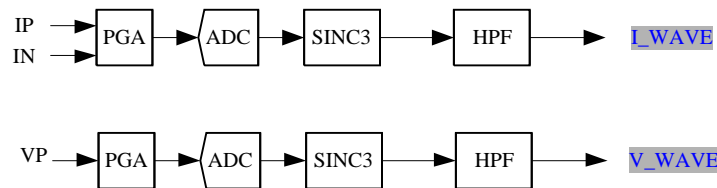## 2.1 Current and Voltage Instantaneous Waveform

Figure 4

The current and voltage waveform data are updated at a rate of 7.8kSPS (samples per second). Each sampling data is 20bit signed value, which is saved in the waveform data register (I_WAVE, V_WAVE).

Note: the register is 24bit. If the number of bits is insufficient, zero is added to the high invalid bit.

address	Register Name	Significant bit	Default	Register Description
0x01	I_WAVE	20	0x00000	Current Waveform Data, signed
0x02	V_WAVE	20	0x00000	Voltage Waveform Data, signed

2.2 Active Power
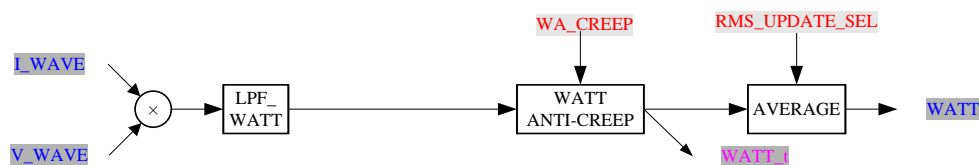
Figure 5

address	Register Name	Significant bit	Default	Register Description
0x06	WATT	24	0x000000	Active power, signed

WATT Register value: WATT= $\dfrac{3537*I(A)*V(V)*\text{COS}（\varphi）}{Vref^2}$

Where:

I(A)/ V(V) is the rms voltage (mV) of analog input PIN(IP&IN, VP&GND).

Φ is the phase angle between current and voltage signals.

Vref is the on-chip reference voltage, the typical value is 1.218V;

This register indicates whether the active power is positive or negative, bit [23] = 0, active power is positive power, bit [23] = 1, active power is negative power, in complement code form.

2.3 Anti-creep of Active Power

BL0942 has a patent active power no-load detection to prevent meter-creep, which ensures that the power of board level noise will not accumulate energy when there is no-load.

Active power anti-creep threshold register (WA_CREEP) is an 8-bit unsigned value, and the default value is 0x0B。When the absolute value of instantaneous active power is less than this threshold, the output active power is set to 0. This can make the value of the active power register is 0 even if there is a tiny noise signal in no-load, and the active energy is not accumulated.

address	Register Name	Significant bit	Default	Register Description
0x14	WA_CREEP	8	0x0B	Active power No-load threshold

The corresponding relationship between the WA_CREEP and WATT register is shown in the following equation:

$$\text{WA\_CREEP} = \text{WATT} * \frac{256}{3125}$$

Note: when the BL0942 is in the Anti-creep state, the current RMS register is also set to 0.

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2.4 Energy Measurement

BL0942 provides energy pulse output. The active energy can be obtained by integrating the instantaneous active power for a period of time, and output the energy calibration pulse (CF). The CF_CNT register stores the number of output energy pulses CF, as shown in the figure below.
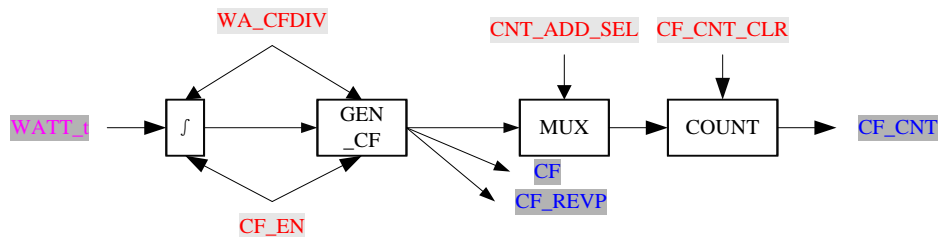

Figure 6

Address	Register Name	Significant bit	Default	Register Description
0x07	CF_CNT	24	0x000000	Active energy pulse counter

BL0942 provide active energy via CF_CNT register. The energy information also can be provided through CF1/CF2/ZX pin.   When the active energy pulse period is shorter than 160mS, the duty cycle of the pulse output is 50%; when the pulse period is longer than 160mS, the high-level fixed pulse width is 80mS.

0x19	MODE		Operating mode register		
No.	name	default	description		
[2]	CF_EN	b1	Active energy and pulse output Enable	0: Disable	
				1: Enable	
[6]	CF_CNT_CLR_SEL	b0	Clear after read of CF_CNT register Enable	0: Disable	
				1: Enable	
[7]	CF_CNT_ADD_SEL	b1	Mode selection of active energy pulse accumulation	0: Algebraic accumulation mode	
				1: Absolute accumulation mode	

Cumulative time of each CF pulse $t_{CF} = \dfrac{1638.4*256}{WATT}$

Where: WATT is the value of active power register(0x06).

2.5 Voltage/Current RMS

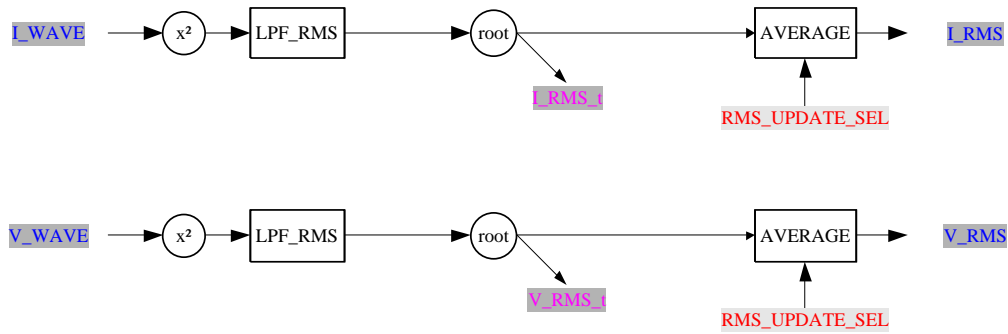The RMS algorithm of current and voltage is shown in the figure below.

Figure 7

Address	Register Name	Significant bit	Default	Register Description
0x03	I_RMS	24	0x000000	Current RMS, unsigned
0x04	V_RMS	24	0x000000	Voltage RMS, unsigned

0x19	MODE	Operating mode register		
No.	name	default value	description	
[3]	RMS_UPDATE_SEL	0b0	Selection of refresh time for RMS	0：400ms
				1：800ms

Current RMS register equation: $I\_RMS = \dfrac{305978*I(A)}{Vref}$

Voltage RMS register equation: $V\_RMS = \dfrac{73989*V(V)}{Vref}$

Where:

Vref : on-chip reference voltage, the typical value is 1.218 V. (the gain config of current is 16)

I(A): the input signal of IP&IN Pins (unit: mV).

V(V): the input signal of VP&GND Pins (unit: mV).

2.6 Over current detection

BL0942 provide over-current detection. The absolute value of I_WAVE_F is accumulated in half cycle or cycle time and stored in I_FAST_RMS register. If I_FAST_RMS[23:8] >= I_FAST_RMS_TH[15:0], the over-current logic output is high level.
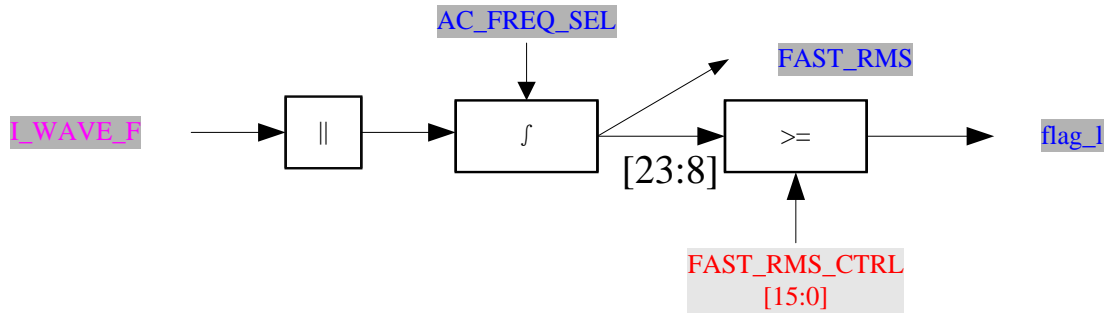
Figure 8

Address	Register Name	Significant bit	Default	Register Description
0x15	I_FAST_RMS_TH	16	0xFFFF	Current fast RMS threshold

Address	Register Name	Significant bit	Default	Register Description
0x05	I_FAST_RMS	24	0x000000	Current fast RMS, unsigned

$$I\_FAST\_RMS \approx I\_RMS * 0.363$$

NOTE: the FAST_RMS is only used for large signal measurement. The accuracy error of FAST_RMS will be worse in small signal because of DC bias on the board.

Address	Register Name	Significant bit	Default	Register Description	
0x16	I_FAST_RMS_CYC	3	0x1	Line cycle for Current fast RMS measurement	
				000	0.5 cycles
				001	1 cycle
				010	2 cycles
				011	4 cycles
				other	8 cycles

The I_FAST_RMS measure period can be config by I_FAST_RMS_CYC register. MODE [5] is used to config AC frequency. If MODE [5]=0, the AC frequency is 50Hz, then 1 cycle is 20mS; if MODE[5]=1, the AC frequency is 60Hz, 1cycle is 16.7mS. the shorter the measure period, the more the measure value jitter. If need remove the DC bias , set MODE[4]=1 to select the waveform after HPF as the FAST_RMS source

0x19	MODE	Operating mode register	
No.	name	default value	description
[4]	FAST_RMS_SET	0b0	FAST_RMS waveform from： 0：full wave；1：AC wave
[5]	AC_FREQ_SEL	0b0	0：50Hz

			AC frequency selection	1：60Hz

2.7 Zero-crossing Detection

Bl0942 includes a zero-crossing detection on voltage and current channel. The voltage and current channel ZX information is configured to be output on CF1/CF2/ZX Pin. As shown in Figure 11, the ZX output goes high on the negative-going edge of the signal zero crossing and low on the positive-going edge of signal zero crossing. A delay of approximately 570uS should be expected on ZX logic output pin due to the time delay of HPF.
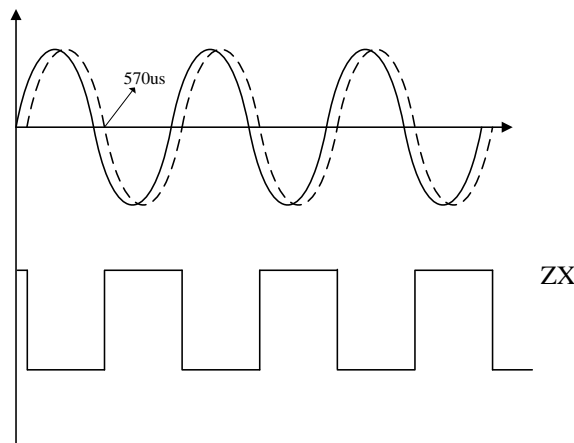
Figure 11

0x18	OT_FUNX		Output configuration register	
No.	name	default value	description	
[1:0]	CF1_FUNX_SEL	0b00	CF1 output selection bit: b00: Active energy pulse Output (CF) b01: Logic output of over-current event(O_C) b10: Logic output of zero crossing voltage (ZX_V) b11: Logic output of zero crossing current (ZX_I)	
[3:2]	CF2_FUNX_SEL	0b01	CF2 output selection bit: b00: Active energy pulse Output (CF) b01: Logic output of over-current event(O_C) b10: Logic output of zero crossing voltage (ZX_V) b11: Logic output of zero crossing current (ZX_I)	
[5:4]	ZX_FUNX_SEL	0b10	ZX output selection bit: b00: Active energy pulse Output (CF) b01: Logic output of over-current event(O_C) b10: Logic output of zero crossing voltage (ZX_V) b11: Logic output of zero crossing current (ZX_I)	

[23:6]	reserved	0b0	reserved

0x19	STATUS		Working status register	
No.	name	default	description	
[8]	I_ZX_LTH_F	0b0	This bit indicates the current signal is below zero crossing current detection threshold	0: Current zero crossing detection is valid
				1: Current zero crossing detection is invalid
[9]	V_ZX_LTH_F	0b0	This bit indicates the current signal is below zero crossing current detection threshold	0: Voltage zero crossing detection is valid
				1: Voltage zero crossing detection is invalid

To prevent spurious zero crossing when a small input is present, there have zero-crossing threshold on all channels of the BL0942.

When the Value of V_RMS register is less then 0x7FFFF, V_ZX_LTH_F =1, the ZX_V keep low-level. When the Value of I_RMS register is less then 0x3FFFF, I_ZX_LTH_F =1, the ZX_I keep low-level.

If any input signal falls below these levels, no zero-crossing signals are produced by BL0942.

2.8 Line Voltage Frequency Detection

BL0942 provides a frequency measurement of the voltage channel. The FREQ register is updated once every set FREQ_CYC cycle.

Address	Register Name	Significant bit	Default	Register Description	
0x08	FREQ	16	0x4e20	Line voltage register, unsigned	
0x17	FREQ_CYC	2	0x3	Line voltage refresh time setting register	
				00	2 cycles
				01	4 cycles
				10	8 cycles
				11	16 cycles

The frequency measurement has a resolution of 2us/LSB, which represents 0.01% when the line frequency is 50Hz and 0.012% when the line frequency is 60Hz.

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The following equation can be used to compute the line frequency using the FREQ register:

$$f_{\text{measure}} = \frac{1000000}{FREQ} \ \text{Hz}$$

In addition, when the RMS voltage is lower than the zero-crossing threshold, the line voltage frequency detection is disable.

3 Communication Interface

BL0942 provides SPI/UART communication interfaces, these communication interface use the same group of pins. So only one mode of communication can be used in each design. The length of the transfer data is 24bits. If the valid data of the register is less than 24bits , the high invalid bit should be fixed with 0, make up 24bits to transfer.

3.1 SPI

- If SEL Pin is pulled up to VDD, the communication method is SPI
- slave mode
- Half duplex communication, the maximum SPI speed is 900kHz
- 8-bits data transmission, data order with MSB-first shifting
- Fixed clock polarity and phase (CPOL = 0, CPHA = 1)
- three or four wire communication method. In three wire mode, A2_NCS is connected to GND. In four-wire mode, the A2_NCS must be driven low for the entire read or write operation.

3.1.1   Operation Mode

CPOL = 0 and CPHA = 1. SCLK has a low-level idle state. Data is received on the falling edge and data is sent on the rising edge.
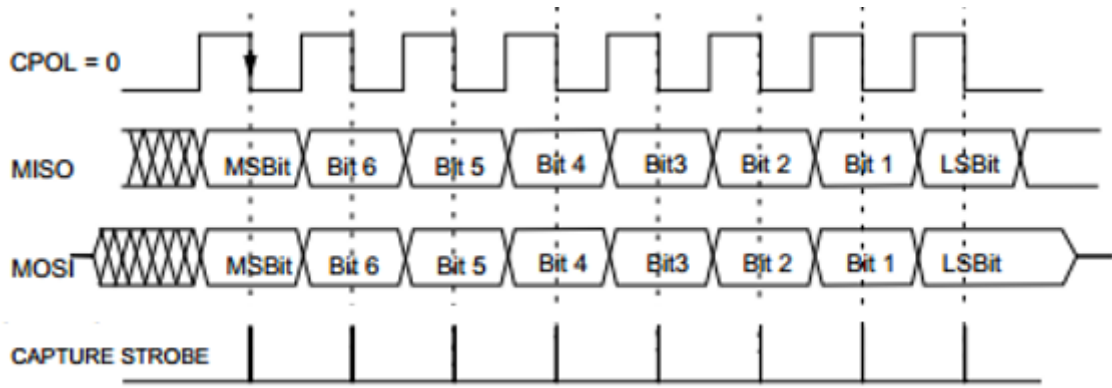
Figure 12

3.1.2   Frame Structure

In SPI communication method, first send 8bit initial byte (0x58) or (0xa8), (0x58) is read operation identification byte, (0xa8) is write operation identification byte, then send register address of BL0942. The following figure shows the data transfer sequence of SPI Write and Read operations.   A complete read/write operation contain 48 bits.

1）Write operation frame

where the checksum byte = ((0xA8 + Address + Data_H + Data_M+ Data_L) & 0xFF) and then bitwise inverted.

2）Read operation frame

where the checksum byte is ((0x58 + Address + Data_H + Data_M+ Data_L) & 0xFF) and then bitwise inverted.

Note: the register data is fixed to 3 bytes (MSB first), if the valid byte of the register data is less than 3 bytes, the invalid bit should be filled with 0)

3.1.3　Fault Tolerant Mechanism of SPI Interface

If MCU send 6 bytes (0xFF), the BL0942 perform a reset function on the SPI communication interface.(using in three-wire SPI mode)

3.2 UART

- SEL pin connected to GND, SEL = 0, UART communication mode.
- slave mode
- Half duplex communication, the baud rate can be configured to 4800bps,9600bps, 19200bps,38400bps.
- 8-bit data transmission, no parity bit, stop bit 1
- Support packet reading
- TSSOP14L package can support the chip address function of the device, and the IC Address can be configured to 0~3 by pins [A2_NCS, A1]. These IC Address set allow communication with multiple devices (maximum 4 pcs of BL0942) on the one UART interface of MCU.

3.2.1　Baud Rate Configuration

BL0942 can configurate Baud Rate by register MODE [9:8] and SCLK_BPS pin.

| 0x19	MODE		Operating mode register			
No.	name	default value	description			
[9:8]	UART_RATE_SEL	0b00	Baud rate selection	00	SCLK_BPS pin = 0: 4800bps	
					SCLK_BPS pin = 1: 9600bps	
				01	Same as 00	
				10	19200bps	
				11	38400bps	

3.2.2　Byte Format
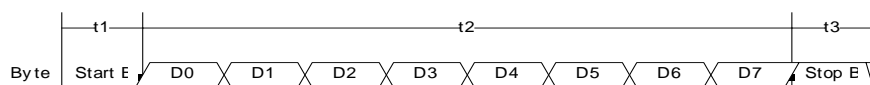
Take baud rate = 4800bps as an example

Start bit low duration t1 = 208us

Valid data bit duration t2 = 208 * 8 = 1664us

Stop bit high duration t3 = 208us

3.2.3 Write Timing

The UART data writing sequence of the host is shown in the figure below. The host first sends command bytes {1,0,1,0,1,0, A2, A1}, then sends the register address that need to write data. Next, the three data bytes are sent (the low byte is first, the high byte is later, if the valid bytes of the data is less than 3 bytes, the invalid byte is supplemented with 0), and finally the CHECKSUM byte is sent.
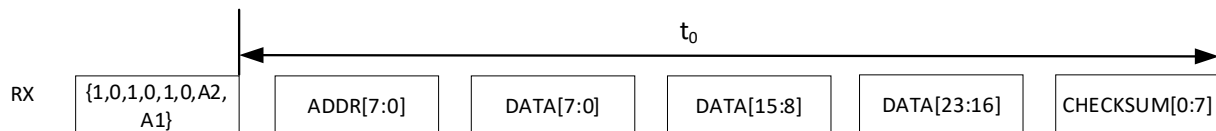
Where:

{1,0,1,0,1,0, A2, A1} is the frame initial byte of the write operation. If PIN A2_NCS=1, A1=0, the BL0942 address is 2, the frame initial byte is 0XAA.
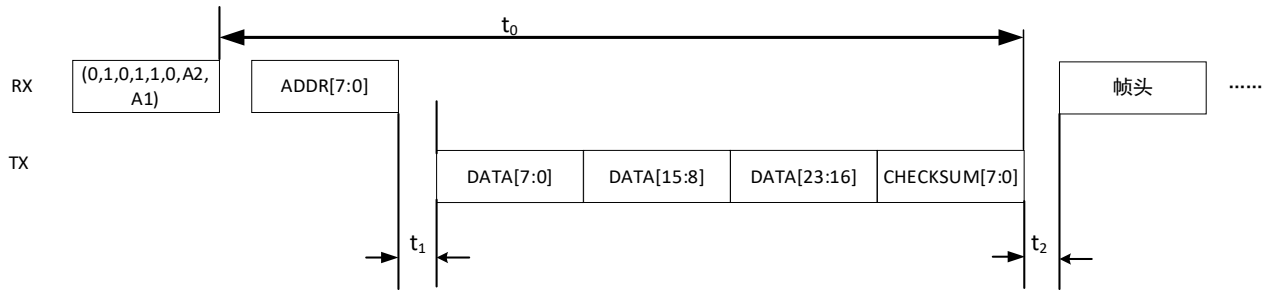
ADDR is the register address of BL0942 that need to write data.

The CHECKSUM byte is ({1,0,1,0,1,0, A2, A1} + ADDR + DATA [7:0] + DATA [15:8] + DATA [23:16]) & 0xff then bitwise inverted.

		Min	Type	Max	Unit
t0	Frame duration（frame identification byte not included）			16	mS

3.2.4 Read Timing

The UART data reading sequence of the host is shown in the figure below. The host first sends command byte {0,1,0,1,1,0, A2, A1}, and then sends the register address to be read. Next, BL0942 will return three data bytes (low byte comes first, high byte comes last, invalid bytes supplemented with 0 if valid byte is less than 3 bytes), and finally CHECKSUM byte.

Where:

{0,1,0,1,1,0, A2, A1} is the frame initial byte of read operation, assuming {A2, A1} = 10, the BL0942 address is 2, the frame initial byte is 0x5A.

ADDR is the register address of BL0942 need to read data.

The CHECKSUM byte is ({0,1,0,1,1,0, A2, A1} + ADDR + DATA [7:0] + DATA [15:8] + DATA [23:16]) & 0xff then bitwise inverted.

		Min	Type	Max	Unit
t0	Frame duration（frame identification byte not included）			16	mS
t1	Interval between the last bit of register address and the first bit of BL0942 returning data		$0.5t_{bit}$		
t2	Frame interval	0.5			uS

**Note: the IC Address of SSOP10L&SOP8 package is 0.**

3.2.5 Packet Reading Mode

The MCU sends a packet of two bytes "{0,1,0,1,1,0, A2, A1} + 0xAA", BL0942 will return a full electric parameter data packet. A total of 23 bytes are returned, which takes about 48ms when 4800bps is used.

All electric parameter package format:

	Send byte order	content
HEAD	0	0x55
I_RMS	1	I_RMS [7:0]
	2	I_RMS [15:8]
	3	I_RMS [23:16]
V_RMS	4	V_RMS [7:0]
	5	V_RMS [15:8]
	6	V_RMS [23:16]
I_FAST_RMS	7	I_FAST_RMS [7:0]
	8	I_FAST_RMS [15:8]
	9	I_FAST_RMS [23:16]
WATT	10	WATT [7:0]
	11	WATT [15:8]
	12	WATT [23:16]
CF_CNT	13	CF_CNT [7:0]
	14	CF_CNT [15:8]
	15	CF_CNT [23:16]
FREQ	16	FREQ [7:0]
	17	FREQ [15:8]
	18	0x00
STATUS	19	STATUS [7:0]
	20	0x00
	21	0x00
CHECKSUM	22	

checksum=(({0,1,0,1,1,0,A2,A1} + 0x55 + data1_l + data1_m + data1_h +……) & 0xff) then bitwise inverted.
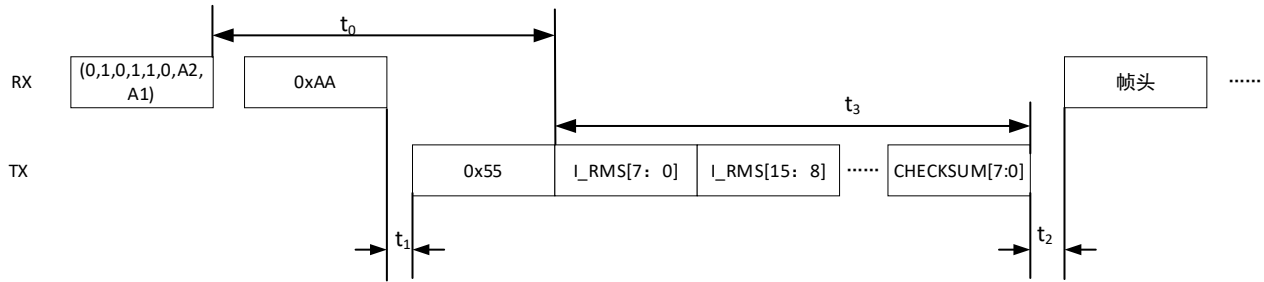
	Packet read timing	Min	Type	Max	Unit
t0	Interval between the end of MCU sending command byte and BL0942 returning the last bit of 0x55			16	mS
t1	Interval between MCU sending last bit of 0xAA and BL0942 return the first bit of 0x55		$0.5t_{bit}$		
t2	Frame interval	0.5			uS
t3	Time of valid data returned by BL0942		$22*t_{byte}$		

3.2.6　Protection Mechanism of UART Interface

● UART communication has a timeout mechanism. Frame timeout will cause the automatic reset of UART.

● If the frame identification byte is incorrect or the checksum byte is incorrect, frame data will be discarded.

● UART module reset, the UART interface of BL0942 continuously receives more than 32 "0", and the UART interface is reset.

Note: in UART mode, multi-chip communication, Frame-to-Frame delay when switching to communicate with another IC should keep above 20mS.
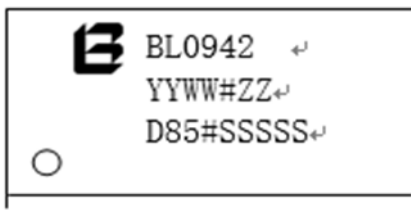
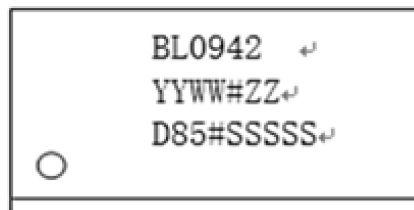# 4 Order Information

BL0942-X　X=SSOP10L: SSOP10L package

X=TSSOP14L:TSSOP14L package

X=SOP8: SOP8 package

5 Marking information

TSSOP14L/SOP8

SSOP10L

"YY" represents the packaging year

"WW" represents packaging week, 01-52 week

"ZZ" represents packaging plant

"#"represents space
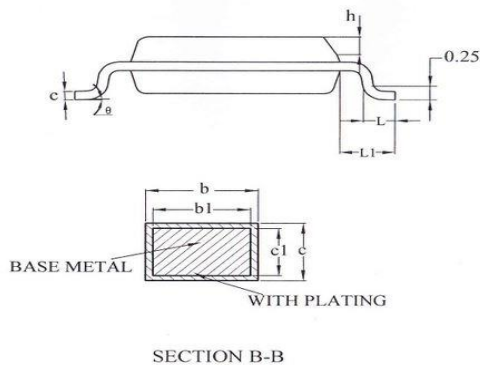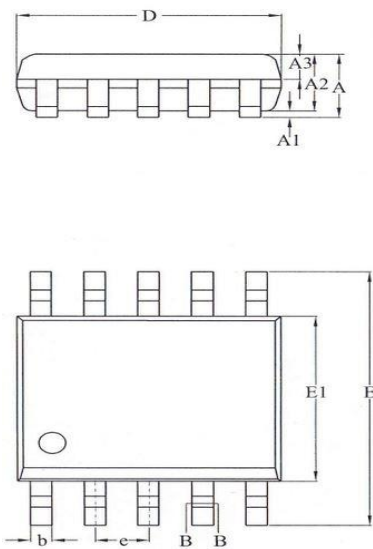
"SSSSS" represents LOT Number

6 Package

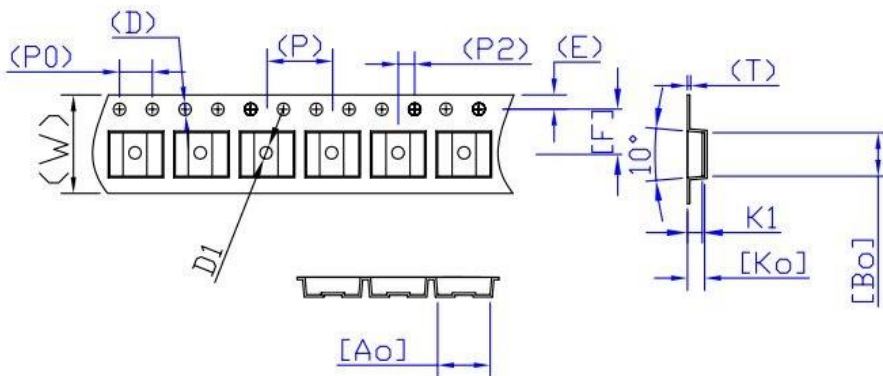Moisture sensitivity grade: MSL3

Quality guarantee period: 2 years

Packaging mode: SSOP10L taping

Minimum package:3000

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.00BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

SECTION B-B

BASE METAL

WITH PLATING

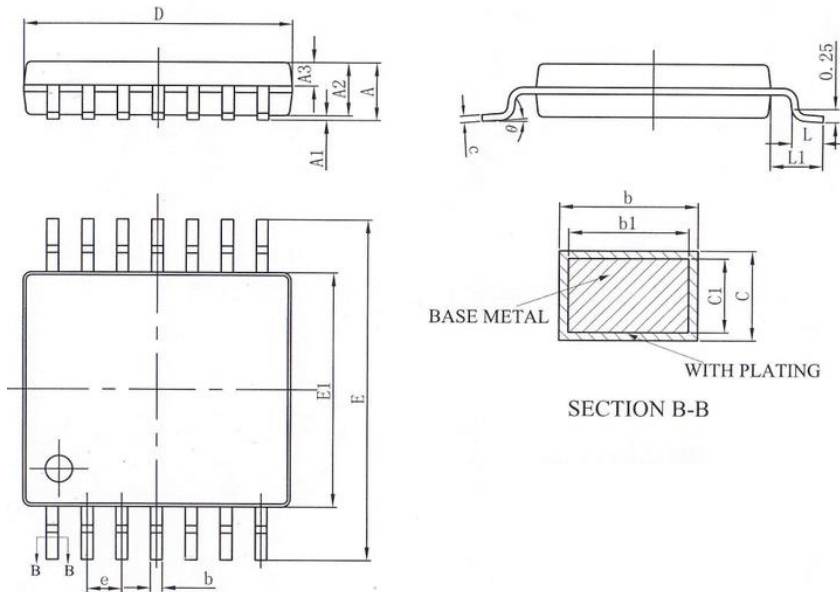| ITEM	W	A0	B0	D	D1	E	F	K1	K0	P0	P2	P	T
DIM	12.0	6.55	5.40	1.5	1.5	1.75	5.50	1.85	2.0	4.0	2.0	8.0	0.30
TOLE	+0.3 -0.3	±0.10	±0.10	+0.1 -0.0	+0.1 -0.0	±0.1	±0.10	±0.05	±0.10	±0.1	±0.1	±0.1	±0.05

Moisture sensitivity grade: MSL3

Quality guarantee period: 2 years

Packaging: TSSOP14L Taping

Minimum package: 3000

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

SECTION B-B

BASE METAL

WITH PLATING
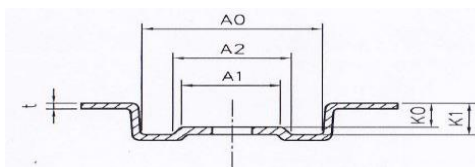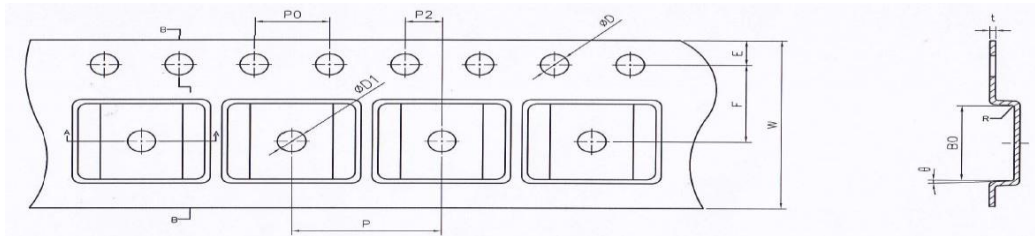
共同尺寸

外观	尺寸(mm)
E	1.75±0.1
F	5.5±0.1
P2	2.0±0.05
D	1.5$^{+0.1}_{0}$
D1	1.5$^{+0.1}_{0}$
P0	4.0±0.1
R	0.5TYP
10P0	40.0±0.20

口袋尺寸

W	12.0±0.1
P	8.0±0.1
A0	6.8±0.1
B0	5.4±0.1
K0	1.3±0.1
t	0.3±0.05
K1	1.7±0.1
A1	3.8±0.2
A2	4.4±0.2
θ	3° TYP

Moisture sensitivity grade: MSL3

Quality guarantee period: 2 years

Packaging: SOP8 Taping

Minimum package: 2500
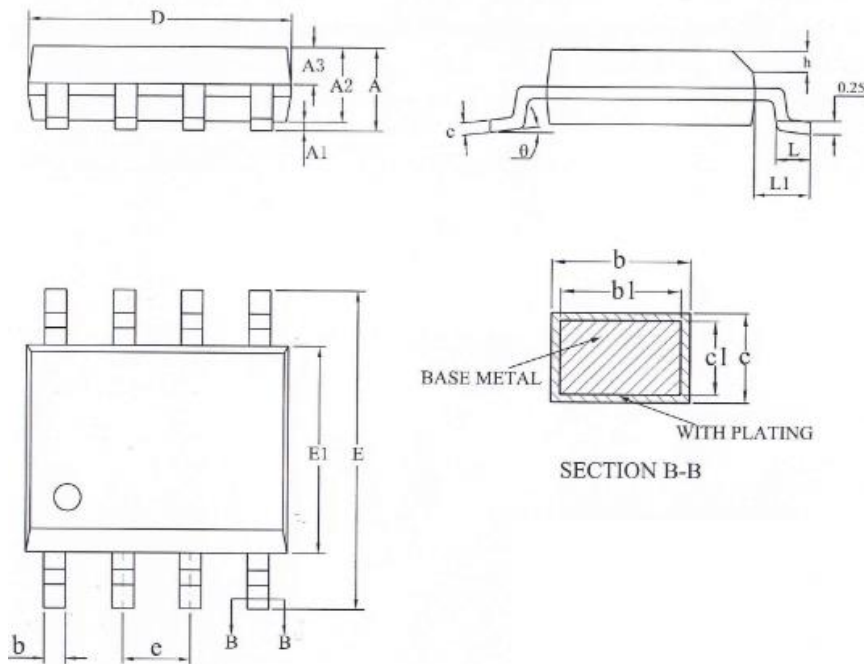
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

SECTION B-B

7 Version update

Version	date	Content
V1.05	2021/08/31	1）Added TSSOP14 package support UART multi-IC communication description 2）Added MODE[4] description 3）Added GAIN_CR register description
V1.06	2021/09/08	Modification
V1.07	2024/06/24	UART timing modification
V1.1	2024/07/16	Add SOP8 package

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