Computer Assignment 2 (Single Cycle MIPS Processor)

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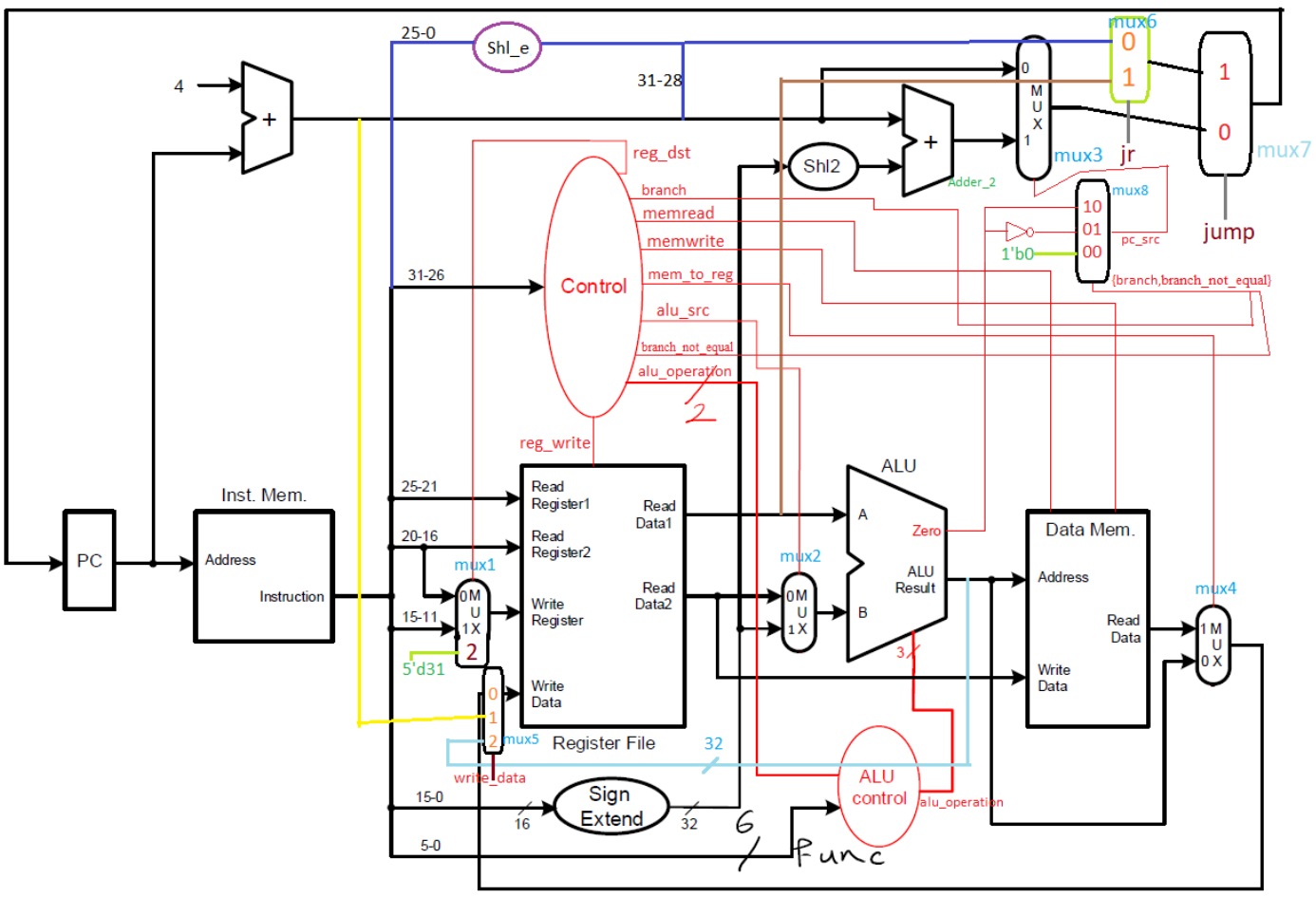
Data Path:



Controller:

	REG_DST	REG_WRITE	ALU_SRC	MEMREAD	MEMWRITE	MEM_TO_REG	WRITE_DATA	BRANCH	BRANCH_NOT_EQUAL	ALU_OPERATION	JUMP	JR
LW	00	1	1	1	0	1	00	0	0	00	0	0
SW	-	0	1	0	1	-	00	0	0	00	0	0
BEQ	-	0	0	0	0	-	00	1	0	01	0	0
BNE	-	0	0	0	0	-	00	0	1	01	0	0
SUB	01	1	0	0	0	0	00	0	0	10	0	0
ADD	01	1	0	0	0	0	00	0	0	10	0	0
ADDI	00	1	1	0	0	0	00	0	0	00	0	0
SLT	01	1	0	0	0	0	00	0	0	10	0	0
SLTI	00	1	1	0	0	0	10	0	0	11	0	0
J	00	0	0	0	0	0	00	0	0	00	1	0
JAL	10	0	0	0	0	0	01	0	0	00	1	0
JR	00	0	0	0	0	0	00	0	00	10	1	1

Test Bench Assembly:

PC	opcode	Opcode bitfields
0	ADD R1,R0,R0	00000000000000000000100000100000
4	SW R1, 2000(R0)	10101100000000010000011111010000
8	FOR SLTI R2,R1,10*4	00101000001000100000000000101000
12	BEQ R2,R0, END_FOR (PC +=6*4 + 4)	00010000010000000000000000000110
16	LW R3,1000(R1)	10001100001000110000001111101000
20	LW R4,2000(R0)	10001100000001000000011111010000
24	ADD R5,R4,R3	00000000011001000010100000100000
28	SW R5, 2000(R0)	10101100000001010000011111010000
32	ADDI R1,R1,4	00100000001000010000000000000100
36	J FOR (PC =4*2)	00001000000000000000000000000010
40	LW R6,2000(R0) END FOR	10001100000001100000011111010000