Computer Assignment 3 (PipeLine MIPS Processor)

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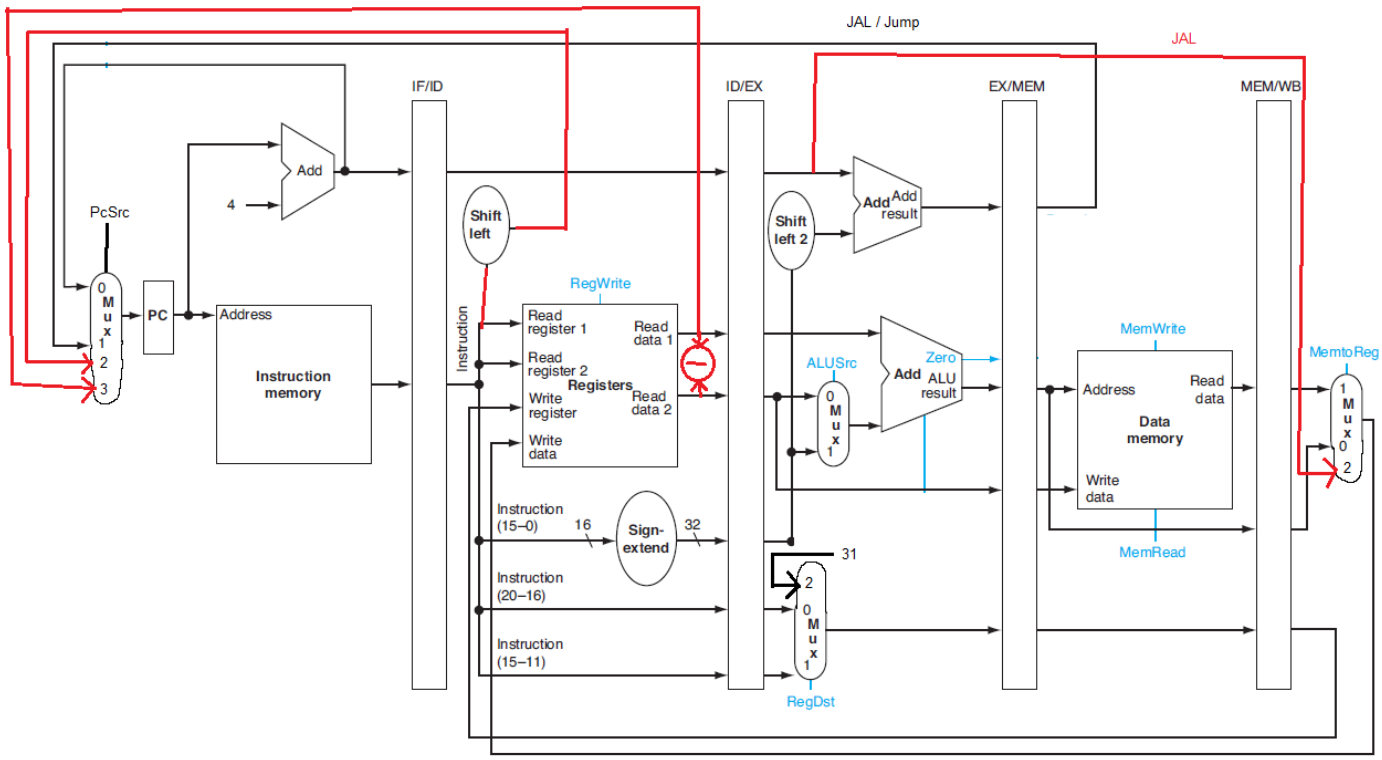
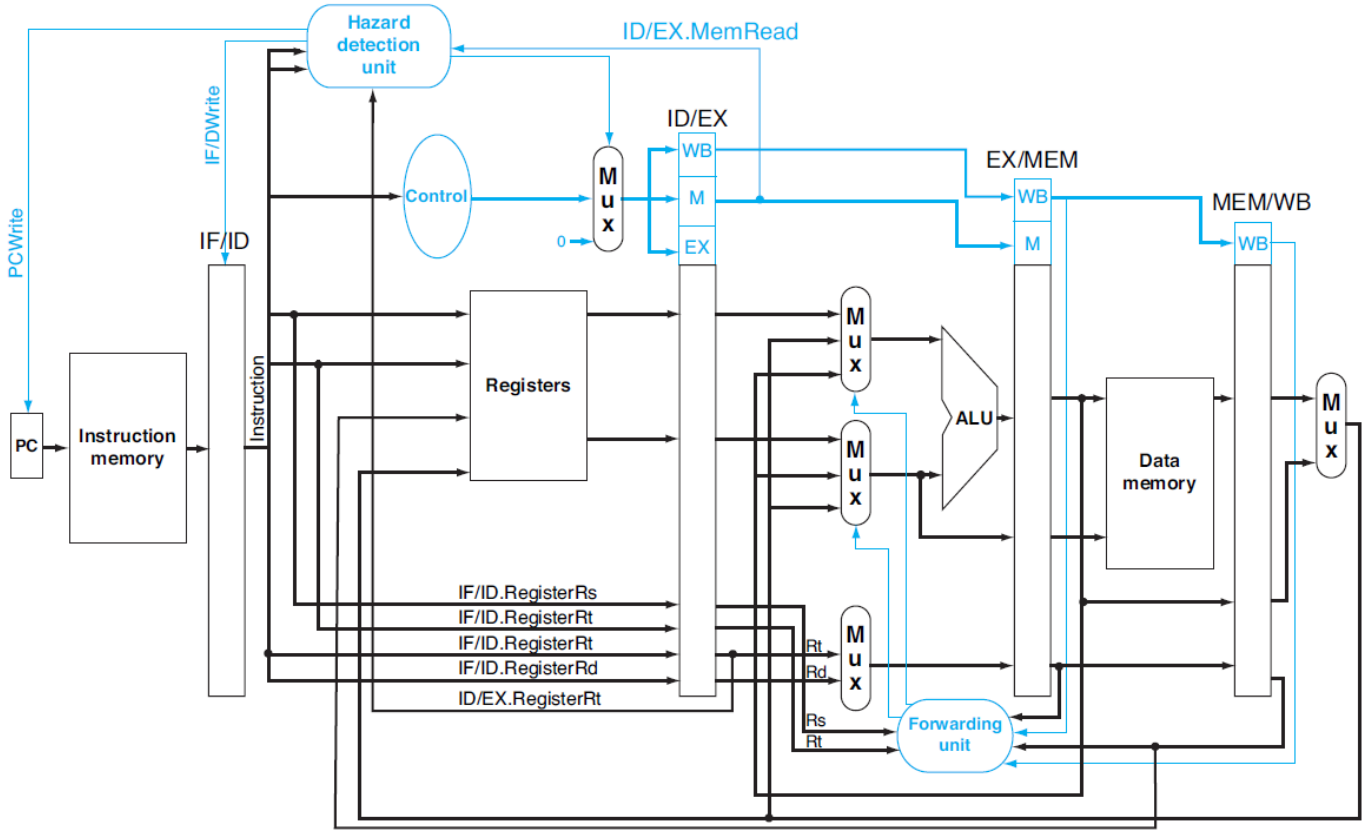
Data Path:



Datapath without forwarding unit and hazard detection unit



Datapath with Forwarding Unit and Hazard Detection Unit

Controller:

	ALUop	*ALUsrc*	*branch*	*flush*	*MemRead*	*MemWrite*	*MemtoReg*	*RegDst*	*RegWrite*	*PcSrc*
add	10	00	00	0	0	0	0	1	1	00
addi	00	01	00	0	0	0	0	0	1	00
sub	10	00	00	0	0	0	0	1	1	00
slt	10	00	00	0	0	0	0	1	1	00
slti	11	01	00	0	0	0	0	0	1	00
lw	00	01	00	0	1	0	1	0	1	00
sw	00	01	00	0	0	1	0	0	0	00
j	00	00	00	1	0	0	0	0	0	10
jal	00	00	00	0	0	0	1	1	0	10
jr	00	00	00	0	0	0	0	0	0	11
beq	01	00	01	1	0	0	0	0	0	01
bne	01	00	10	1	0	0	0	0	0	01

Test Bench:

PC	Opcode	Opcode Bitfields
0	Add R1,R0,R0	00000000000000000000100000100000
1	Addi R2,R0,10	00100000000000100000000000001010
2	Add R3,R0,R0	00000000000000000000110000100000
3	Add R4,R0,R0	00000000000000000010000000100000
4	NOP	00000000000000000000000000000000
5	NOP	00000000000000000000000000000000
6	FOR Beq R1,R2, END_FOR (PC += 6+1)	00010000001000100000000000000110
7	LW R5,1000(R3)	10001100011001010000001111101000
8	Add R4,R5,R4	00000000100001010010000000100000
9	Addi R3,R3,4	00100000011000110000000000000100
10	Addi R1,R1,1	00100000001000010000000000000001
11	NOP	00000000000000000000000000000000
12	J FOR (PC = 6)	00001000000000000000000000000110
13	SW R4,2000(R0) END_FOR	10101100000001000000011111010000