Experiment 1 - Clock and Periodic Signal Generation

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***Abstract*— In This report we explain about our activities for experiment 1 in DLD lab and it's related to clock generation.**

***Keywords*— LM555, Ring Oscillator, Schmitt Trigger Oscillator, Frequency Divider, T Flip-Flop.**

1. Clock Generation using ICs and Analog components.

1.1 Ring Oscillator

1. The circuit that we made:

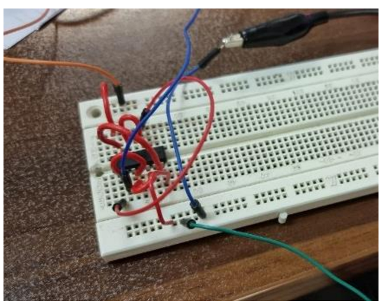

Fig. 1 Ring oscillator circuit

Result of circuit:

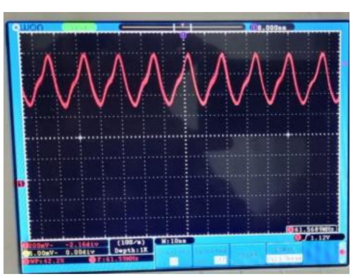

Fig. 2 Ring oscillator waveform

f = 61.59MHz => T_{delay} = 1/f = 16.23ns

2. N = 5

$T_{delay}=2N*T_{Inv}$ => 16.23=10*T_{Inv} => T_{Inv}=1.623ns

1.2 LM555 timer

1. The circuit:

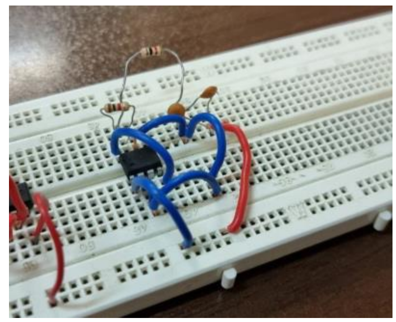

Fig. 3 LM555 circuit

Oscillator Result for R = 50KΩ :

Fig. 4 wave of 50KΩ circuit

f = 1.206 KHz , Duty Cycle = 49.3%

2. Oscillator Result for R_2 = 100KΩ:

Fig. 5 wave of 100KΩ circuit

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f = 618.8 Hz , Duty Cycle = 49.3%

calculation values:

$R_2 = 100K\Omega$
$T = 0.693(2R_2 + R_1)C \Rightarrow T = 1.393$ ms
$\Rightarrow f = 1/(1.393m) = 717.87$ Hz
Duty Cycle = (R2 + R1)/ (2R2 + R1)
=> Duty Cycle = 101/201 = 0.502 = 50.2 %

Oscillator Result for $R_2 = 10K\Omega$:

Fig. 6 wave of 10KΩ circuit

f = 5.806 KHz , Duty Cycle = 51.2%

calculation values:

$R_2 = 10K\Omega$
$T = 0.693(2R_2 + R_1)C \Rightarrow T = 145.53\mu s$
$\Rightarrow f = 1/(145.53\mu) = 6.871$ KHz
Duty Cycle = (R2 + R1)/ (2R2 + R1)
=> Duty Cycle = 11/21 = 0.523 = 52.3 %

Oscillator Result for $R_2 = 1K\Omega$:

Fig. 7 wave of 1KΩ circuit

f = 36.83 KHz , Duty Cycle = 62.9%

calculation values:

$R_2 = 1K\Omega$
$T = 0.693(2R_2 + R_1)C \Rightarrow T = 20.79\ \mu s$
$\Rightarrow f = 1/(20.79\mu) = 48.1$ KHz
Duty Cycle = (R2 + R1)/ (2R2 + R1)
=> Duty Cycle = 2/3 = 0.666 = 66.6 %

As we can see in calculations, our results are close to the clock signal we see on the output and the formula is a good approximate.

1.3 Schmitt Trigger Oscillator

1. The circuit:

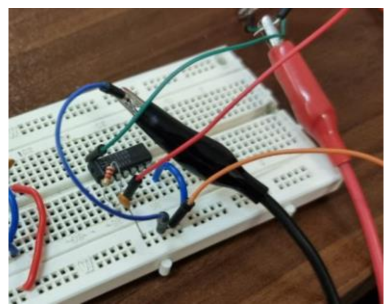

Fig. 8 Schmitt inverter oscillator circuit

R = 2200 Ω:

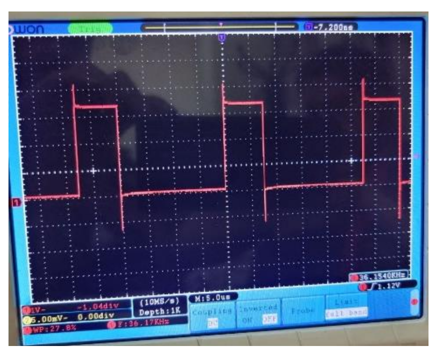

Fig. 9 wave of 2200Ω circuit

f = 36.17 KHz

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R = 470 Ω:

Fig. 10 wave of 470Ω circuit

f = 165.6 KHz

R = 1 KΩ:

Fig. 11 wave of 1000Ω circuit

f = 79.62 KHz

2. Finding α

f = α/RC , C = 10nF

R = 2200Ω => α = 0.79574

R = 470Ω => α = 0.77832

R = 1000Ω => α = 0.7962

As we can see results of calculating α parameter are close to each other and all of them are close to 0.79 .

1.4 Synchronous Counter as a Frequency Divider

1. We used part 1.1 circuit and generate a clock signal which you can see here

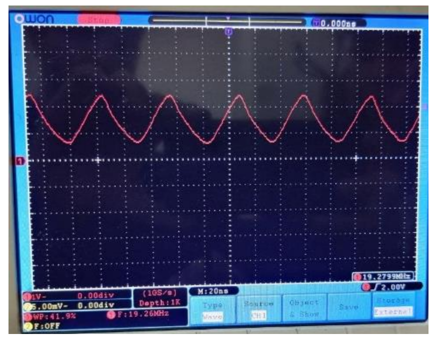

Fig. 12 clock signal from part 1

2. As you can see we closed the circuit, by using 74HC08 as a AND gate. According to the sheet and based on what value we want to divide (divide by 200) , we initialized 56 (256 – 200) With Vcc and Gnd .

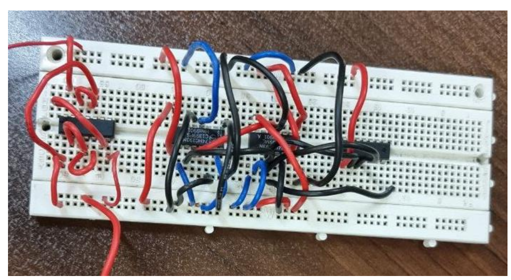

Fig. 13 Frequency divider circuit

3. We can see the result here

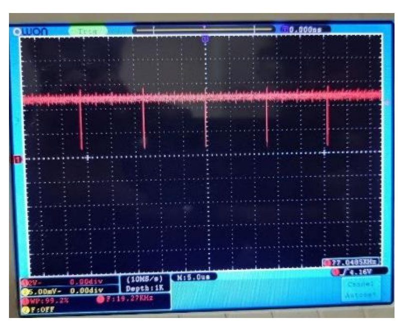

Fig. 14 output waveform

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F = 19.27 KHz

1.5 T Flip-Flop

Add a T Flip-Flop to circuit

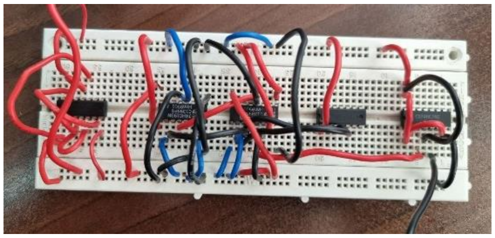

Fig. 15 T Flip-Flop circuit

Now we can see the result

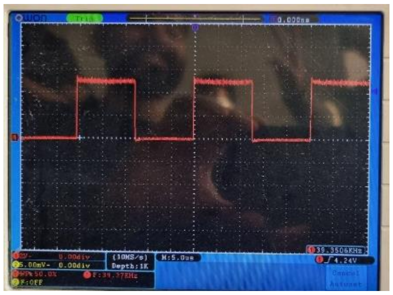

Fig. 16 T Flip-Flop waveform

As we can see 50% duty cycle has been produced after adding T Flip-Flop.