



ARQUITECTURA DE COMPUTADORES + Extensión vectorial

SET DE INSTRUCCIONES

Instrucción	Operación	Inst
add <dest>, <a>, </dest>	R[rd] = R[ra] + R[rb]	001000
sub <dest>,<a>,</dest>	R[rd] = R[ra] - R[rb]	000101
div <dest>,<a>,</dest>	R[rd] = R[ra]/R[rb]	010000
add <dest>,<a>,<imm></imm></dest>	R[rd] = R[rd] + Imm8	001000
sub <dest>,<a>,<imm></imm></dest>	R[rd] = R[rd] - Imm8	000101
div <dest>,<a>,<imm></imm></dest>	R[rd] = R[rd]/Imm8	010000
addv <dest>, <a>, </dest>	V[rd] = V[ra]+V[rb]	011000
subv <dest>, <a>, </dest>	V[rd] = V[ra]-V[rb]	010101
divv <dest>,<a>,</dest>	V[rd] = V[ra]/V[rb]	011000
mulv <dest>,<a>,</dest>	V[rd] = V[rd]*V[rb]	010000
str <dest>,<src>,<imm></imm></src></dest>	M[rd] = R[rs+off]	011001
<pre>ldr <dest>, <src>, <imm></imm></src></dest></pre>	R[rd] = M[rs+off]	110000
strv <dest>,<src>,<imm></imm></src></dest>	M[rd] = V[rs+off]	011001
<pre>ldrv <dest>, <src>, <imm></imm></src></dest></pre>	V[rd] = M[rs+off]	110000
bz <tag></tag>	pc = pc+4, pc = tag	10000X
bne <tag></tag>	pc = pc+4, pc = tag	10000X
bgt <tag></tag>	pc = pc+4, pc = tag	10000X
blt <tag></tag>	pc = pc+4, pc = tag	10000X
bge <tag></tag>	pc = pc+4, pc = tag	10000X
ble <tag></tag>	pc = pc+4, pc = tag	10000X

OPS

Op	Tipo de Instrucción
00	I=O -> Registro / I = 1 -> Inmediato [R/I]
01	L=0 -> Store/ L = 1 -> Load [M]
10	Condicional (B)

FORMATO DE INSTRUCCIONES

0	vect	vect: vector/escalar cond: Flag de condición
T	cond	op: ver tabla OPS*
3:2	ор	
9:4	fn	fn: I[4], P[5], U[6], B[7],W[8], L[9]
12:10	rα	Operación: [1] rd = ra ? rb [2] rd = ra ? imm
15:13	rd	[2] 10 - 14 : 111111
23:16	imm	imm: 8 bits de valor inmediato
26:24	rb	

REGISTROS ESCALARES

Registro	Número	Uso
r0	0	
r1	1	
r2	2	arqs
r3	3	91
r4	4	
r5	5	
r6	6	
r7	7	
рс	15	program counter

REGISTROS VECTORIALES

Registro	0:31	32:63	64:95	96:127	128:159	160:191	192:223	224:255
r0	32b	32b	32b	32b	32b	32b	32b	32b
r1	32b	32b	32b	32b	32b	32b	32b	32b
r2	32b	32b	32b	32b	32b	32b	32b	32b
r3	32b	32b	32b	32b	32b	32b	32b	32b
r4	32b	32b	32b	32b	32b	32b	32b	32b
r5	32b	32b	32b	32b	32b	32b	32b	32b
r6	32b	32b	32b	32b	32b	32b	32b	32b
r7	32b	32b	32b	32b	32b	32b	32b	32b