A Modular Multilevel Pulsating DC-Link Inverter for Electric Vehicle Drives with Increased Efficiency

Zhongxi Li[1], *Student Member, IEEE*, Aobo Yang[2], Gerry Chen[1], Zhiyong Zeng[1], *Member, IEEE*, Angel V. Peterchev[1], *Senior Member, IEEE*, and Stefan M. Goetz[1], *Member, IEEE*

[1] Duke University, Durham, NC, USA
[2] Tsinghua University, Beijing, P.R. China

Correspondence: Stefan Goetz
Duke University
200 Trent Dr., Durham, NC 27710, USA
Box 3620 DUMC
stefan.goetz@duke.edu
Tel: +1-919-613-0322
Fax: +1-919-681-8744

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ABSTRACT

This paper proposes a motor drive suitable for electric vehicles (EVs) with significantly reduced losses as compared to conventional solutions and with integrated battery balancing. Different from the conventional topology with hard-wired batteries, the proposed drive assembles the dc-link with cascaded half-bridges, each interfacing a battery. Such a modular multilevel backend grants arbitrary dc-link waveform, which is specifically shaped to shave off the overmodulation region of the frontend inverter—in this case a two-level three-phase inverter. As such, the frontend inverter only switches one phase leg at a time, eliminating 2/3 switching actions. The saved switching duty in the frontend inverter is committed by the modular multilevel backend, but with much less loss due to the fractionized switching voltage and the use of field-effect transistors (FETs). At high speeds, the proposed converter halves the total loss compared to a conventional setup; at lower speeds, the advantage is even more prominent because of the dynamically lowered dc-link voltage. Other benefits of the proposed motor drive include alleviated insulation stress for motor windings and direct battery balancing. The proposed motor drive is verified on a 2.7-kW downscaled setup with eight modules at the backend.

I. INTRODUCTION

Concerns about the environmental impact and future shortage of fossil fuels has spurred the popularization of electric vehicles (EVs), where two-level three-phase inverters dominate the motor drives because of their simplicity, compactness, and ruggedness [1]–[5]. There, all batteries are hard-wired to meet the desired current and voltage ratings. Despite the simplicity, such configuration encounters the following problems: First, the dc-link voltage is fixed, imposing maximum switching and insulation stresses regardless of the operating speeds [6]–[8]. Second, depending on the chemistry, the battery output voltage can vary significantly with respect to the SOC (state of charge). As such, the main inverter has to encounter the maximum dc-link voltage, leading to an oversized design [9], [10]. Finally, since there is no controllability over the individual batteries, costly and even lossy cell-balancing circuits are mandatory [10].

Many of the above problems can be solved by applying a variational dc-link voltage, e.g., regulating the dc-link voltage with respect to the speed. Such variational dc-link is typically achieved via a buck, boost, or buck-boost dc/dc stage between the battery pack and the three-phase inverter [6], [8], [10], [11]. At low speeds, the lowered dc-link voltage alleviates the switching loss in the inverter and notably improves the total efficiency; at higher operating speeds, however, the dc/dc stage is less beneficial to the frontend inverter while producing noticeable losses itself [7]. The dc/dc stage also requires large passive components which impedes efforts at weight reduction [12]–[14].

This paper presents a modular multilevel implementation of the dc-link for EV motor drives ("backend", see Fig. 1). The batteries are individually interfaced by cascaded half-bridges (CHB), whereas the outputs are produced by a two-level three-phase inverter ("frontend", see Fig. 1). The multilevel dc-link allows 1) flexible battery management without external circuits, 2) variational dc-link which inherits all advantages of the abovementioned two-stage motor drives, and 3) arbitrary pulsating waveform at the dc-link without large passive components. In particular, we produce a six-pulse rectified waveform at the dc-link to dynamically shape the modulation region and, consequently, to keep two phases in a fixed switching position. Equivalently, no zero-voltage vectors are required at any time. As such, the frontend inverter spares 2/3 switching actions compared to the conventional space-vector pulse-width modulation (SVPWM) or 1/2 compared to the discontinuous pulse-width modulation (DPWM) [14]–[16]. Of course, the spared switching duty is relegated to the multilevel backend, but the latter incurs much less switching loss due to the fractionized switching voltage and the use of field-effect transistors (FETs). In fact, SPICE simulations show significant loss reduction for all tested conditions compared to a conventional setup with fixed dc-link voltage. The advantage is most prominent at lower modulation indices (emulating low speeds and smaller back emf) or at lower power factors (matching field-weakening at high speeds). The saved loss mostly owes to the reduced switching loss of the insulated gate bipolar transistors (IGBTs) in the frontend inverter, which cannot easily benefit from more silicon in parallel; the reduced switching loss can be traded for better conduction loss in the IGBT selection. Furthermore, the output quality of the proposed converter remains good across all modulation ranges whereas SVPWM and DPWM with fixed dc-link voltage inevitably suffer higher distortion at lower modulation indices. The proposed topology is verified on a 2.7 kW setup with eight modules at the backend and a two-level three-phase IGBT module at the frontend.

A. Relation to Prior Work

Similar to the proposed solution, the star-configured CHB [17], [18] is also a great candidate to confer similar benefits including excellent output quality, very low dv/dt, and flexible management of the energy storage elements. However, in battery-based applications, the star-configured CHB loads the batteries with large second-order ripple current, which significantly limits its practicality [19]–[26]. In comparison, the proposed converter does not suffer second-order ripple currents due to trigonometric cancellation while retaining flexible battery management. Since the proposed topology only entails one unipolar module string, it uses 70% fewer transistors compared to the star-configured CHB at the same output voltage.

The concept of using the pulsating dc-link to reduce the switching loss was proposed in [15], which henceforth branched out to various implementations. In [15], [16], [27], a full-bridge circuit is inserted be-

tween the dc-link and the frontend inverter to adjust the dc-link waveform—the use of the full-bridge relegates the high-voltage switching to low-voltage parts. However, when used for battery-based applications, those topologies only offer a narrow dc-link voltage range, and the added semiconductor cannot offer additional controllability over the batteries. Topologies of [8], [14] use a buck or a boost stage and therefore much fewer components compared to the proposed multilevel backend; nevertheless, the transistors in the buck or boost stages [8], [14] must match the system's maximum voltage and current ratings, rendering it less beneficial—sometimes less efficient—to complement the frontend switching actions. Larger magnetic components are also mandatory in a buck or boost stage, imposing a trade-off between weight and efficiency.

This paper is organized as follows. Section II introduces the topology and the modulation principle for the frontend inverter. Section III discusses the modular multilevel backend. Section IV quantitatively compares the proposed solution with existing similar solutions. Section V presents experiment results.

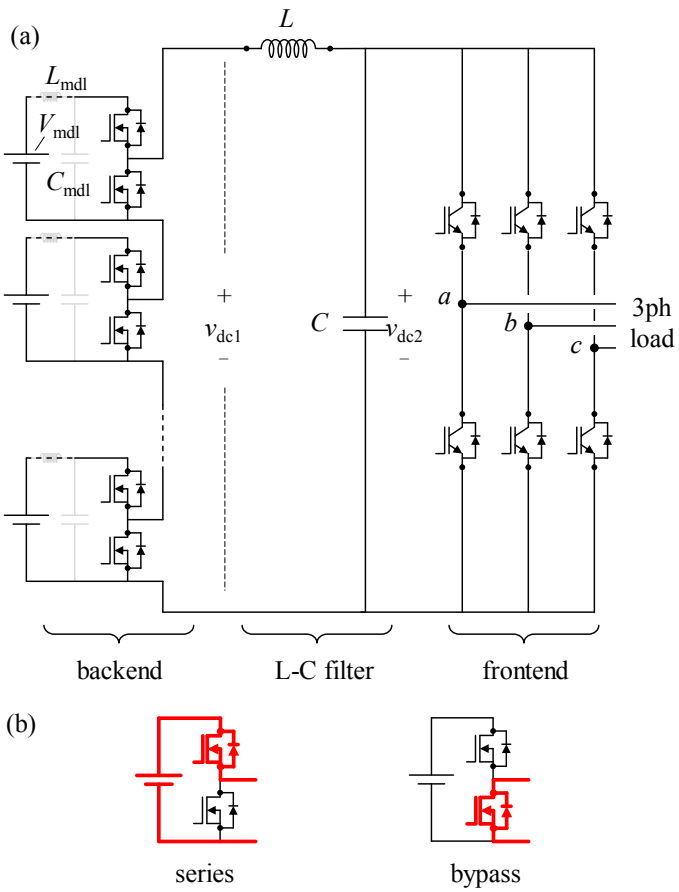

Fig. 1. (a) Proposed three-phase pulsating dc-link motor drive. A small L-C filter is implemented between dc-links v_{dc1} and v_{dc2}. Each module can incorporate an optional battery filter (L_{mdl} and C_{mdl}). (b) Switching states of the backend converter, where the battery filters are ignored.

II. Topology and Operating Principle

A. Topology

Fig. 1 shows the proposed three-phase motor drive. It contains a modular multilevel converter as the backend, a three-phase two-level inverter as the frontend, and a small L-C filter in between. The backend converter produces high-frequency variational voltage v_{dc1}, which is further filtered by the L-C filter to produce v_{dc2}. Voltage v_{dc2} serves as the dc-link voltage of the front-end inverter.

B. Operating Principle

Let us first ignore the backend and assume that v_{dc2} can be freely controlled. We set v_{dc2} as

$$\begin{aligned} v_{dc2} &= \max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\} \\ &= \max\{v_{ab}, v_{bc}, v_{ca}, -v_{ab}, -v_{bc}, -v_{ca}\} \end{aligned}, \quad (1)$$

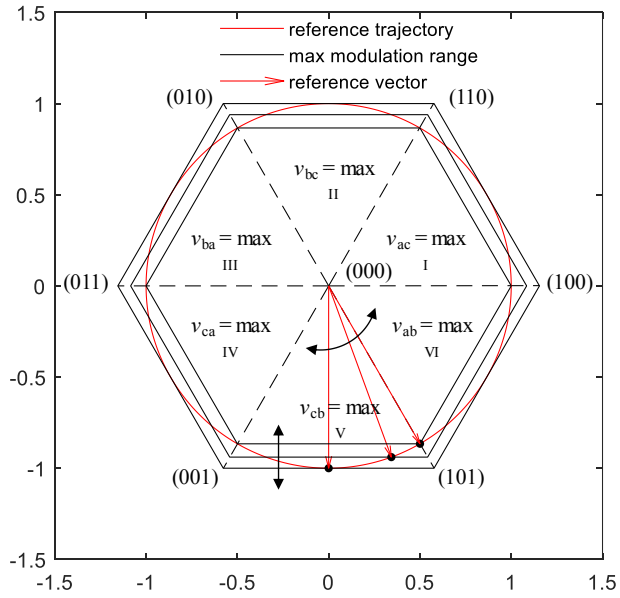

Fig. 2. Equivalent space-vector diagram. Black arrows indicate progression in time.

TABLE I
Activated sectors and modulation references

max line voltage	v_{ac}	v_{bc}	v_{ba}	v_{ca}	v_{cb}	v_{ab}
sector #	I	II	III	IV	V	VI
m_a	1	v_{ac}/v_{dc2}	0	0	v_{ab}/v_{dc2}	1
m_b	v_{bc}/v_{dc2}	1	1	v_{ba}/v_{dc2}	0	0
m_c	0	0	v_{ca}/v_{dc2}	1	1	v_{cb}/v_{dc2}

where v_a, v_b, v_c are reference phase voltages. Since at any time there is a line voltage magnitude equal to v_{dc2}, two inverter phases remain unswitched.

Such exploitation of the variational dc-link was presented in [15] with a simpler topology and subsequently studied [8], [14]–[16], [27], [28]. The reduction in the switching loss is clear when viewed in the space-vector diagram in Fig. 2. In Fig. 2, the circular reference trajectory is inferred from upper-level controls. The hexagon(s) reflect the dynamic modulation range v_{dc2} and therefore has a variating size. Equation (1) sets v_{dc2} in such a way that the hexagon always coincides with the momentary reference vector (Fig. 2) and effectively eliminating the overmodulation region. Therefore, the reference can be conveniently synthesized by the two adjacent active vectors without zero vectors [15], and only one phase leg switches at high frequency. Compared to the SVPWM scheme, the elimination of the zero vector spares 2/3 switching actions. Precise evaluation of the overall loss depends on the load angle, output current, as well as the loss of the backend converter, which are detailed in Section IV. In short, the overall loss is reduced because regulating v_{dc2} takes much less effort using the backend MOSFETs than switching the frontend IGBTs. In fact, for power factors larger than 0.5, the frontend IGBTs never switch at current apexes, reducing more than 2/3 of the switching loss.

Control of the frontend inverter requires 1) identifying the active sector; and 2) modulation between the two adjacent active vectors. The sector is identified by the momentarily largest line voltage, as is labeled in Fig. 2. For instance, v_{ab} = max activates Sector VI, whereas v_{ba} = max activates Sector III. The sector determines which half-bridge to modulate. The gate signal is obtained by comparing a reference with a unipolar triangle. TABLE I lists the modulation references according to the activated sectors, which are further unified below [15]:

$$m_x = \frac{v_x - \min\{v_a, v_b, v_c\}}{\max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\}}, x = a, b, c. \quad (2)$$

III. Modular Multilevel Backend Converter

Variational dc-link v_{dc2} can be achieved by various topologies. For instance, [15], [16] insert a low-voltage full-bridge module between a fixed dc-link and the frontend inverter. The efficiency of this topology benefits from the low-voltage switching at the full-bridge module, but v_{dc2} is limited to a narrow range. References [27], [28] also feature auxiliary converter stages to take over part of the hard switching from the main inverters. However, [27], [28] involve isolated transformers which entail a trade-off between the switching loss and weight. References [8], [14] implement a simple dc/dc stage to regulate v_{dc2}. Since the dc/dc converter performs hard switching at maximum dc-link voltage and rated current, the efficiency gain is at best marginal.

A. Modular Multilevel Backend Converter

Previous studies [8], [14]–[16], [27], [28] share the same idea of relegating the switching actions of the frontend inverter to a backend stage. Following the same idea, we use a modular multilevel split-battery converter as the backend dc-link (Fig. 1). The backend is implemented with a cascaded structure where each module is rated at a fraction of the total voltage and incorporates a battery unit. As such, high-current MOSFETs can be used. The backend's physical modularity is perfectly suited for this pulsating-dc-link EV drive mainly because of 1) flexible control over individual batteries and thus extended mileage [29]–[31] and 2) excellent output quality while causing negligible switching loss [32]–[36]. Importantly, we will show that the high-fidelity output allows a much smaller L-C filter and thus a rapid response.

Fig. 1(b) lists the switching states. The backend dc-link voltage v_{dc1} is determined by the number of series states,

$$v_{dc1} = n_{series} V_{mdl}, \quad (3)$$

where V_{mdl} is the battery voltage, n_{series} is the number of series states.

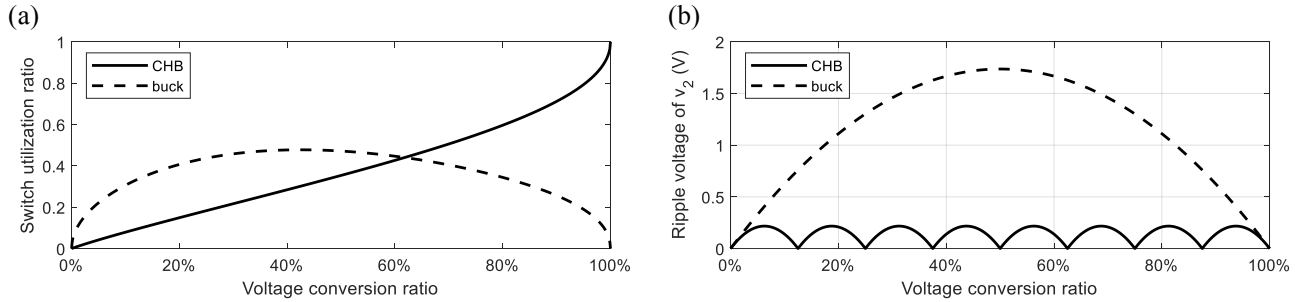

Fig. 3. (a) Switch utilization ratios (SUR). (b) Estimated ripple voltage of CHB- and buck-backend converters. L = 30 μH, C = 60 μF, N_{mdl} = 8, f_{s}(buck) = N_{mdl}, f_{s}(CHB) = 40 kHz, and V_{mdl} = 40 V. The influence of the frontend inverter is ignored.

B. Modulation

We use phase-shifted carrier (PSC) scheme to modulate the CHB backend. Specifically, the PSC scheme assigns a carrier C_k ($0 \le C_k \le 1$) to the kth module. The switching state is determined by

$$\begin{aligned} \mathrm{state}(k) &= \begin{cases} \text{series}, & \text{if } m_{\mathrm{dc}} \ge C_k, \\ \text{bypass}, & \text{if } m_{\mathrm{dc}} < C_k, \end{cases} \\ m_{\mathrm{dc}} &= \frac{\max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\}}{N_{\mathrm{mdl}} V_{\mathrm{mdl}}}, \end{aligned} \tag{4}$$

where N_{mdl} denotes the number of backend modules.

C. Balancing

For CHB-based split-battery in general, battery balancing can be achieved without additional hardware or losses by superimposing small dc values $\Delta m_{x,k}$ to the modulation indices [37], [38]. As long as $\Sigma\Delta m_{x,k} = 0$, there is no influence on the external load. The differential load for the kth module of phase x is

$$\Delta p_{x,k} = \Delta m_{x,k} V_{\mathrm{mdl}} i_x, \tag{5}$$

where i_x is the current of phase x.

IV. Analysis

This section compares the proposed motor drive with some similar alternatives. In terms of alternative two-stage pulsating dc-link inverters, we compare the proposed modular multilevel backend with a buck converter backend to show the superiority in both the switch utilization ratio (SUR) and the quality of the dc-link waveform. In terms of motor drives in general, we compare the proposed solution with the conventional single-stage two-level three-phase inverter to show the advantage in efficiency under various operating conditions.

TABLE II
Simulation settings

Shared parameters		
Output power	P	100 kW (100% modulation index)
Output current		200 Apk
Output frequency	f	50 Hz
Frontend inverter		IGBT: 300 A/1200 V (FF300R12ME4†, Infineon)
IGBT gate driver		+15 V /−5 V ideal, r_g = 1.8 Ω
Frontend switching frequency	f_{inv}	10 kHz (i.e., 3.3 kHz per switch)
Case 1: Proposed modular multilevel dc-link motor drive		
Backend modules		40 V × 16
DC-link voltage	v_{dc2}	0–640 V adjustable
Module switch		MOSFET: 0.75 mΩ, 300 A/60 V (IPT007N06N‡, Infineon)
Module switching frequency	f_{mdl}	5 kHz (i.e., 90 kHz at v_{dc1})
MOSFET gate driver		+15 V /−5 V ideal, r_g = 1.8 Ω
Frontend reference	m_x	Eq. (2)
Backend reference	m_{dc}	Eq.(4)
Cases 2 and 3: two-level three-phase inverter		
DC-link voltage	v_{dc}	640 V fixed

† Provided in PSpice default library.
‡ SPICE model available at www.infineon.com.

A. Switch Utilization Ratio

The CHB backend is essentially a multilevel step-down dc/dc converter. We compare its switch utilization ratio (SUR) with that of a buck converter according to [39]

$$\mathrm{SUR} = P_{\mathrm{load}} / S, \quad S = \Sigma V_j I_j, \qquad (6)$$

where S is the "total active switch stress", defined as the sum of the products of the peak voltage V_j and rms current I_j seen by each switch. The SURs are shown in Eq. (7). In the buck converter, we implement synchronous switching scheme to guarantee bidirectional power flow.

$$\begin{cases} (\mathrm{CHB})\ S = N_{\mathrm{mdl}} V_{\mathrm{mdl}} \left(\sqrt{m_{\mathrm{dc}}} + \sqrt{1 - m_{\mathrm{dc}}} \right) I_{\mathrm{dc}}, & \mathrm{SUR} = \dfrac{m_{\mathrm{dc}}}{\sqrt{m_{\mathrm{dc}}} + \sqrt{1 - m_{\mathrm{dc}}}}; \\ (\mathrm{buck})\ S = P_{\mathrm{load}} \left(\dfrac{m_{\mathrm{dc}}}{\sqrt{1 - m_{\mathrm{dc}}}} + \dfrac{1}{\sqrt{m_{\mathrm{dc}}}} \right), & \mathrm{SUR} = 1 \Big/ \left(\dfrac{m_{\mathrm{dc}}}{\sqrt{1 - m_{\mathrm{dc}}}} + \dfrac{1}{\sqrt{m_{\mathrm{dc}}}} \right). \end{cases} \qquad (7)$$

The results are visualized in Fig. 3 with various voltage conversion ratios m_{dc}. The CHB is advantageous in high modulation region, which corresponds to medium-to-high operating speeds of the motor.

B. Voltage Ripple Caused by the Backend Converter

The SURs reflect the conduction loss with the same semiconductor budget. Further comparisons should evaluate the quality of v_{dc2} under the same effective switching frequencies, which infers the size of the dc-link filter.

We assume $N_{mdl}V_{mdl}$ at the input of the buck converter, matching the maximum voltage of the CHB. With the same L-C filter, the two topologies produce the following voltage ripple at v_{dc2}:

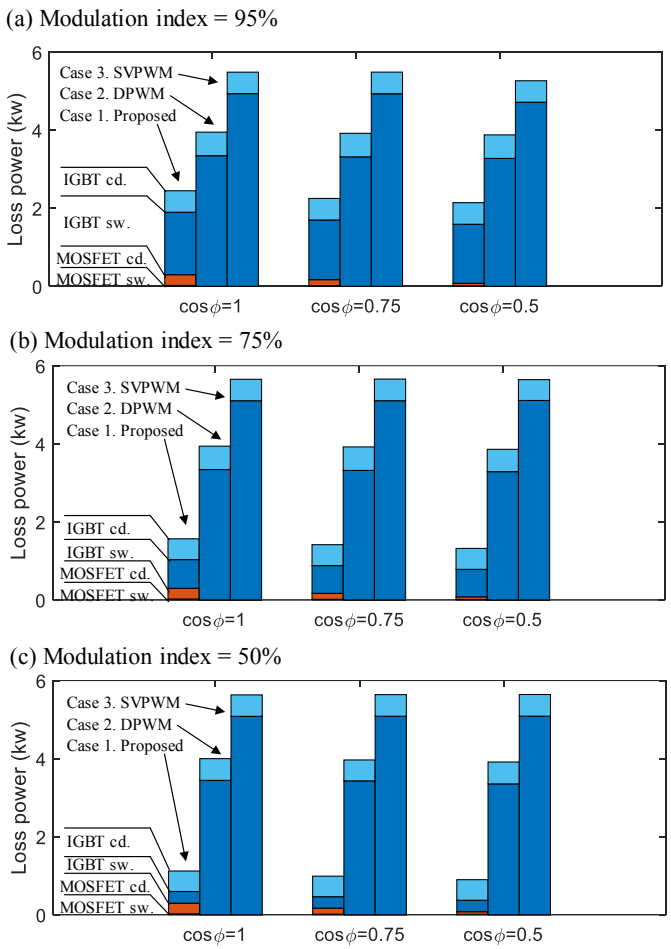

Fig. 4. Loss breakdown of three different cases under (a) 95% modulation index, (b) 75% modulation index, and (c) 50% modulation index. The switching loss of the MOSFETs is negligible and is barely visible in the bar plots.

$$\begin{cases} \Delta v_{\mathrm{dc}2}\left(\mathrm{CHB}\right)=\dfrac{V_{\mathrm{mdl}}\left(\left\lceil m_{\mathrm{dc}}N_{\mathrm{mdl}}\right\rceil-m_{\mathrm{dc}}N_{\mathrm{mdl}}\right)\left(m_{\mathrm{dc}}N_{\mathrm{mdl}}-\left\lfloor m_{\mathrm{dc}}N_{\mathrm{mdl}}\right\rfloor\right)}{16LCf_s^{\,2}N_{\mathrm{mdl}}^{\,2}}; \\ \Delta v_{\mathrm{dc}2}\left(\mathrm{buck}\right)=\dfrac{N_{\mathrm{mdl}}V_{\mathrm{mdl}}\left(1-m_{\mathrm{dc}}\right)m_{\mathrm{dc}}}{16LCf_s^{\,2}}. \end{cases} \tag{8}$$

The numerical results are shown in Fig. 3(b), with the parameters of TABLE II. The effective switching frequencies of both topologies are matched. The CHB produces much smaller voltage ripple because of the fractioned switching voltage. As such, the CHB can use a much smaller L-C filter and/or switching frequency than that of a buck backend.

C. Loss Comparison

We compare the losses across three cases through SPICE simulations: the proposed modulated dc-link, conventional inverter with SVPWM, and conventional inverter with discontinuous PWM (DPWM) [14]–[16]. In SVPWM, the transistors are always switching, whereas DPWM injects a special common-mode modulation reference, e.g.,

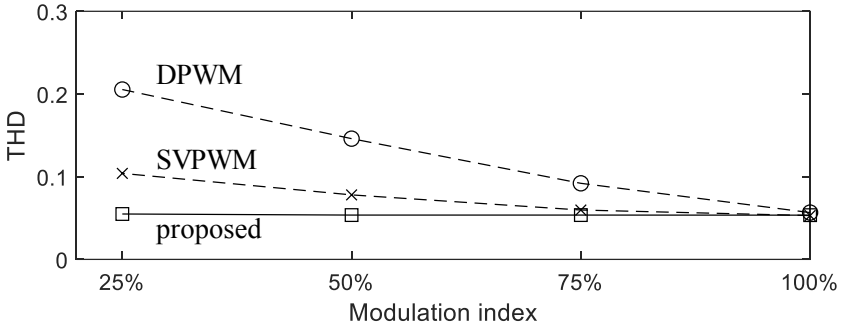

Fig. 5. THDs under series R-L passive load (1.75 Ω/200 μH). The modulation index refers to the utilization of the maximum dc-link voltage. See TABLE II for other settings. The carrier frequencies are identical across three cases.

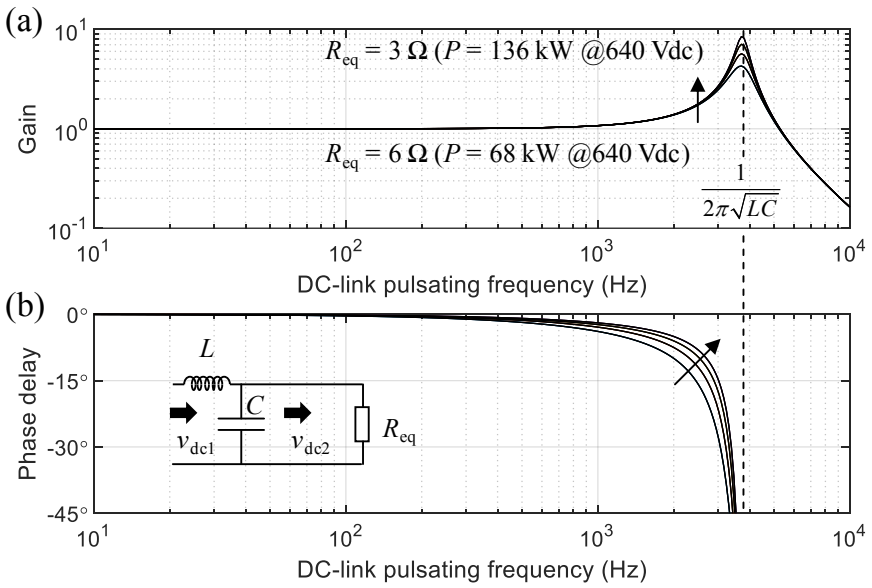

Fig. 6. Gain and phase shift across the L-C filter at the dc-link. The dc-link pulsating frequency is six times of the electrical output frequency.

$$m_{\underset{(\mathrm{DPWM})}{\mathrm{com}}} = \begin{cases} 1-\max\{m_a,m_b,m_c\}, & \text{if } \max\{m_a,m_b,m_c\} > -\min\{m_a,m_b,m_c\}; \\ \min\{m_a,m_b,m_c\}-1, & \text{if } \max\{m_a,m_b,m_c\} \le -\min\{m_a,m_b,m_c\}. \end{cases} \quad (9)$$

so that 1/3 switches remain untoggled. Even compared to DPWM, the proposed solution halves the switching actions. The detailed simulation settings are listed in TABLE II. In the conventional setup, the dc-link is fixed at 640 V and the main inverter is kept the same as that of the proposed solution (FF300R12ME4, Infineon). Across all cases, we fix the peak output current at 200 A but vary the modulation index and the power factor. Low modulation indices emulate smaller back emf under low speeds, whereas the combination of higher modulation indices and low power factors (cosφ) reflect field-weakening under high speeds.

Fig. 4 details the converter losses. Despite the additional loss in the MOSFETs, the proposed topology notably reduces the overall loss under all conditions thanks to the fewer switching actions in the frontend inverter. The relative ratio of the IGBT switching losses for the three evaluated cases is approximately

1:2:3 as predicted. The IGBTs' conduction losses are identical across all cases because of the controlled output current; whereas the MOSFET loss reduces at lower power factors due to the cancellation at the dc-link.

We select FF300R12ME4 (IGBT) and IPT007N06N (MOSFET) based on the availability of the simulation model and the matched cost. The relative benefit of the proposed solution depends on the choice of the frontend IGBT. There are several motor drive-specific features favoring the prosed solution: 1) at low speeds and thus smaller back emf, the frontend IGBTs of the proposed solution experience significantly less switching stress as is evidenced by Fig. 4; 2) at high speeds and thus lower power factor due to field-weakening, the currents mostly cancel upon the dc-link, producing small conduction loss at the MOSFETs; and 3) the MOSFET loss is dominated by the conduction loss, which can be reduced and easily scaled for higher current loads by paralleling more silicon, whereas the IGBT's switching loss does not decrease in the same manner.

We further set passive loads to evaluate the total harmonic distortion (THD) of the three configurations. For each phase R_{load} = 1.75 Ω, L_{load} = 200 μH. The results are shown in Fig. 5. The proposed converter remains a low THD (5.3%) across all modulation indices whereas both DPWM and SVPWM suffer higher distortions at lower modulation indices.

D. Design of the L-C Filter

The size of the batteries in the EV drive system entails nonnegligible stray inductances in the wiring (Fig. 7). As such, there must be a (small) dc-link capacitor placed near the frontend inverter to absorb the switching transients. An inductor L is consequently inserted to suppress the surge current, forming an L-C filter between v_{dc1} and v_{dc2}.

The L-C filter introduces phase lag and amplitude change into v_{dc2}. Fig. 6 quantifies these effects, where the frontend inverter is modeled by R_{eq}. At 136 kW and thus R_{eq} = 3 Ω, v_{dc2} is delayed by 3.9° and amplified by 7.6% when v_{dc1} pulsates at 1 kHz. Note that the dc-link pulsating frequency is six times of the intended sinusoidal output frequency.

Further increasing the pulsating frequency to 2 kHz, for example, matches 333.3 Hz inverter output but creates 140% amplitude gain and 10° delay in v_{dc2}. Reducing such distortions requires a smaller L × C and consequently a higher resonant frequency. However, the L-C resonant frequency should also be kept well below the switching frequency of the frontend inverter to avoid heavy oscillations. In summary, the L-C filter, frontend switching frequency, and the motor operating frequency must be matched in the design phase. Model-based feedforward control of v_{dc1} can also compensate the effect of the L-C filter, but it is out of the scope of this paper.

V. Experiment Results

A. Setup

We implement the backend converter with eight half-bridge modules. Each module contains several MOSFETs, a LiPo battery, and an L-C filter with L_{mdl} = 10 μH, C_{mdl} = 1.5 mF to smoothen the battery current. Between the backend and the frontend converters, we implemented a dc-link filter with L = 30 μH and C = 60 μF, which resonate at 3.75 kHz. To avoid resonating with the filter, the frontend inverter is modulated by a 10-kHz carrier. Under the proposed modulation scheme, each transistor switches at 3.33 kHz on average; whereas the backend modules switch at 5 kHz and thus effectively 40 kHz at v_{dc1}. Both the frontend and the backend converters are controlled by an FPGA (sbRIO 9627, National Instruments). The converter setup is detailed in TABLE III and shown in Fig. 7. All passive components and backend electronics exceed the batteries' current rating by several times, yet they have relatively negligible size and cost (see L, C, L_{mdl}, C_{mdl}, and the surface-mounted FETs atop the backend modules in Fig. 7).

B. Results

Induction motor. Fig. 8 shows the start-up process of an induction motor (TABLE IV). The line voltage and electric frequency respectively ramp up to 90 V(peak) and 10 Hz in one second. The waveform of v_{dc1} shows clear voltage stepping. The high-quality waveform of v_{dc1} justifies the use of the small L-C filters, which also grants fast response dynamics.

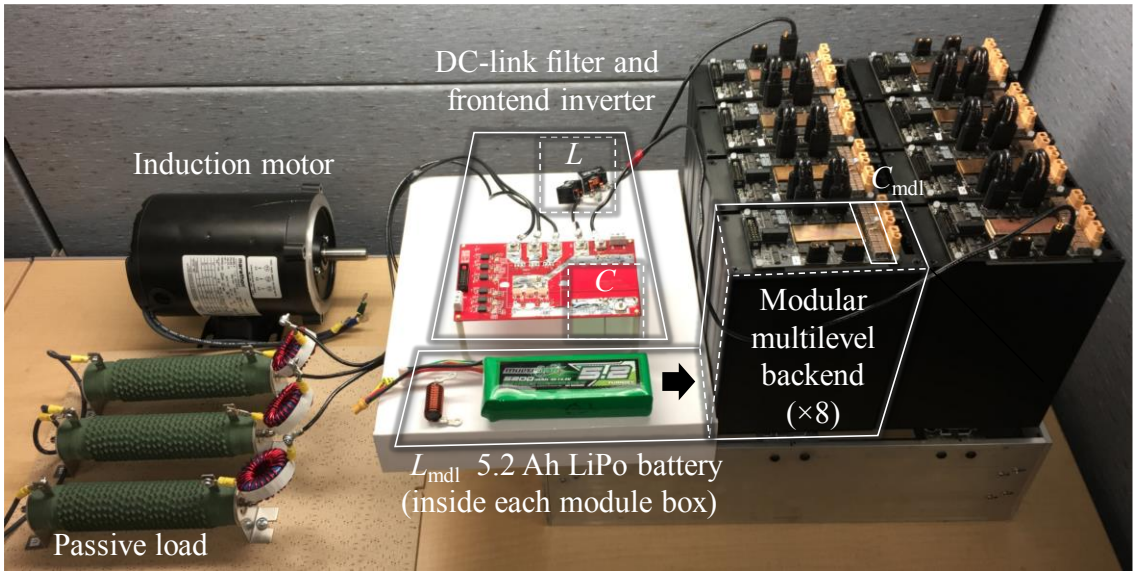

Fig. 7. Experiment setup. L = 30 μH, C = 60 μF, and L_{mdl} = 10 μH.

TABLE III
Setup specifications

Module inductor	L_{mdl}	10 μH (744711015, Wurth Electronics)
Module capacitor	C_{mdl}	1.5 mF/25 V
Module battery		Lithium Polymer (5.2 Ah, 16.4 V)
Module transistors		300 A/30 V (IPT004N03L, Infineon)
DC-link inductor	L	15 μH × 2 (7443641500, Wurth Electronics)
DC-link capacitor	C	30 μF × 2 (C4AQQBW5300A3MJ, KEMET)
Frontend IGBT		650 V/100 A (FS75R07W2E3, Infineon)
Backend carrier frequency	f_{mdl}	5 kHz (effectively 40 kHz at vdc1)
Frontend carrier frequency	f_{inv}	10 kHz (effectively 3.3 kHz per switch)

TABLE IV
Load specifications

Induction motor		
Nominal power	P_{motor}	250 W
Nominal voltage	V	230 V
Nominal speed	f_{motor}	1800 rpm
Passive load		
Total power	P_{load}	2.7 kW
Modulation index	m	0.95
Load resistance	R_{load}	2.2 Ω
Load inductance	L_{load}	100 μH
Load frequency	f_{load}	50 Hz

Passive load. Fig. 9 presents the measurements under 2.7-kW inductive load, where each phase is implemented with 2.2 Ω and 100 μH in series. The waveforms of v_{dc1} and v_{dc2} show a negligible phase lag. The dc-link current is relatively constant. Comparing the phase voltage v_a, phase current i_a, and modulation reference m_a, it is clear that 1) only a third of the frontend transistors are switching; and 2) the frontend transistors only switch at low currents. The same observations apply to other phases. As long as the power factor $\cos\varphi > 0.5$, the current peaks are shaped exclusively by the backend converter, which presents small switching ripples and distortion despite the low switching effort.

The above passive-load tests are operated at the modulation index of 95% (i.e., 95%×1.13 = 107% utilization of the dc-link voltage); meanwhile, the modulation references within the backend converter are intentionally modified to create an active balancing current between batteries #1 and #3 (bottom of Fig. 9). Only a mild differential current (~2%) is created due to the limited overhead room of the modulation index at 95%; however, the differential current is still sufficient for battery balancing in practice.

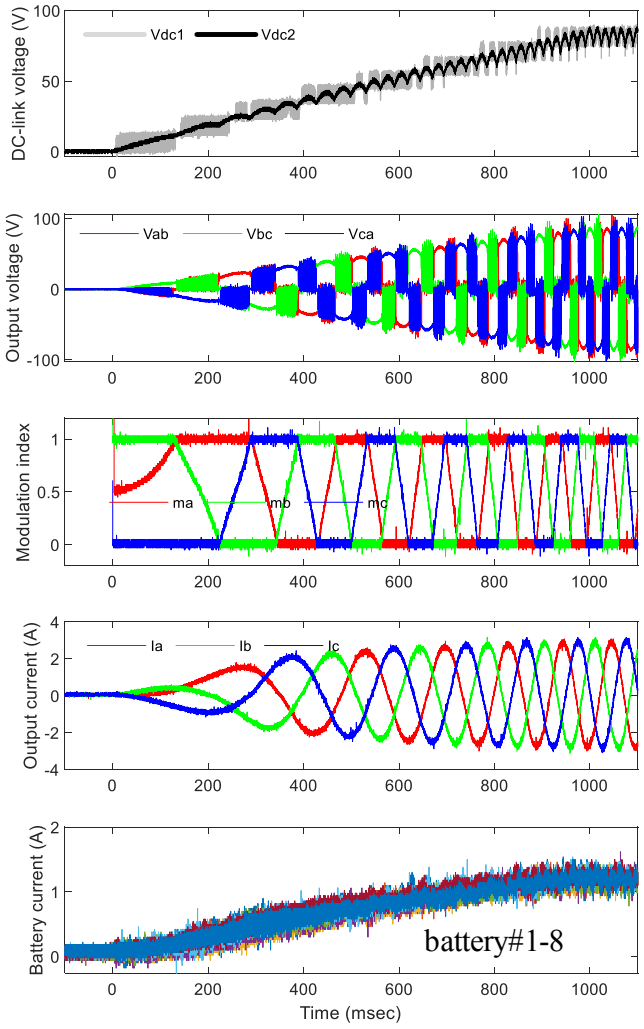

Fig. 8. Start-up process of an induction motor. The x-axis is in ms.

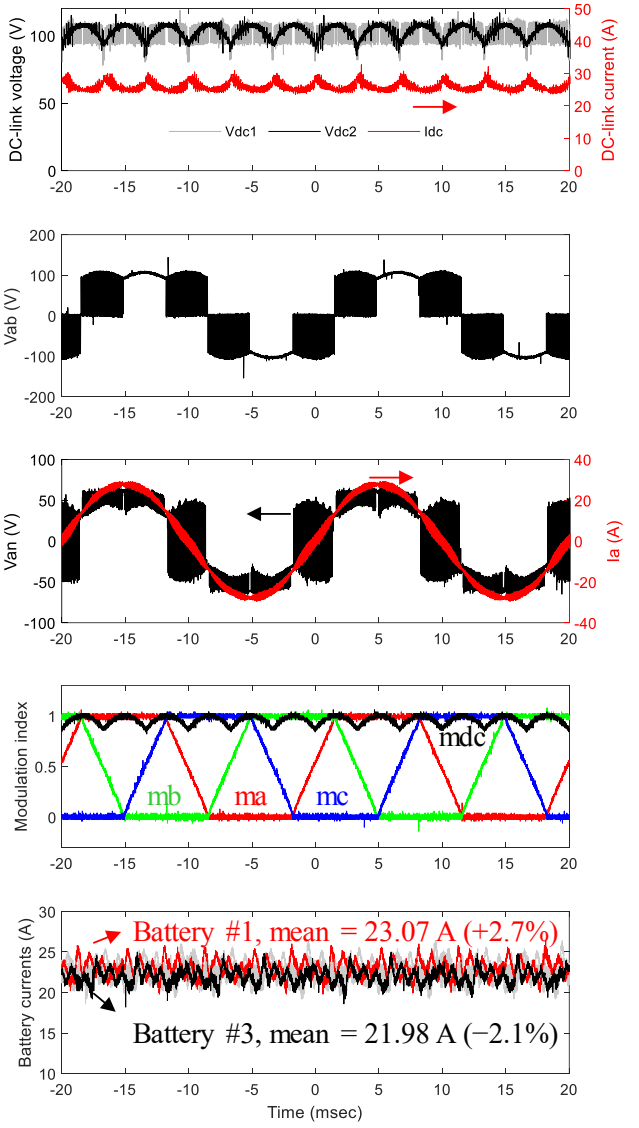

Fig. 9. Waveforms under 2.7 kW three-phase passive load. Balancing is active between battery #1 and #3. The x-axis is in ms.

VI. Conclusion

Variational dc-link voltage has great potential in reducing motor insulation stress and switching loss as well as increasing the output quality and round-trip efficiency. However, existing solutions have various disadvantages including limited operating range and marginal efficiency gain that barely justifies the additional transistors and passive components.

This paper proposes a split-battery modular multilevel converter to modulate the dc-link voltage. This modular backend allows the use of FETs and thus surrogates the hard switching of the main inverter at a negligible switching effort. Despite the additional loss in the FETs, the proposed solution notably reduces the overall loss under various modulation indices and power factors, which effectively emulate a wide

range of motor operating conditions. Additionally, the split-battery modular multilevel backend offers direct balancing control, sparing external balancing circuits of the conventional motor drives. The drawbacks, however, include additional cost and complexity at the backend, as well as the high-frequency current ripple in the batteries that demands small L-C filters. The advantages of the proposed solution are quantified by SPICE simulations and verified by experiments.

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