Floating Point Multiplier

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Floating point multiplier that supports single precision/double precision and custom precision floating point in binary format

1. Features

Fully pipelined architecture with adjustable latency

Single precision, double precision and custom non-standard precision

Compliant with IEEE754 binary format with the following exceptions:

- Subnormal numbers are not supported and will be rounded to be zero before calculation is carried out. Subnormal results are rounded to zero.
- Only round-to-neatest even is supported

2. Interface

Parameter	IO	Required	Description and *Default* value
pTechnology		Y	Possible values: ***"ALTERA"***
pFamily		Y	Possible values: ***"CYCLONE V"***
pPrecision		Y	Possible Values 0: Custom precision, widths of mantissa and exponent are defined by pWidthMan and pWidthExp ***1: Single Precision*** 2: Double Precision
pWidthExp		Y	Width of Exponent for custom Precision, do not assign if pPrecision = 1 or 2
pWidthMan		Y	Width of Mantissa for custom Precision, do not assign if pPrecision = 1 or 2
pPipeline		Y	Latency of the denormalizer multiplier Default = 5 Minimum Latency = 3

Name	Size	Required	Description
iv_InputA	I[S-1:0]	Y	Input A following IEEE754 binary format of single or double precision S = pWidthMan+pWidthExp+1
iv_InputB	I[S-1:0]	Y	Input B following IEEE754 binary format of single or double precision
i_Dv	I	Y	Data valid input
o3_InputID	O[2:0]	N	ID of the input, this is to track input and output values When i_Dv is asserted, a non-zero ID is returned in the same cycle at o4_InputID. When i_Dv is deasserted, o4_InputID = 0
o3_OutputID	O[2:0]	N	ID of the output, non-zero values indicate valid data
ov_Result	O[S-1:0]	Y	Floating point output Result
o_Overflow	O	N	Overflow flag
o_NAN	O	N	Not a number flag
o_Underflow	O	N	Underflow flag
o_PINF	O	N	Positive infinity
o_NINF	O	N	Negative Infinity
i_Clk	I	Y	Clock input
i_ClkEn	I	Y	Clock enable input, deassert this input to disable the whole engine
i_Arst	I	Y	Async active high reset

3. Performance

Table Area and Performance for Altera Devices

Device	Setting	Post-fit LEs/LUT LAB/ALUT	Register	DSP block	Post Fit Max Frequency (Restricted) in MHz
Cyclone III	Single Precision Latency =5 SpeedGradeC8	281/246	149	7 x 9-bit	208 (200)
Cyclone IV GX	Single Precision Latency = 5 SpeedGradeC8	280/246	149	7 x 9-bit	211 (200)
Cyclone V GX	Single Precision Latency = 5 SpeedGradeC8	153	154	1 x 27-bit	207
Arria II GX	Single Precision Latency = 3 SpeedGradeC6	170	85	4 x 18-bit	157
	Single Precision Latency = 5 SpeedGradeC8	157	119	4 x 18-bit	257 (220)
Cyclone III	Double Precision Latency =5 SpeedGradeC8	851/582	612	28 x 9-bit	123
Cyclone IV	Double Precision Latency = 5 SpeedGradeC8	381	368	28 x 9-bit	123
Cyclone V	Double Precision Latency=5 SpeedGrade C8	435	478	4 x 27 bit	186
Arria V	Double Precision Latency=5 SpeedGrade C4	435	506	4 x 27 bit	275[1]
Note	Quartus II 12.0sp2 Webpack Build 263 8/2/2012 (1) Quartus II 12.0sp2 SE Build 263 8/2/2012				

4. Verification

The core has been tested in real-time against output of Intel CPU with 10 millions random values. The snapshot below shows our verification method.

```
printf("Testing Multiplication operation with 10 million numbers\n");
for(T=0;T<10000000;T++)
{
    *(unsigned *)(&valA)=rand();
    *(unsigned *)(&valB)=rand();
    //Check The exponent part is not zero
    if(((*(unsigned*)&valA)&0x7F800000)==0) {T--;continue;}
    if(((*(unsigned*)&valB)&0x7F800000)==0) {T--;continue;}
    if(((*(unsigned*)&valA)&0x7F800000)==0x7F800000) {T--;continue;}
    if(((*(unsigned*)&valB)&0x7F800000)==0x7F800000) {T--;continue;}

    *(TYPE*)virt_addr=valA;
    *(TYPE*)(virt_addr+4)=valB;
    wait(200);
    ref=valA*valB;
    res=*(TYPE*)(virt_addr+12);
    stat=*(unsigned *)(virt_addr+16);
    if(ref!=res && stat==0)
        {
        printf("%1.10e *  %1.10e = %1.10e, %1.10e,%1.10e,\n",valA,valB,ref,res,(ref-res));
        printf("%08X %08X %08X %08X\n",*(unsigned*)&valA,*(unsigned*)&valB,*(unsigned*)&ref,*(unsigned*)&res);
        }
    if((T&0xFFFF)==0) {printf(".");fflush(0);}
}
```

5. Revision History

Date	Author	Core's Revision	Description
21/09/2012	Jeff Lieu	1.0	Initial Release Clock Enable has not been tested