40Gbps CRC32 256bit

1. OVERVIEW

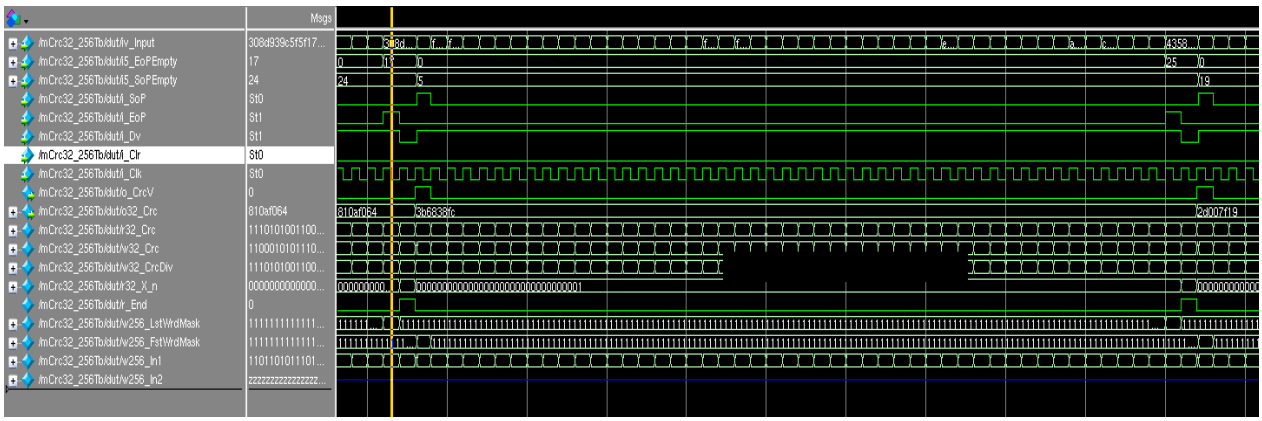
CRC23 is used widely in digital communication for packet validation. This core implements parallel CRC32 engine with 256-bit input data-path. This core can reach 40Gbps at 156.25MHz clock

2. INTERFACES

Port name	Description
i256_Din	Packet data input 256 bit wide, 32 byte
i5_SoPEmpty	Number of empty bytes in the start of packet line
i5_EoPEmpty	Number of empty bytes in the end of packet line
i_SoP	Start of Packet, should be 1 cycle long
i_EoP	End of Packet, should be 1 cycle long
i_Dv	Data valid
i_Clr	Synchronous clear to clear internal registers
i_Clk	Clock input, 156.25MHz to achieve 40Gbps throughput
o32_CRC	32bit CRC Output
o_CrcV	CRC valid flag

Clk		Bit 255 Byte 0		Bit0 Byte31
1	Start of Packet	Empty Bytes	Valid packet Data	
2	Packet Data	Valid packet Data		
	….	Valid packet Data		
n	End of Packet	Valid packet Data		Empty Bytes

3. PERFORMANCE



The engine requires an additional cycle after end of packet to compute the CRC value. The next packet should only start 1 cycle after end of previous packet.

Parameters	**ArriaVGXC5ES**		
Registers	199		
ALM	1380		
Max Speed Slow 1100mV 85ºC	176MHz		

4. VERIFICATION

The CRC results are verified against traditional serial method of CRC calculation for 1 million packets with random sizes.

The algorithm to generate referenced CRC is shown below

```
integer I;

function [31:0] mCrcCal;
        input [8*2000-1:0] iv_Data;

        reg [31:0] Poly;
        reg [31:0] Crc;
        reg Inbit;
        integer I;

        begin
                Poly = 32'h04C1_1DB7;
                Crc = 32'h0;
                for(I=8*2000-1;I>=-32;I=I-1)
                        begin
                                Inbit = (I>=0)?iv_Data[I]:1'b0;
                                Crc = (Crc[31]==1'b0)?{Crc[30:0],Inbit}:({Crc[30:0],Inbit}^Poly);
                        end
                mCrcCal = Crc;
        end
endfunction

mCrc32_256 dut(
```

5. REVISION HISTORY

Date	Author	Core's Revision	Description
30Mar13	JL	1.0	Initial Release