

# CSCI 463 Assignment 2 – Simple Microcode Machine

20 Points – Due Tuesday, October 15, 2019 at 23:59

## Abstract

In this assignment, you will use the machine simulator demonstrated in lecture to design, write and debug a microcode program that will store the eight ASCII letters: A B C D E F G H into the memory starting at address 0x80.

## 1 Input

The simulator reads two files:

1. Microcode expressed as one 16-bit binary value per line.
2. Up to 256 bytes expressed in hex that will be loaded into the system memory before the microcode starts executing.

Your microcode must generate and store the character data into the memory (in other words, you can not put the solution in your initial memory dump.)

Microcode for this machine matches that discussed in class and appearing on page four of the handout named “*cpu8c-schematic (microcode)*” whose microcode is described in “*microcode for cpu8c (version 2)*” reproduced, in part, below:

<i>alu_func[1:0]</i>	<i>alu_comp_b</i>	<i>alu_ci</i>	<i>reg_we</i>	<i>mbr_alu</i>	<i>mar_we</i>	<i>mem_we</i>	<i>mbr_out_we</i>	<i>mbr_in_we</i>	<i>reg_addr_we[1:0]</i>	<i>alu_reg_a[1:0]</i>	<i>alu_reg_b[1:0]</i>	operation	note
00	0	0	0	0	0	0	0	0	00	00	00	$alu\_q \leftarrow r0 + r0$	fully specified addition
00	0	0	0	0	0	0	0	0	dd	aa	bb	$alu\_q \leftarrow raa + rbb$	aa and bb are parameterized
00	0	0	0	0	0	0	0	0	xx	aa	bb	$alu\_q \leftarrow raa + rbb$	<i>reg_addr_we[1:0]</i> doesn't matter
01	0	0	0	0	0	0	0	0	xx	aa	bb	$alu\_q \leftarrow raa \oplus rbb$	XOR
10	0	0	0	0	0	0	0	0	xx	aa	bb	$alu\_q \leftarrow raa \wedge rbb$	AND

The headings in the above table match the columns and number of bits in each field of the microcode input file you must create.

As seen below, your microcode can have comments. Anything after the pound-sign '#' is ignored as are blank lines and lines that only have comments in them.

### An Example Microcode Input File

```
1 00 0 1 0 0 0 0 0 0 00 00 00 # alu_q = 1, reg_in = 1
2 00 0 1 0 0 0 0 0 0 11 00 00 # alu_q = 1, reg_in = 1, route reg_we to R3
3 00 0 1 1 0 0 0 0 0 11 00 00 # alu_q = 1, reg_in = 1, clock R3
4 00 0 1 0 0 0 0 0 0 11 00 00 # alu_q = 1, reg_in = 1, falling edge on R3 reg_we
```

Your initial memory dump MUST NOT have the ASCII result character values in it. If you do not need an initial memory image dump, you may omit the `prog2.dump` file from your solution.

A memory image dump file is formatted as a set of whitespace-separated hex byte values as many or as few per line as you prefer as shown below. The byte values will be placed into memory starting at address zero in the order appearing in your input file.

#### An Example 32-byte Memory Dump Input File

```
1 0F 1F 2F 3F 4F 5F 6F 7F 8F 9F AF BF CF DF EF FF
2 f0 f1 f2 f3 f4 f5 f6 f7 f8 f9 fa fb fc fd fe ff
3 01 02 03 04
4 05 06 07 08
5 09 0a 0b 0c
```

## 2 Output

The simulator will reset the CPU, load your input memory dump, print the initial memory contents then proceed to print your microcode instructions as they are executed and after the microcode instructions have all completed it will print the memory contents again.

Your program must complete with the proper values stored in memory. Any values in any memory location are acceptable **EXCEPT** that your program **MUST** leave the proper ASCII values in bytes 0x80-0x87 as shown here:

#### Example correct ASCII output

```
1 winans@hopper:~$ ~winans/csci463/a2/ucsim prog2.uc
2 0000: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
3 0010: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4 0020: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
5 0030: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
6 0040: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
7 0050: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
8 0060: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
9 0070: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
10 0080: 41 42 43 44 45 46 47 48 00 00 00 00 00 00 00 00 <--- this row counts!
11 0090: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
12 00A0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
13 00B0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
14 00C0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
15 00D0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
16 00E0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
17 00F0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

## 3 File You Must Write

You will create and submit two files for this assignment.

Create a directory named `prog2` and place your source files for this assignment within. Implement your solution for this assignment in two files named `prog2.uc` and `prog2.dump`.

When we grade your assignment, we will compile and run it on `hopper.cs.niu.edu` using one of these commands (depending on the presence of a `prog2.dump` file):

- `~winans/csci463/a2/ucsim prog2.uc`
- `~winans/csci463/a2/ucsim prog2.uc prog2.dump`

## 4 How To Hand In Your Program

When you are ready to turn in your assignment, make sure that the only files in your `prog2` directory are the `prog2.uc` and, optionally, `prog2.dump` files discussed above. Then, in the parent of your `prog2` directory, use the `mailprog.463` command to send the contents of the files in your `prog2` project directory to your TA like this:

```
mailprog.463 prog2
```

If `mailprog.463` detects and problems, it will inform you that you have not followed the instructions given above and provide some hints how to proceed. If you followed these instructions you will see the following:

```
winans@hopper:~/ $ mailprog.463 prog2
```

```
*****
* WARNING : Do NOT use this program to mail notes to your Instructor *
*           Doing so may result in the loss of your program !!       *
*****
```

```
Enter program number for your assignment : 2
shar: Saving /tmp/mailprog.11111 (text)
winans@hopper:~/ $
```

## 5 Grading

The grade you receive on this programming assignment will scored according to the syllabus and its ability to execute on the CSCI Department's computer.

It is your responsibility to test your program thoroughly.

## 6 Hints

- Add a `-v1` flag to the simulator to dump the state of the registers and signals withing the CPU after each microcode instruction. Note that the items printed with an asterisk `'*'` in first column are the fields provided by the microde instruction.
- Add a `-v2` flag to dump the entire memory as well as the signal and register states.

For example:

#### Example simulator run as seen in class

```

1 winans@hopper:~$ ~winans/csci463/a2/ucsim prog2.uc
2 Memory before execution begins:
3 0000: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4 0010: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
5 0020: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
6 0030: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
7 0040: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
8 0050: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
9 0060: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
10 0070: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
11 0080: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
12 0090: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
13 00A0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
14 00B0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
15 00C0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
16 00D0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
17 00E0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
18 00F0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
19
20 insn: 1000 '00 0 1 0 0 0 0 0 0 00 00 00 # alu_q = 1, reg_in = 1'
21 insn: 1030 '00 0 1 0 0 0 0 0 0 11 00 00 # alu_q = 1, reg_in = 1, route reg_we to R3'
22 insn: 1830 '00 0 1 1 0 0 0 0 0 11 00 00 # alu_q = 1, reg_in = 1, clock R3'
23 insn: 1030 '00 0 1 0 0 0 0 0 0 11 00 00 # alu_q = 1, reg_in = 1, falling edge on R3 reg_we'
24
25 Memory after execution ends:
26 0000: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
27 0010: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
28 0020: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
29 0030: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30 0040: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
31 0050: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
32 0060: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
33 0070: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
34 0080: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
35 0090: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
36 00A0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
37 00B0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
38 00C0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
39 00D0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
40 00E0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
41 00F0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

```

#### Example simulator run with v1 debugging enabled

```

1 winans@hopper:~$ ~winans/csci463/a2/ucsim -v1 prog2.uc
2
3 ...
4
5 insn: 1000 '00 0 1 0 0 0 0 0 0 00 00 00 # alu_q = 1, reg_in = 1'
6 *   alu_func = 0x0
7 *   alu_comp_b = 0x0
8 *   alu_ci = 0x1
9 *   reg_we = 0x0
10 *   mbr_alu = 0x0
11 *   mar_we = 0x0
12 *   mem_we = 0x0
13 *   mbr_out_we = 0x0
14 *   mbr_in_we = 0x0
15 *   reg_addr_we = 0x0
16 *   alu_reg_a = 0x0
17 *   alu_reg_b = 0x0
18 *   alu_so = 0x0
19 *   alu_uo = 0x0
20 *   alu_a = 0x00

```

```
21     alu_b = 0x00
22     alu_q = 0x01
23     reg_in = 0x01
24     mbr_in = 0x00
25     d_out = 0x00
26     d_in = 0x00
27     addr_out = 0x00
28     reg(0) = 0x00
29     reg(1) = 0x00
30     reg(2) = 0x00
31     reg(3) = 0x00
32
33 ...
```

### Example simulator run with v2 debugging enabled

```
1 winans@hopper:~$ ~winans/csci463/a2/ucsim -v2 prog2.uc
2
3 ...
4
5 insn: 1000 '00 0 1 0 0 0 0 0 0 00 00 00 # alu_q = 1, reg_in = 1'
6 *   alu_func = 0x0
7 *   alu_comp_b = 0x0
8 *   alu_ci = 0x1
9 *   reg_we = 0x0
10 *   mbr_alu = 0x0
11 *   mar_we = 0x0
12 *   mem_we = 0x0
13 *   mbr_out_we = 0x0
14 *   mbr_in_we = 0x0
15 *   reg_addr_we = 0x0
16 *   alu_reg_a = 0x0
17 *   alu_reg_b = 0x0
18     alu_so = 0x0
19     alu_uo = 0x0
20     alu_a = 0x00
21     alu_b = 0x00
22     alu_q = 0x01
23     reg_in = 0x01
24     mbr_in = 0x00
25     d_out = 0x00
26     d_in = 0x00
27     addr_out = 0x00
28     reg(0) = 0x00
29     reg(1) = 0x00
30     reg(2) = 0x00
31     reg(3) = 0x00
32 0000: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
33 0010: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
34 0020: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
35 0030: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
36 0040: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
37 0050: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
38 0060: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
39 0070: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
40 0080: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
41 0090: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
42 00A0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
43 00B0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
44 00C0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
45 00D0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
46 00E0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
47 00F0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
48
49 ...
```