

FPGA HYGRO Sensor Readings Tester, Version 1

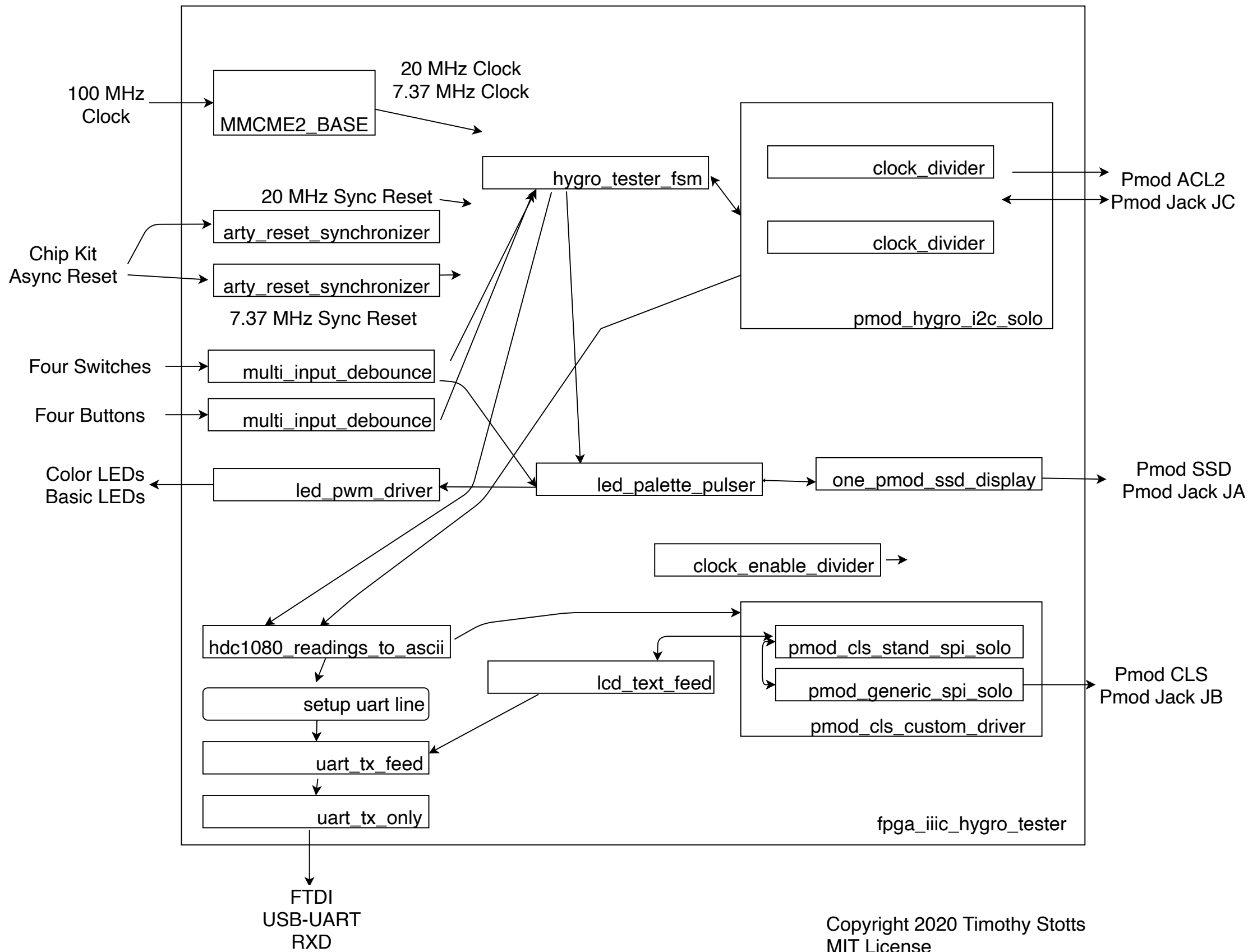
by Timothy Stotts

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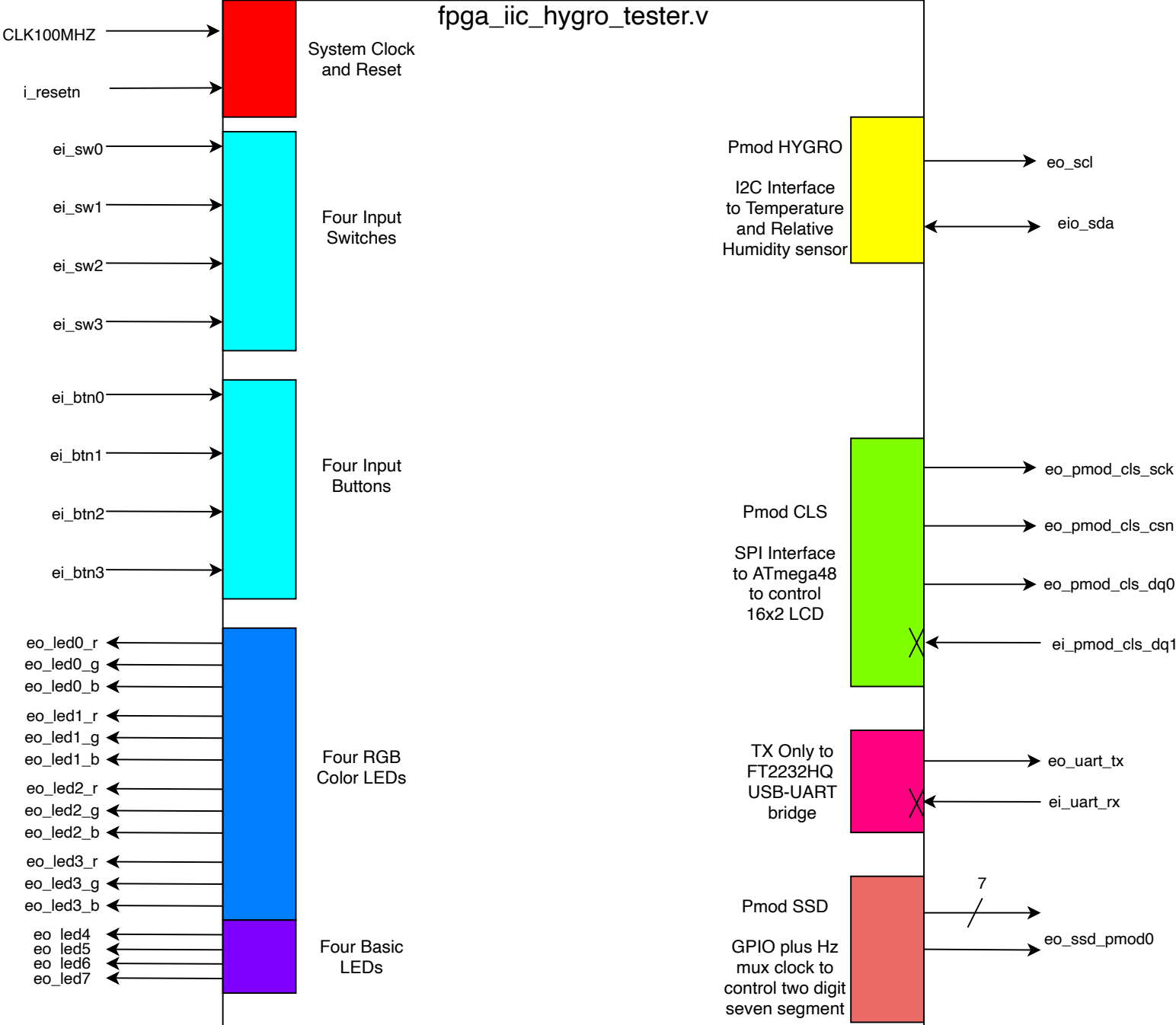
<https://github.com/timothystotts/fpga-iic-hygro-tester-1>

HYGRO-Tester-Design-Diagrams document revision 2A



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Block and Process Architecture of  
the fpga-iic-hygro-tester-1 design.



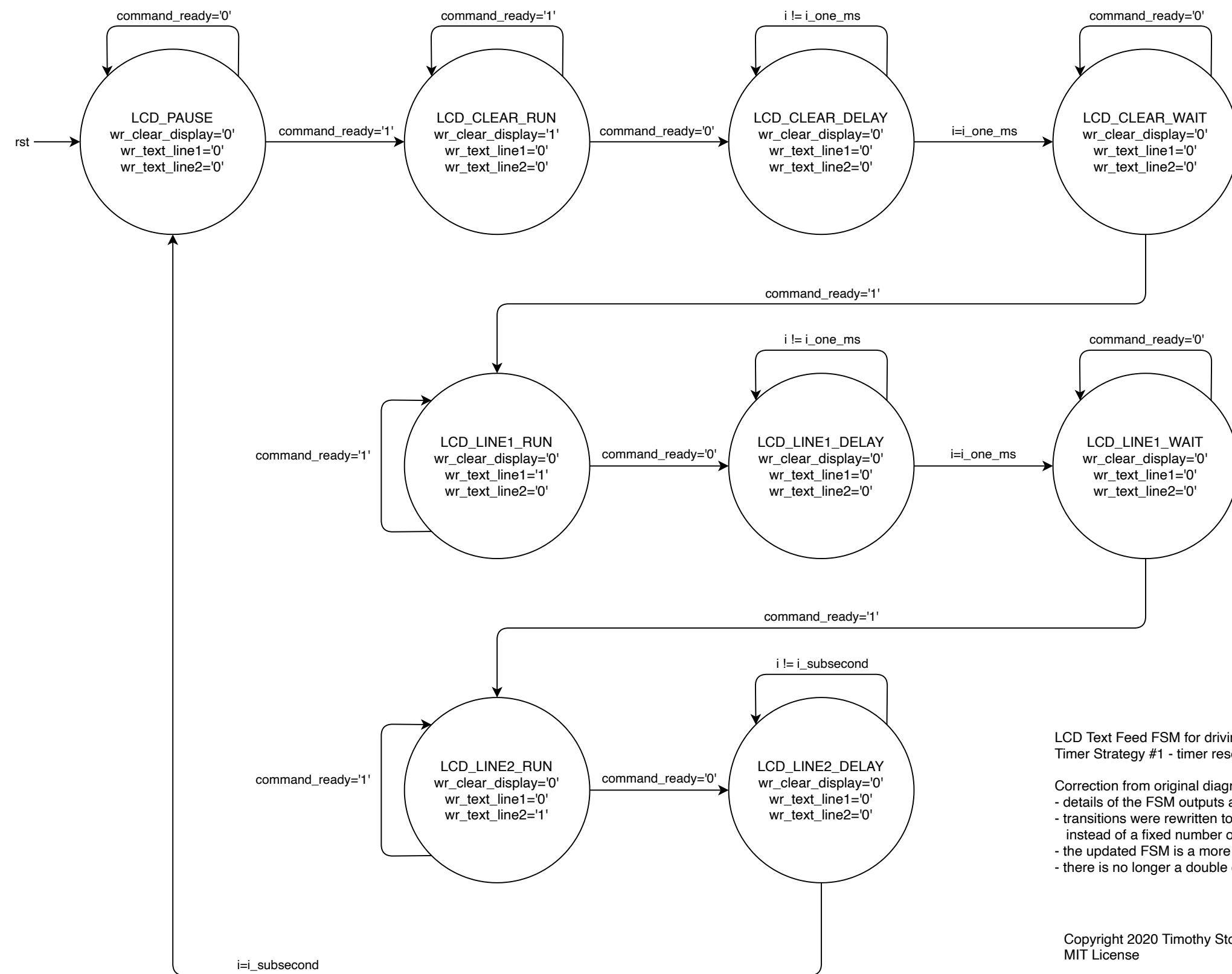
This top-level FPGA module operates the Pmod HYGRO to obtain sensor readings, converts these readings to ASCII data and text, and then outputs the ASCII data on the UART TX and the ASCII text on the Pmod CLS LCD. The switches select the one possible operational mode: Stream Measurements to Display. The driver for the Pmod HYGRO is hardcoded to configure the HDC1080 to stream both Temperature and Relative Humidity sensor readings in one bus read operation. The color LEDs LD0, LD1, LD2, LD3 display information as to whether the sensor is being operated, as well as which display format is being output to the LCD and Terminal.

The Pmod CLS is selected to operate with SPI output and no SPI input, even though the Pmod CLS additionally supports UART and I2C modes.

Switch 0 controls the program to run or stop running. Buttons 0, 1, 2, 3 are pressed to select one of five different display formats to be applied to the ASCII text lines displayed on the Pmod CLS LCD and the UART terminal.

HYGRO driver Ports diagram  
Placeholder

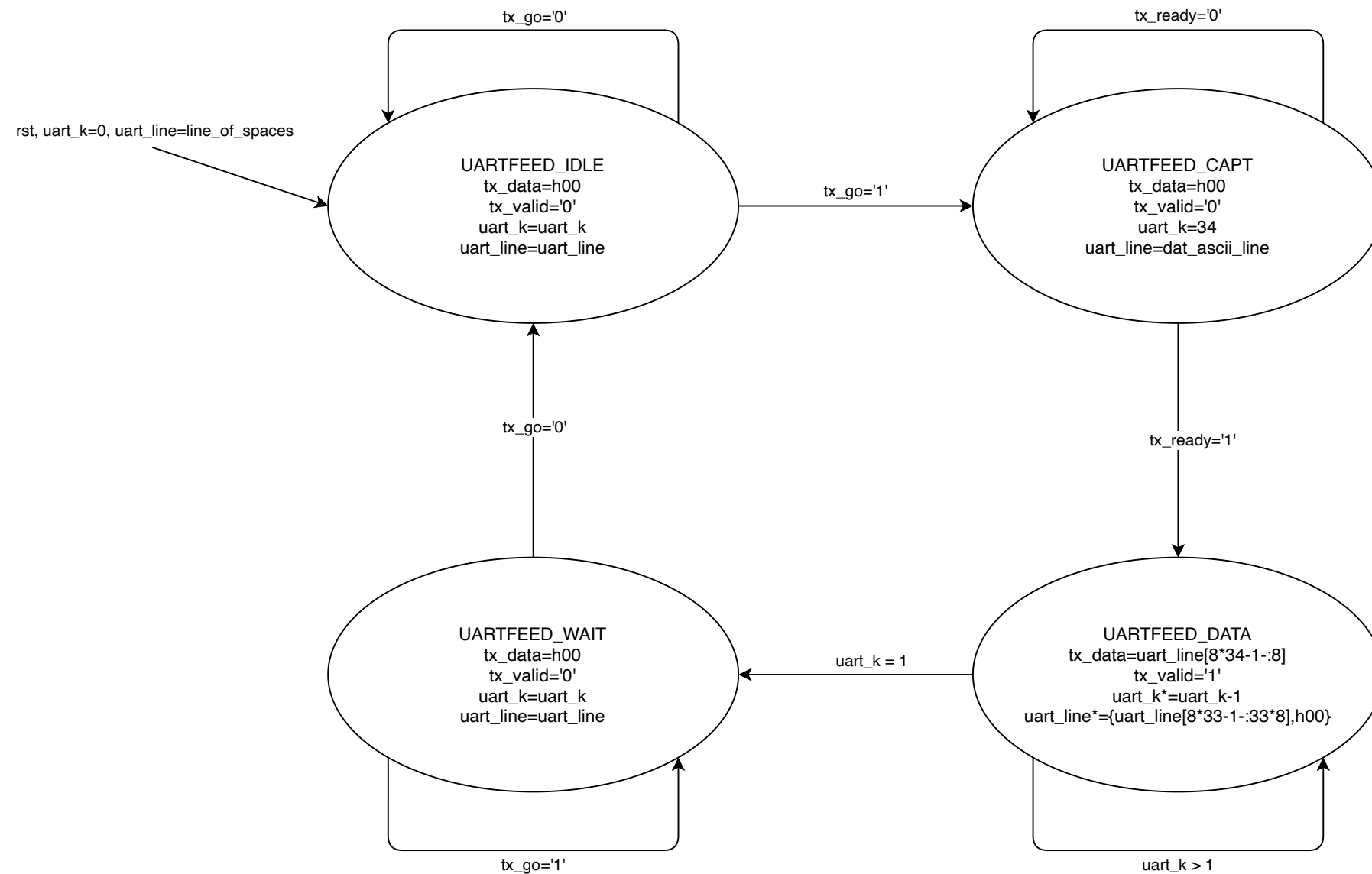
HYGRO driver FSM Diagram  
Placeholder



LCD Text Feed FSM for driving the commands of the custom Pmod CLS driver.  
Timer Strategy #1 - timer resets on state change and runs from zero to `i_subsecond`.

Correction from original diagram:  
 - details of the FSM outputs and timer "i"  
 - transitions were rewritten to hold commands according to `command_ready` handshake instead of a fixed number of clock cycles during a state  
 - the updated FSM is a more proper FSM diagram design  
 - there is no longer a double delay between the end of Line 2 and the start of Clear.

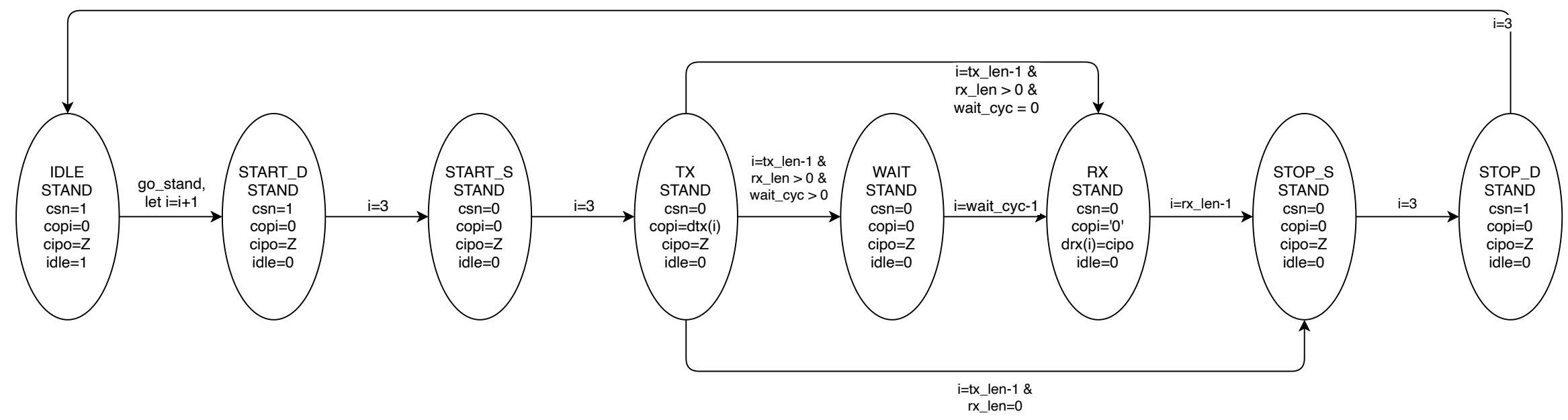
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# UART TX Feed FSM

This FSM feeds the TX FIFO of the `uart_tx_only` module. The data to feed to the TX FIFO is always a 34 8-bit character line of ASCII text. The `tx_go` input is triggered by the corresponding `wr_clear_display` pulse on the Pmod CLS custom driver, such that the UART TX Feed occurs when the LCD is starting to update on the FSM cycle of that driver.

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In each transition, tx\_len and rx\_len are to be multiplied by 8 from the FSM input signals, as it only makes sense to input into the FSM a byte count, while the FSM requires transitioning based upon a bit count.

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Generic SPI FSM, with only one SPI slave on the bus.

This diagram is incomplete and is shown as the first draft of designing the Standard SPI Single Slave Device driver.



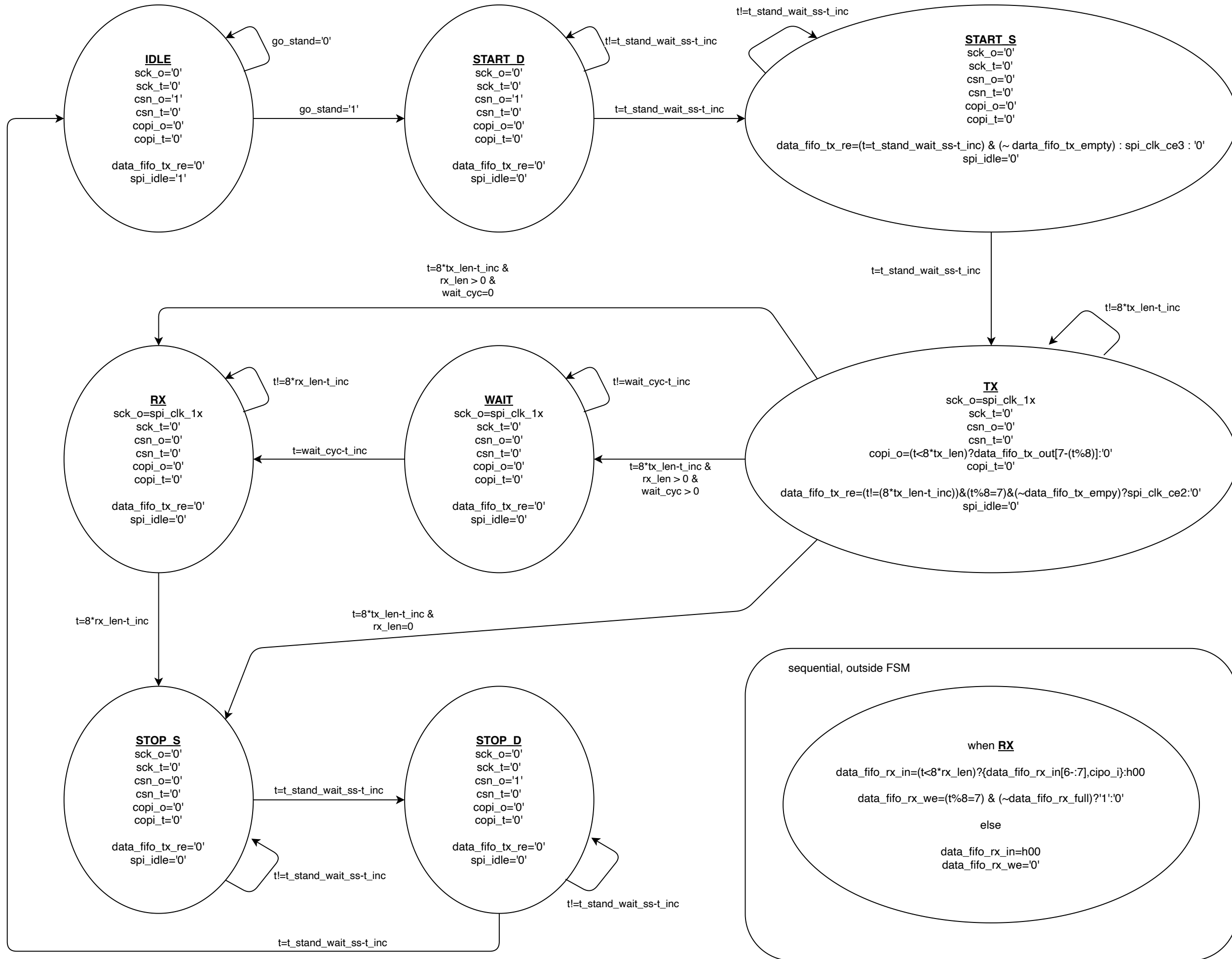












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Generic SPI FSM, with only one SPI  
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In each transition, tx\_len and rx\_len are  
to be multiplied by 8 from the FSM input  
signals, as it only makes sense to input  
into the FSM a byte count, while the  
FSM requires transitioning  
based upon a bit count.

The main FSM combinatorial operates  
all states, but processes data on in the  
TX state when TX data is written out the  
copi port.

A side sequential process processes  
data only on the RX state when RX data  
is read from the cipo input port.

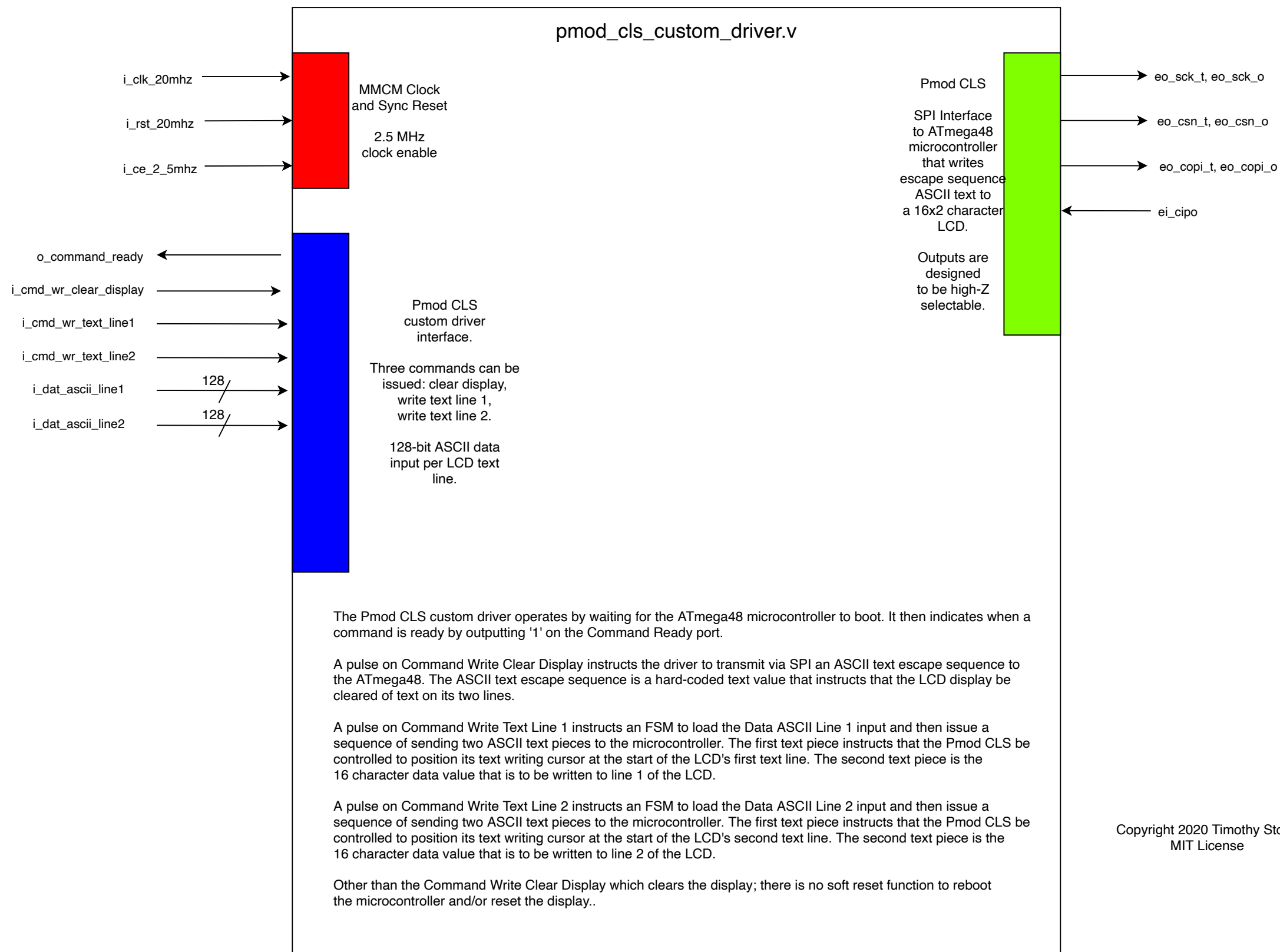
A general timer is used to time the SPI  
clock cycles (and thus bits). The timer  
is reset to zero at the transition from  
a state to a different state.

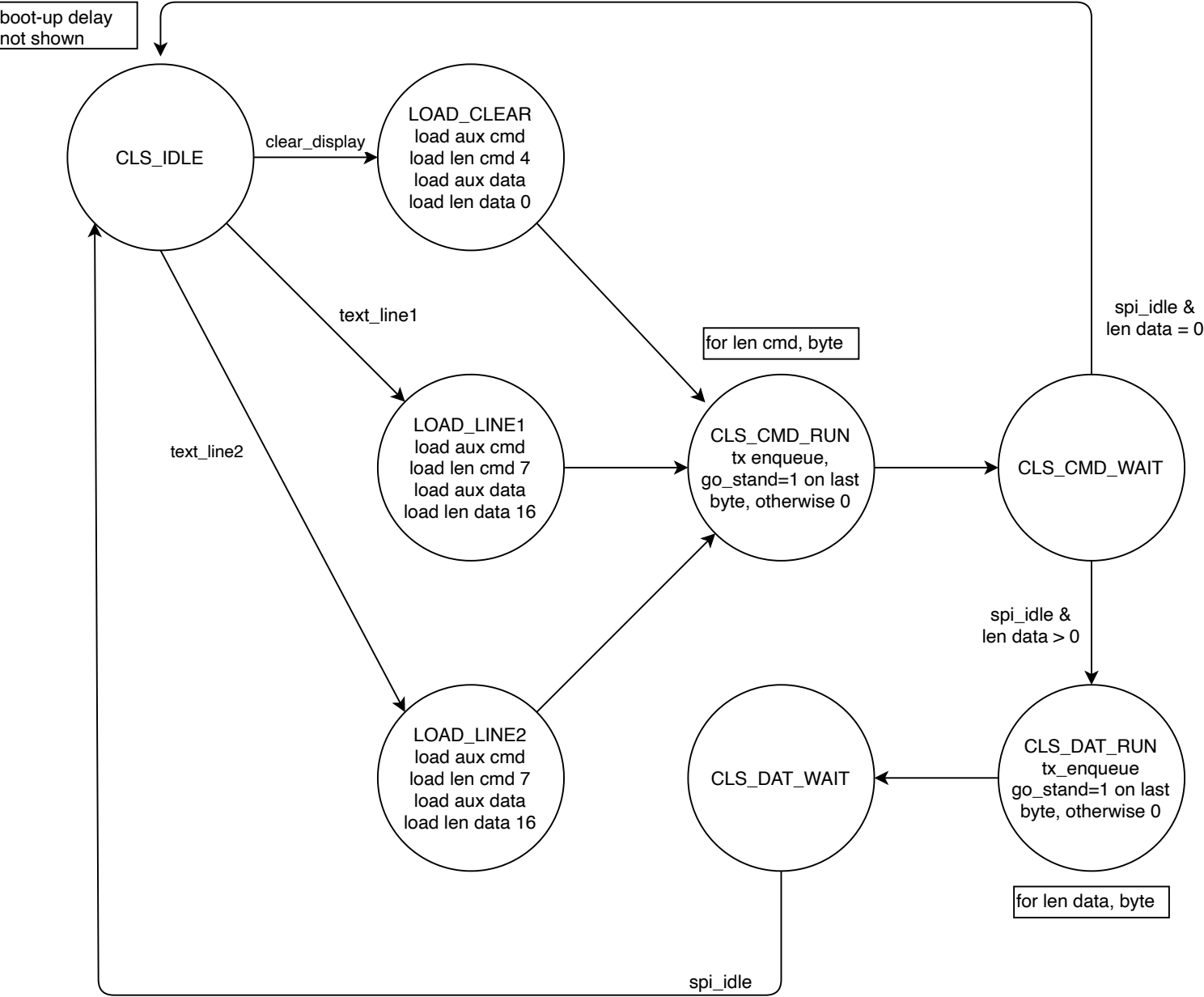
This machine could be considered a  
hybrid Moore and Mealy machine.  
The outputs during a state can  
change based upon timer and FIFO  
control inputs; but the diagram is  
drawn as a Moore machine.

The TX state controls reading byte  
by byte from a TX fifo and write its  
bits to COPI until the timer has  
reached 8\*tx\_len cycles.

The RX standalone sequential  
controls reading a byte bit by bit  
from CIPO and then writing the  
full byte to a RX fifo when the  
full byte has been received.  
The main FSM still controls when  
the FSM is in the **RX** state or has  
transitioned to **STOP S** state.

Note that clock enables such as  
spi\_clk\_ce2 are omitted from most  
of the diagram, but are still required  
for proper function of the design to  
write data on the falling edge of the  
SPI clock output and read data on  
the rising edge of the SPI clock  
output. Refer to the source code.





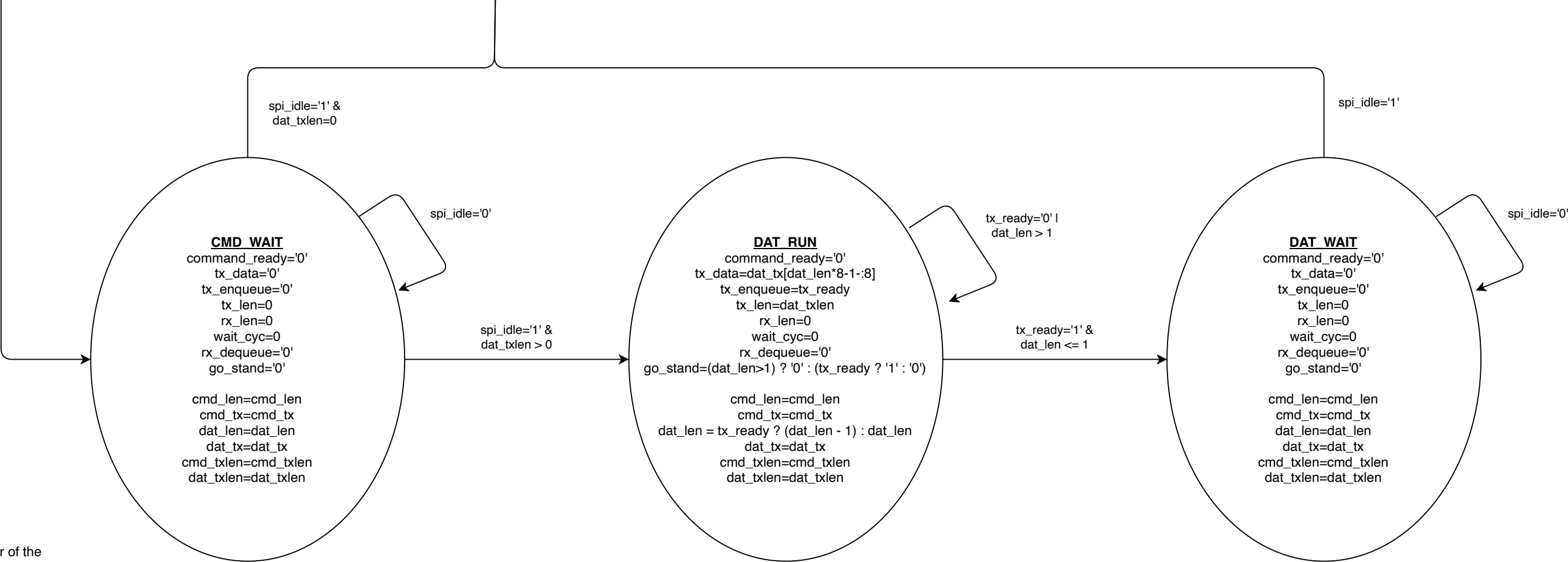
A FSM to operate the Digilent Inc. PMOD CLS LCD display communication via the single slave SPI-machine FSM of this document.

This diagram is incomplete and does not show boot-time delay. Also, some state-bypass preventions and iterations may not be shown. This is the first design draft, and the complete FSM diagram is shown on another page.

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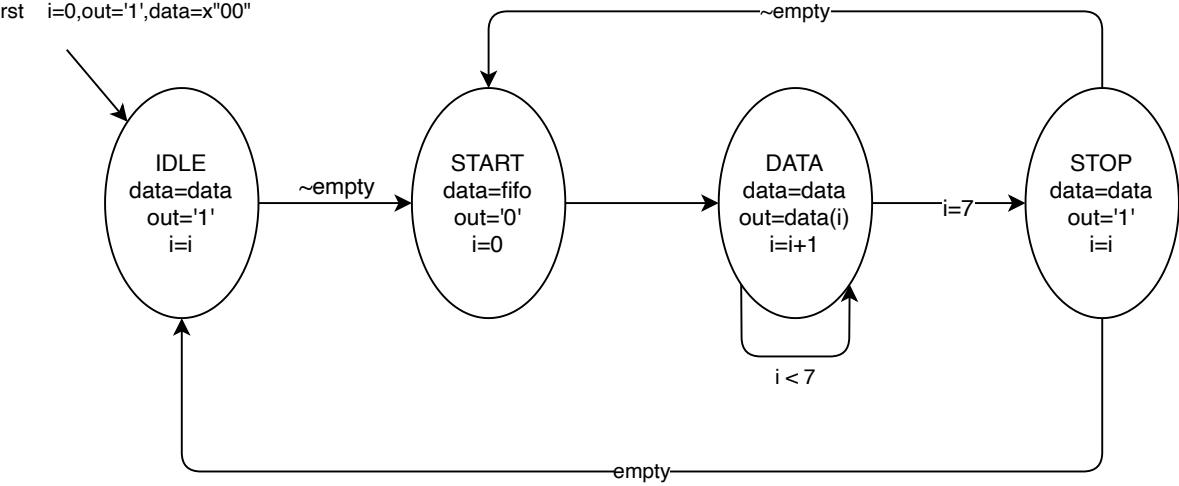




CLS Stand SPI Driver of the CLS Custom Driver. The FSM works by waiting for a command to (a) write a clear display command to the CLS, (b) write a 16-character line to the first line of the CLS, or (c) write a 16-character line to the second line of the CLS. The clear display command only writes an ANSI escape sequence with no textual data after it. The write line 1 and write line 2 commands write an ANSI escape sequence to position the cursor at the beginning of one of the two lines, and then 16 characters of text. The CLS microcontroller processes each command and line data. The clear display clears the 16x2 LCD; and the write line writes new text to the specified line of the 16x2 LCD.

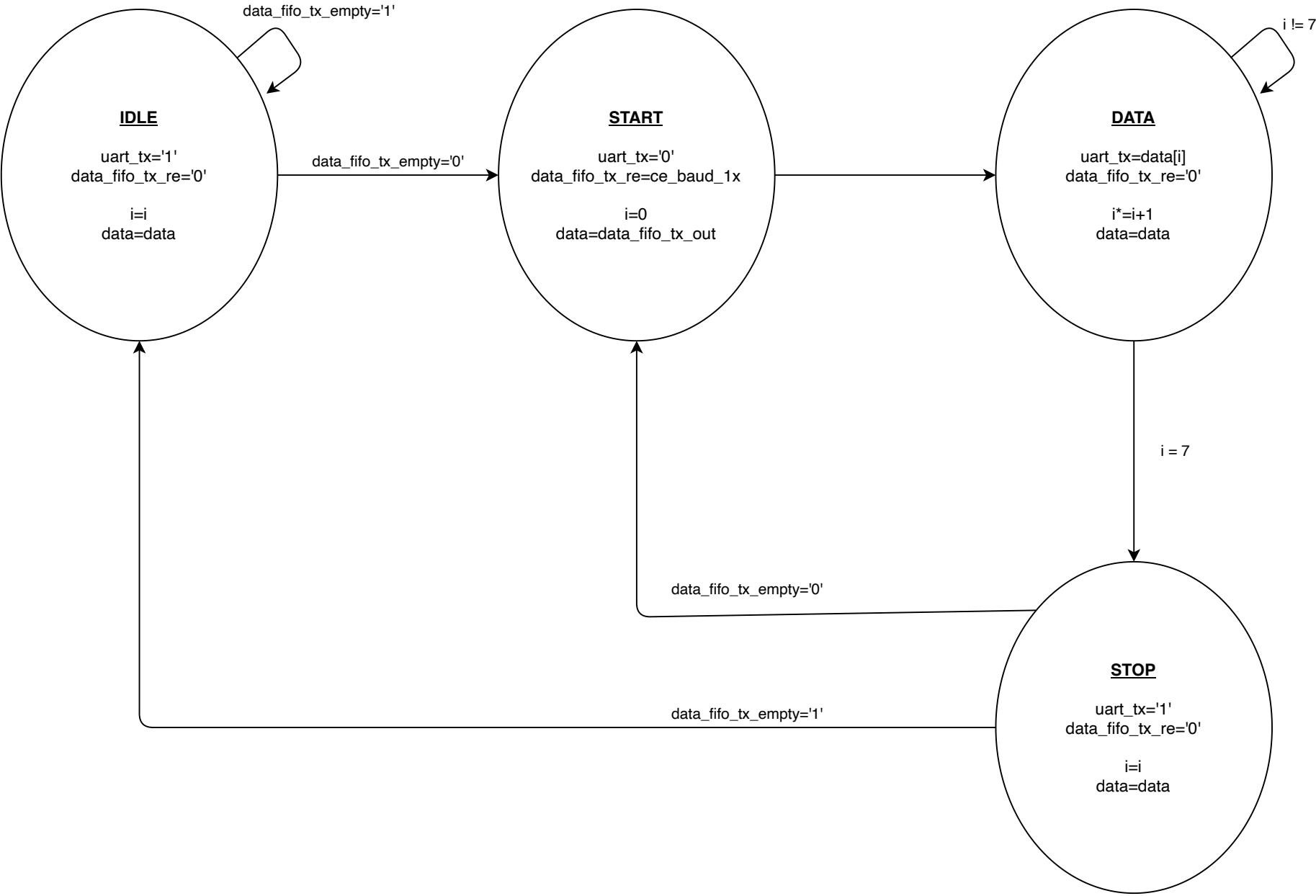
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The first group of Moore machine outputs in each state bubble are FSM outputs, some of them with combinatorial output that is normally only seen in a Mealy machine. (This FSM could be said to be a hybrid Moore and Mealy machine.) The second group of outputs are recursive auxiliary outputs that retain state from one state to the next when assigned to itself.



A TX ONLY UART output to UART chip from the FPGA, with the FSM executing at BAUD rate as its clock enable.

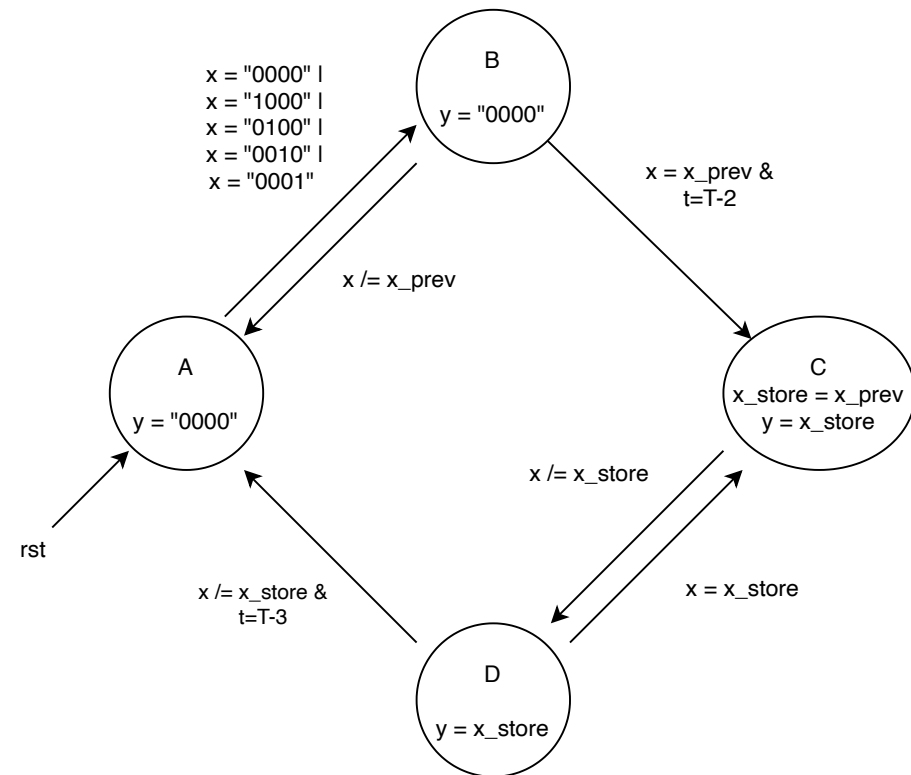
This is the first design draft,  
and the complete FSM diagram  
is shown on another page.



A TX ONLY UART output to UART chip from the FPGA, with the FSM executing at BAUD rate as its clock enable.

The FSM dequeues the UART TX FIFO when there is at least one more byte in the FIFO. No extra STOP/IDLE bits are generated except when the UART TX FIFO reaches empty.

The TX ONLY UART FSM generates a single START bit, 8 bits of DATA, a single STOP bit, and no parity bits.



Full 4-button combined debouncer.

x is defined as a four-bit value.

x\_prev is defined as a four-bit value that holds the previous clock cycle value of x.

x\_store is defined as a four-bit value that holds the value of x and updates the debouncer FSM entered state C during the transition BC..

The registers x\_prev and x\_store could be combined into one register, with its capture of X being a clock-enable during transitions and states of a more complex diagram.

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