Category	Instruction	Operands	Operation	Opcode	Fields	
No-operation	nop	N/A	none	00 00 00	ΦΦ ΦΦΦΦ ΦΦΦΦ	ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ
	add	rt,ra,rb	rt <= ra + rb	00 10 00	ΦΦ ΦΦΦΦ ΦΦΦΦ	BBBB BAAA AAФT TTTT
	sub	rt,ra,rb	rt <= ra – rb	00 01 00	ΦΦ ΦΦΦΦ ΦΦΦΦ	BBBB BAAA AAФT TTTT
	addi	rt,ra,imm	rt <= ra + immediate value	00 10 01	II IIII IIII	IIII ФААА ААФТ TTTT
	subi	rt,ra,imm	rt <= ra – immediate value	00 01 01	II IIII IIII	IIII ФААА ААФТ TTTT
	inc	rt,ra	rt <= ra + 1	00 10 10	ΦΦΦΦΦ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
Arithmetic	dec	rt,ra	rt <= ra – 1	00 01 10	ΦΦΦΦ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
	not	rt,ra	rt <= NOT ra	01 11 11	ΦΦΦΦ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
	and	rt,ra,rb	rt <= ra AND rb	01 01 00	ΦΦΦΦΦ ΦΦΦΦ	BBBB BAAA AAФT TTTT
	or	rt,ra,rb	rt <= ra OR rb	01 10 00	ΦΦΦΦΦ ΦΦΦΦ	BBBB BAAA AAФT TTTT
	xor	rt,ra,rb	rt <= ra XOR rb	01 11 00	ΦΦΦΦΦ ΦΦΦΦ	BBBB BAAA AAФT TTTT
	andi	rt,ra,imm	m rt <= ra AND immediate value	01 01 01	II IIII IIII	IIII ФААА ААФТ TTTT
	ori	rt,ra,imm	rt <= ra OR immediate value	01 10 01	II IIII IIII	IIII ФААА ААФТ TTTT
	xori	rt,ra,imm	rt <= ra XOR immediate value	01 11 01	II IIII IIII	IIII ФААА ААФТ TTTT
	shl	rt,ra,n	rt <= ra shifted left by n bits	01 00 01	ΦΦ ΝΝΝΝ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
	shr	rt,ra,n	rt <= ra shifted right by n bits	01 00 00	ΦΦ ΝΝΝΝ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
	rol	rt,ra,n	n rt <= ra rotated left by n bits	01 00 11	ΦΦ ΝΝΝΝ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
Logic	ror	rt,ra,n	rt <= ra rotated right by n bits	01 00 10	ΦΦ ΝΝΝΝ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
	move	rt,ra	rt <= ra	10 00 00	ΦΦΦΦΦ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
	loadi	rt,addr	rt <= DMEM[addr] {direct addressing}	10 01 01	AA AAAA AAAA	ΑΑΑΑ ΑΑΑΑ ΑΑΦΤ ΤΤΤΤ
	loadr	rt,ra	rt <= DMEM[ra] {register indirect addressing}	10 01 10	ΦΦΦΦΦ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
	loado	rt,ra,off	rt <= DMEM[ra+off] {base plus offset addressing}	10 01 11	00 0000 0000	ΟΟΟΟ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
	stori	rt,addr	DMEM[addr] <= rb {direct addressing}	10 10 01	AA AAAA AAAA	ΑΑΑΑ ΑΑΑΑ ΑΑΦΤ ΤΤΤΤ
	storr	rt,ra	DMEM[ra] <= rb {register indirect addressing}	10 10 10	ΦΦΦΦΦ ΦΦΦΦ	ΦΦΦΦ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
Transfer	storo	rt,ra,off	DMEM[ra+off] <= rb {base plus offset addressing}	10 10 11	00 0000 0000	ΟΟΟΟ ΦΑΑΑ ΑΑΦΤ ΤΤΤΤ
and the l	jmp	off	Jump to IMEM[PC+off]	11 00 00	00 0000 0000	0000 0000 0000 0000
	buo	ro cond off	f If condition is true, then jump to IMEM[PC+off], else continue	11 10 00	00 0000 0000	0000 4444 4444 4666
control	brc	ra,cond,off	Conditions: ra = 0; ra \neq 0; ra = 1; ra < 0; ra > 0; ra \leq 0; ra \geq 0	11 10 00	00 0000 0000	ΟΟΟΟ ΦΑΑΑ ΑΑΦΦ ΦССС