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# Meerkat

## i.MX7D based 96Boards

001-013-02

<b>NovTech, Inc. Engineering Firm</b> 7401 Wiles Road, Suite 229, Coral Springs, FL 33067 <a href="http://www.novtech.com">www.novtech.com</a> (954) 341-3320			<b>novtech</b>
<b>Customer:</b> <b>NovTech, Inc.</b>			<a href="http://www.novtech.com">www.novtech.com</a>
<b>Engineer:</b> <b>G.Guy</b>	<b>Project:</b> <b>001-013-02 MX7_96BOARDS</b>	<b>Board:</b>	<b>Meerkat</b>
<b>Drawn By:</b> <b>T.Ortiz</b>			
<b>Checked By:</b> <b>Y.Har-Nov</b>	<b>Size:</b> <b>B</b>	<b>Title:</b> <b>Openinjg Page</b>	<b>Rev:</b> <b>01</b>
<b>Approved By:</b> <b>*</b>	<b>Date:</b> *		<b>Sheet 1 of 20</b>

# Place keeper for future revs

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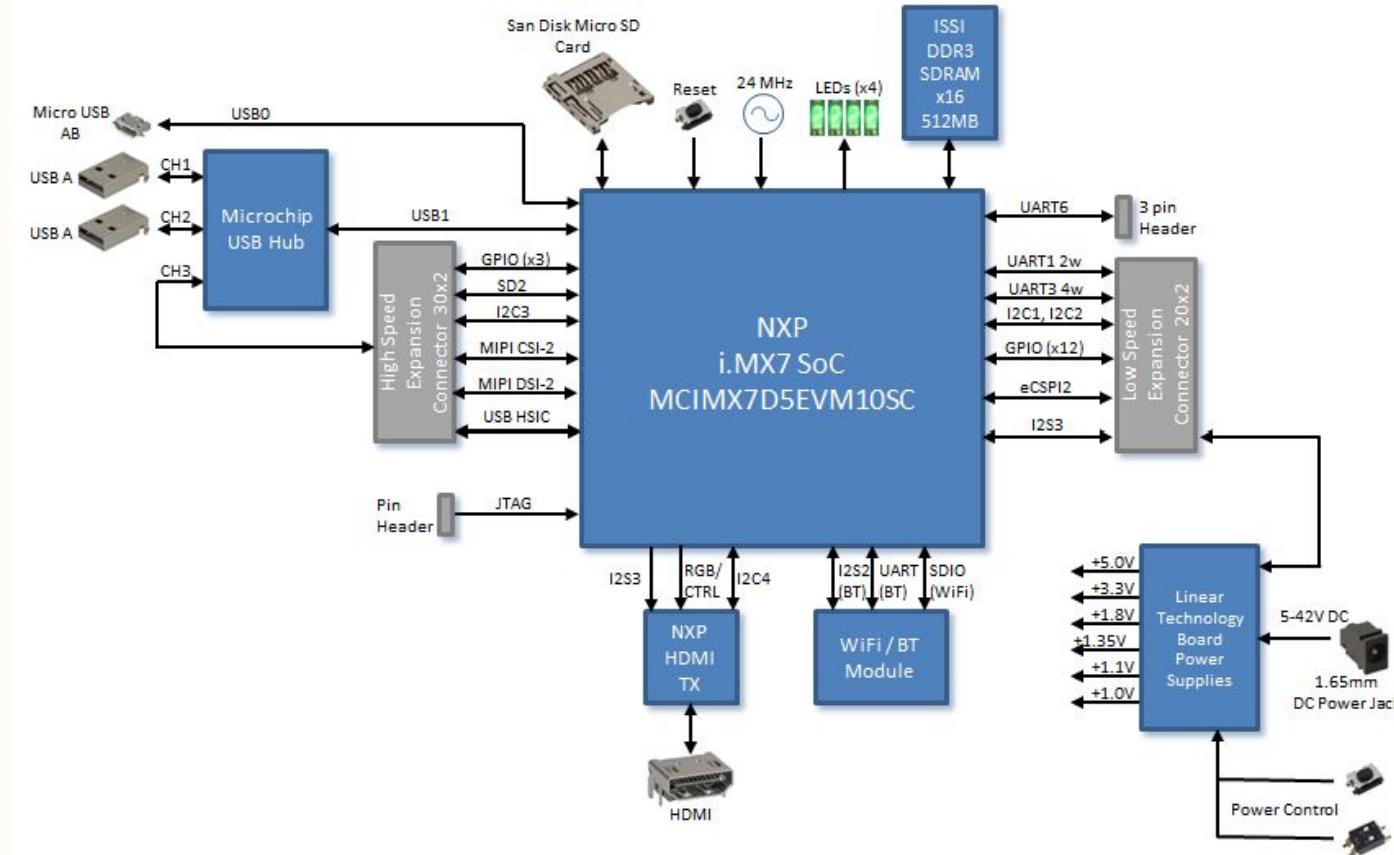
C

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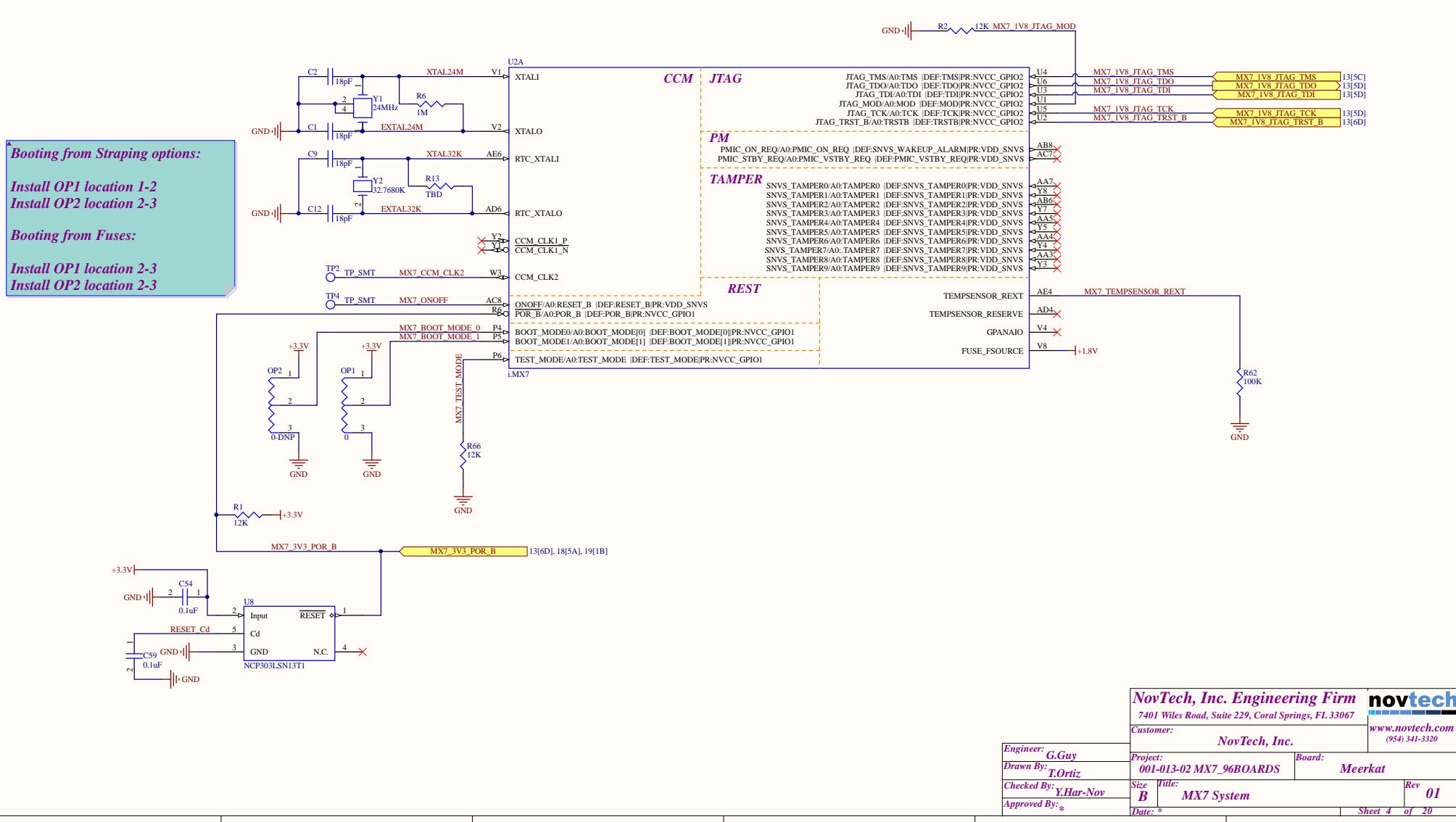
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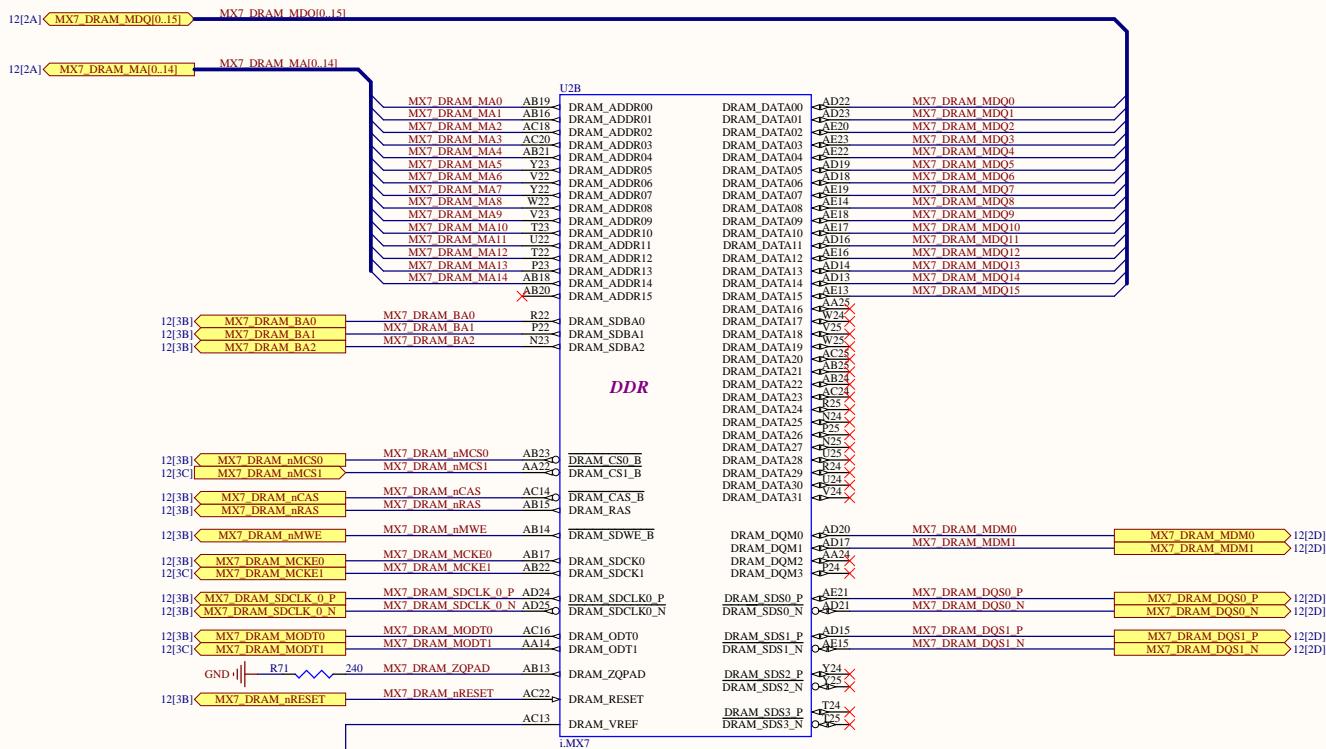
D

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<b>Drawn By:</b>	<b>T.Ortiz</b>	<b>001-013-02 MX7_96BOARDS</b>	<b>Meerkat</b>
<b>Checked By:</b>	<b>Y.Har-Nov</b>	<b>Size:</b>	<b>Title:</b>
<b>Approved By:</b> *	<b>B</b>	<b>Design Notes</b>	<b>Rev:</b>
			<b>01</b>
		<b>Date:</b> *	<b>Sheet 2 of 20</b>



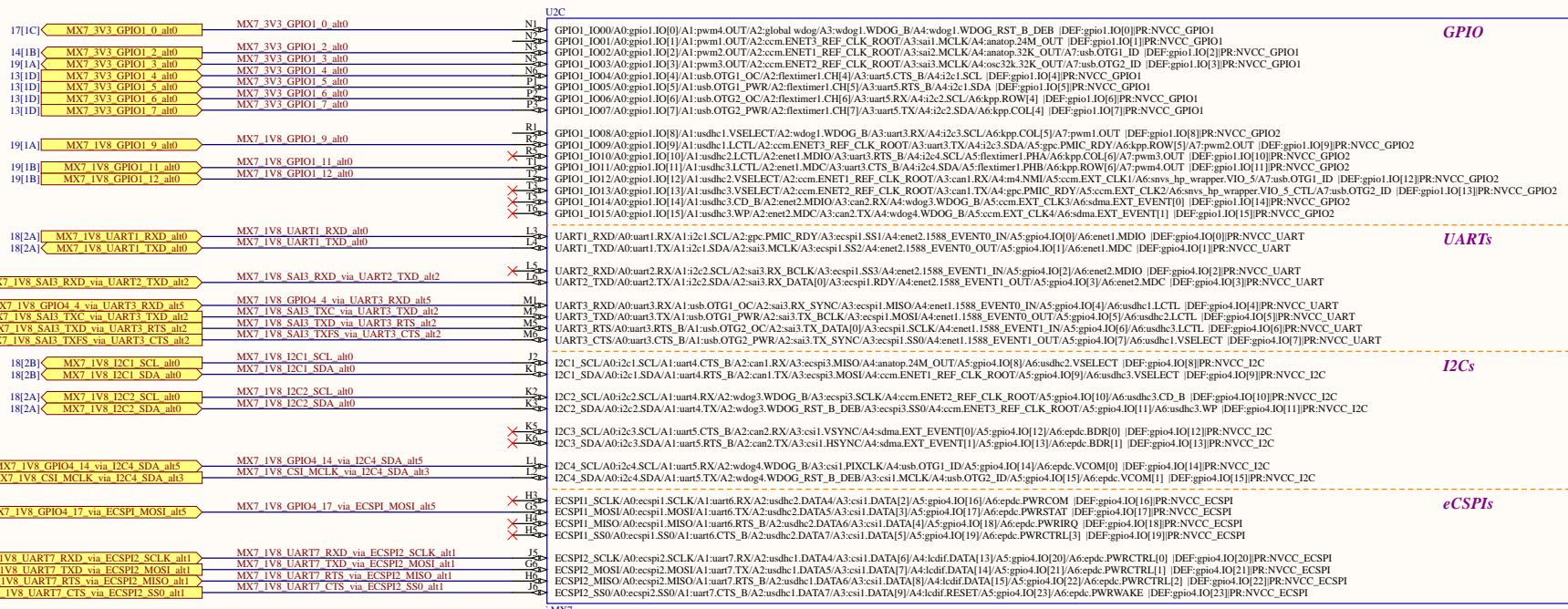
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7401 Wiles Road, Suite 229, Coral Springs, FL 33067		
<b>Customer:</b>	<b>NovTech, Inc.</b>	<b>Board:</b>
<b>Engineer:</b> G.Guy	<b>Project:</b> 001-013-02 MX7_96BOARDS	<b>Rev:</b> 01
<b>Drawn By:</b> T.Ortiz		<b>Meerkat</b>
<b>Checked By:</b> Y.Har-Nov	<b>Title:</b> Block Diagram	<b>Date:</b> *
<b>Approved By:</b> *		<b>Sheet:</b> 3 of 20





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<b>Drawn By:</b>	T.Ortiz	<b>Board:</b>
<b>Checked By:</b>	Y.Har-Nov	<b>Title:</b>
<b>Approved By:</b> *	<b>Rev:</b>	<b>01</b>
<b>Date:</b> *	<b>Sheet:</b> 5	<b>of:</b> 20

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B	13[6B]	MX7_3V3_UART6_RXD_via_SD1_CD_B.alt2	MX7_3V3_UART6_RXD_via_SD1_CD_B.alt2	C6	SD1_CD_B/A@usdhc1_CD/B@2uart6_RX/X@scsp4_MSDO@4/fleximer1.CH0/[A5:gpio5.I0 0] [DEF:gpio5.I0 0]PR:NVCC_SD1
	13[6B]	MX7_3V3_UART6_RXD_via_SD1_WP.alt5	MX7_3V3_BT_LED_as_GPIOs_2_via_SD1_RESET.alt5	C7	SD1_WP_B/A@usdhc1_WP@2uart6_RX/X@scsp4_MSDO@4/fleximer1.CH0/[A5:gpio5.I0 0] [DEF:gpio5.I0 0]PR:NVCC_SD1
	13[6B]	MX7_3V3_BT_LED_as_GPIOs_2_via_SD1_RESET.alt5	MX7_3V3_SD1_CLK.alt0	B4	SD1_RESET_B/A@usdhc1.RESET_B/A@sa3.MCLK/A2uart6_RTS_B/A3scsp4_SCLK/A4/fleximer1.CH0/[A5:gpio5.I0 2] [DEF:gpio5.I0 2]PR:NVCC_SD1
	13[4A4]	MX7_3V3_SD1_CMD.alt0	MX7_3V3_SD1_CMD.alt0	B5	SD1_CLK_A0/usdhc1(CLKA1sa3.RX_SYNC/A2uart6_CTS_B/A3scsp4_SS0/A4/fleximer1.CH0/[A5:gpio5.I0 3] [DEF:gpio5.I0 3]PR:NVCC_SD1
	13[4A4]	MX7_3V3_SD1_DATA0.alt0	MX7_3V3_SD1_DATA0.alt0	C5	SD1_CMD/A0/usdhc1.CMD/A1sa3.RX_BCLKA3scsp4_SS1/A4/fleximer1.CH0/[A5:gpio5.I0 4] [DEF:gpio5.I0 4]PR:NVCC_SD1
	13[4A4]	MX7_3V3_SD1_DATA1.alt0	MX7_3V3_SD1_DATA1.alt0	A5	SD1_DATA0/A0/usdhc1.DAT0/A1sa3.RX_DATA0/A2uart7_RX/X@scsp4_SS2/A4/fleximer2.CH1/[A5:gpio5.I0 5] [A6:cmEXT_CLK1] [DEF:gpio5.I0 5]PR:NVCC_SD1
	13[4A4]	MX7_3V3_SD1_DATA1.alt0	MX7_3V3_SD1_DATA2.alt0	D5	SD1_DATA0/A0/usdhc1.DAT0/A1sa3.RX_DATA0/A2uart7_RX/X@scsp4_SS3/A4/fleximer2.CH1/[A5:gpio5.I0 6] [A6:cmEXT_CLK2] [DEF:gpio5.I0 6]PR:NVCC_SD1
	13[4A4]	MX7_3V3_SD1_DATA2.alt0	MX7_3V3_SD1_DATA2.alt0	E5	SD1_DATA0/A0/usdhc1.DAT0/A1sa3.RX_DATA0/A2uart7_RX/X@scsp4_SS4/A4/fleximer2.CH1/[A5:gpio5.I0 7] [A6:cmEXT_CLK3] [DEF:gpio5.I0 7]PR:NVCC_SD1
	13[4A4]	MX7_3V3_SD1_DATA3.alt0	MX7_3V3_SD1_DATA3.alt0	F5	SD1_DATA0/A0/usdhc1.DAT0/A1sa3.RX_DATA0/A2uart7_RTS_B/A3scsp4_SS1/A4/fleximer1.PHA/A5:gpio5.I0 8] [A6:cmEXT_CLK4] [DEF:gpio5.I0 8]PR:NVCC_SD1
	18[2B]	MX7_1V8_GPIO5_9_via_SD2_CD_B.alt5	MX7_1V8_GPIO5_9_via_SD2_CD_B.alt5	G5	SD2_CD_B/A@usdhc2_CD_B/A@enet1.MDIO/A2enet2.MDIO/A3scp3_SS2/A4/fleximer1.PHB/A5:gpio5.I0 9] [A6:cmEXT_EVENT0] [DEF:gpio5.I0 9]PR:NVCC_SD2
	18[2B]	MX7_1V8_GPIO5_10_via_SD2_WP.alt5	MX7_1V8_GPIO5_10_via_SD2_WP.alt5	H5	SD2_WP_B/A@usdhc2_WP@1enet1.MDC/A2enet2.MDC/A3scp3_SS2/A4:wp OTG1_ID/A5:gpio5.I0 10] [A6:cmEXT_EVENT1] [DEF:gpio5.I0 10]PR:NVCC_SD2
	18[2B]	MX7_1V8_SD2_CLK.alt0	MX7_1V8_SD2_CLK.alt0	I5	SD2_RESET_B/A@usdhc2.RESET_B/A1sa2.MCLK/A2:usdhc2.RESET/A3scp3_RDY/A4:usdhc2_OTG2_ID/A5:gpio5.I0 11] [DEF:gpio5.I0 11]PR:NVCC_SD2
C	18[2B]	MX7_1V8_SD2_CMD.alt0	MX7_1V8_SD2_CMD.alt0	J5	SD2_CLK_A0/usdhc2(CLKA1sa2.RX_SYNC/A2:msm.RIGHT/A3:gp4(CLK/A5:gpio5.I0 12] [DEF:gpio5.I0 12]PR:NVCC_SD2
	18[2B]	MX7_1V8_SD2_DATA0.alt0	MX7_1V8_SD2_DATA0.alt0	K5	SD2_CMD/A0/usdhc2.CMD/A1sa2.RX_BCLKA2:mqi.LEFT/A3:gp4.CAPTURE1/A4:sim2.PORT1_RTS_B/A5:gpio5.I0 13] [DEF:gpio5.I0 13]PR:NVCC_SD2
	18[2B]	MX7_1V8_SD2_DATA1.alt0	MX7_1V8_SD2_DATA1.alt0	L5	SD2_DATA0/A0/usdhc2.DAT0/A1sa2.RX_DATA0/A2:uart4_RX/X@3:gp4.CAPTURE2/A4:sim2.PORT1_CLK/A5:gpio5.I0 14] [DEF:gpio5.I0 14]PR:NVCC_SD2
	18[2B]	MX7_1V8_SD2_DATA1.alt0	MX7_1V8_SD2_DATA2.alt0	M5	SD2_DATA1/A0/usdhc2.DAT0/A1sa2.TX_BCLKA2:uart4_RX/X@3:gp4.COMPARE1/A4:sim2.PORT1_RTS_B/A5:gpio5.I0 15] [DEF:gpio5.I0 15]PR:NVCC_SD2
	18[2B]	MX7_1V8_SD2_DATA2.alt0	MX7_1V8_SD2_DATA3.alt0	N5	SD2_DATA2/A0/usdhc2.DAT0/A1sa2.TX_SYNC/A2:uart4CTS_B/A3:gp4.COMPARE2/A4:sim2.PORT1_SVEN/A5:gpio5.I0 16] [DEF:gpio5.I0 16]PR:NVCC_SD2
	18[2B]	MX7_1V8_SD2_DATA3.alt0	MX7_1V8_SD2_DATA3.alt0	O5	SD2_DATA2/A0/usdhc2.DAT0/A1sa2.TX_SYNC/A2:uart4CTS_B/A3:gp4.COMPARE3/A4:sim2.PORT1_PD/A5:gpio5.I0 17] [DEF:gpio5.I0 17]PR:NVCC_SD2
	17[1A1]	MX7_1V8_SD3_CLK.alt0	MX7_1V8_SD3_CLK.alt0	P5	SD3_CLK_A0/usdhc3(CLKA1rawand_CLE/A2:scp4_MISO/A3:sa3.RX_SYNC/A4:gp4(CLKA5:gpio6.I0 0] [DEF:gpio6.I0 0]PR:NVCC_SD3
	17[1A1]	MX7_1V8_SD3_CMD.alt0	MX7_1V8_SD3_CMD.alt0	Q5	SD3_CMD/A0/usdhc3.CMD/A1rawand_ALE/A2:scp4_MOSI/A3:sa3.RX_BCLKA4:gp3.CAPTURE1/A5:gpio6.I0 1] [DEF:gpio6.I0 1]PR:NVCC_SD3
	17[1A1]	MX7_1V8_SD3_DATA0.alt0	MX7_1V8_SD3_DATA0.alt0	R5	SD3_DATA0/A0/usdhc3.DAT0/A1rawand.DAT0/A2:scp4_SS0/A3:sa3.RX_DATA0/A4:gp3.CAPTURE2/A5:gpio6.I0 2] [DEF:gpio6.I0 2]PR:NVCC_SD3
	17[1A1]	MX7_1V8_SD3_DATA1.alt0	MX7_1V8_SD3_DATA1.alt0	S5	SD3_DATA1/A0/usdhc3.DAT0/A1rawand.DAT0/A2:scp4_SS1/A3:sa3.RX_DATA0/A4:gp3.CAPTURE1/A5:gpio6.I0 3] [DEF:gpio6.I0 3]PR:NVCC_SD3
D	17[1A1]	MX7_1V8_SD3_DATA2.alt0	MX7_1V8_SD3_DATA2.alt0	T5	SD3_DATA2/A0/usdhc3.DAT0/A1rawand.DAT0/A2:2:3:SDA/A3:sa3.TX_SYNC/A4:gp3.COMPARE1/A5:gpio6.I0 4] [DEF:gpio6.I0 4]PR:NVCC_SD3
	17[1A1]	MX7_1V8_SD3_DATA3.alt0	MX7_1V8_SD3_DATA3.alt0	U5	SD3_DATA3/A0/usdhc3.DAT0/A3:2:3:SDA/A3:sa3.TX_DATA0/A4:gp3.COMPARE3/A5:gpio6.I0 5] [DEF:gpio6.I0 5]PR:NVCC_SD3
	18[2A]	MX7_1V8_UART3_RXD_via_SD3_DATA4.alt3	MX7_1V8_UART3_RXD_via_SD3_DATA4.alt3	V5	SD3_DATA4/A0/usdhc3.DAT0/A4/A1rawand.DAT0/A4:3uart3.RX/A4:can2.RX/A5:gpio6.I0 6] [DEF:gpio6.I0 6]PR:NVCC_SD3
	18[2A]	MX7_1V8_UART3_RXD_via_SD3_DATA5.alt3	MX7_1V8_UART3_RXD_via_SD3_DATA5.alt3	W5	SD3_DATA5/A0/usdhc3.DAT0/A5/A1rawand.DAT0/A5:3uart3.TX/A4:can1.TX/A5:gpio6.I0 7] [DEF:gpio6.I0 7]PR:NVCC_SD3
	18[2A]	MX7_1V8_UART3 RTS_via_SD3_DATA6.alt3	MX7_1V8_UART3 RTS_via_SD3_DATA6.alt3	X5	SD3_DATA6/A0/usdhc3.DAT0/A6/A1rawand.DAT0/A6:2usdhc3.WP/A3:uart3.RTS_B/A4:can2.TX/A5:gpio6.I0 8] [DEF:gpio6.I0 8]PR:NVCC_SD3
	18[2A]	MX7_1V8_UART3_CTS_via_SD3_DATA7.alt3	MX7_1V8_UART3_CTS_via_SD3_DATA7.alt3	Y5	SD3_DATA7/A0/usdhc3.DAT0/A7/A1rawand.DAT0/A7:2usdhc3.CD_B/A3:uart3.CTS_B/A4:can1.RX/A5:gpio6.I0 9] [DEF:gpio6.I0 9]PR:NVCC_SD3
	18[5B]	MX7_1V8_GPIO6_10_via_SD3_STROBE.alt5	MX7_1V8_GPIO6_10_via_SD3_STROBE.alt5	Z5	SD3_STROBE/A0/usdhc3.STROBE/A1rawand.RE_B/A5:gpio6.I0 10] [DEF:gpio6.I0 10]PR:NVCC_SD3
	18[5B]	MX7_1V8_GPIO6_11_via_SD3_RESET_B.alt5	MX7_1V8_GPIO6_11_via_SD3_RESET_B.alt5	G5	SD3_RESET_B/A@usdhc3.RESET_B/A1rawand.WE_B/A2:usdhc3.RESET/A3:sa3.MCLK/A5:gpio6.I0 11] [DEF:gpio6.I0 11]PR:NVCC_SD3

iMX7

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<b>Engineer:</b>	<b>G.Guy</b>	<b>Project:</b>	<b>001-013-02 MX7_96BOARDS</b>
<b>Drawn By:</b>	<b>T.Ortiz</b>	<b>Board:</b>	<b>Meerkat</b>
<b>Checked By:</b>	<b>Y.Har-Nov</b>	<b>Title:</b>	<b>MX7 SDs</b>
<b>Approved By:</b> *	<b>B</b>	<b>Rev:</b>	<b>01</b>
<b>Date:</b> *		<b>Sheet 8 of 20</b>	

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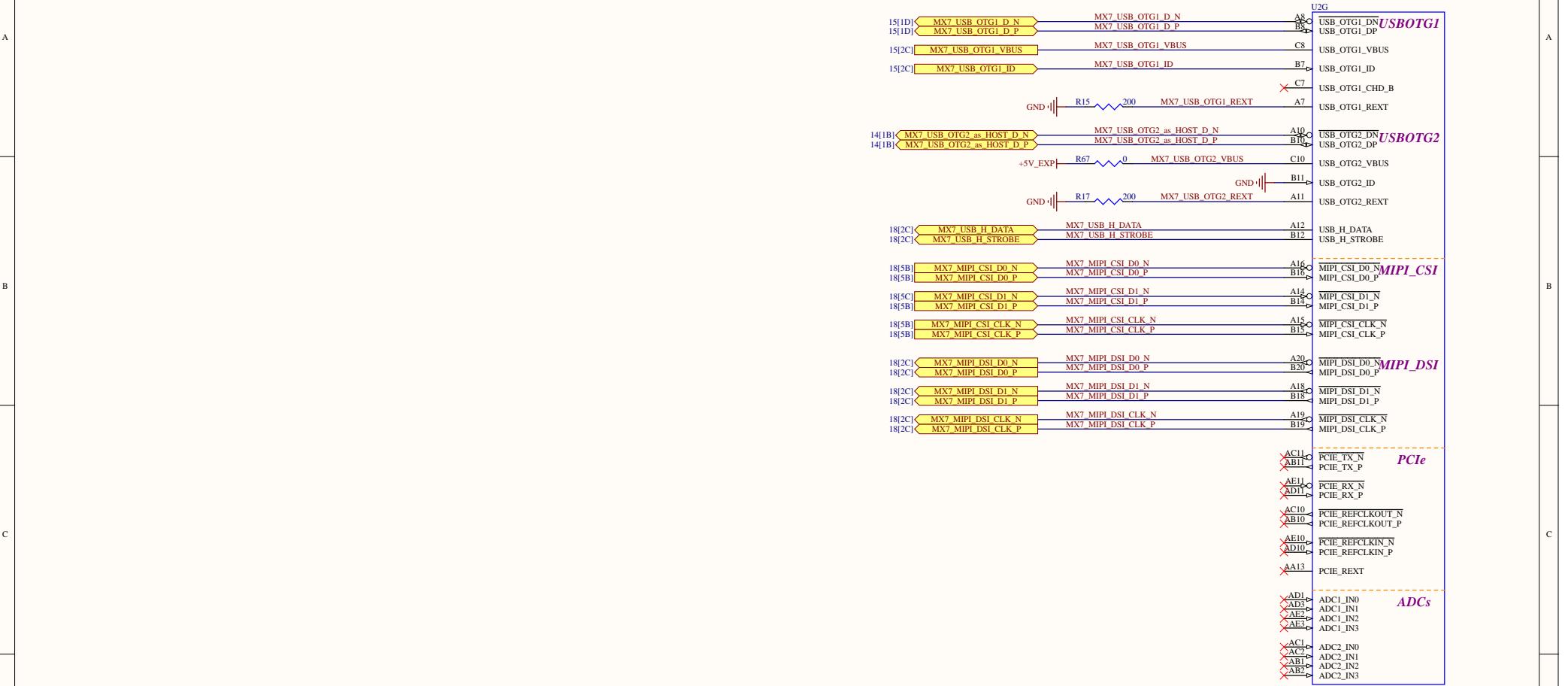
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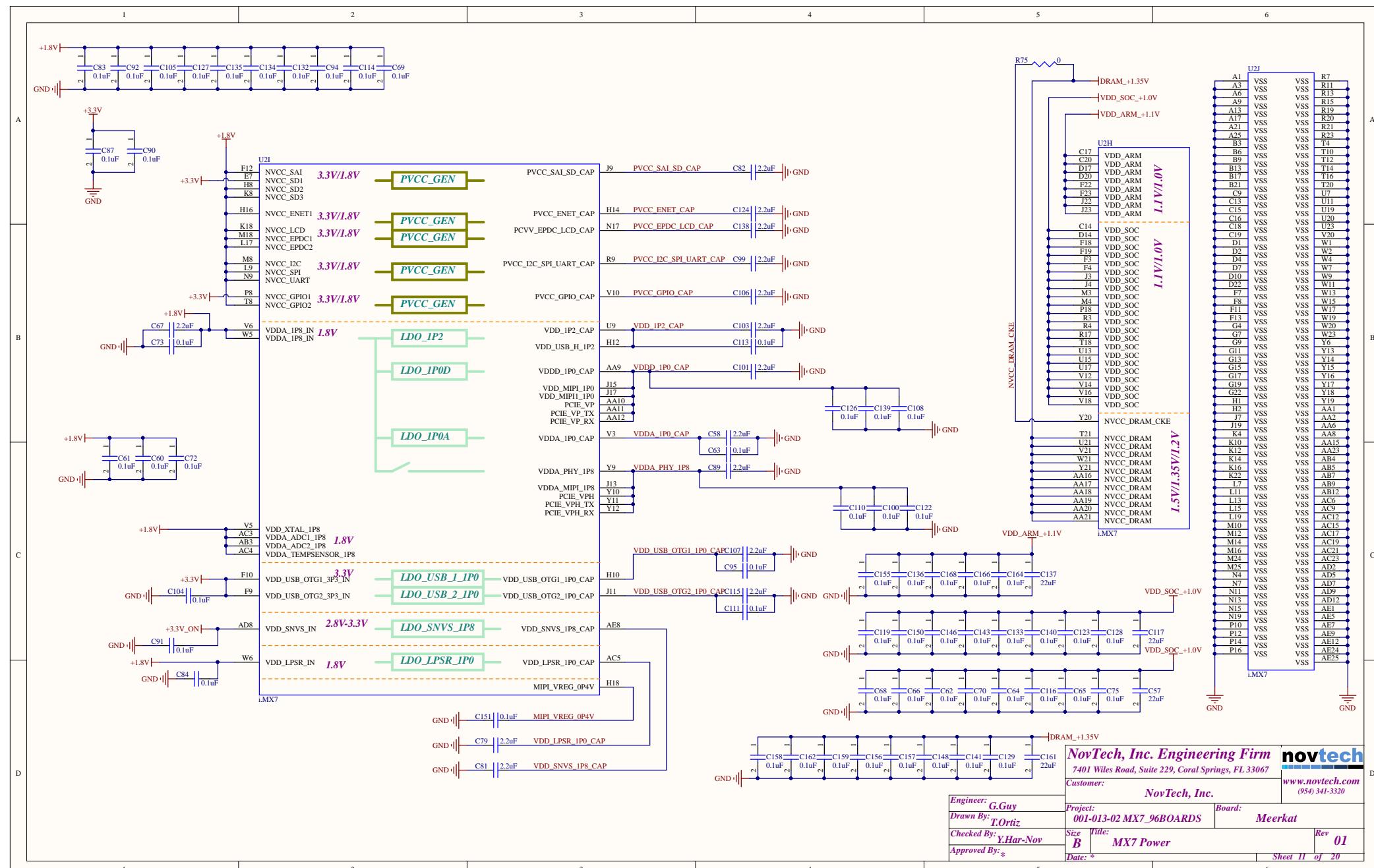
		SAII																																		
B		MX7_1V8 GPIO6_13_vin_SAI1_TXC_alt2	MX7_1V8 GPIO6_13_via_SAI1_TXC_alt5	E12	SAII_RXD/A0/sai1.RX,DATA[0][0]A1:rawand.CE1,B/A2:uart5.RX/A3:can1.RX/A4:sim1.PORT1,TRXD/A5:gpio6.IO[12] DEF:gpio6.IO[12] PR:NVCC_SAI	C12	SAII_TXC/A0/sai1.TX,BCLK/A1:rawand.CE0,B/A2:uart5.TX/A3:can1.TX/A4:sim1.PORT1,CLK/A5:gpio6.IO[13] DEF:gpio6.IO[13] PR:NVCC_SAI	D1	SAII_RXIS/A0/sai1.TX,SYNC/A1:rawand.DOS/A2:uart5.CTS,B/A3:can2.RX/A4:sim1.PORT1,RST,B/A5:gpio6.IO[14] DEF:gpio6.IO[14] PR:NVCC_SAI	E1	SAII_TXD/A0/sai1.TX,DATA[0][0]A1:rawand.READY,B/A2:uart5.RTS,B/A3:can2.TX/A4:sim1.PORT1,SVEN/A5:gpio6.IO[15] DEF:gpio6.IO[15] PR:NVCC_SAI	C12	SAII_RXFS/A0/sai1.RX,SYNC/A1:rawand.CE2,B/A2:sai2.RX,SYNC/A3:j2e4.SCL/A4:sim1.PORT1,PD/A5:gpio6.IO[16] A6:mqx.RIGHT DEF:gpio6.IO[16] PR:NVCC_SAI	D1	SAII_RXC/A0/sai1.RX,BCLK/A1:rawand.CE3,B/A2:sai2.RX,BCLK/A3:j2e4.SDA/A4:flextime2.PHA/A5:gpio6.IO[17] A6:mqx.LEFT DEF:gpio6.IO[17] PR:NVCC_SAI	E1	SAII_MCLK/A0/sai1.MCLK/A1:rawand.WP,B/A2:sai2.MCLK/A3:pmic.PMIC,RDY/A4:flextime2.PH/A5:gpio6.IO[18] DEF:gpio6.IO[18] PR:NVCC_SAI																			
16[1B], 19[1A]	MX7_1V8 I2C4_SCL_via_SAI1_RXFS_alt3	MX7_1V8 I2C4_SDA_via_SAI1_RXC_alt3	16[1C], 19[1A]	MX7_1V8 I2C4_SDA_via_SAI1_RXC_alt3	16[1B]	MX7_1V8 SAII_MCLK_alt0	17[1B]	MX7_1V8 SAII_TXF5_alt0	17[1B]	MX7_1V8 SAII_RXC_alt0	17[1B]	MX7_1V8 SAII_RXD_alt0	17[1B]	MX7_1V8 SAII_RXD_alt0	D9	SAII_RXFS/A0/sai2.TX,SYNC/A1:espi3.MISO/A2:uart4.RX/A3:uart1.CTS,B/A4:flextime2.CH[4]/A5:gpio6.IO[19] DEF:gpio6.IO[19] PR:NVCC_SAI	D8	SAII_RXC/A0/sai2.TX,BCLK/A1:espi3.MOSI/A2:uart4.RX,A3:uart1.RTS,B/A4:flextime2.CH[5]/A5:gpio6.IO[20] DEF:gpio6.IO[20] PR:NVCC_SAI	E9	SAII_RXD/A0/sai2.RX,DATA[0][0]A1:espi3.SCLK/A2:uart4.CTS,B/A3:uart2.CTS,B/A4:flextime2.CH[6]/A5:gpio6.IO[21] A6:kpp.COL[7] DEF:gpio6.IO[21] PR:NVCC_SAI	E8	SAII_TXD/A0/sai2.TX,DATA[0][0]A1:espi3.SSO/A2:uart4.RTS,B/A3:uart2.RTS,B/A4:flextime2.CH[7]/A5:gpio6.IO[22] A6:kpp.ROW[7] DEF:gpio6.IO[22] PR:NVCC_SAI														
C		MX7_1V8 I2C3_SCL_via_ENET1_RD0_alt2	MX7_1V8 I2C3_SDA_via_ENET1_RD1_alt2	E14	ENET1_RDO/A0:enet1.RGMII_RDO/A1:pwm1.OUT/A2:j2e3.SCL/A3:uart1.CTS,B/A4:epdc:VCOM[0]/A5:gpio7.IO[0] A6:kpp.ROW[3] DEF:gpio7.IO[0] PR:NVCC_ENET1	F14	ENET1_RDI/A0:enet1.RGMII_RDI/A1:pwm2.OUT/A2:j2e3.SDA/A3:uart1.RTS,B/A4:epdc:VCOM[1]/A5:gpio7.IO[1] A6:kpp.COL[3] DEF:gpio7.IO[1] PR:NVCC_ENET1	D14	ENET1_RD2/A0:enet1.RGMII_RD2/A1:cam1.RX/A2:espi2.SCLK/A3:uart1.RX,A4:epdc:SDCE[4]/A5:gpio7.IO[2] A6:kpp.ROW[2] DEF:gpio7.IO[2] PR:NVCC_ENET1	E14	ENET1_RD3/A0:enet1.RGMII_RD3/A1:cam1.TX/A2:espi2.MOSI/A3:uart1.TX,A4:epdc:SDCE[5]/A5:gpio7.IO[3] A6:kpp.COL[2] DEF:gpio7.IO[3] PR:NVCC_ENET1	F14	ENET1_RX_CTL/A0:enet1.RGMII_RX_CTL/A1:cam1.RX,B/A2:espi2.SS,B/A3:uart1.RX,A4:epdc:SDCE[6]/A5:gpio7.IO[4] A6:kpp.ROW[4] DEF:gpio7.IO[4] PR:NVCC_ENET1	D14	ENET1_RX_CTL/A0:enet1.RGMII_RX_CTL/A1:cam1.RX,B/A2:espi2.SS,B/A3:uart1.RX,A4:epdc:SDCE[7]/A5:gpio7.IO[5] PR:NVCC_ENET1	E14	ENET1_TD0/A0:enet1.RGMII_TD0/A1:espi3.OUTPUT/A2:espi3.SS/A4:epdc:SDCE[8]/A5:gpio7.IO[6] A6:kpp.ROW[10] DEF:gpio7.IO[6] PR:NVCC_ENET1	F14	ENET1_TD1/A0:enet1.RGMII_TD1/A1:pwmnd.OUT/A2:espi2.RDV/A4:epdc:SDCE[9]/A5:gpio7.IO[7] A6:kpp.COL[9] DEF:gpio7.IO[7] PR:NVCC_ENET1	D14	ENET1_TD2/A0:enet1.RGMII_TD2/A1:cam2.RX/A2:espi2.MISO/A3:j2e4.SCL/A4:epdc:SDOED/A5:gpio7.IO[8] DEF:gpio7.IO[8] PR:NVCC_ENET1	E14	ENET1_TD3/A0:enet1.RGMII_TD3/A1:cam2.TX/A2:espi2.SSO/A3:j2e4.SDA/A4:epdc:SDQE[2]/A5:gpio7.IO[9] PR:NVCC_ENET1	F14	ENET1_TX_CTL/A0:enet1.RGMII_TX_CTL/A1:enel1.TX,EN/A2:sai1.RX,SYNC/A3:gp[2].COMPARE[1]/A4:epdc:PWRCTRL[1]/A5:gpio7.IO[10] DEF:gpio7.IO[10] PR:NVCC_ENET1	D14	ENET1_TX_CTL/A0:enet1.TX_CTL/A1:enel1.TX,ER/A2:sai1.RX,BCLK/A3:gp[2].COMPARE[2]/A4:epdc:PWRCTRL[3]/A5:gpio7.IO[11] DEF:gpio7.IO[11] PR:NVCC_ENET1	E14	ENET1_TX_CLK/A0:enet1.TX_CLK/A1:enel1.TX,CLK/A1:enet1.REF_CLK.ROOT/A2:sai1.RX,DATA[0][0]A3:gp[2].COMPARE[3]/A4:epdc:PWRCTRL[4]/A5:gpio7.IO[12] A6:ccm:EXT_CLK1 DEF:gpio7.IO[12] PR:NVCC_ENET1	F14	ENET1_RX_CLK/A0:enet1.RX_CLK/A1:wdog2.WDOG/B/A2:sai1.TX,BCLK/A3:gp[2].CAPTURE[1]/A4:epdc:PWRCTRL[0]/A5:gpio7.IO[13] A6:ccm:EXT_CLK2 DEF:gpio7.IO[13] PR:NVCC_ENET1	D14	ENET1_RX_CLK/A0:enet1.RX_CLK/A1:wdog2.WDOG_B_DEB/A2:sai1.TX,SYNC/A3:gp[2].CAPTURE[1]/A4:epdc:PWRCTRL[1]/A5:gpio7.IO[14] A6:ccm:EXT_CLK3 DEF:gpio7.IO[14] PR:NVCC_ENET1	E14	ENET1_COL/A0:enet1.COL/A1:global.wdog/A2:sai1.TX,DATA[0][0]A3:gp[2].CAPTURE[2]/A4:epdc:PWRCTRL[1]/A5:gpio7.IO[15] A6:ccm:EXT_CLK4 DEF:gpio7.IO[15] PR:NVCC_ENET1	F14
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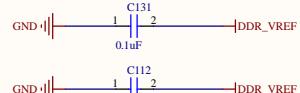
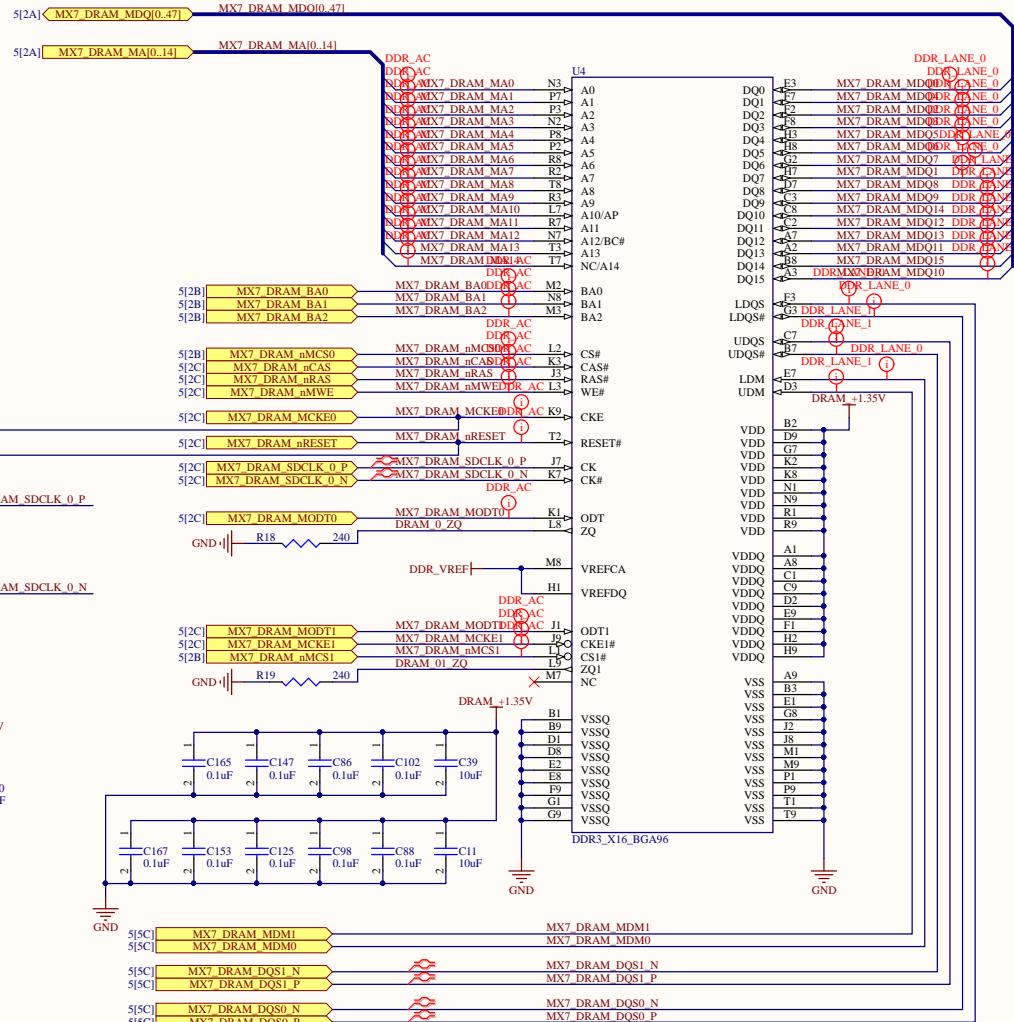
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Customer:	NovTech, Inc.
Engineer:	G.Guy
Drawn By:	T.Ortiz
Checked By:	Y.Har-Nov
Approved By:	B
Date:	*

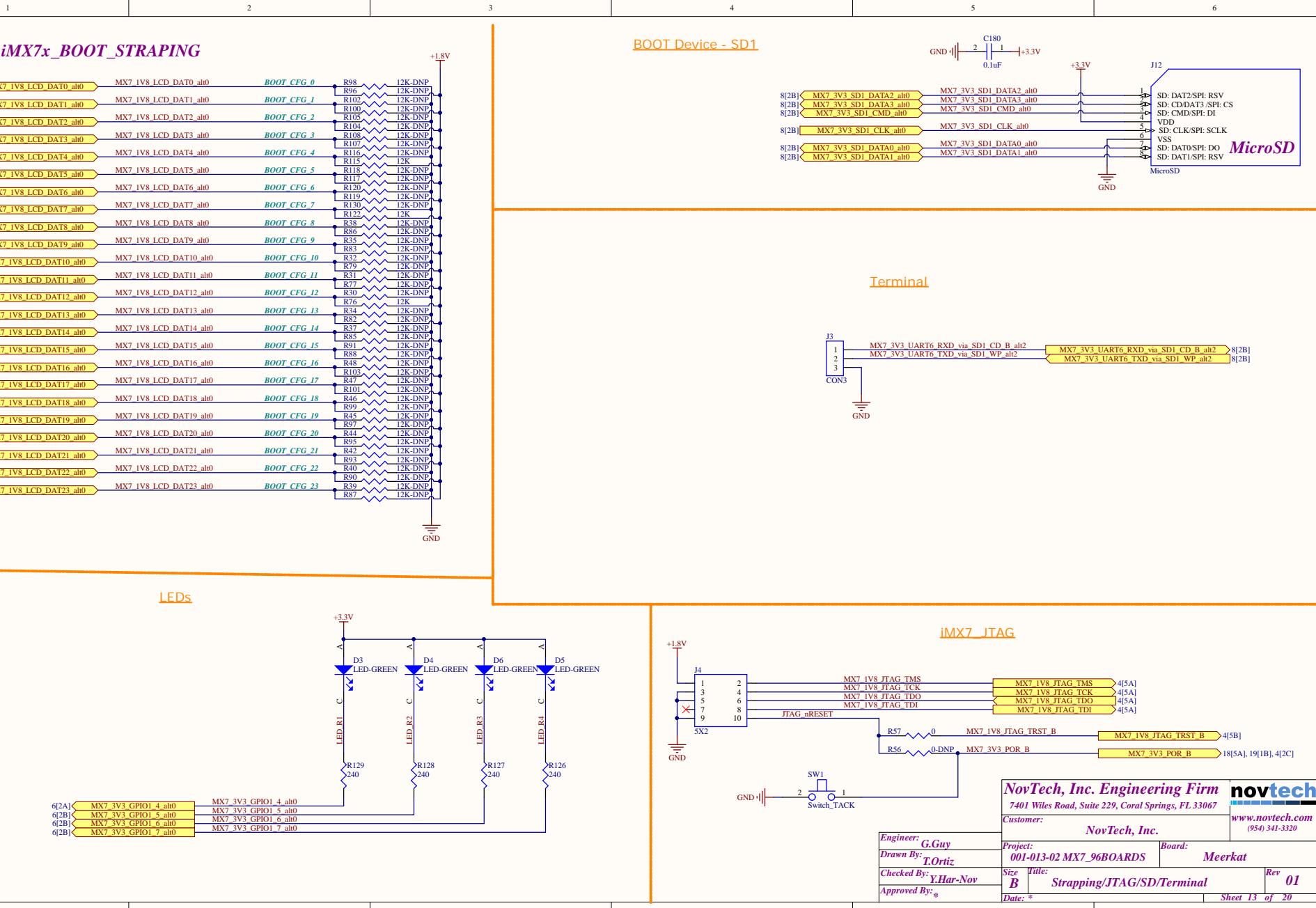




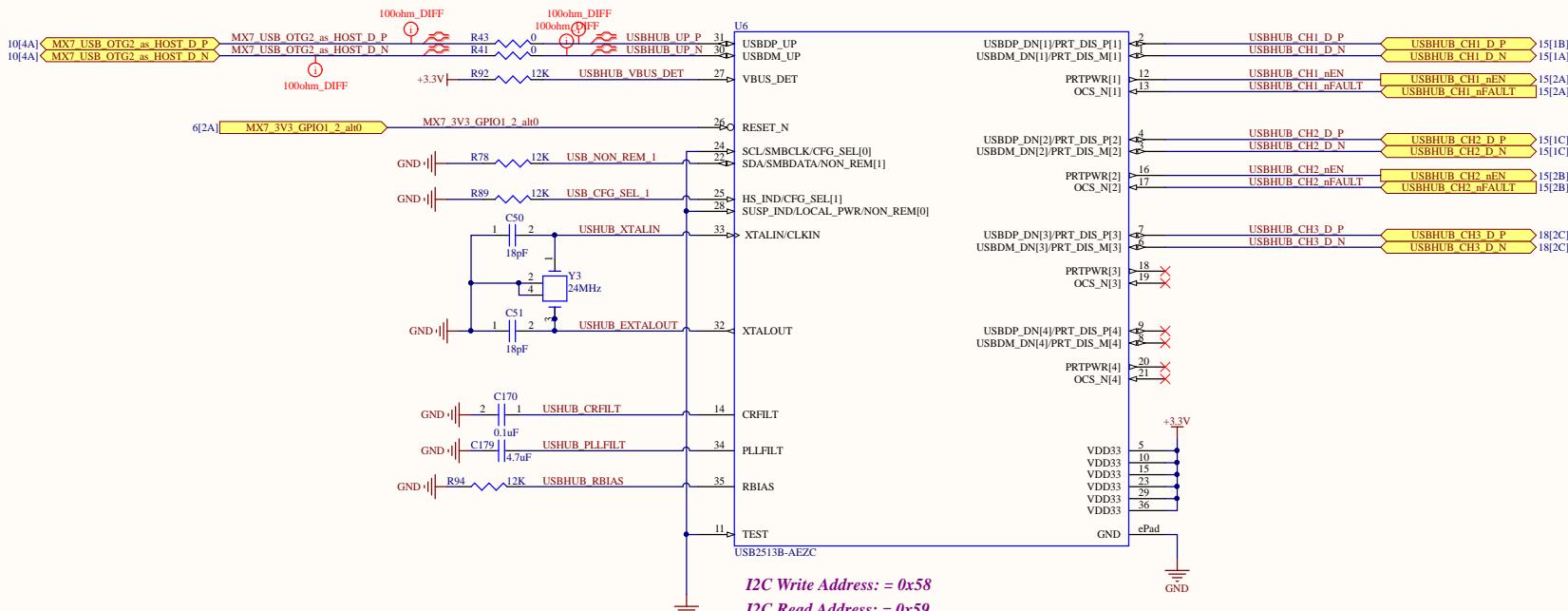


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<b>Drawn By:</b>	T.Ortiz	
<b>Checked By:</b>	Y.Har-Nov	
<b>Approved By:</b> *	B	DDR3L
<b>Date:</b> *		Rev 01
Sheet 12 of 20		

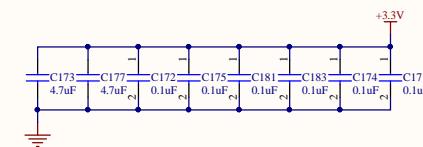
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A

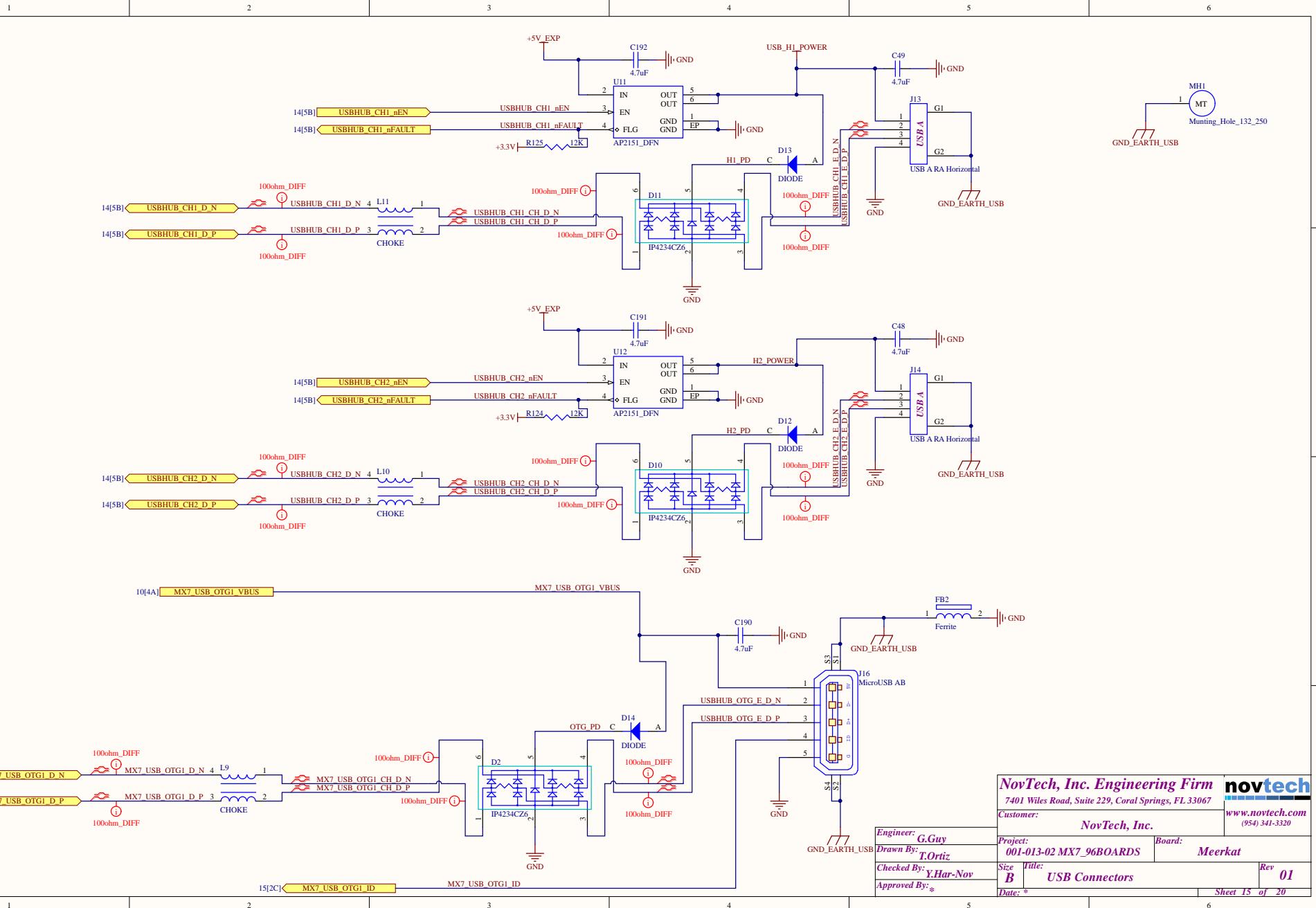


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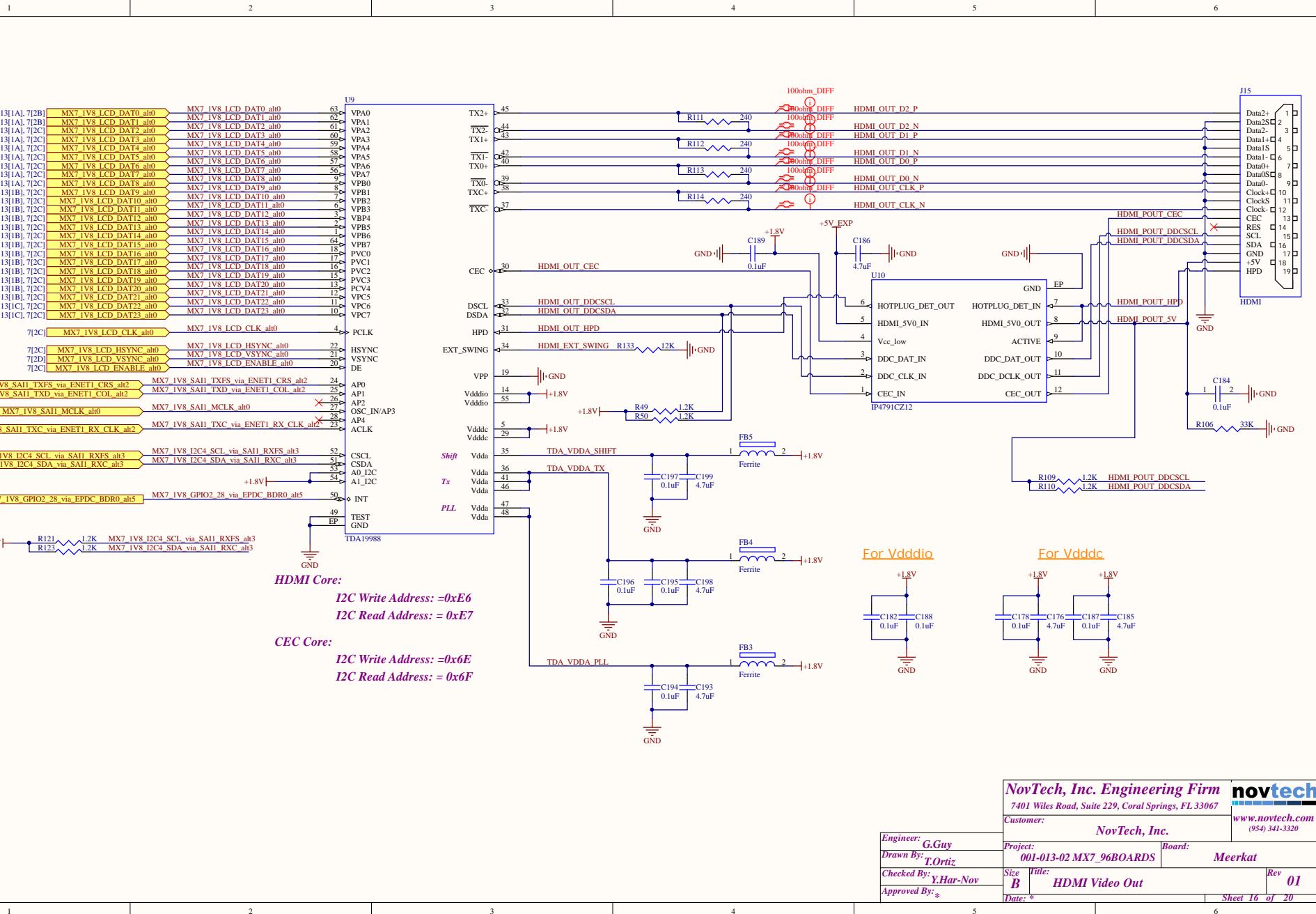


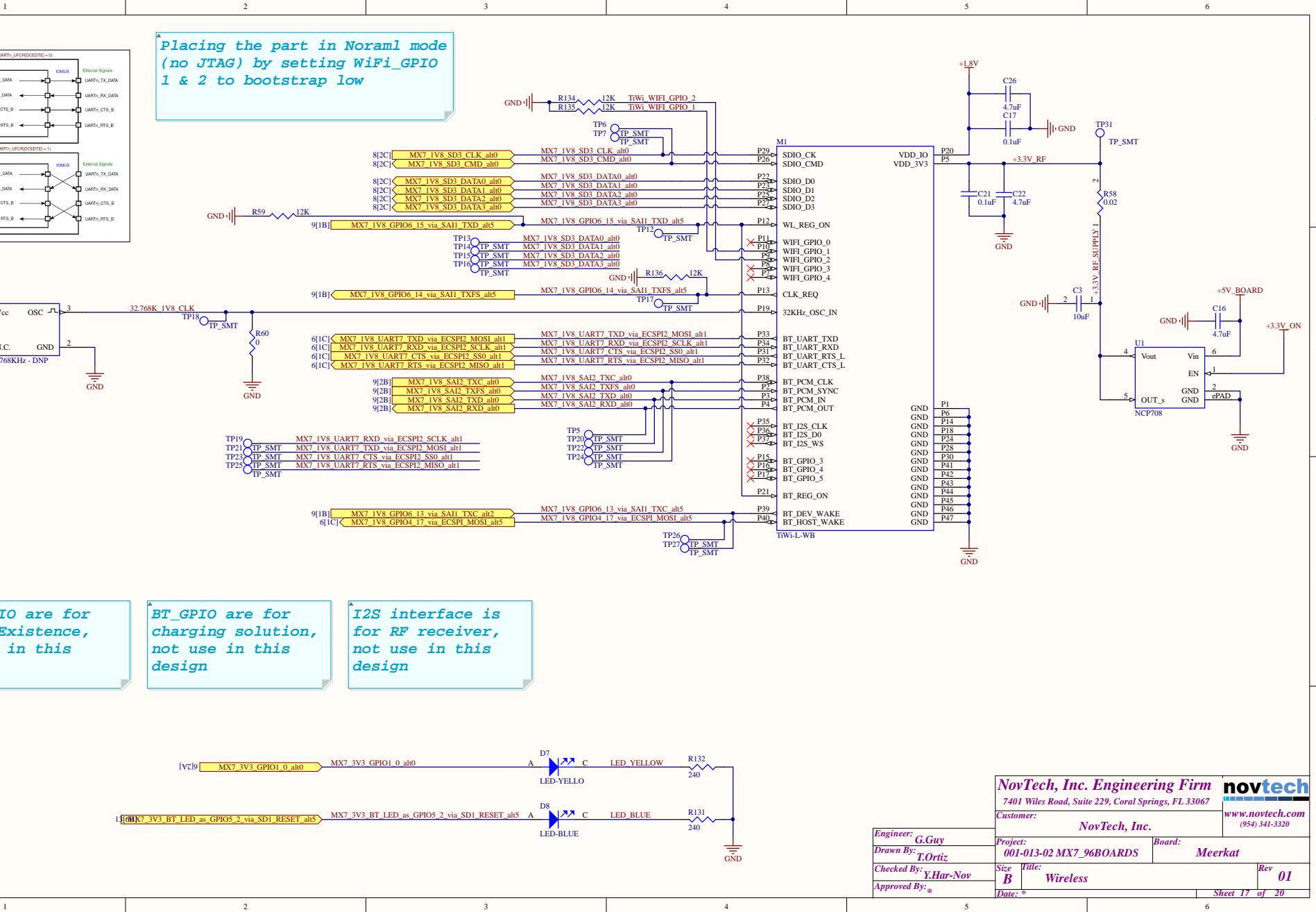
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7401 Wiles Road, Suite 229, Coral Springs, FL 33067		
Customer: NovTech, Inc.		
Engineer: G.Guy	Project: 001-013-02 MX7_96BOARDS	Board: Meerkat
Drawn By: T.Ortiz		
Checked By: Y.Har-Nov	Size: B	Title: USBs Rev 01
Approved By: *	Date: *	



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 Engineer: G.Guy  
 Drawn By: T.Ortiz  
 Checked By: Y.Har-Nov  
 Approved By: \*  
 Project: 001-013-02 MX7\_96BOARDS Board: Meerkat  
 Size: B Title: USB Connectors Rev: 01  
 Date: \* Sheet 15 of 20

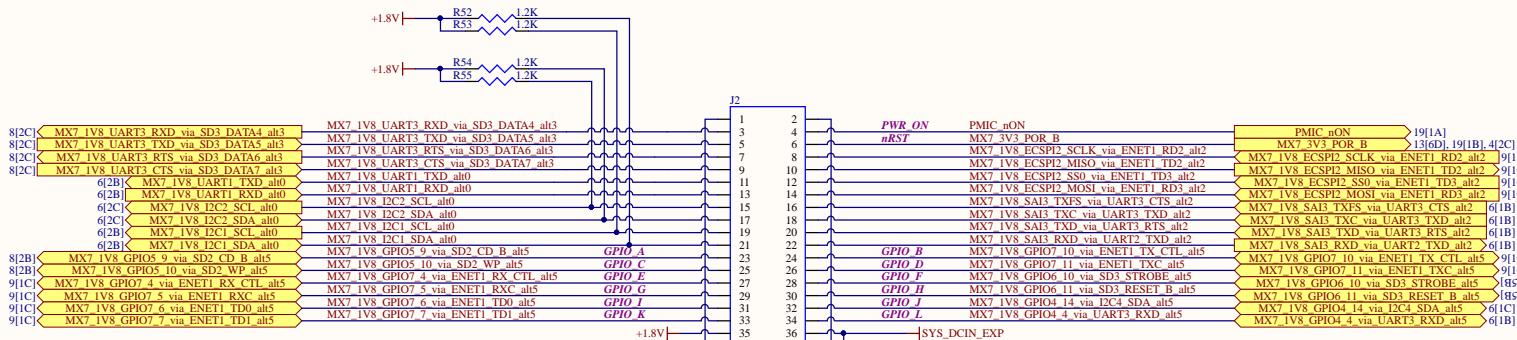




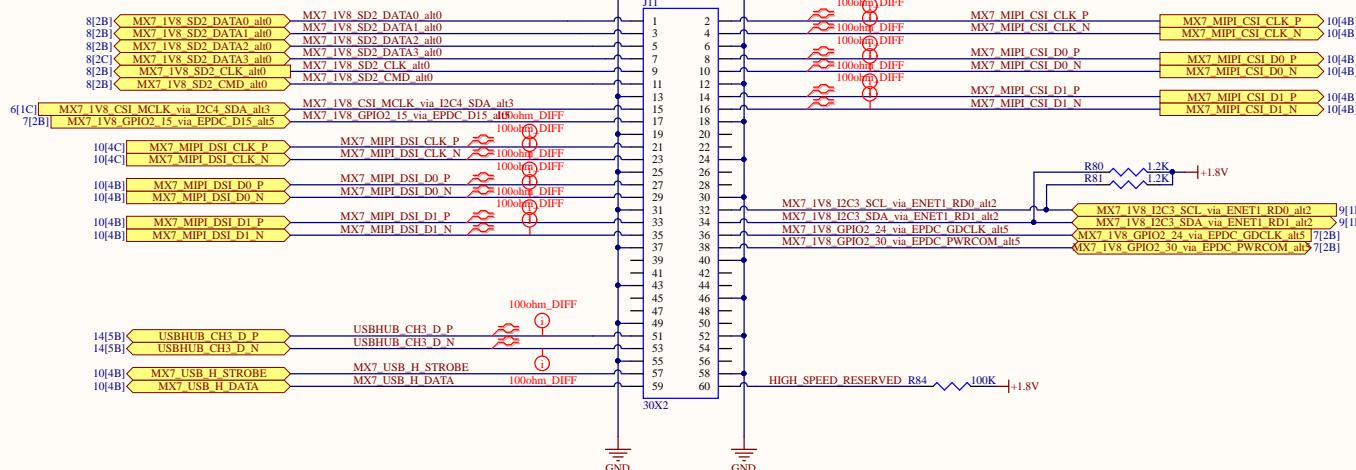
**NovTech, Inc. Engineering Firm**  
7401 Wiles Road, Suite 229, Coral Springs, FL 33067  
**Customer:** NovTech, Inc.  
**Project:** 001-013-02 MX7\_96BOARDS  
**Board:** Meerkat  
**Engineer:** G.Guy  
**Drawn By:** T.Ortiz  
**Checked By:** Y.Har-Nov  
**Approved By:**\*  
**Date:** \*  
**Size:** B  
**Title:** Wireless  
**Rev:** 01  
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**Sheet 17 of 20**

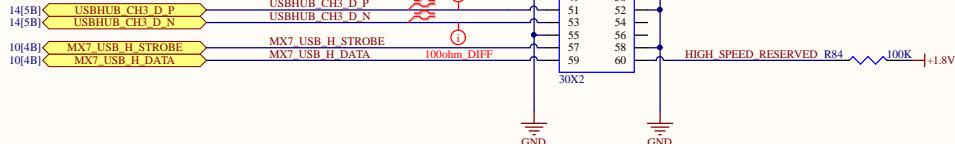
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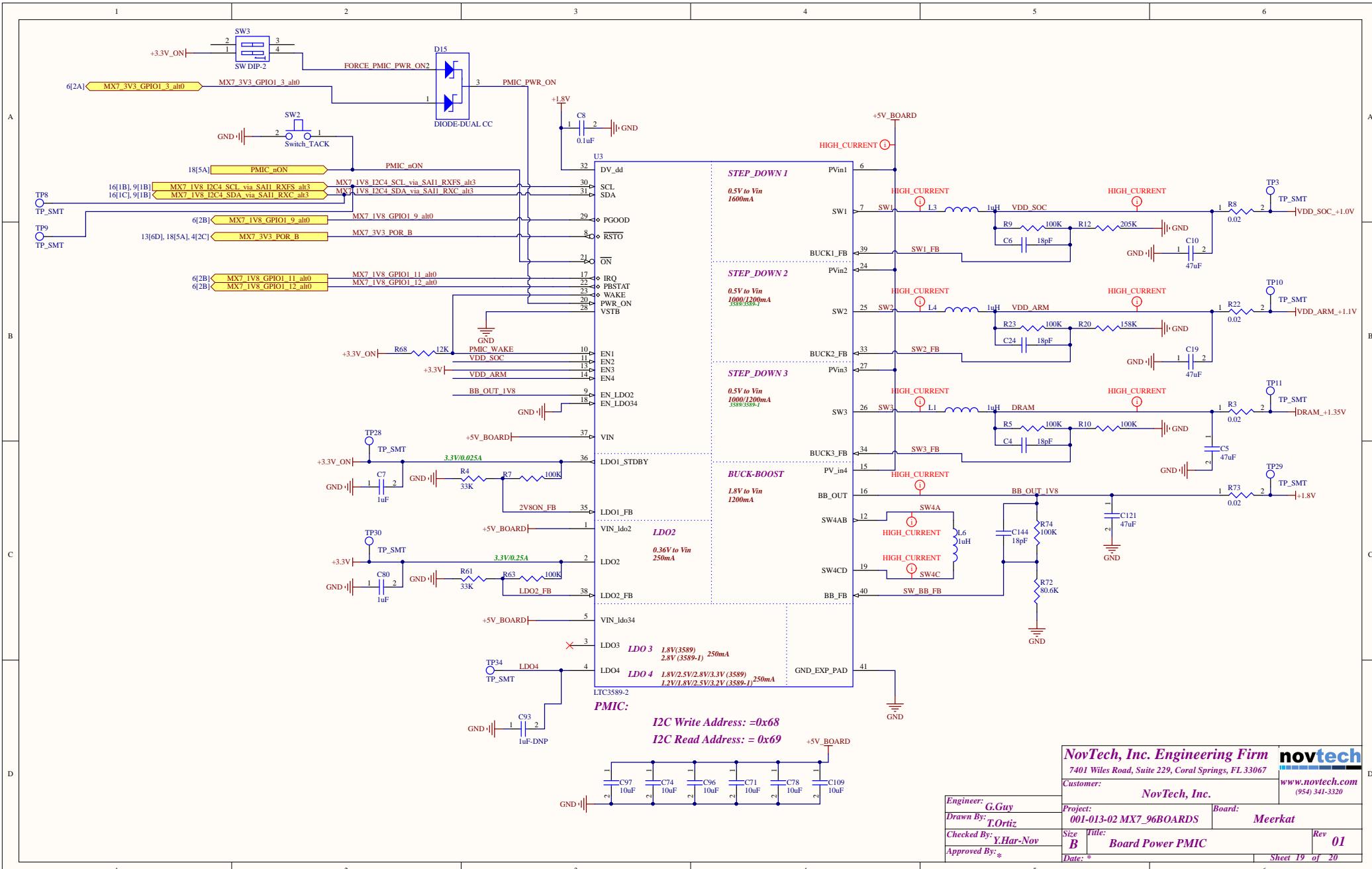
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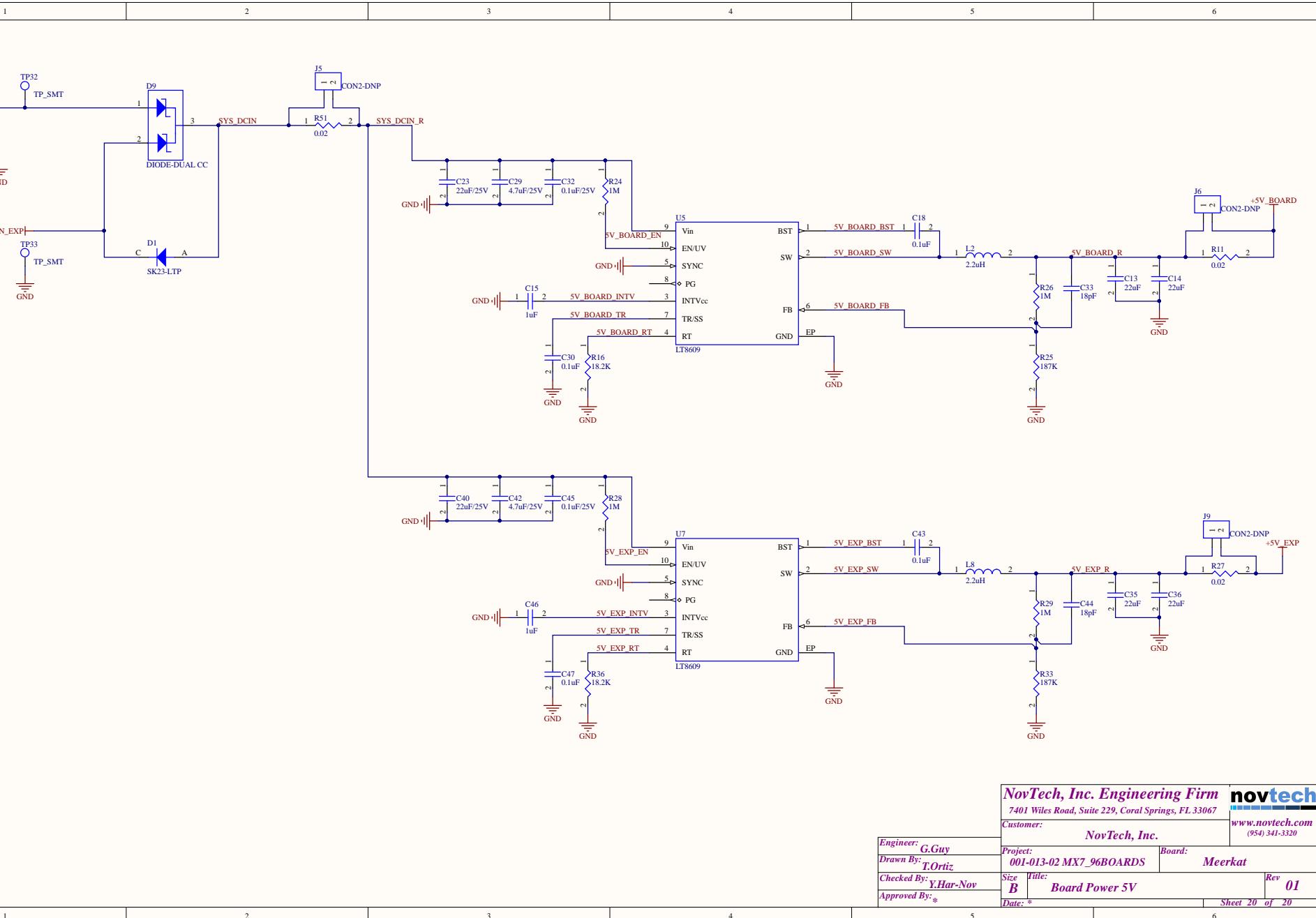


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Customer:	NovTech, Inc.
Engineer:	G.Guy
Drawn By:	T.Ortiz
Checked By:	Y.Har-Nov
Approved By:	*
Size:	B
Title:	Board Power 5V
Rev:	01
Date:	*
Sheet 20 of 20	