```
lbi r0, 0
lbi r5, 43
lbi r6, 43
lbi r7, 43
ld r1, r0, 0
st r5, r1, 0
ld r1, r0, 2
st r6, r1, 1
ld r1, r0, 4
st r7, r1, 1
halt
```

Cycle 1: // No stall, no instruction retired
Cycle 2: // No stall, no instruction retired
Cycle 3: // No stall, no instruction retired
Cycle 4: // No stall, no instruction retired
Cycle 5: // No stall, lbi r0, 0 is retired
Cycle 6: // No stall, lbi r5, 43 is retired
Cycle 7: // No stall, lbi r6, 43 is retired
Cycle 8: // Stall on decode for st r5, r1, 0 and fetch for ld r1, r0, 2; lbi r7, 43 is retired
Cycle 9: // No stall, ld r1, r0, 0 is retired
Cycle 10: // No stall, no instruction retired
Cycle 11: // Stall on decode for st r7, r1, 1; st r5, r1, 0 is retired
Cycle 12: // No stall, ld r1, r0, 2 is retired
Cycle 13: // No stall, no instruction retired
Cycle 14: // No stall, st r7, r1, 1 is retired
Cycle 15: // No stall, halt is retired